CMOS IC Application Note

# S-19989/19999 Series EXTERNAL PARTS SELECTION

Rev.1.1_00



This application note is a method of external parts selection and recommended board layouts for the S-19989/19999 Series.
Refer to the datasheet for details and specs.

## Contents

## 1. Selecting Major External Parts

Major circuits are shown in **Figure 1**, operating conditions in **Table 1** and external part constants in **Table 2**.
The output voltage ($V_{OUT}$) during boost operation is set as the output regulation voltage ($V_{OUT\_REG}$) inside the IC, which allows you to set 6.80 V or 8.50 V optionally.

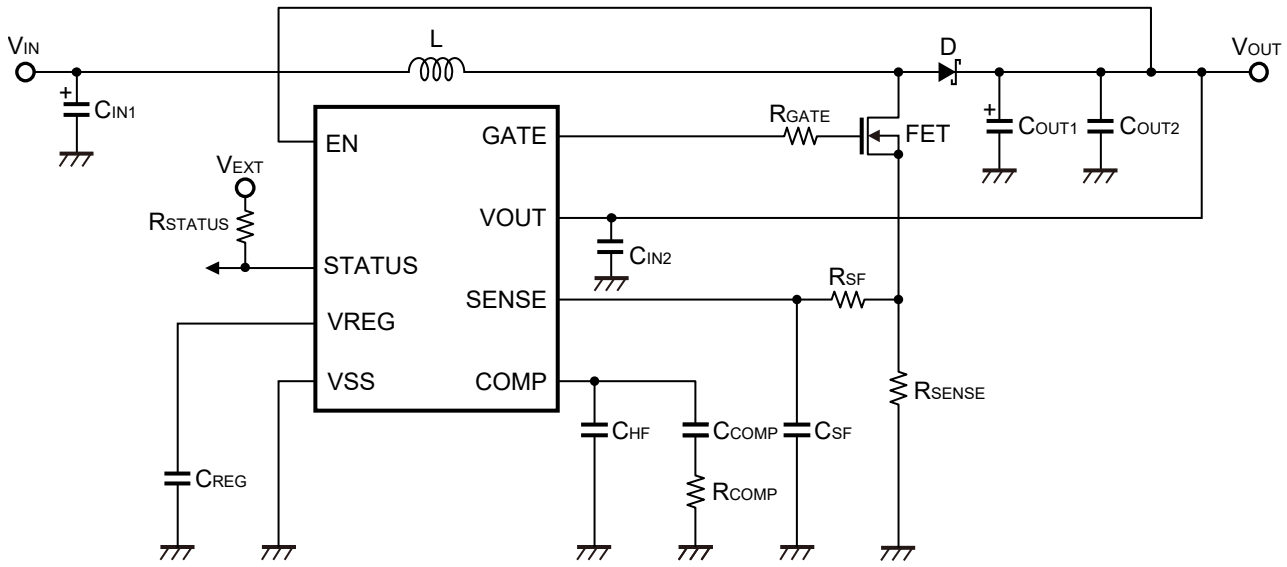



**Figure 1 Typical Circuits**

**Table 1 Design Example**

| Design Parameter | Value |
|---|---|
| Input voltage ($V_{IN}$) | 6 V |
| Output voltage ($V_{OUT}$) | 6.80 V or 8.50 V (Set in the IC) |
| Load current ($I_{LOAD}$) | 2 A |
| Oscillation frequency ($f_{OSC}$) | 2.2 MHz |

**Table 2 Constants for External Components**

| Symbol | Value | Quantity | Part Number | Manufacture |
|---|---|---|---|---|
| L | 0.47 µH | 1 | SPM5030VT-R47M-D | TDK Corporation |
| FET | – | 1 | IPC50N04S5L-5R5 | Infineon Technologies |
| D | – | 1 | PMEG045V100EPD | Nexperia B.V. |
| $C_{IN1}$ | 33 µF | 2 | GYC1H330MCQ1GS | NICHICON CORPORATION |
| $C_{IN2}$ | 0.1 µF | 1 | CGA4J2X8R1H104K | TDK Corporation |
| $C_{OUT1}$ | 100 µF | 3 | GYC1H101MCQ1GS | NICHICON CORPORATION |
| $C_{OUT2}$ | 10 µF | 1 | CGA5L1X7R1H106K | TDK Corporation |
| $R_{GATE}$ | 10 Ω | 1 | MCR3 series (1608) | ROHM CO., LTD. |
| $R_{SENSE}$ | 4 mΩ | 1 | TLR2BPDTD4L00F75 | KOA CORPORATION |
| $R_{SF}$ | 22 Ω | 1 | MCR3 series (1608) | ROHM CO., LTD. |
| $R_{STATUS}$ | 100 kΩ | 1 | MCR3 series (1608) | ROHM CO., LTD. |
| $C_{SF}$ | 10 nF | 1 | CGA3E2X8R1H103K | TDK Corporation |
| $C_{REG}$ | 1 µF | 1 | CGA5L3X8R1H105K | TDK Corporation |
| $R_{COMP}$ | 12 kΩ | 1 | MCR3 series (1608) | ROHM CO., LTD. |
| $C_{COMP}$ | 4.7 nF | 1 | CGA3E2X8R1H472K | TDK Corporation |
| $C_{HF}$ | 220 pF | 1 | CGA3E2NP01H221J | TDK Corporation |

**Caution The above connection diagram and the constant do not guarantee proper operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.**

# 2. Selecting Optional External Parts

This section provides detailed information about parts and a guideline on selecting parts for use with the step-up controller in continuous conduction mode (CCM).

## 2. 1 Guideline for selecting parts

### 2. 1. 1 Definition of design parameters

Design parameters required in calculations used for selecting parts are defined below.

| | |
|---|---|
| $V_{IN\_MIN}$: | Minimum input voltage [V] |
| $V_{IN\_MAX}$: | Maximum input voltage [V] |
| $I_{IN\_MIN}$: | Minimum average input current [A] |
| $I_{IN\_MAX}$: | Maximum average input current [A] |
| $V_{OUT}$: | Output voltage [V] |
| $I_{OUT\_MIN}$: | Minimum load current [A] |
| $I_{OUT\_MAX}$: | Maximum load current [A] |
| $\eta$: | Conversion efficiency |
| $f_{OSC}$: | Oscillation frequency [Hz] |

### 2. 1. 2 Calculating minimum and maximum duty cycle

Use the following equations to calculate minimum duty cycle ($D_{MIN}$) and maximum duty cycle ($D_{MAX}$) including power loss for the step-up converter.

$$D_{MIN} = \frac{V_{OUT} + V_F - V_{IN\_MAX}}{V_{OUT} + V_F - (R_{ON} + R_{SENSE}) \times I_{IN\_MIN}}$$

$$D_{MAX} = \frac{V_{OUT} + V_F - V_{IN\_MIN}}{V_{OUT} + V_F - (R_{ON} + R_{SENSE}) \times I_{IN\_MAX}}$$

$V_F$ is diode forward voltage, $R_{ON}$ is MOS FET on-resistance and $R_{SENSE}$ is a sense resistor for detecting inductor current.
As can be seen from the following efficiency equation, $I_{IN\_MIN}$ and $I_{IN\_MAX}$ are expressed as follows.

$$I_{IN\_MIN} = \frac{V_{OUT} \times I_{OUT\_MIN}}{V_{IN\_MAX} \times \eta}$$

$$I_{IN\_MAX} = \frac{V_{OUT} \times I_{OUT\_MIN}}{V_{IN\_MAX} \times \eta}$$

The duty cycle range must conform to two parameters: minimum duty cycle ($t_{ON\_MIN} \times f_{OSC}$) and maximum duty cycle (MaxDuty) specified by electrical characteristics.

| | |
|---|---|
| $D_{MIN} > t_{ON\_MIN} \times f_{OSC}$: | Lower limit |
| $D_{MAX} <$ MaxDuty: | Upper limit |

If the upper duty cycle limit ($D_{MAX} <$ MaxDuty) is not met, boost operation becomes impossible.

If the lower duty cycle limit ($D_{MIN} > t_{ON\_MIN} \times f_{OSC}$) is not met, pulse skip operation (PFM control) is always performed. PFM control is a function to prevent efficiency loss at light loads. Use PWM control to ensure regulation performance at normal and heavy loads. It is recommended to set a duty cycle tailored to the requirements.

### 2. 1. 3 Selecting an inductor

#### (1) Calculating inductor value

Operate in current continuous mode to suppress inductor current ripple and output voltage ripple. To do so, calculate to find the inductance value where the inductor current ripple ratio (r) is 0.2 to 0.6 to the maximum average inductor current ($I_{L\_MAX}$).
Set inductor current ripple ratio (r) higher than the above (> 1) and operate in discontinuous conduction mode (DCM) to enable selecting a smaller inductor value and reduce the cost.
This will result in better transient characteristics, but the peak value of the inductor current will be larger, which is expected to increase electromagnetic interference (EMI).

$I_{L\_MAX}$ can be obtained as follows.

$$I_{L\_MAX} = I_{IN\_MAX} = \frac{I_{OUT\_MAX}}{1 - D_{MAX}}$$

The input current and inductor current are equal. The inductor current ripple ($\Delta I_L$) can be obtained from the following equation.

$$\Delta I_L = r \times I_{L\_MAX}$$

Thus, the minimum inductor value can be calculated as shown below.

$$L_{MIN} = \frac{V_{IN\_MIN} \times D_{MAX}}{\Delta I_L \times f_{OSC}}$$

Set a standard inductance value (L) to take variations into account.

#### (2) Inductor peak current

Inductor peak current should never reach the saturation current rating of the inductor. The maximum inductor peak current ($I_{LPEAK\_MAX}$) can be calculated from the maximum inductor current ripple value ($\Delta I_{LPP\_MAX}$) as follows.

$$I_{LPEAK\_MAX} = I_{L\_MAX} + \frac{\Delta I_{LPP\_MAX}}{2} = \frac{I_{OUT\_MAX}}{1 - D_{MAX}} + \frac{V_{IN\_MIN} \times D_{MAX}}{2 \times L \times f_{OSC}}$$

$$\Delta I_{LPP\_MAX} = \frac{V_{IN\_MIN}}{L} \times \frac{D_{MAX}}{f_{OSC}}$$

#### (3) Inductor RMS current

Inductor RMS current, like inductor peak current, must always meet the RMS current rating. The maximum inductor RMS current ($I_{LRMS\_MAX}$) can be obtained from the following equation.

$$I_{LRMS\_MAX} = \sqrt{I_{L\_MAX}^2 + \frac{\Delta I_{LPP\_MAX}^2}{12}} = \sqrt{\left(\frac{I_{OUT\_MAX}}{1 - D_{MAX}}\right)^2 + \frac{1}{12} \times \left(\frac{V_{IN\_MIN} \times D_{MAX}}{L \times f_{OSC}}\right)^2}$$

### 2. 1. 4 Selecting a sense resistor ($R_{SENSE}$)

The sense resistor ($R_{SENSE}$) is connected between the SENSE pin and GND of the IC and detects inductor current information as ramp voltage. This ramp voltage is used for overcurrent protection (OCP) and peak current mode control.

The overcurrent protection settings are shown below, but make sure that the stability conditions for peak current mode are also met.

#### (1) Overcurrent protection settings

The S-19989/19999 Series integrates a pulse-by-pulse overcurrent protection function. When the peak inductor current flows through $R_{SENSE}$ and the SENSE pin voltage ($V_{SENSE}$) exceeds the threshold ($V_{LIM}$), the MOS FET turns off. In the next switching cycle, the MOS FET goes on. However, if $V_{SENSE} > V_{LIM}$, the MOS FET turns off again and continues the same operation in subsequent cycles. The IC returns to normal operation when $V_{SENSE} < V_{LIM}$.

The overcurrent and short-circuit protection (Hiccup control) of the S-19989/19999 Series provides no means to limit the current from input to output should a short circuit occur at the output of the converter. Use fuses or limit the current of the main power supply if protection against short circuits is required.

The recommended overcurrent detection value is the maximum inductor peak current ($I_{LPEAK\_MAX}$) plus 20%. Use the following equation to calculate $R_{SENSE}$ at this time.

$$R_{SENSE} = \frac{V_{LIM}}{1.2 \times I_{LPEAK\_MAX}}$$

#### (2) Peak current mode stability conditions

The current control loop becomes unstable in peak current mode control and may cause sub-harmonic oscillations. For this reason, regulation will maintain operation of the voltage loop without oscillations. However, the pulses from the PWM alternate between long and short and increase output ripple voltage. This state occurs only when the converter operates in continuous mode at a duty cycle of 50% or more.

The S-19989/19999 Series integrates a slope compensation function as a countermeasure to subharmonic oscillations. Inside the IC, a sawtooth slope compensation ramp current ($I_{SLOPE}$ = 10 μA max.) flows through a 5 kΩ resistor to generate a slope compensation ramp voltage ($S_E$). The SENSE pin outputs the sawtooth current and offset current ($I_{OS}$ = 30 μA fixed).

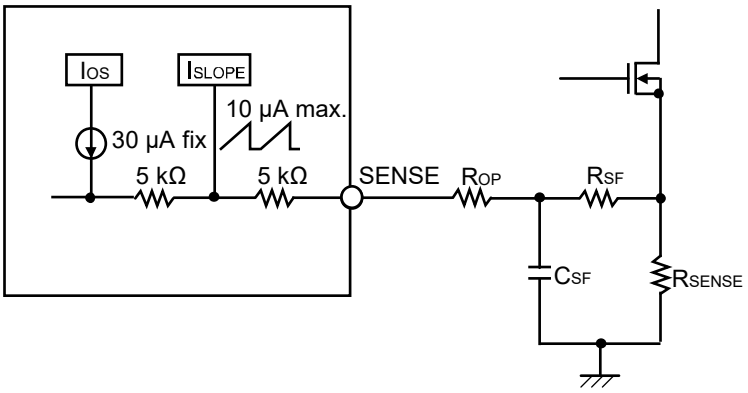



**Figure 2 SENSE Pin Area Simplified Diagram**

$$S_E = 10\ \mu A \times 5\ k\Omega \times f_{OSC}$$

The theoretical condition for preventing subharmonic oscillations is $S_E > 0.5 \times S_F$. $S_F$ is the ramp voltage generated by inductor current and $R_{SENSE}$. The $R_{SENSE}$ condition is indicated by the following equation.

$$S_F = \frac{V_{OUT} + V_F - V_{IN\_MIN}}{L} \times R_{SENSE}$$

$$R_{SENSE} < \frac{100\ mV \times f_{OSC} \times L}{V_{OUT} + V_F - V_{IN\_MIN}}$$

If there is a risk of subharmonic oscillations even when the above setting conditions are satisfied, add a resistor ($R_{OP}$) between the SENSE pin and $R_{SENSE}$ to increase the slope of slope compensation. At this time, $S_E = 10\ \mu A \times (5\ k\Omega + R_{OP}) \times f_{OSC}$ and $R_{SENSE}$ is obtained by the following equation.

$$R_{SENSE} < \frac{20\ \mu A \times (5\ k\Omega + R_{OP}) \times f_{OSC} \times L}{V_{OUT} + V_F - V_{IN\_MIN}}$$

Since 40 μA max. (sawtooth current + offset current) × $R_{OP}$ offset voltage are generated and becomes $V_{LIM} \rightarrow V_{LIM} - 40\ \mu A \times R_{OP}$, make sure the overvoltage current protection threshold does not decrease. Note that if the slope compensation slope is made too large, the inductor current information becomes relatively small. Therefore, this control resembles voltage mode control, and may lower the quality of the input response.

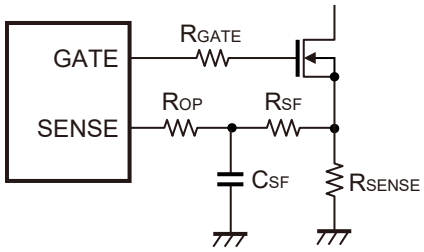



**Figure 3 RC Filter**

**(3) SENSE signal filtering**

When the MOS FET is turned on and off, the resonance of the parasitic inductor, MOS FET output capacitance and diode junction capacitance caused by PC board wiring leads to overshoot / undershoot and ringing exceeding several 10 MHz in the switching waveform.
If these are propagated to the SENSE pin, the inductor current information is incorrectly detected making regulation operation unstable.
In the S-19989/19999 Series, a blanking time (equivalent to $t_{ON\_MIN}$) is set immediately after turning on the MOS FET to mask this noise. If the ringing exceeds the blanking time, add the RC filters ($R_{SF}$ and $C_{SF}$) shown in **Figure 3** between the $R_{SENSE}$ and the SENSE pin to reduce ringing.

Check the cycle of the ringing waveform and set the time constant of the RC filter to about 10 times the ringing cycle. Setting a high $R_{SF}$ will impact the detection value of overcurrent protection so a value of 50 Ω or less is recommended.

Refer also to "**(6) Ringing countermeasures in switching waveforms**" in "**2. 1. 10 Selecting a MOS FET**", for information on how to reduce ringing waveforms in switching waveforms.

### 2. 1. 5 Selecting a diode

To increase efficiency, adding a Schottky diode with low forward voltage and small reverse leakage current is recommended.

#### (1) Rated voltage and current

The diode is reverse biased while the MOS FET is on. Provide a proper margin between the maximum peak reverse voltage rating of the diode and regulator output voltage ($V_{OUT}$).

The diode conducts while the MOS FET is off, supplying energy stored in the inductor to the output capacitor. Therefore, over one switching cycle, the maximum average diode current ($I_{D\_MAX}$) is equal to maximum load current ($I_{OUT\_MAX}$).

$$I_{D\_MAX} = I_{OUT\_MAX}$$

Set the maximum forward average diode current ($I_{F\_MAX}$) to be larger than the maximum load current ($I_{OUT\_MAX}$).

$$I_{F\_MAX} > I_{D\_MAX}$$

#### (2) Power consumption and temperature

Diode power consumption is $P_D = V_F \times I_D$. Ensure that the junction temperature Tj [°C] does not exceed the maximum junction temperature rating of the diode even at maximum ambient temperature.

$$T_j = Ta + \theta_{JA} \times P_D$$

Ta is ambient temperature [°C] and $\theta_{JA}$ is the thermal resistance of the diode [°C/W].

### 2. 1. 6 Selecting an output capacitor

The rated voltage of the capacitor must be higher than maximum output voltage. Specifically, when MLCC capacitors are used, the capacitance may vary depending on temperature and applied DC voltage, so a sufficient margin should be considered when making a selection.

Output capacitors that meet the desired output voltage ripple ($\Delta V_{OUT}$) and output RMS ripple current should be selected.

#### (1) Calculating output voltage ripple

Output voltage ripple is the sum of voltage fluctuations caused by capacitor ($C_{OUT}$) charging and discharging and the ripple current in the equivalent series resistance ($R_{ESR}$) of the capacitor, as shown in the equation below.

$$\Delta V_{OUT} = \left( \frac{I_{OUT\_MAX} \times D_{MAX}}{C_{OUT} \times f_{OSC}} \right) + R_{ESR} \times \left( \frac{I_{OUT\_MAX}}{1 - D_{MAX}} + \frac{V_{IN\_MIN} \times D_{MAX}}{2 \times L \times f_{OSC}} \right)$$

There is actually a phase difference between the two ripples, but this is simplified in the equation.

#### (2) Calculating RMS ripple

The RMS ripple current ($I_{COUTRMS}$) of the output capacitor can be calculated as shown in the following equation.

$$I_{COUTRMS} = \sqrt{(1 + D_{MAX}) \times \left\{ \frac{D_{MAX}}{(1 - D_{MAX})^2} \times I_{OUT\_MAX}{}^2 + \frac{\Delta I_L}{12} \right\}}$$

Select a $C_{OUT}$ value so that the RMS ripple current satisfies the rating. If it does not, add capacitors in parallel. ESR reduction can also be expected.

### 2. 1. 7 Phase compensation element selection

A phase compensation element is required to add phase compensation to the error amplifier in order to achieve high power supply stability.

The system control is a closed loop, which controls the switching operation through the adjustment of an appropriate duty cycle. This makes it possible to achieve the required output voltage and output load.

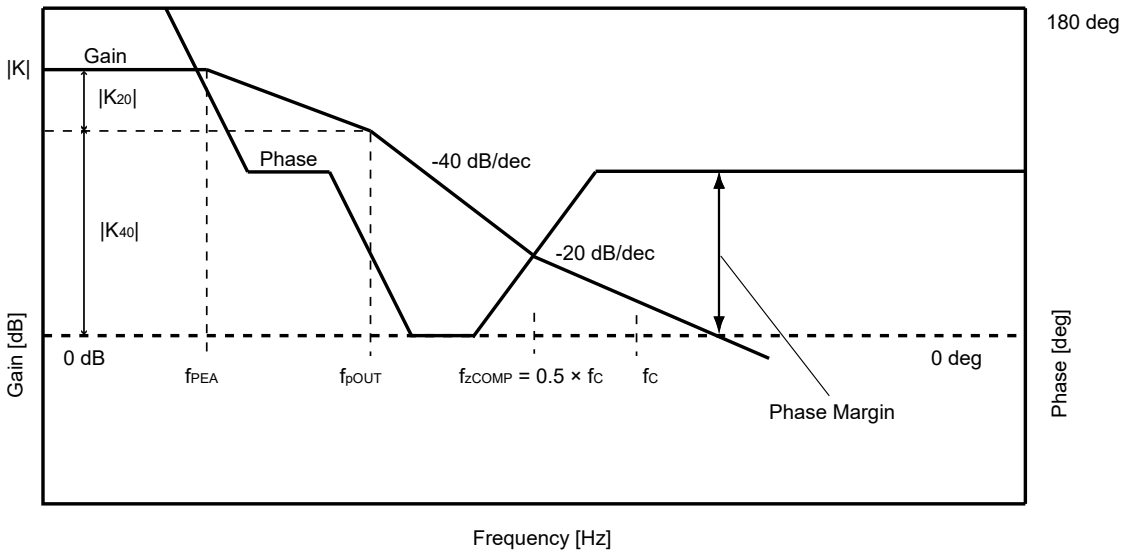



**Figure 4 Bode plot of the S-19989/19999 Series**

The transfer function from this closed loop can be used to express the parameters shown in **Figure 4** as shown in the formula below.

$$|K| = 20 \times \log_{10}\left(\frac{R_{OUT} \times (1 - D_{MIN})}{2 \times R_{SENSE}} \times gm \times R_{EA} \times \frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right)$$

$$f_{PEA} = \frac{f_{pOUT}}{10^{\frac{|K| - 40 \times \log_{10}(f_C / f_{pOUT})}{20}}}$$

$$f_{pOUT} = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}}$$

$$f_{zESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

$$f_{zRHP} = \frac{R_{OUT}}{2\pi \times L} \times (1 - D_{MIN})^2$$

**Remark** Output load resistance: $R_{OUT} = V_{OUT} / I_{OUT}$ [**Ω**]
$C_{OUT}$ equivalent series resistance: $R_{ESR}$ [**Ω**]
Error amplifier transconductance: gm [S]
Error amplifier output resistance: $R_{EA} \approx 10$ [M**Ω**]

Also, $R_{FB}$ varies depending on $V_{OUT}$, so please refer to the values in **Table 3**.

**Table 3**

| Design Parameter | $V_{OUT}$ | |
|---|---|---|
| | 6.80 V | 8.50 V |
| $R_{FB1}$ | 450 kΩ | 580 kΩ |
| $R_{FB2}$ | 60 kΩ | 60 kΩ |

If the phase margin < 0 deg at the frequency at which the closed loop gain is 0 dB (crossover frequency ($f_C$)), oscillation will occur. Set the phase margin and gain margin as shown below to prevent this oscillation from occurring.

Phase Margin ≈ 45 deg to 60 deg
Gain Margin ≥ 10 dB

This setting is achieved by appropriately configuring the phase compensation element. Therefore, it is necessary to place zeros at the appropriate frequencies in order to restore the phase.

Instability (subharmonic oscillation) at duty cycle settings of 50% of higher is not referenced because this IC is equipped with slope compensation.
In addition, the crossover frequency ($f_C$) should also be set to whichever of the following is smallest in order to eliminate any effects of phase delay at the double pole and right half plane zero which are at half of the normal switching frequency ($f_{OSC}/2$).
However, if $f_{zESR}$ or $f_{zRHP}$ are at similar frequency digits to $f_C$, it is recommended that $f_C$ be set to 1/10th of those frequencies.

$$f_C < \frac{1}{10} \times f_{zESR} \text{ [Hz]}$$

$$f_C < \frac{1}{10} \times f_{zRHP} \text{ [Hz]}$$

**Remark** For $R_{COMP}$ and $C_{COMP}$ listed in **Table 2** and $R_1$ and $C_9$ listed in **Table 5**, $f_C$ is set lower than the above to approximately 5 kHz to eliminate the effect of the right half plane zero.
To set $f_C$ even higher, follow the above equations.

**(1) Phase compensation capacity calculation**

The phase compensation capacity can be found from the DC gain and $f_{PEA}$ as shown below.

$$C_{COMP} = \frac{1}{2\pi \times R_{EA} \times f_{PEA}}$$

**(2) Phase compensation resistance calculation**

$$R_{COMP} = \frac{1}{2\pi \times C_{COMP} \times 0.5 \times f_C}$$

The error amplifier zero $f_{zCOMP}$ is placed and phase compensation is carried out. The $f_{zCOMP}$ position should be set to approximately $0.5 \times f_C \leq f_{zCOMP} < f_C$. In **Figure 4** this is set to $f_{zCOMP} = 0.5 \times f_C$.

**(3) High frequency noise blocking capacitor ($C_{HF}$) calculation**

Connect a capacitor calculated using the following formula to the COMP pin in order to prevent malfunctions resulting from switching noise.

$$C_{HF} < \frac{1}{2\pi \times R_{COMP} \times 10 \times f_C}$$

Also take the following into consideration when carrying out actual power supply design.

- Verify the phase margin and gain margin using a network analyzer.
- If the phase margin is insufficient, increase $R_{COMP}$.
- If it is still insufficient, reset the $f_C$ to a lower value.

### 2. 1. 8 Selecting input capacitors

When AC current is supplied to an inductor, input capacitors are required to reduce input voltage ripple.

In current continuous mode, only input voltage ripple need to be considered since the input current caused by the steady-state boost operation is continuous and the selection conditions are not as strict as for $C_{OUT}$. However, large input and load variations in current discontinuous mode, may require an additional capacitor with larger capacitance to buffer the input voltage.

#### (1) IC bypass capacitor

It is recommended to connect a ceramic capacitor with low ESR of about 0.1 μF to 1 μF near the $V_{IN}$ – VSS pin of the IC to lower input impedance in order to prevent malfunctions caused by noise and other factors.

#### (2) Input capacitor for step-up converter

As an inductor is connected in series with the input of a step-up converter, the input current waveform becomes a continuous triangular waveform when the MOS FET is turned on and off. This current generates input voltage ripple ($\Delta V_{IN}$) in $C_{IN}$, which can be roughly estimated by the following equation.

$$\Delta V_{IN} = \Delta I_L \times \left( R_{ESR} + \frac{1}{8 \times f_{OSC} \times C_{IN}} \right)$$

$R_{ESR}$ is the equivalent series resistance of $C_{IN}$. To reduce voltage ripple and ensure stable operation during input and load transients, connect a low ESR ceramic capacitor (33 μF to 100 μF) or a conductive polymer hybrid aluminum electrolytic capacitor to $C_{IN}$.

Also verify that the capacitor meets its rated ripple with respect to withstand voltage, operating temperature, and input current root mean square value ($I_{INRMS}$) as calculated by the equation below.

$$I_{INRMS} = \frac{1}{2\sqrt{3}} \times \Delta I_L$$

### 2. 1. 9 Selecting VREG pin capacitors

$V_{REG}$ is the internal power supply voltage of an IC output by the VREG pin and used to operate some internal IC circuits. Also, when the MOS FET is turned on, a current for charging the GATE momentarily flows from $V_{REG}$. Connect a low ESR ceramic capacitor near the VREG – VSS pin to prevent VREG from dropping during this brief ON period. A capacitance value of 1 μF is recommended.
Do not connect any external parts or loads other than a ceramic capacitor to the VREG pin.

### 2. 1. 10 Selecting a MOS FET

MOS FET is the main switching element in step-up converters. Rated voltage and current needs to be considered in their selection.
Power loss is mainly caused by conduction loss, switching loss and gate drive loss.

#### (1) Rated voltage and current

During the MOS FET off period, the drain-source voltage is equal to $V_{OUT} + V_F$. If ringing occurs at the switching node, a margin must be provided with respect to the rated voltage.

Also, maximum input current ($I_{IN\_MAX}$) should not exceed the MOS FET drain current rating.

#### (2) Conduction loss ($P_{COND}$)

$P_{COND}$ is power lost in the on-resistor when the MOS FET is on.
The maximum RMS current ($I_{SWRMS\_MAX}$) at this time can be calculated as follows.

$$I_{SWRMS\_MAX} = \sqrt{D_{MAX}} \times \sqrt{\left(\frac{I_{OUT\_MAX}}{1 - D_{MAX}}\right)^2 + \frac{\Delta I_L^2}{12}}$$

Thus, MOS FET conduction loss ($P_{COND}$) can be obtained by the following equation.

$$P_{COND} = R_{ON} \times D_{MAX} \times \left\{\left(\frac{I_{OUT\_MAX}}{1 - D_{MAX}}\right)^2 + \frac{\Delta I_L^2}{12}\right\}$$

#### (3) Switching loss ($P_{SW}$)

$P_{SW}$ is the loss generated by the flow of current and voltage between drain and source when a MOS FET is turned on and off.

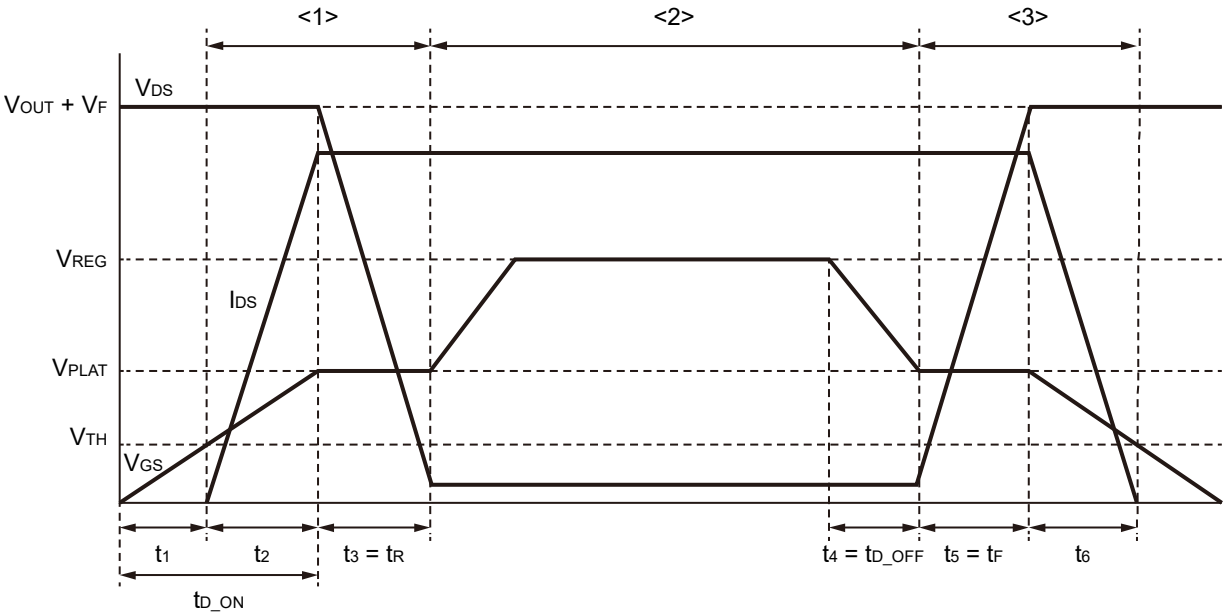
$$P_{SW} = \frac{V_{OUT} + V_F}{2} \times I_{L\_MAX} \times f_{OSC} \times (t_{TR\_ON} + t_{TR\_OFF})$$

$$t_{TR\_ON} = t_{D\_ON} - R_G \times C_{ISS} \times \ln\left(\frac{V_{REG}}{V_{REG} - V_{TH}}\right) + t_R$$

$$t_{TR\_OFF} = R_G \times C_{ISS} \times \ln\left(\frac{V_{PLAT}}{V_{TH}}\right) + t_F$$

The following parameters are listed in the MOS FET data sheet.

| | |
|---|---|
| $C_{ISS}$: | Input capacitance |
| $V_{TH}$: | Threshold voltage |
| $V_{PLAT}$: | Plateau voltage |
| $t_{D\_ON}$: | Turn On delay time |
| $t_R$: | Rise time |
| $t_F$: | Fall time |
| $t_{D\_OFF}$: | Turn Off delay time |
| $R_G$: | Internal MOS FET gate resistor + gate drive circuit on-resistor + option resistor ($R_{GATE}$) between MOS FET gate and drive circuit output |




<1> Turn on period: $P_{SW}$ occurrence
<2> MOS FET on period: $P_{COND}$ occurrence
<3> Turn off period: $P_{SW}$ occurrence

**Figure 5 MOS FET On and Off Voltage and Current Transitions**

### (4) Gate drive loss ($P_{GATE}$)

$P_{GATE}$ is the loss caused by charging and discharging input capacitance in driving the MOS FET gate.

$$P_{GATE} = C_{ISS} \times V_{REG}^2 \times f_{OSC}$$

### (5) Total MOS FET loss ($P_{TOTAL}$) and junction temperature

As indicated in (2) to (4), total MOS FET power loss is $P_{TOTAL} = P_{COND} + P_{SW} + P_{GATE}$.

Make sure that junction temperature $T_j$ [°C] does not exceed the maximum MOS FET junction temperature rating even at maximum ambient temperature.

$$T_j = Ta + R_{\theta jA} \times P_{TOTAL}$$

$R_{\theta jA}$ is the thermal resistance between the IC chip junction and the ambient environment.

### (6) Ringing countermeasures in switching waveforms

Connecting a gate resistor ($R_{GATE}$) of several 10 ohms to reduce ringing in switching waveforms is also effective, but note that there is a trade-off with efficiency due to resistor losses.

# 3. Board Layout Precautions

PCB layout and component placement are essential in ensuring stable operation of the switching regulator and to achieve good regulation performance, conversion efficiency, and noise reduction. We will explain points to note in PCB layout using our PCB as an example.

## 3. 1 Application circuit diagram

**Figure 6** shows the circuit diagram of a step-up application created by ABLIC Inc.
Connect the $V_{OUT}$ and VOUT pin via JP1 to create a bootstrap configuration. Connect the EN pin to the $V_{OUT}$ via JP2, or leave JP2 open to apply voltage externally.

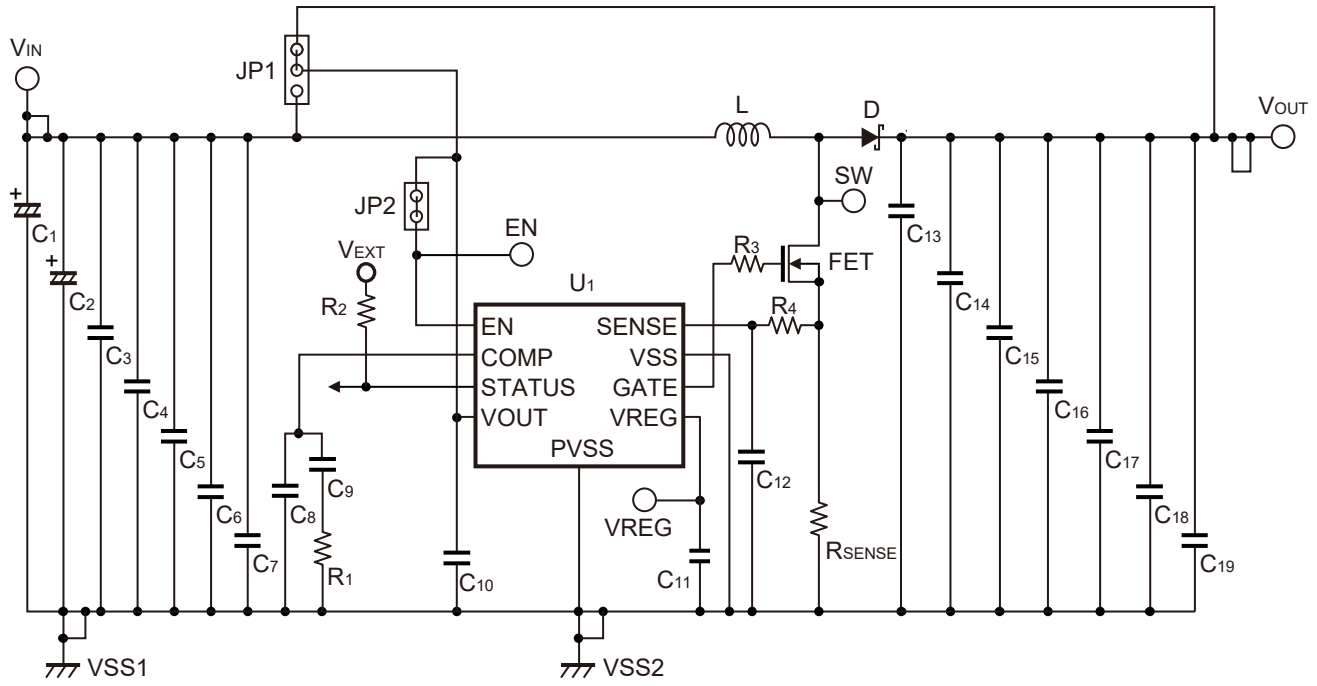



**Figure 6**

**Table 4 Design Example**

| Design Parameter | Value |
|---|---|
| Input voltage ($V_{IN}$) | 6 V |
| Output voltage ($V_{OUT}$) | 6.80 V or 8.50 V (Set in the IC) |
| Load current ($I_{LOAD}$) | 2 A |
| Oscillation frequency ($f_{OSC}$) | 2.2 MHz |

### 3. 2 External components list

**Table 5** shows external components used in the connection examples: **Figure 6**.

**Table 5 External Components**

| Symbol | Value | Part Number | Manufacture |
|---|---|---|---|
| $U_1$ | – | S-19989/19999 Series | ABLIC Inc. |
| $C_1$ | 33 μF | GYC1H330MCQ1GS | NICHICON CORPORATION |
| $C_2$ | 33 μF | GYC1H330MCQ1GS | NICHICON CORPORATION |
| $C_3$ | User settings | – | – |
| $C_4$ | User settings | – | – |
| $C_5$ | User settings | – | – |
| $C_6$ | User settings | – | – |
| $C_7$ | User settings | – | – |
| $C_8$ | 220 pF | CGA3E2NP01H221J | TDK Corporation |
| $C_9$ | 4.7 nF | CGA3E2X8R1H472K | TDK Corporation |
| $C_{10}$ | 0.1 μF | CGA4J2X8R1H104K | TDK Corporation |
| $C_{11}$ | 1 μF | CGA5L3X8R1H105K | TDK Corporation |
| $C_{12}$ | 10 nF | CGA3E2X8R1H103K | TDK Corporation |
| $C_{13}$ | User settings | – | – |
| $C_{14}$ | 10 μF | CGA5L1X7R1H106K | TDK Corporation |
| $C_{15}$ | User settings | – | – |
| $C_{16}$ | 10 μF | CGA5L1X7R1H106K | TDK Corporation |
| $C_{17}$ | 100 μF | GYC1H101MCQ1GS | NICHICON CORPORATION |
| $C_{18}$ | 100 μF | GYC1H101MCQ1GS | NICHICON CORPORATION |
| $C_{19}$ | 100 μF | GYC1H101MCQ1GS | NICHICON CORPORATION |
| $C_{20}$ | User settings | – | – |
| $R_1$ | 12 kΩ | MCR3 series (1608) | ROHM CO., LTD. |
| $R_2$ | 100 kΩ | MCR3 series (1608) | ROHM CO., LTD. |
| $R_3$ | 10 Ω | MCR3 series (1608) | ROHM CO., LTD. |
| $R_4$ | 22 Ω | MCR3 series (1608) | ROHM CO., LTD. |
| $R_5$ | User settings | – | – |
| $R_{SENSE}$ | 4 mΩ | TLR2BPDTD4L00F75 | KOA CORPORATION |
| JP1 | – | – | – |
| JP2 | – | – | – |
| L | 0.47 μH | SPM5030VT-R47M-D | TDK Corporation |
| FET | – | IPC50N04S5L-5R5 | Infineon Technologies |
| D | – | PMEG045V100EPD | Nexperia B.V. |

**Caution 1. The above constants may be changed without notice.**
**2. The above constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**

### 3. 3 PCB layout

The board we have created for the application circuit diagram in **Figure 6** has four layers, which are shown in **Figure 7** to **Figure 10.**

- Top layer: A layout containing most parts and wiring
- Internal layer 1: A layer that reinforces VIN and VSS wiring
- Internal layer 2: A layer that reinforces VSS
- Bottom layer: Wiring that is difficult to route in the top layer and does not require significant attention and reinforces VSS

**"3. 4 Board layout precautions"** describe the precautions to take in performing these layouts.

### 3. 4 Board layout precautions

- Place $C_{IN}$ ($C_{10}$) as close to the VOUT pin and the VSS pin as possible. Prioritize the layout of $C_{IN}$.
- Place $C_{REG}$ ($C_{11}$) as close to the VREG pin and the VSS pin as possible.
- GATE pin patterns should not create wiring below the IC.
- To provide proper ventilation, connect the rear heat dissipation pad to the VSS pattern and place thermal vias.
- Make the switching loop composed of $C_{OUT}$ ($C_{13}$ to $C_{19}$) → D → FET → $R_{SENSE}$ → $C_{OUT}$ ($C_{13}$ to $C_{19}$) as small as possible. This measure effectively reduces inductive high-frequency noise.
- The SW wiring area (Dashed line area in "**Figre 7 Top Layer (First Layer)**") should be as small as possible to reduce high-frequency radiation noise.
- All copper foil on the back of the inductor (L) should be removed to avoid losses due to eddy currents.
- A ringing signal is superimposed on the SENSE signal during switching. If the ringing is large enough to cause malfunction, attenuate it using an RC filter ($R_4$, $C_{12}$). Place the RC filter as close to the IC as possible.
- Place $R_{SENSE}$ close to the FET source.
- If SW waveform ringing is large, place ceramic capacitors ($C_{15}$, $C_{16}$) near the D cathode and between it and VSS to reduce the ringing.
- If the SW waveform ringing propagates to $V_{OUT}$ and causes unstable operation, place ceramic capacitors ($C_{13}$, $C_{14}$) near the VOUT pin and between it and VSS.
- To reduce ringing in the SW waveform, inserting a resistor ($R_3$) in the FET gate line is effective, but is a trade-off with efficiency.

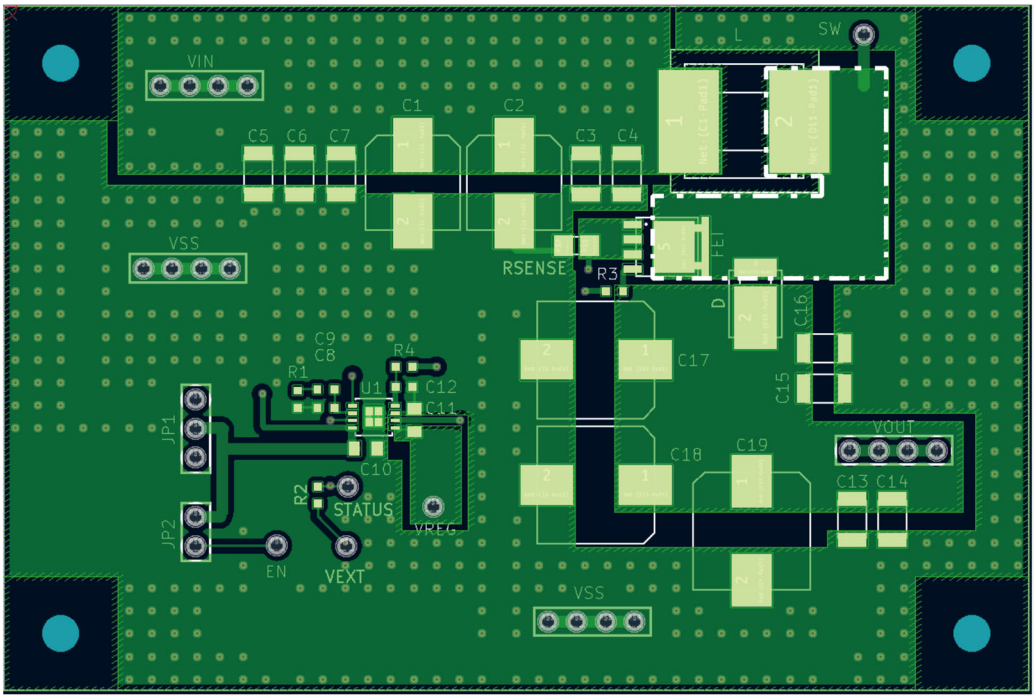



**Figure 7 Top Layer (First Layer)**

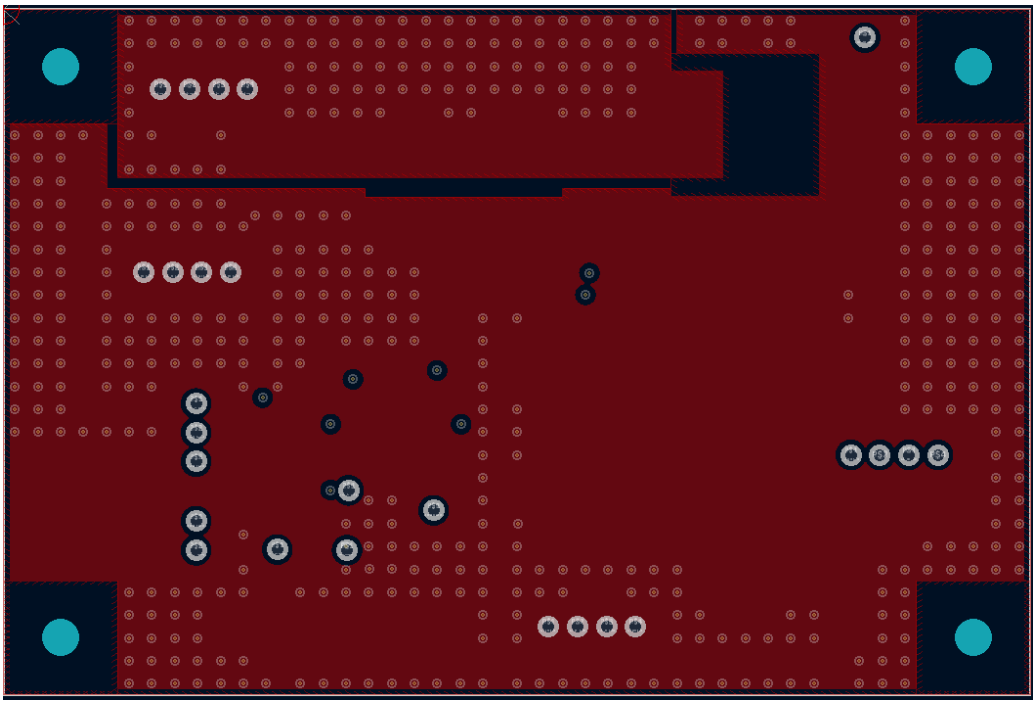


**Figure 8 Internal Layer 1 (Second Layer)**

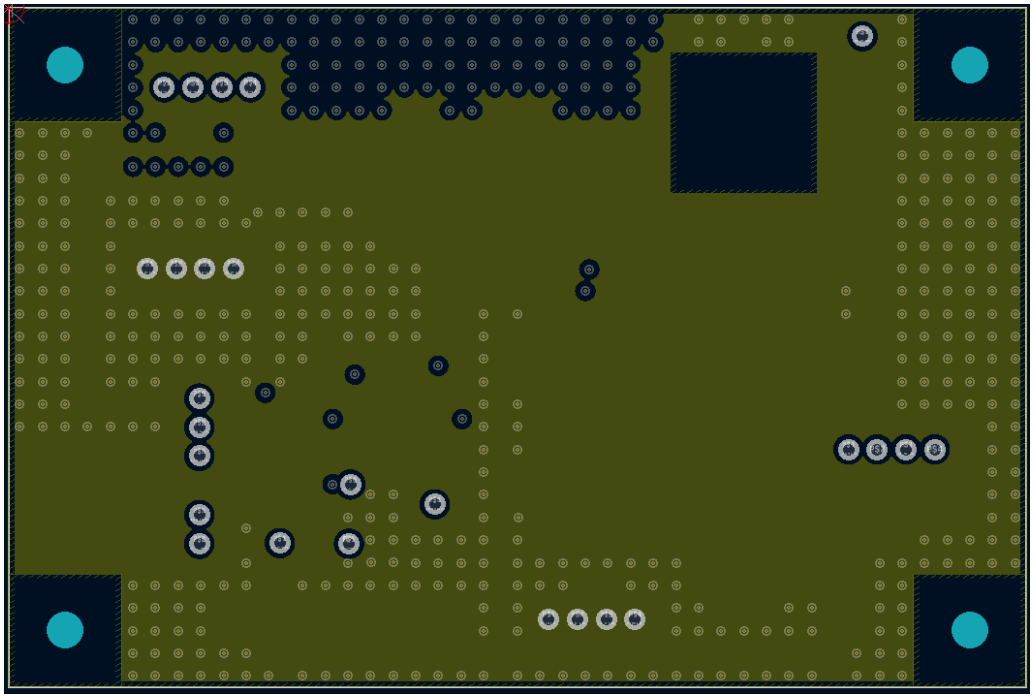


**Figure 9 Internal Layer 2 (Third Layer)**

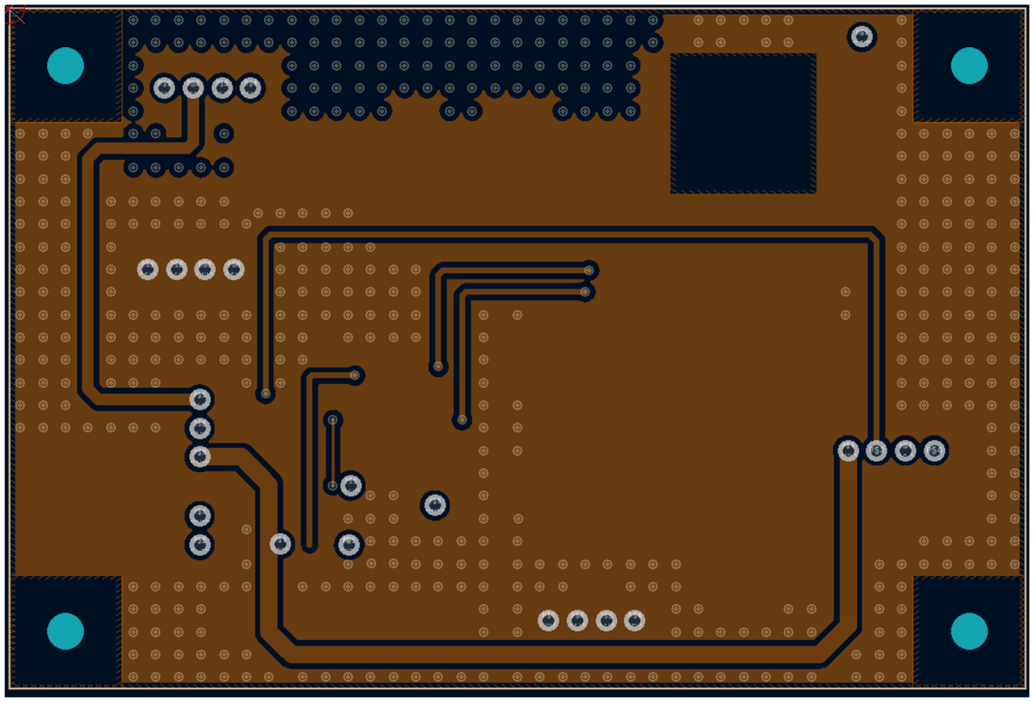


**Figure 10 Bottom Layer (Fourth Layer)**

**Caution The above pattern diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to determine the pattern.**

## 4. Precautions

- The usages described in this application note are typical examples using ICs of ABLIC Inc.
  Perform thorough evaluation before use.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
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## 5. Related Sources

Refer to the following datasheet for details of the S-19989/19999 Series.

**S-19989 Series Datasheet**
**S-19999 Series Datasheet**

The information described in this application note and the datasheet is subject to change without notice.
Contact our sales representatives for details.
Regarding the newest version of the datasheet, select product category and product name on our website, and download the PDF file.

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