CMOS IC Application Note

S-19932/19933 Series NOISE COUNTERMEASURES AND CISPR25 MEASUREMENT RESULTS

Rev.1.0_00

This application note is a reference describing recommended noise suppression parts and board layouts that help reduce conductive noise and emission noise for the S-19932/19933 Series. It also summarizes CISPR25 compliant measurement results.

Refer to the datasheets of the S-19932/19933 Series for details and specs.

Contents

1. Need for Noise Suppression Parts

Figure 1 shows the results of a voltage method measurement of a circuit to which no noise suppression parts have been applied. Although the measurement results significantly exceeded the CISPR25 class 5 specifications, this is not limited to the S-19932/19933 Series as general switching regulator ICs exhibit the similar tendency. For this reason, noise suppression parts must be applied to allow the IC to meet the stringent CISPR25 class 5 requirements.

S-19933A (2.2 MHz), V_{IN} = 13 V, V_{OUT} = 5 V, I_{OUT} = 600 mA, without noise suppression parts

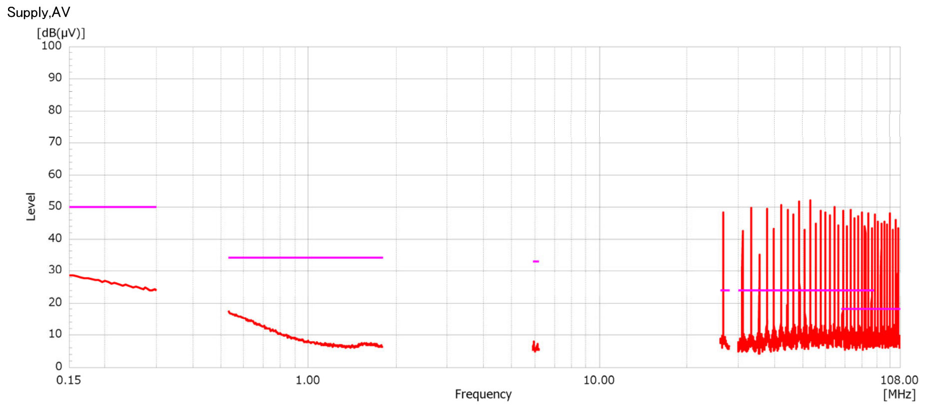


Figure 1

Figure 2 is a circuit diagram to which the recommended noise suppression parts L2, C_{F2}, and C_{F4} listed in **Table 1** have been added. **Figure 3** shows the results of a voltage method measurement carried out on this circuit. The addition of noise suppression parts reduces noise by as much as 20 MHz or more allowing the IC to meet CISPR25 class 5 requirements. Also, the S-19932/19933 Series optimally adjusts the SW pin slew rate in the IC so that the minimum of noise suppression parts will obtain a substantial margin.

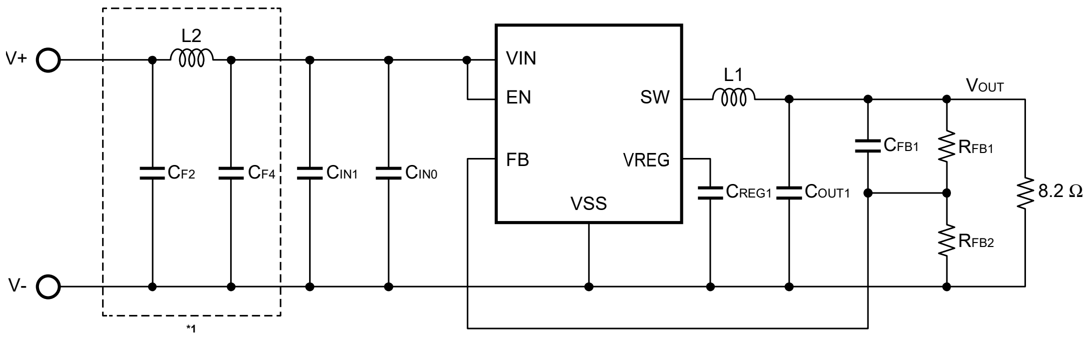


Table 1

Parts Name	Value
C_{F2}	4.7 μF
L2	4.7 μH
C_{F4}	4.7 μF

***1.** Noise suppression parts

Figure 2

S-19933A (2.2 MHz), V_{IN} = 13 V, V_{OUT} = 5 V, I_{OUT} = 600 mA, with noise suppression parts

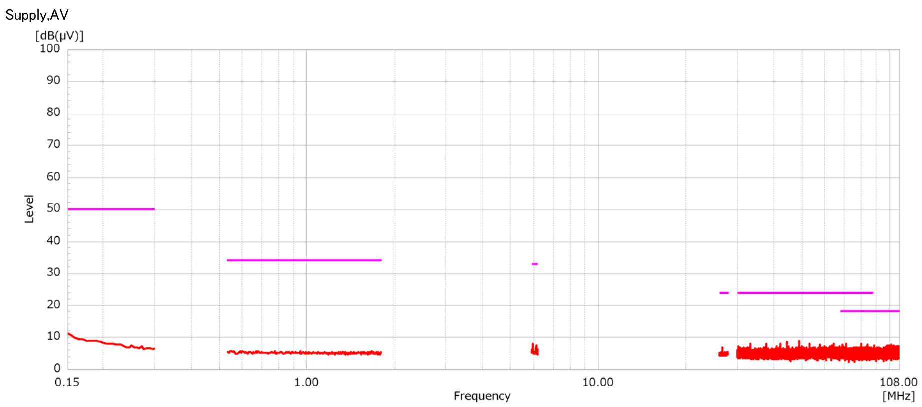


Figure 3

2. Board Layout

2. 1 Placement of input capacitors (C_{IN0}, C_{IN1}) and VIN and VSS layouts

The placement of input capacitors and VIN and VSS wirings are crucial. The input capacitors are of paramount importance and should be placed as close to the IC as possible and on the same surface layer.
C_{IN1} is an essential capacitor to ensure stable IC operation and to suppress noise. C_{IN0} is a capacitor of approximately 0.1 μF which is connected in parallel to C_{IN1}. Add this capacitor as required to suppress mainly 10 MHz or larger noise.
Figure 4 shows an example of placing input capacitors in the immediate vicinity of the IC. The bold line indicates the current path the instant the high side power MOS FET in the IC turns on. First, current flows from the input capacitors to the VIN pin. Next, the current goes through the high side power MOS FET which is ON and the parasitic capacitance of low side power MOS FET which is OFF, both of which are inside the IC, in turn. Finally, the current returns to the input capacitors from the VSS pin. In this example, the reduction of impedance in the current path minimizes the noise generated in VIN and VSS wirings.
By contrast, **Figure 5** shows an example of input capacitors placed away from the IC and where the VSS pin is not connected to the VSS directly below the IC. At this time, there is a parasitic capacitance (L_{p1}) between the input capacitors and the VIN pin. In addition, as the current path between the input capacitors and the VSS pin is significantly extended, the parasitic capacitances ($L_{p2} + L_{p3} + L_{p4}$) extremely become large. In this example, impedance in the current path is increased and the noise generated in VIN and VSS wirings become larger.

Good example

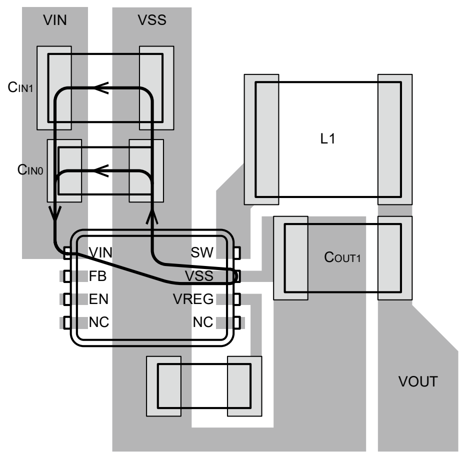


Figure 4

Bad example

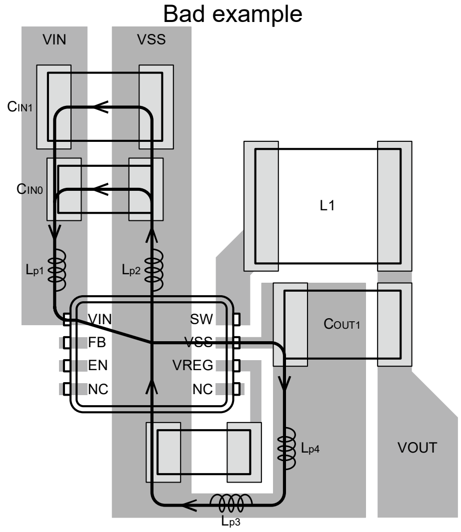


Figure 5

2. 2 Placement and layout of Inductor (L1)

The wiring area of the SW pin should be minimized. Reduce the wiring length within the allowable current capacity range. The rectangular wave voltage output from the SW pin contains high-frequency components, which could cause SW wiring to act as an antenna and thereby increase emission noise. In addition, as the high-frequency components in the rectangular wave voltage previously mentioned are transmitted from the SW pin to VOUT via the parasitic capacitance, SW wiring must be kept apart from VOUT wiring. Select a closed magnetic path inductor with low emission noise.
Figure 6 shows an example where the wiring area between the SW pin and L1 is reduced and the distance between SW wiring and VOUT wiring is extended.
By contrast, **Figure 7** shows an example where the SW wiring area is excessively large, the distance between SW wiring and VOUT wiring is short, and the parasitic capacitance (C_p) is large.

Good example

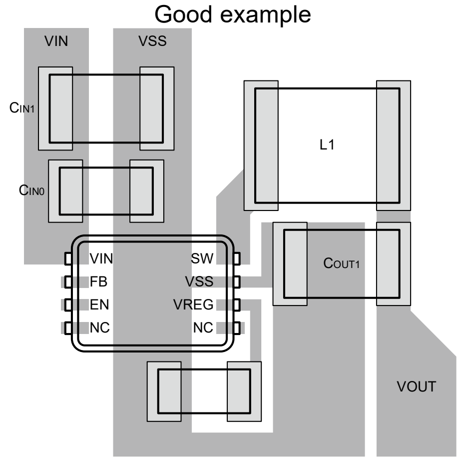


Figure 6

Bad example

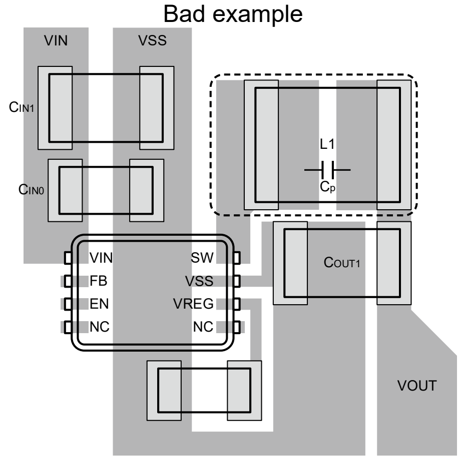


Figure 7

2. 3 Placement and layout of output capacitor (C_{OUT1})

Place C_{OUT1} close to the IC.
If the area of the current path indicated by the bold line (SW pin → L1 → C_{OUT1} → VSS pin) is reduced, the emission noise to be generated will be minimized.
Be sure to pull out VOUT wiring after routing through the C_{OUT1} land. If this is not the case, smoothing due to L1 and C_{OUT1} is weakened causing high-frequency components in the rectangular wave voltage of SW pin to be conducted to VOUT. Similarly, when increasing the line width, pull out a wiring after routing through C_{OUT1} land.

Figure 8 is an example where the current path area is narrowed. VOUT wiring is pulled out after routing through the C_{OUT1} land.
By contrast, **Figure 9** is an example where the distance between the IC and C_{OUT1} is long and the current path area is large. VOUT wiring is pulled out from L1 land without routing through C_{OUT1} land.
Figure 10 is an example where VOUT line width is excessively increased before routing through C_{OUT1} land.

Good example

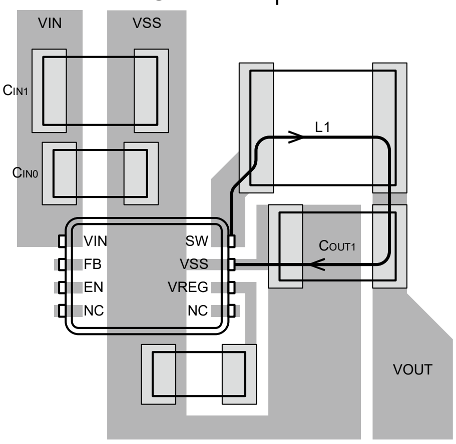


Figure 8

Bad example 1

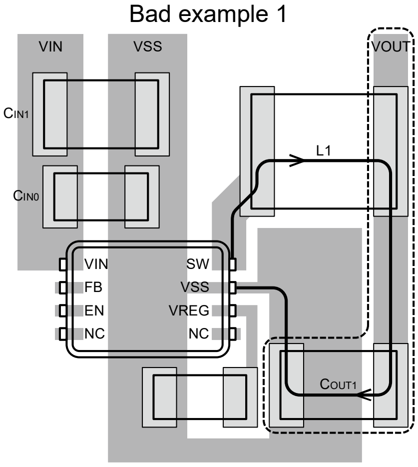


Figure 9

Bad example 2

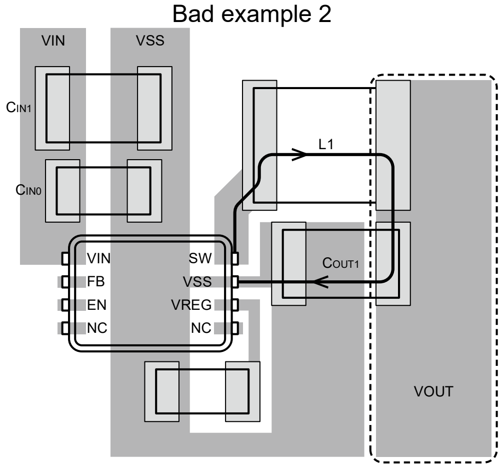


Figure 10

2. 4 Recommended board layout

Figure 11 shows the recommended board layout that reflects the explanations previously mentioned.

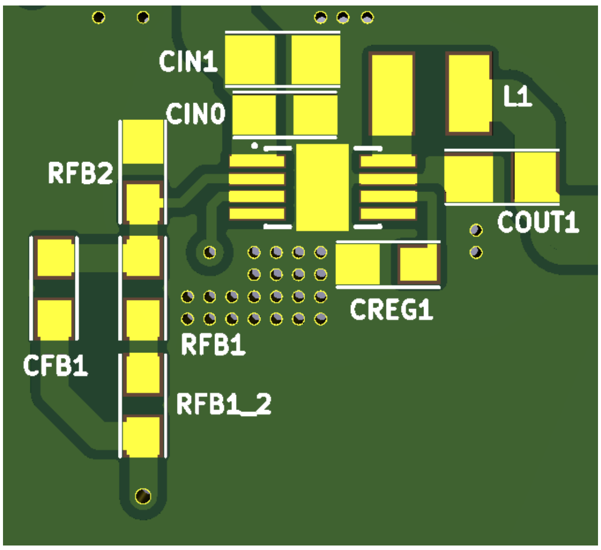


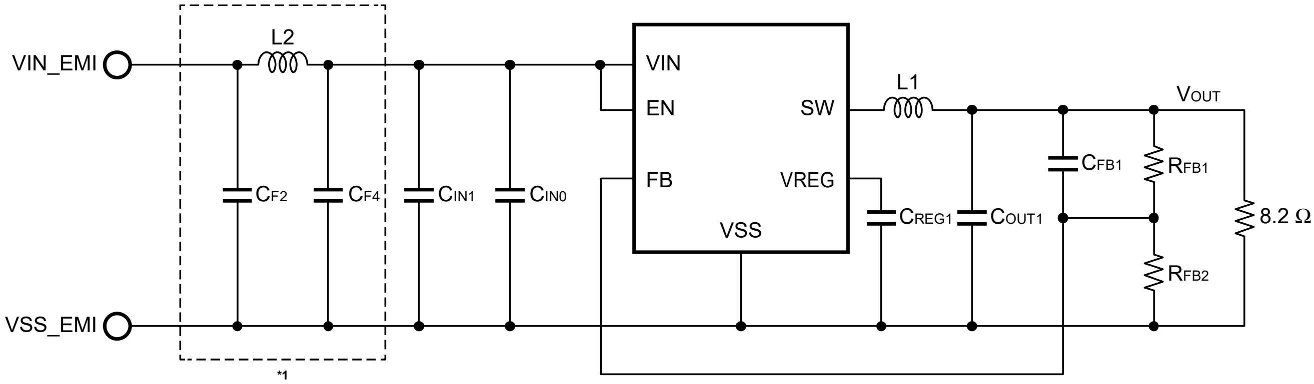
Figure 11

3. Measurement Conditions and Measurement Results

3. 1 Measurement condition 1

Figure 12 shows a circuit diagram of S-19933A Evaluation Board. The parts listed in **Table 2** are mounted.

S-19933A (2.2 MHz), V_{IN} = 13 V, V_{OUT} = 5 V, I_{OUT} = 600 mA,
Compliant with CISPR25 Edition 4.0 2016-10



***1.** Noise suppression parts

Figure 12 Circuit Diagram of S-19933A Evaluation Board

Table 2

Symbol	Value	Part Number	Manufacturer
C_{F2}	4.7 μF	CGA4J1X7R1H475K125AC	TDK Corporation
L2	4.7 μH	TFM252012ALVA4R7MTAA	TDK Corporation
C_{F4}	4.7 μF	CGA4J1X7R1H475K125AC	TDK Corporation
C_{IN1}	4.7 μF	CGA4J1X7R1H475K125AC	TDK Corporation
C_{IN0}	0.1 μF	CGA3E2X7R1H104K	TDK Corporation
L1	4.7 μH	TFM252012ALVA4R7MTAA	TDK Corporation
C_{REG1}	1.0 μF	CGA3E1X7R1C105K080AC	TDK Corporation
C_{OUT1}	10 μF	CGA4J3X7S1A106K125AB	TDK Corporation
C_{FB}	33 pF	–	–
R_{FB1}	84 kΩ	–	–
R_{FB2}	16 kΩ	–	–

Figure 13 shows the actual board.

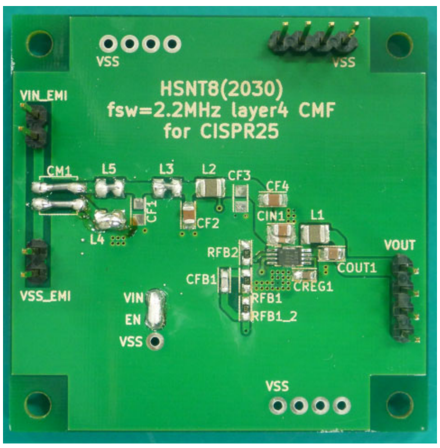
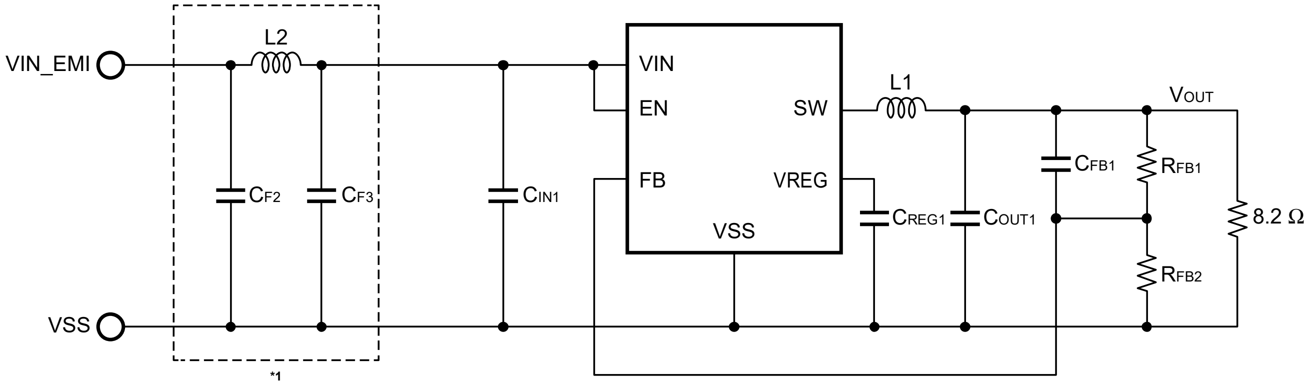


Figure 13

3. 2 Measurement condition 2

Figure 14 shows a circuit diagram of S-19933C Evaluation Board. The parts listed in **Table 3** are mounted.

S-19933C (400 kHz), V_{IN} = 13 V, V_{OUT} = 5 V, I_{OUT} = 600 mA,
Compliant with CISPR25 Edition 4.0 2016-10



***1.** Noise suppression parts

Figure 14 Circuit Diagram of S-19933C Evaluation Board

Table 3

Symbol	Value	Part Number	Manufacturer
C_{F2}	4.7 μF	CGA4J1X7R1H475K125AC	TDK Corporation
L2	4.7 μH	TFM252012ALVA4R7MTAA	TDK Corporation
C_{F4}	4.7 μF	CGA4J1X7R1H475K125AC	TDK Corporation
C_{IN1}	4.7 μF	CGA4J1X7R1H475K125AC	TDK Corporation
L1	33 μH	SPM6545VT-330M-D	TDK Corporation
C_{REG1}	1.0 μF	CGA3E1X7R1C105K080AC	TDK Corporation
C_{OUT1}	47 μF	CGA9N3X7R1C476M230KB	TDK Corporation
C_{FB}	100 pF	–	–
R_{FB1}	525 kΩ	–	–
R_{FB2}	100 kΩ	–	–

Figure 15 shows the actual board.

Figure 15

3. 3 Measurement results of voltage method

Figure 16 and **Figure 17** show measurement results of voltage method.

S-19933A (2.2 MHz) Supply: VIN_EMI, Return: VSS_EMI, AV: average

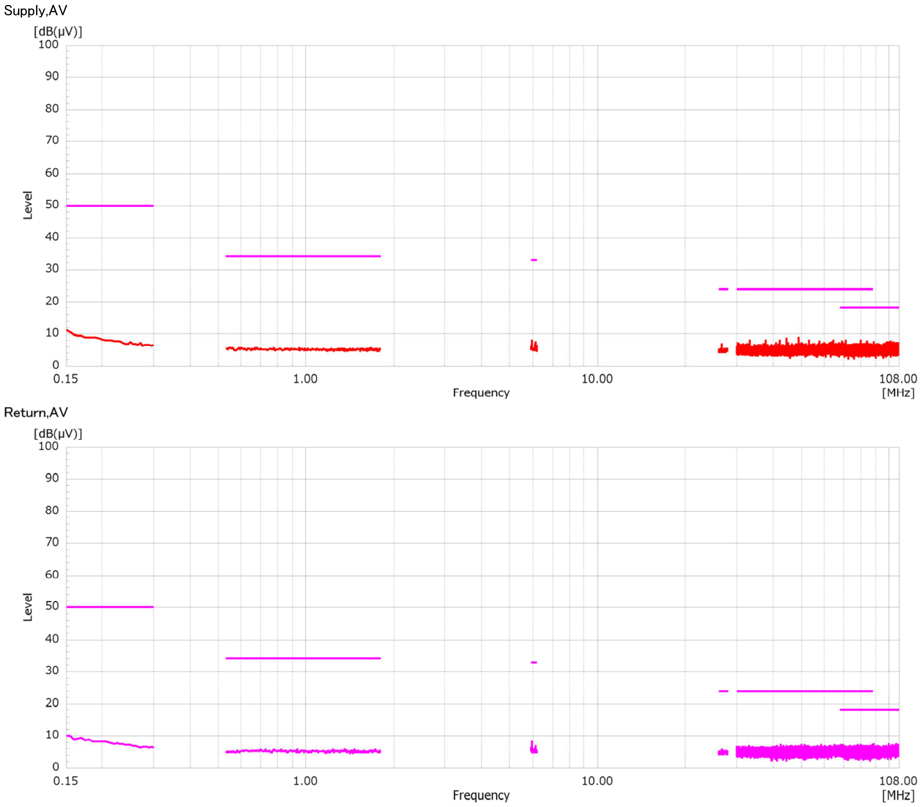


Figure 16

S-19933C (400 kHz) Supply: VIN_EMI, Return: VSS, AV: average

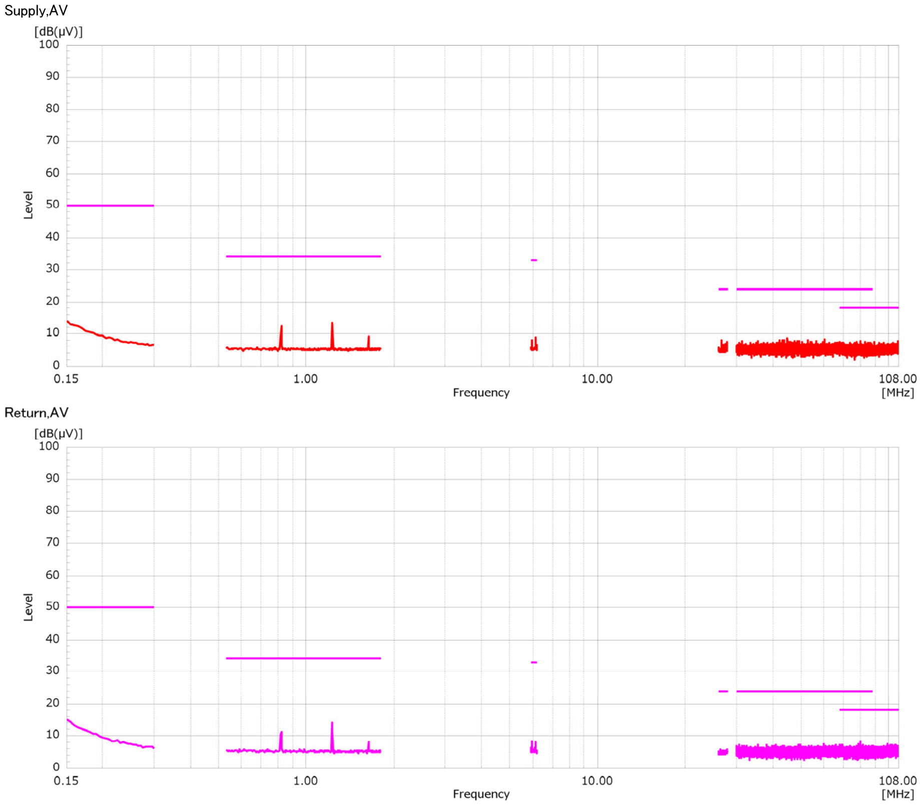


Figure 17

3. 4 Measurement results of ALSE method

Figure 18 to **Figure 21** show measurement results of ALSE method.

S-19933A (2.2 MHz) V: vertical, H: horizontal, AV: average

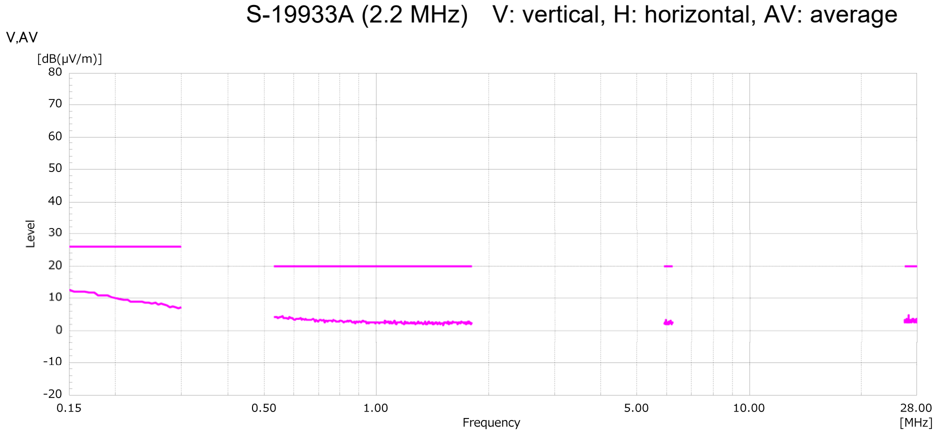


Figure 18

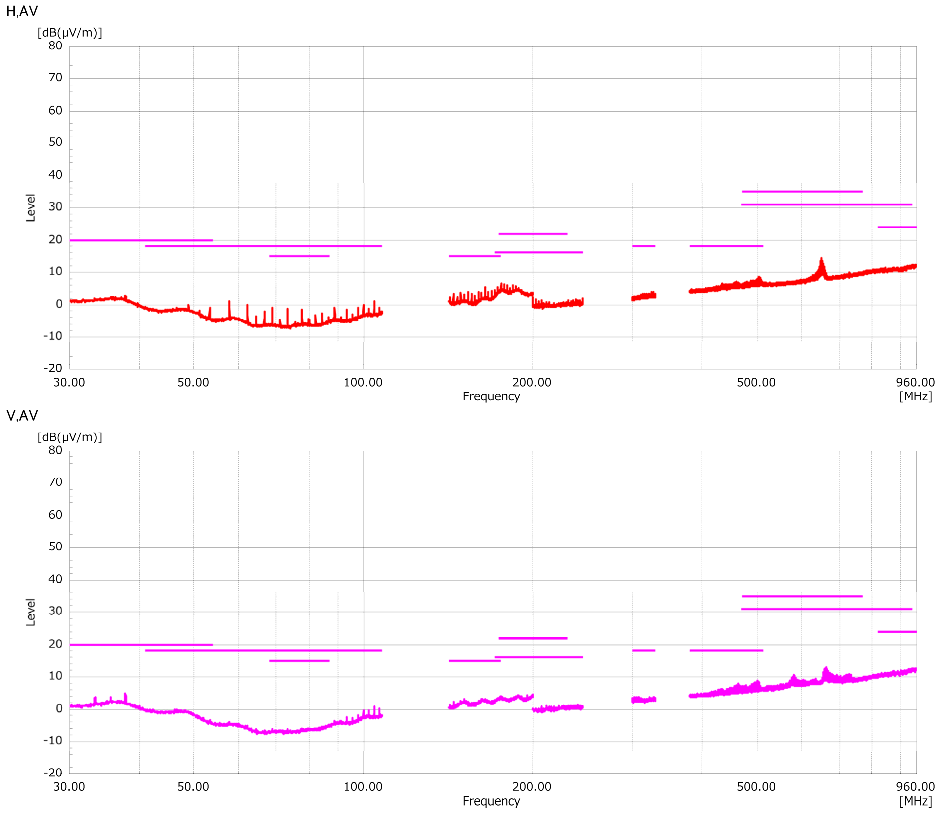


Figure 19

S-19933C (400 kHz) V: vertical, H: horizontal, AV: average

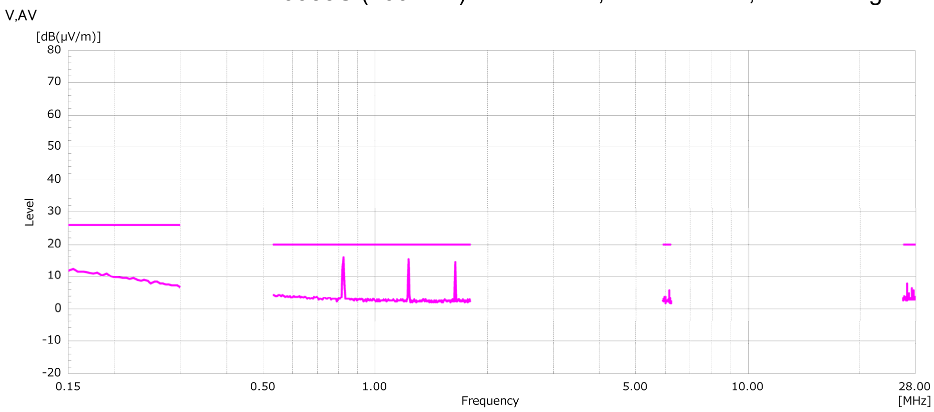


Figure 20

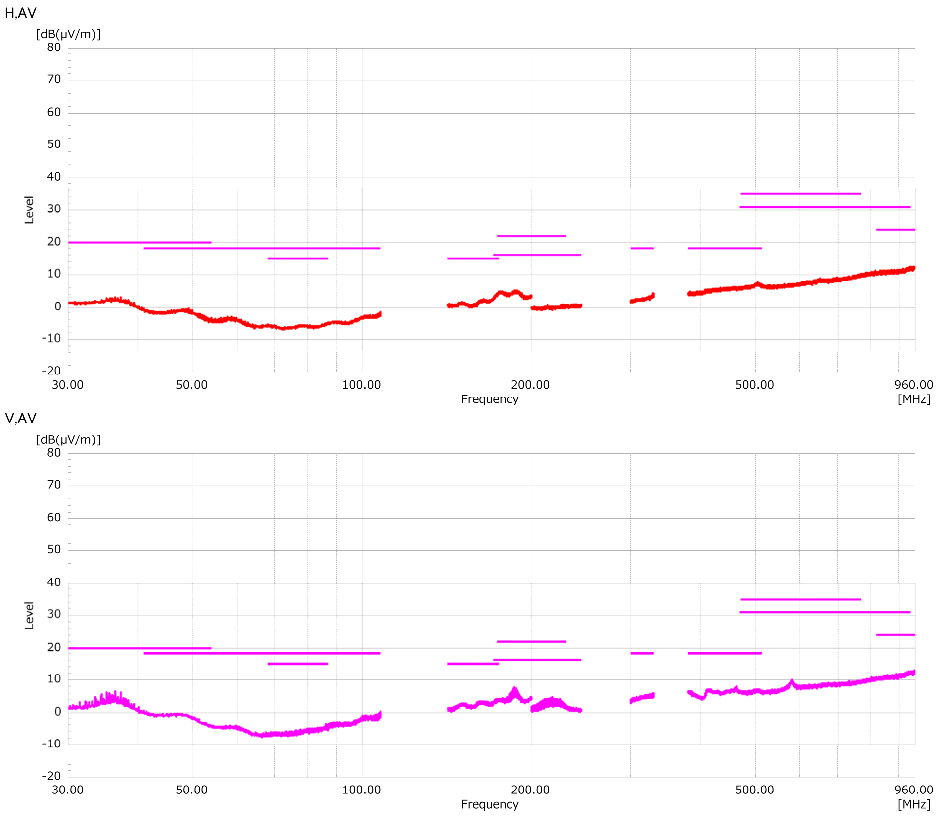


Figure 21

4. Precautions

- The usages described in this application note are typical examples using ICs of ABLIC Inc.
  Perform thorough evaluation before use.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

5. Related Sources

Refer to the following datasheets for details of the S-19932/19933 Series.

S-19932A/19932B/19933A/19933B Series Datasheet
S-19932C/19932D/19933C/19933D Series Datasheet

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