CMOS IC Application Note

# S-19560B Series Application Examples and Component Selection Methods

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This application note is a method of external parts selection and recommended board layouts for the S-19560B Series. Refer to the datasheet for details and specs.

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# 1. Ch1 Output Current Calculation Method

The S-19560B Series power supply configuration is shown in **Figure 1**.
The VOUT1 pin serves as both the Ch1 feedback pin (FB) and the Ch2 and Ch3 power supply. As such, note that it is not possible to supply the entire Ch1 output current ($I_{OUT1}$) to the load.

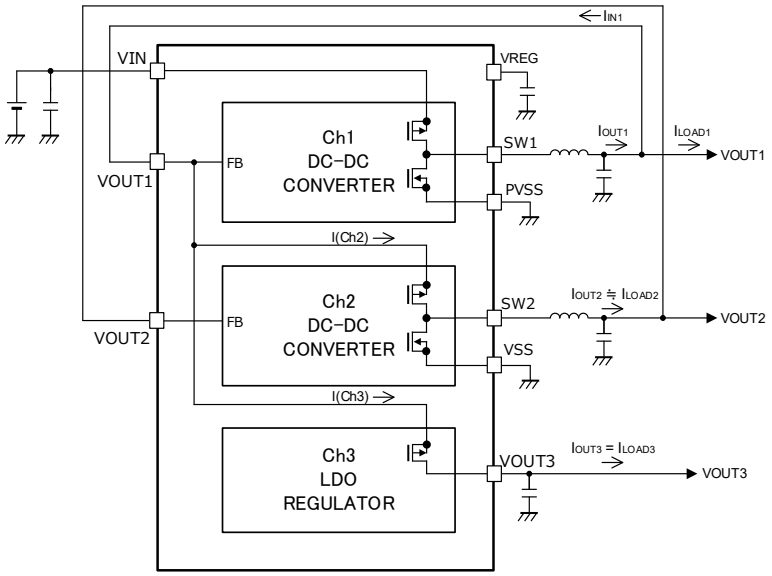



**Figure 1 Power Supply Configuration Diagram**

## 1. 1 Step-down DC-DC converter input current calculation method

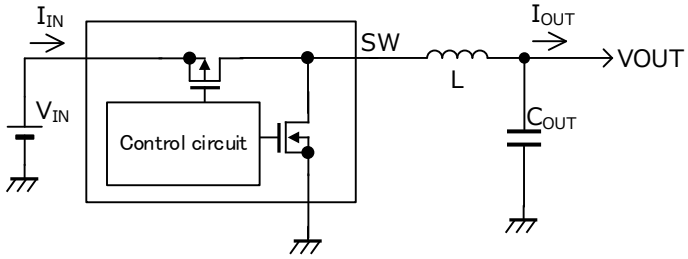



**Figure 2 Standard Step-down DC-DC Converter**

Each of the variables in **Figure 2** are defined as follows.

| | |
|---|---|
| $V_{IN}$: | Input voltage |
| $I_{IN}$: | Input current |
| $V_{OUT}$: | Output voltage |
| $I_{OUT}$: | Output current |
| η: | Conversion efficiency |

Input power × efficiency = output current, so

$V_{IN} \times I_{IN} \times \eta^{*1} = V_{OUT} \times I_{OUT}$

The DC-DC converter input current is

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad \text{..... (1)}$$

***1.** The control circuit self-power consumption is reflected in η.

### 1. 2 LDO regulator input current calculation method

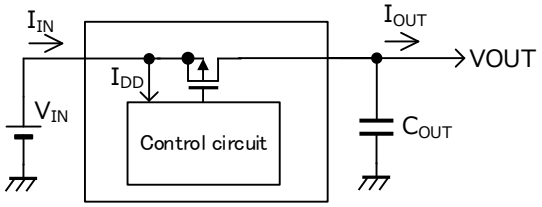



**Figure 3 Standard LDO Regulator**

Each of the variables in **Figure 3** are defined as follows.

| | |
|---|---|
| $V_{IN}$: | Input voltage |
| $I_{IN}$: | Input current |
| $I_{DD}$: | Self-consumption current |
| $V_{OUT}$: | Output voltage |
| $I_{OUT}$: | Output current |

The LDO regulator input current is

$$I_{IN} = I_{OUT} + I_{DD}$$

Here, $I_{OUT} > I_{DD}$, so

$$I_{IN} \approx I_{OUT} \quad \text{..... (2)}$$

### 1. 3 S-19560B Series VOUT1 pin input current calculation

The power supply for the S-19560B Series Ch2 (DC-DC converter) and Ch3 (LDO regulator) are supplied from the VOUT1 pin.
In order to determine the allowable current level ($I_{LOAD1}$) that can be supplied from the VOUT1 output voltage to the load, it is necessary to calculate the input currents of Ch2 and Ch3.
In addition, because the VOUT1 pin also functions as the Ch1 feedback pin, a separate power supply cannot be connected.

Each of the variables in the following formulas are defined as follows. Refer to **Figure 1** for the relationships between $I_{OUT1}$, $I_{OUT2}$, $I_{OUT3}$, $I_{LOAD1}$, $I_{LOAD2}$, and $I_{LOAD3}$.

| | |
|---|---|
| $V_{OUT1}$: | VOUT1 output voltage |
| $V_{OUT2}$: | VOUT2 output voltage |
| $I_{OUT1}$: | Ch1 output current |
| $I_{OUT2}$: | Ch2 output current |
| $I_{OUT3}$: | Ch3 output current |
| $I_{LOAD1}$: | VOUT1 load current |
| $I_{LOAD2}$: | VOUT2 load current |
| $I_{LOAD3}$: | VOUT3 load current |
| $\eta_2$: | Ch2 conversion efficiency |

As such, if the Ch2 input current ($I_{(Ch2)}$) and Ch3 input current ($I_{(Ch3)}$) are calculated using formulas (1) and (2), then the VOUT2 pin input current will be extremely small, so

$$I_{OUT2} \approx I_{LOAD2}$$

therefore, the following formula is derived from formula (1).

$$I_{(Ch2)} = \frac{V_{OUT2} \times I_{LOAD2}}{V_{OUT1} \times \eta_2}$$

From **Figure 1**

$$I_{OUT3} = I_{LOAD3}$$

therefore, the following formula is derived from formula (2).

$$I_{(Ch3)} \approx I_{LOAD3}$$

The VOUT1 pint input current ($I_{IN1}$) will be as follows.

$$I_{IN1} = I_{(Ch2)} + I_{(Ch3)}$$

$$= \frac{V_{OUT2} \times I_{LOAD2}}{V_{OUT1} \times \eta_2} + I_{LOAD3}$$

The maximum Ch1 output current ($I_{OUT1}$) is 600 mA. The maximum current ($I_{LOAD1(max)}$) which Ch1 can directly supply to the load is this value minus the current ($I_{IN1}$) supplied to Ch2 and Ch3.

$$I_{LOAD1(max)} = 600\ mA - I_{IN1}$$

## 2. Relationship between Loss and Heat Generation

Loss generated in the S-19560B Series becomes heat, increasing the temperature of the junction. Therefore, the estimation of loss is extremely important.
Each of the variables in the following formulas are defined as follows.

| | |
|---|---|
| $V_{OUT1}$: | VOUT1 output voltage |
| $V_{OUT2}$: | VOUT2 output voltage |
| $I_{OUT1}$: | Ch1 output current |
| $I_{OUT2}$: | Ch2 output current |
| $I_{OUT3}$: | Ch3 output current |
| $\eta_1$: | Ch1 conversion efficiency |
| $\eta_2$: | Ch2 conversion efficiency |

### 2. 1 Ch1, Ch2 (DC-DC converter) loss

The main sources of loss in a DC-DC converter are losses generated inside the IC and loss generated by external components. The total loss value can be estimated from the efficiency characteristics.
The loss for Ch1 and Ch2 ($P_{LOSS1}$, $P_{LOSS2}$) can be calculated from the following formulas.

$$P_{LOSS1} = V_{OUT1} \times I_{OUT1} \times \left(\frac{1 - \eta_1}{\eta_1}\right)$$

$$P_{LOSS2} = V_{OUT2} \times I_{OUT2} \times \left(\frac{1 - \eta_2}{\eta_2}\right)$$

Estimate loss within the output current range that will actually be used.

### 2. 2 Ch3 (LDO regulator) loss

The main source of loss in an LDO regulator can be found by multiplying the input-output voltage difference by the output current.
The loss for Ch3 ($P_{LOSS3}$) can be calculated from the following formula.

$$P_{LOSS3} = (V_{OUT1} - V_{OUT3}) \times I_{OUT3}$$

For the S-19560B Series, reducing the VOUT1 output voltage will decrease the Ch3 (LDO regulator) loss. Determine the setting value for VOUT1 output voltage while taking the following conditions into consideration.

- Possible setting range: 3.3 V to 5.5 V
- At least 0.7 V higher than the $V_{OUT2}$ setting voltage
- At least 0.3 V higher than the $V_{OUT3}$ setting voltage
- If connecting an external LDO regulator, ensure that the input-output voltage difference required for the external LDO regulator is secured.

### 2. 3 Heat generation amount calculation

Overall loss in the S-19560B Series can be calculated from the following formula.

$$P_{LOSS} = P_{LOSS1} + P_{LOSS2} + P_{LOSS3}$$

The junction temperature ($T_j$) caused by the generated loss $P_{LOSS}$ can be calculated from the following formula. The thermal resistance value ($\theta_{JA}$) is shown in **Table 1**.

$$T_j = P_{LOSS} \times \theta_{JA} + Ta$$

**Table 1**

| Item | Symbol | Condition | | Min. | Typ. | Max. | 単位 |
|---|---|---|---|---|---|---|---|
| Junction-to-ambient thermal resistance*1 | $\theta_{JA}$ | HSNT-8(2030) | Board A | - | 181 | - | °C/W |
| | | | Board B | - | 135 | - | °C/W |
| | | | Board C | - | 40 | - | °C/W |
| | | | Board D | - | 42 | - | °C/W |
| | | | Board E | - | 32 | - | °C/W |

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ **Power Dissipation**" and "**Test Board**" of S-19560B Series datasheet for details.

# 3. Typical Usage Examples

## 3. 1 Example use as a power supply for a camera module

The input voltage of 4 V to 16 V from VIN is first stepped down to approximately 3.3 V to 3.6 V in Ch1, then output to VOUT1.
The VOUT1 output voltage is reduced to low noise in the S-19255 series (LDO regulator)*1 and used as an analog power supply for the image sensor. For the Core power supply, which requires the most current, the VOUT2 output voltage which is the output from Ch2 is used to support the high current requirement. The VOUT3 output voltage which is the Ch3 output is used as the power supply for the I/O and serializer.

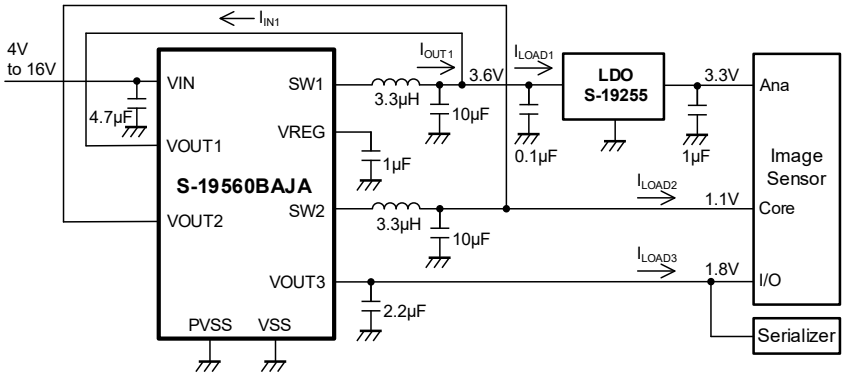



**Figure 4**

【Design example】
$V_{IN}$ = 6.0 V
S-19560BAJA
$V_{OUT1}$ = 4.0 V
$V_{OUT2}$ = 1.1 V
$V_{OUT3}$ = 1.8 V
$I_{LOAD1}$ = 200 mA
$I_{LOAD2}$ = 400 mA
$I_{LOAD3}$ = 200 mA
$\eta_1$ = 87%*2
$\eta_2$ = 84%*2
$\theta_{JA}$ = 32°C/W

$$I_{IN1} = \frac{V_{OUT2} \times I_{LOAD2}}{V_{OUT1} \times \eta_2} + I_{LOAD3}$$
$$= 331 \text{ mA}$$

$$I_{OUT1} = I_{IN1} + I_{LOAD1}$$
$$= 531 \text{ mA}$$

$$P_{LOSS} = P_{LOSS1} + P_{LOSS2} + P_{LOSS3}$$
$$= V_{OUT1} \times I_{OUT1} \times \left(\frac{1 - \eta_1}{\eta_1}\right) + V_{OUT2} \times I_{OUT2} \times \left(\frac{1 - \eta_2}{\eta_2}\right) + (V_{OUT1} - V_{OUT3}) \times I_{OUT3}$$
$$= 317 \text{ mW} + 83 \text{ mW} + 440 \text{ mW}$$
$$= 841 \text{ mW}$$

Increasing junction temperature
$\Delta T_j = 0.841 \times 32 = 26.9°C$

***1***. Refer to S-19255 Series datasheet for details.
***2***. Refer to "■ **Reference Data**" of S-19560B Series datasheet for details.

**Caution The above are theoretical calculation values. Perform thorough evaluation and verify characteristics in the actual application.**

### 3. 2 Example where Ch2 output is unused

VOUT2 is the feedback input pin for Ch2. The SW2 pin will be either "L" or "H" level depending on the relationship between the VOUT2 setting voltage value and the actual VOUT2 pin voltage. Therefore, if a voltage close to the setting value is applied to the VOUT2 pin, the SW2 pin output may repeatedly switch between "L" and "H". So, connecting VOUT2 to VOUT1, which has a sufficiently higher voltage, the SW2 pin voltage is fixed at "L" and becomes stable.

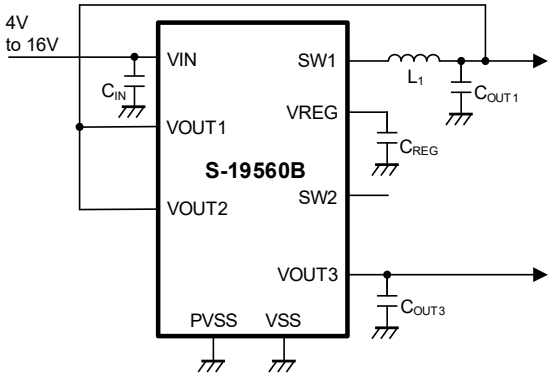



**Figure 5**

### 3. 3 Example where Ch3 output is unused

If an output capacitance is not connected to the VOUT3 pin, the VOUT3 output voltage may become unstable, becoming an unintended source of noise. Even if Ch3 is not used, connect $C_{OUT3}$. If $C_{OUT3}$ must be left unconnected, connect VOUT3 to VOUT1. This will prevent the VOUT3 output voltage from becoming a noise source.

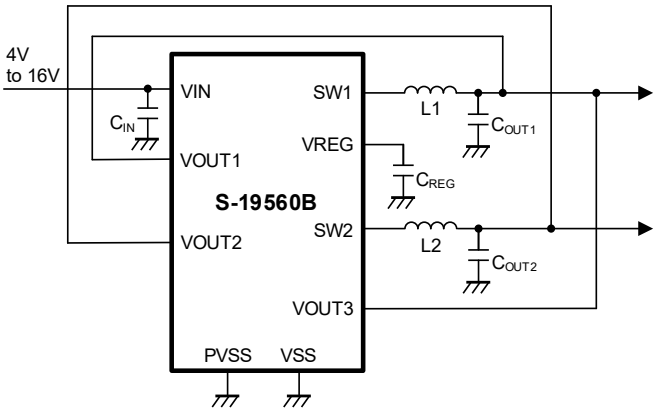



**Figure 6**

# 4. Inductor Selection

The recommended inductance value for the S-19560B Series is 3.3 µH. If a 2.2 µH inductor can be used, the mounting area can be reduced. In general, reducing the inductance value will increase the ripple components which flow through the coil, resulting in a higher peak current ($I_{PK}$) even at the same $I_{OUT}$. As such, the current limit value may be exceeded in some conditions.
In addition, the ripple voltage generated in the output will also increase.
Furthermore, there will also be an increased likelihood of subharmonic oscillation, which is a characteristic phenomenon of DC-DC converters in current mode. It is recommended to use in conditions where Duty < 50% in order to reduce the risk of subharmonic oscillation.

## 4. 1 Inductor peak current calculation

The peak current ($I_{PK}$) which flows to a standard step-down DC-DC converter inductor shown in **Figure 2** can be calculated from the following formula.
$f_{OSC}$ represents the switching frequency.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{OSC} \times L \times V_{IN}}$$

$$I_{PK} = I_{OUT} + \frac{\Delta I_L}{2}$$

## 4. 2 VOUT ripple voltage calculation

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times f_{OSC} \times C_{OUT}}$$

## 4. 3 Step-down DC-DC converter duty calculation

$$\text{Duty} = \frac{V_{OUT}}{V_{IN}}$$

## 4. 4 Specific product examples with an inductance value of 2.2 µH

**Table 2**

| Manufacturer | Part Number | Withstanding Voltage | Temperature Range | Dimensions (L × W × H) |
|---|---|---|---|---|
| TDK Corporation | TFM201210ALMA2R2MTAA | 20 V | -55°C to 150°C | 2.0 mm × 1.25 mm × 1.0 mm |
| TDK Corporation | TFM201610ALMA2R2MTAA | 20 V | -55°C to 150°C | 2.0 mm × 1.6 mm × 1.0 mm |
| Murata Manufacturing Co., Ltd. | DFE2MCAH2R2MJ0 | 40 V | -40°C to 150°C | 2.0 mm × 1.6 mm × 1.2 mm |
| TAIYO YUDEN CO., LTD. | LCCNF2012KKT2R2MAD | 20 V | -55°C to 150°C | 2.0 mm × 1.25 mm × 1.0 mm |
| TAIYO YUDEN CO., LTD. | LCENA2016MKT2R2M0TK | 20 V | -40°C to 150°C | 2.0 mm × 1.6 mm × 1.2 mm |
| Würth Elektronik | 74438343022 | 80 V | -40°C to 125°C | 2.0 mm × 1.6 mm × 1.0 mm |

## 4. 5 Reference data (Inductance value 2.2 µH)

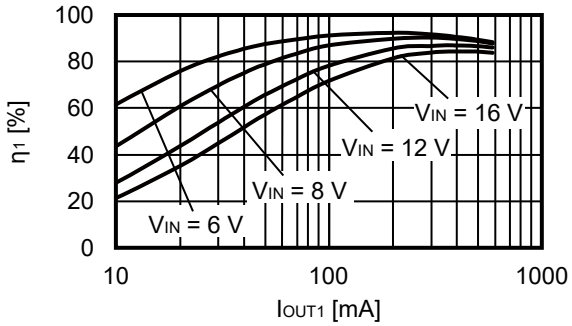
The external parts shown in **Table 3** are used in the reference data. Refer to "■ **Reference Data**" on the S-19560B Series datasheet for reference data for the inductance value of 3.3 µH.

**Table 3**

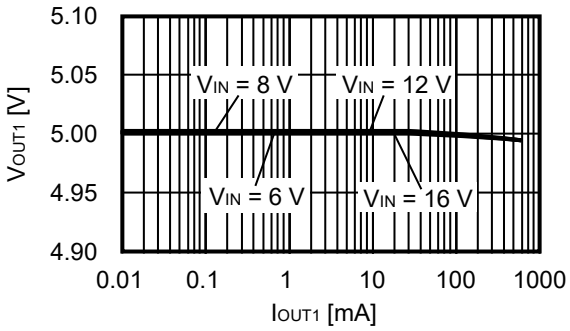
| Symbol | Part Number | Constant | Withstanding Voltage | Dimensions (L × W × H) | Manufacturer |
|---|---|---|---|---|---|
| $C_{IN}$ | CGA4J1X7R1E475K125AC | 4.7 µF | 25 V | 2.0 mm × 1.25 mm × 1.25 mm | TDK Corporation |
| $C_{OUT1}$, $C_{OUT2}$ | CGA4J3X7S1A106K125AB | 10 µF | 10 V | 2.0 mm × 1.25 mm × 1.25 mm | TDK Corporation |
| $C_{OUT3}$ | CGA3E1X7R0J225K080AC | 2.2 µF | 6.3 V | 1.6 mm × 0.8 mm × 0.8 mm | TDK Corporation |
| $C_{REG}$ | CGA3E1X7R1C105K080AC | 1 µF | 16 V | 1.6 mm × 0.8 mm × 0.8 mm | TDK Corporation |
| $L_1$, $L_2$ | TFM201610ALMA2R2MTAA | 2.2 µH | 20 V | 2.0 mm × 1.6 mm × 1.0 mm | TDK Corporation |

### 4. 5. 1 $V_{OUT1}$ = 5.0 V

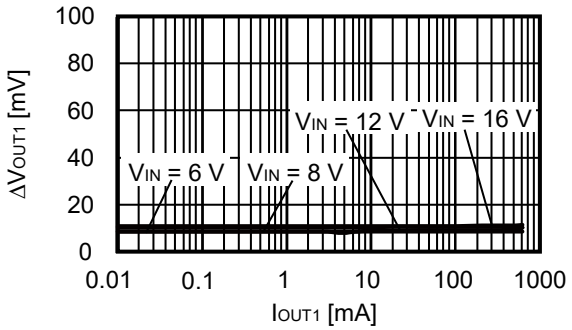
#### 4. 5. 1. 1 Efficiency ($\eta_1$) vs Output current ($I_{OUT1}$)




#### 4. 5. 1. 2 Output voltage ($V_{OUT1}$) vs Output current ($I_{OUT1}$)

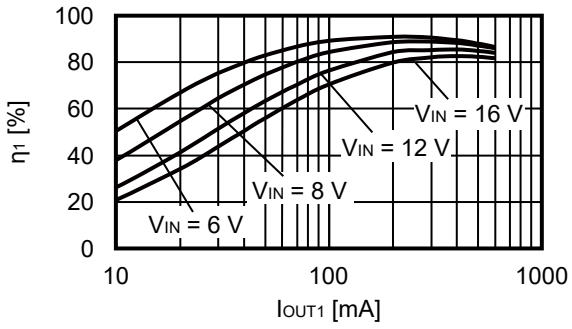



#### 4. 5. 1. 3 Ripple voltage ($\Delta V_{OUT1}$) vs Output current ($I_{OUT1}$)

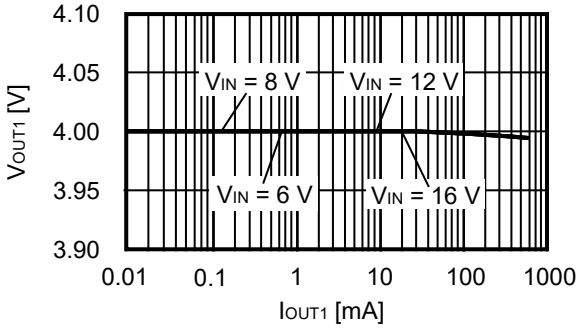


### 4. 5. 2 $V_{OUT1}$ = 4.0 V

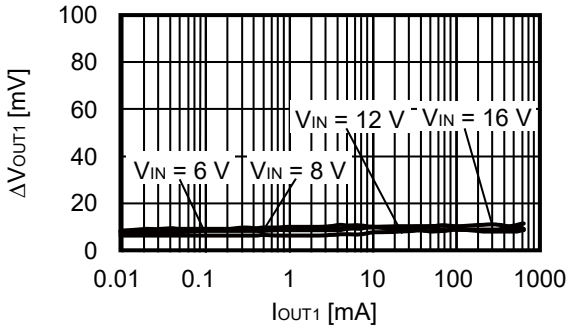
#### 4. 5. 2. 1 Efficiency ($\eta_1$) vs Output current ($I_{OUT1}$)




#### 4. 5. 2. 2 Output voltage ($V_{OUT1}$) vs Output current ($I_{OUT1}$)

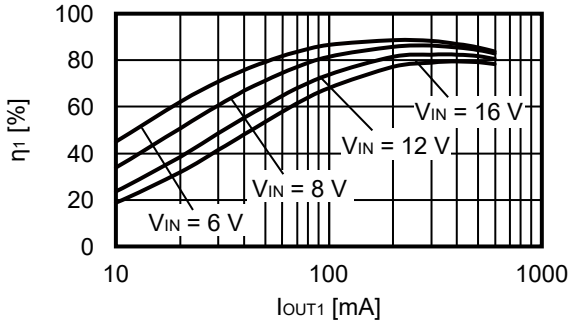



#### 4. 5. 2. 3 Ripple voltage ($\Delta V_{OUT1}$) vs Output current ($I_{OUT1}$)

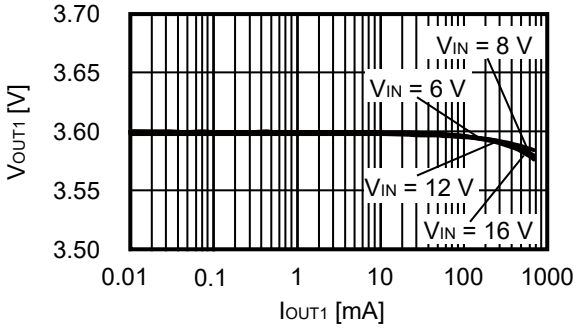



### 4. 5. 3 $V_{OUT1}$ = 3.6 V

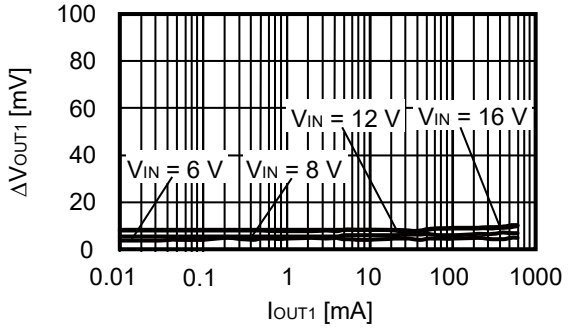
#### 4. 5. 3. 1 Efficiency ($\eta_1$) vs Output current ($I_{OUT1}$)




#### 4. 5. 3. 2 Output voltage ($V_{OUT1}$) vs Output current ($I_{OUT1}$)

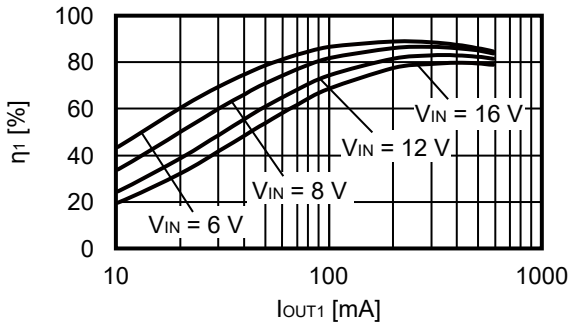



#### 4. 5. 3. 3 Ripple voltage ($\Delta V_{OUT1}$) vs Output current ($I_{OUT1}$)

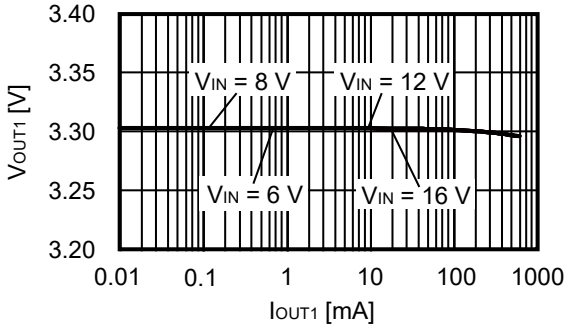


### 4. 5. 4 $V_{OUT1}$ = 3.3 V

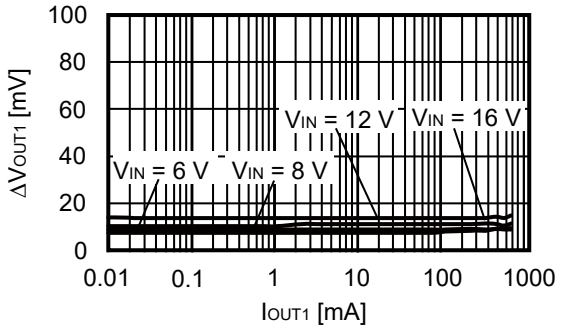
#### 4. 5. 4. 1 Efficiency ($\eta_1$) vs Output current ($I_{OUT1}$)




#### 4. 5. 4. 2 Output voltage ($V_{OUT1}$) vs Output current ($I_{OUT1}$)

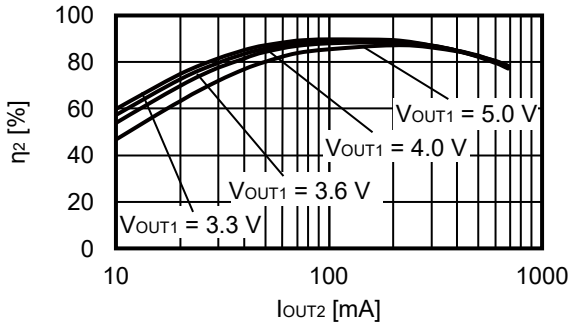



#### 4. 5. 4. 3 Ripple voltage ($\Delta V_{OUT1}$) vs Output current ($I_{OUT1}$)

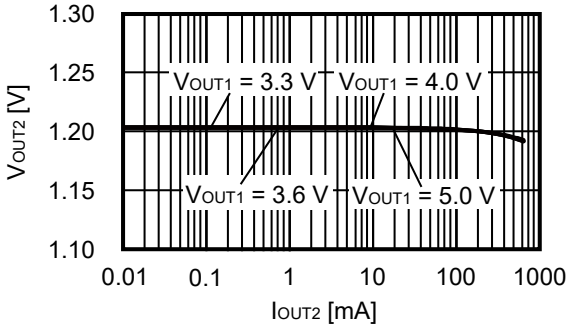



### 4. 5. 5 $V_{OUT2}$ = 1.2 V

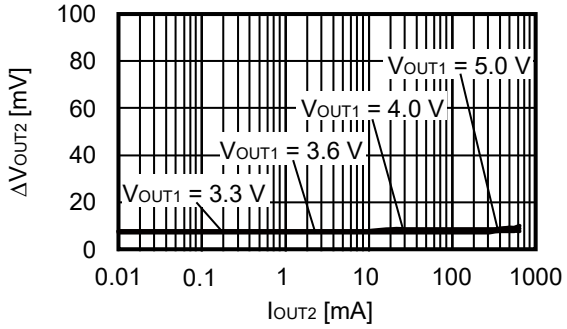
#### 4. 5. 5. 1 Efficiency ($\eta_2$) vs Output current ($I_{OUT2}$)




#### 4. 5. 5. 2 Output voltage ($V_{OUT2}$) vs Output current ($I_{OUT2}$)

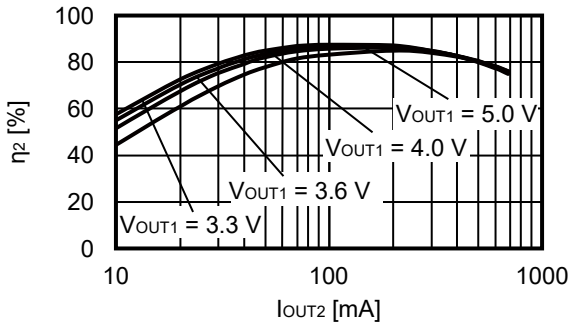



#### 4. 5. 5. 3 Ripple voltage ($\Delta V_{OUT2}$) vs Output current ($I_{OUT2}$)

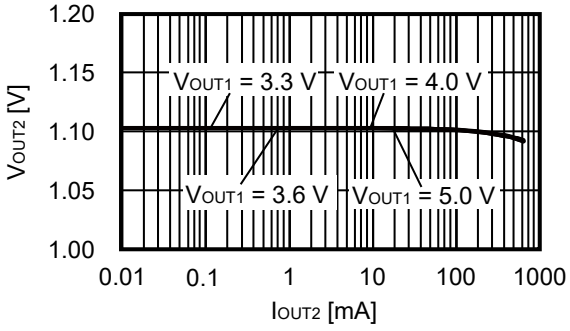


### 4. 5. 6 $V_{OUT2}$ = 1.1 V

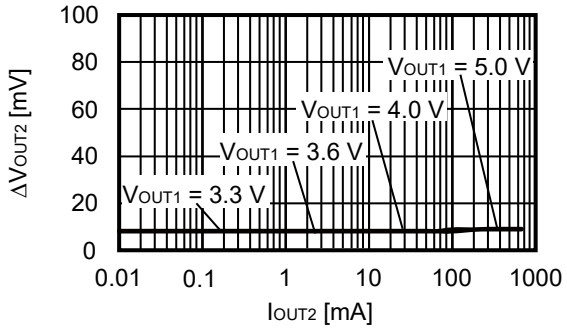
#### 4. 5. 6. 1 Efficiency ($\eta_2$) vs Output current ($I_{OUT2}$)




#### 4. 5. 6. 2 Output voltage ($V_{OUT2}$) vs Output current ($I_{OUT2}$)

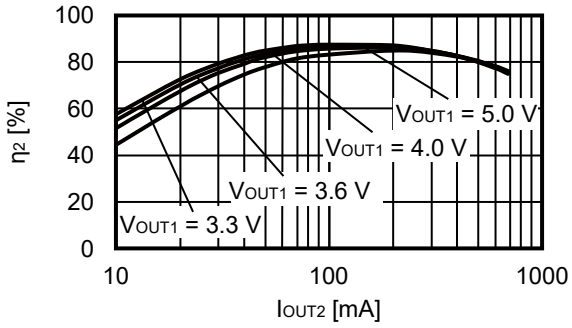



#### 4. 5. 6. 3 Ripple voltage ($\Delta V_{OUT2}$) vs Output current ($I_{OUT2}$)

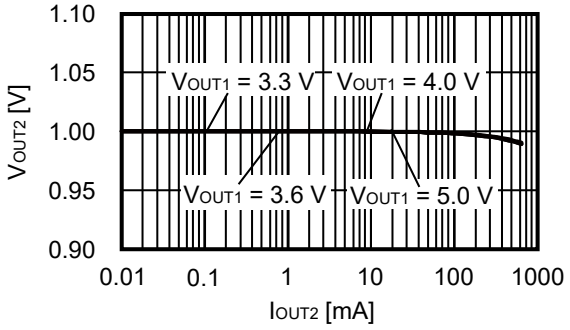



### 4. 5. 7 $V_{OUT2}$ = 1.0 V

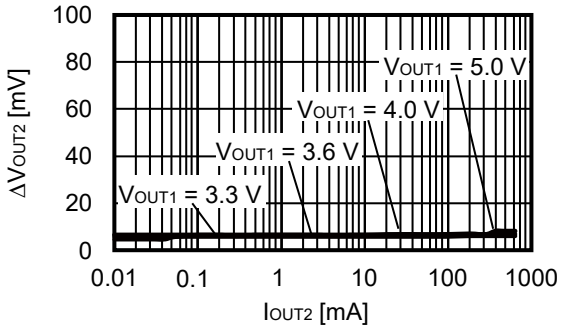
#### 4. 5. 7. 1 Efficiency ($\eta_2$) vs Output current ($I_{OUT2}$)




#### 4. 5. 7. 2 Output voltage ($V_{OUT2}$) vs Output current ($I_{OUT2}$)




#### 4. 5. 7. 3 Ripple voltage ($\Delta V_{OUT2}$) vs Output current ($I_{OUT2}$)



# 5. Board Layout Precautions

The PCB board layout and component placement are extremely important to ensure stable operation of the DC-DC converter, and achieve regulator performance, conversion efficiency, and noise reduction. This section will explain key points for board layout using a PCB board created by ABLIC Inc.

## 5. 1 Application circuit diagram

**Figure 7** shows a PCB board application circuit diagram for the S-19560B Series and S-19255 Series created by ABLIC Inc. The S-19255 Series is connected to the VOUT1 output to generate a low noise analog power supply.

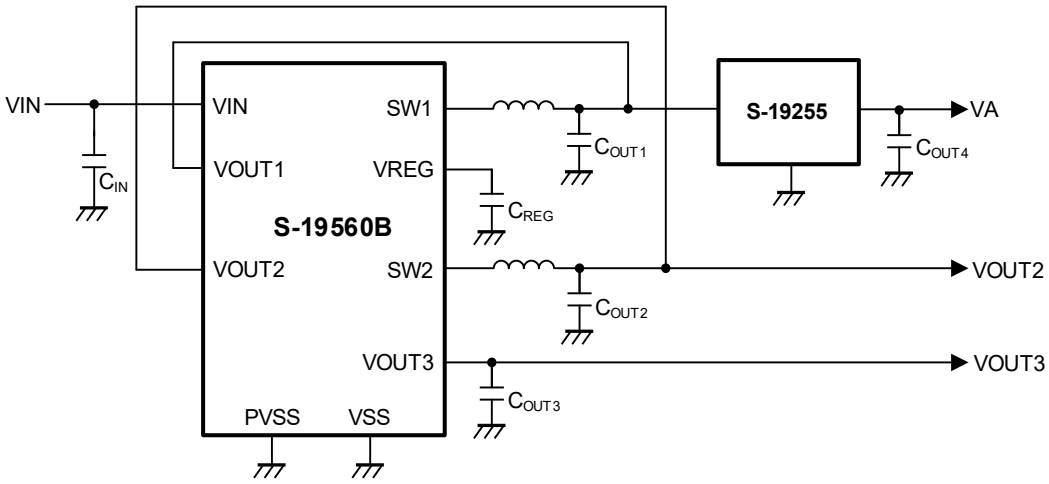



**Figure 7**

## 5. 2 PCB board layout

The board created by our company for the application circuit in **Figure 7** is a double-sided board. If further heat dissipation is required, use a 4-layer board.

- TOP layer: Layout of most components and wiring
- BOTTOM layer: Most of the area is VSS to improve heat dissipation and reduce noise

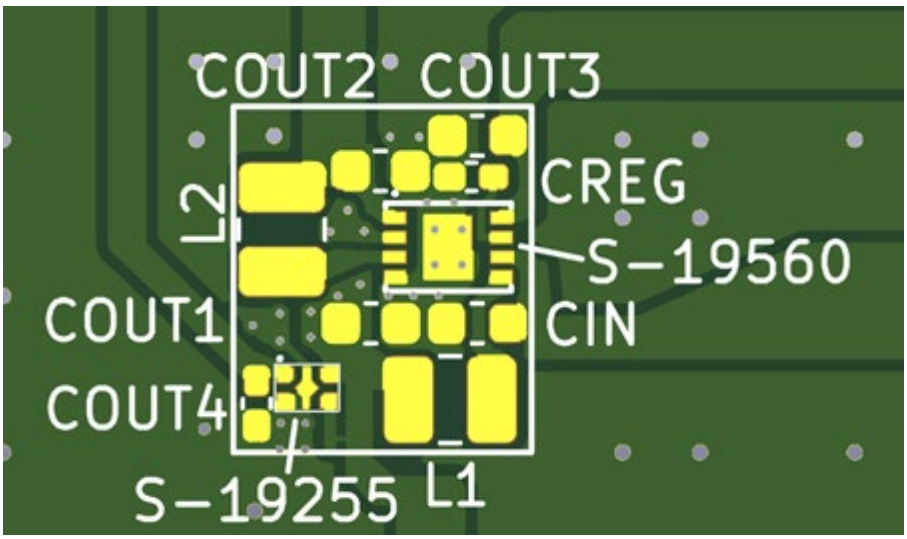



**Figure 8 Board Layout Example (Enlarged)**

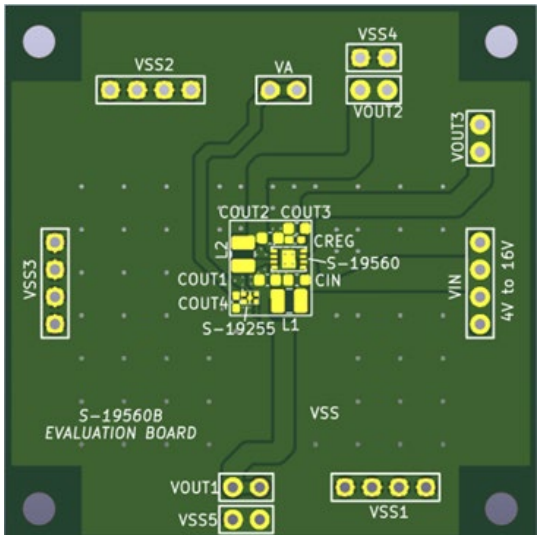



**Figure 9 Overall TOP Layer View (Layer 1)**

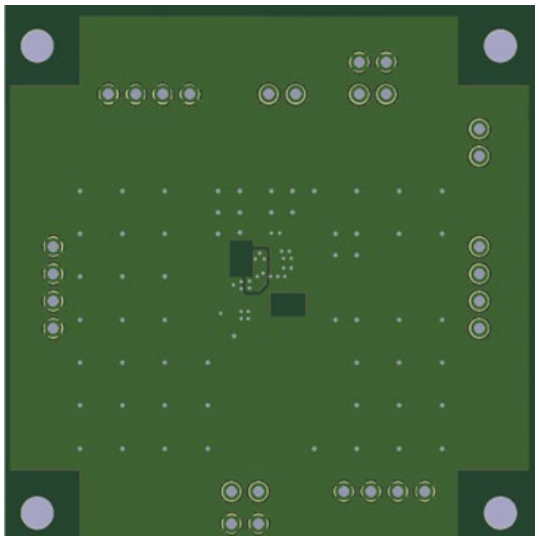


**Figure 10 Overall BOTTOM Layer View (Layer 2)**

### 5. 3 Board layout precautions

- Place $C_{IN}$ as close to the VIN pin and the VSS pin as possible. Prioritize the layout of $C_{IN}$.
- Place $C_{REG}$ as close to the VREG pin and the VSS pin as possible.
- Mount $C_{IN}$ and $C_{REG}$ on the same surface layer as the IC. If they are connected through thermal vias, the impedance of the thermal vias may influence the operation, resulting in unstable condition.
- Make the GND pattern as wide as possible.
- Place thermal vias in the GND pattern to ensure sufficient heat dissipation.
- Large current will flow to the SW1 pin and SW2 pin. Make the wiring area of the pattern to be connected to the SW1 pin and SW2 pin small to minimize parasitic capacitance and emission noise.
- Keep the SW1 pin → $L_1$ → $C_{OUT1}$ → VSS pin, SW2 pin → $L_2$ → $C_{OUT2}$ → VSS pin loop wiring short. This is an effective way to reduce emission noise.
- Do not wire the SW1 pin or SW2 pin pattern under the IC.
- In the board layout example in **Figure 8**, the distance between the S-19255 Series input and $C_{OUT1}$ is shortened in order to omit the input capacitor for the S-19255 Series. If the S-19255 Series will be installed in a more distant location, add an input capacitor for the S-19255 Series.

## 6. Precautions

- The usages described in this application note are typical examples using ICs of ABLIC Inc.
  Perform thorough evaluation before use.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

## 7. Related Sources

Refer to the following datasheet for details of our products.

**S-19560B Series Datasheet**
**S-19255 Series Datasheet**

The information described in this application note and the datasheet is subject to change without notice.
Contact our sales representatives for details.
Regarding the newest version of the datasheet, select product category and product name on our website, and download the PDF file.

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