The S-1011 Series is a high-accuracy voltage detector developed using CMOS technology. The detection voltage is fixed internally, and the accuracy of the S-1011 Series A / C / E / G type is ±1.5%. It operates with current consumption of 600 nA typ.

Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared in the SENSE detection product, so the output is stable even if the SENSE pin falls to 0 V.

The detection signal and release signal can be delayed by setting a capacitor externally, and the detection delay time accuracy is ±20% (CN = 3.3 nF, Ta = +25°C), the release delay time accuracy is ±20% (CP = 3.3 nF, Ta = +25°C). Output form is Nch open-drain output.

### Features
- Detection voltage: 3.0 V to 10.0 V (0.05 V step) (SENSE detection product)
- Detection voltage: 3.6 V to 10.0 V (0.05 V step) (VDD detection product)
- Detection voltage accuracy: ±1.5% (A / C / E / G type)
- Detection delay time accuracy: ±20% (CN = 3.3 nF)
- Release delay time accuracy: ±20% (CP = 3.3 nF)
- Current consumption: 600 nA typ.
- Operation voltage range: 1.8 V to 36.0 V
- Hysteresis width: "Available" (5.0% typ.) / "unavailable" is selectable.
- Operation temperature range: Ta = −40°C to +85°C
- Output form: Nch open-drain output
- Lead-free (Sn 100%), halogen-free

### Applications
- Power supply monitor for microcomputer and reset for CPU
- Constant voltage power supply monitor for TV and home appliance etc.
- Power supply monitor for Blu-ray recorder, notebook PC and digital still camera
- Industrial equipment, housing equipment

### Package
- SOT-23-6
### Block Diagrams

1. **S-1011 Series A / J type (VDD detection product)**

   - **Function Status**
     - Voltage detection: VDD detection
     - Hysteresis width: Available (5.0% typ.)

   ![Figure 1](image1.png)
   *1. Parasitic diode

2. **S-1011 Series C / L type (VDD detection product)**

   - **Function Status**
     - Voltage detection: VDD detection
     - Hysteresis width: Unavailable

   ![Figure 2](image2.png)
   *1. Parasitic diode
3. **S-1011 Series E / N type (SENSE detection product)**

![Figure 3](image)

<table>
<thead>
<tr>
<th>Function</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage detection</td>
<td>SENSE detection</td>
</tr>
<tr>
<td>Hysteresis width</td>
<td>Available (5.0% typ.)</td>
</tr>
</tbody>
</table>

*1. Parasitic diode

4. **S-1011 Series G / Q type (SENSE detection product)**

![Figure 4](image)

<table>
<thead>
<tr>
<th>Function</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage detection</td>
<td>SENSE detection</td>
</tr>
<tr>
<td>Hysteresis width</td>
<td>Unavailable</td>
</tr>
</tbody>
</table>

*1. Parasitic diode
### Product Name Structure

Users can select the product type and detection voltage value for the S-1011 Series. Refer to "1. Product name" regarding the contents of product name, "2. Function list of product types" regarding the product types, "3. Package" regarding the package drawings and "4. Product name lists" regarding details of the product name.

**1. Product name**

S-1011 x xx - M6T1 U 4

- **Environmental code**
  - U: Lead-free (Sn 100%), halogen-free

- **Package abbreviation and IC packing specifications**
  - M6T1: SOT-23-6, Tape

- **Detection voltage value**
  - 30 to A0
  - (e.g., when the output voltage is 3.0 V, it is expressed as 30.
    when the output voltage is 10.0 V, it is expressed as A0.)

- **Product type**
  - A, C, E, G, J, L, N, Q

*1. Refer to the tape drawing.*
*2. Refer to "2. Function list of product types".

**Remark** Although the detection voltage in the S-1011 Series is 10.0 V max., the detection voltage exceeding 10.0 V with an external resistor can be set. Refer to "2. SENSE pin" in "Operation" for details.

**2. Function list of product types**

<table>
<thead>
<tr>
<th>Product Type</th>
<th>Voltage Detection</th>
<th>Output Logic</th>
<th>Hysteresis Width</th>
<th>Detection Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>VDD detection</td>
<td>Active &quot;L&quot;</td>
<td>Available (5.0% typ.)</td>
<td>5.0 V to 10.0 V</td>
</tr>
<tr>
<td>C</td>
<td>VDD detection</td>
<td>Active &quot;L&quot;</td>
<td>Unavailable</td>
<td>5.0 V to 10.0 V</td>
</tr>
<tr>
<td>E</td>
<td>SENSE detection</td>
<td>Active &quot;L&quot;</td>
<td>Available (5.0% typ.)</td>
<td>5.0 V to 10.0 V</td>
</tr>
<tr>
<td>G</td>
<td>SENSE detection</td>
<td>Active &quot;L&quot;</td>
<td>Unavailable</td>
<td>5.0 V to 10.0 V</td>
</tr>
<tr>
<td>J</td>
<td>VDD detection</td>
<td>Active &quot;L&quot;</td>
<td>Available (5.0% typ.)</td>
<td>3.6 V to 4.95 V</td>
</tr>
<tr>
<td>L</td>
<td>VDD detection</td>
<td>Active &quot;L&quot;</td>
<td>Unavailable</td>
<td>3.6 V to 4.95 V</td>
</tr>
<tr>
<td>N</td>
<td>SENSE detection</td>
<td>Active &quot;L&quot;</td>
<td>Available (5.0% typ.)</td>
<td>3.0 V to 4.95 V</td>
</tr>
<tr>
<td>Q</td>
<td>SENSE detection</td>
<td>Active &quot;L&quot;</td>
<td>Unavailable</td>
<td>3.0 V to 4.95 V</td>
</tr>
</tbody>
</table>

**3. Package**

<table>
<thead>
<tr>
<th>Package Name</th>
<th>Dimension</th>
<th>Tape</th>
<th>Reel</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOT-23-6</td>
<td>MP006-A-P-SD</td>
<td>MP006-A-C-SD</td>
<td>MP006-A-R-SD</td>
</tr>
</tbody>
</table>
4. Product name lists

4.1 S-1011 Series A type
Voltage detection: VDD detection  
Output logic: Active "L"  
Hysteresis width: Available (5.0% typ.)  
Detection voltage: 5.0 V to 10.0 V

Table 3

<table>
<thead>
<tr>
<th>Detection Voltage</th>
<th>SOT-23-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0 V ± 1.5%</td>
<td>S-1011A50-M6T1U4</td>
</tr>
<tr>
<td>6.0 V ± 1.5%</td>
<td>S-1011A60-M6T1U4</td>
</tr>
<tr>
<td>7.0 V ± 1.5%</td>
<td>S-1011A70-M6T1U4</td>
</tr>
<tr>
<td>8.0 V ± 1.5%</td>
<td>S-1011A80-M6T1U4</td>
</tr>
<tr>
<td>9.0 V ± 1.5%</td>
<td>S-1011A90-M6T1U4</td>
</tr>
<tr>
<td>10.0 V ± 1.5%</td>
<td>S-1011AA0-M6T1U4</td>
</tr>
</tbody>
</table>

Remark  Please contact our sales office for products with specifications other than the above.

4.2 S-1011 Series C type
Voltage detection: VDD detection  
Output logic: Active "L"  
Hysteresis width: Unavailable  
Detection voltage: 5.0 V to 10.0 V

Table 4

<table>
<thead>
<tr>
<th>Detection Voltage</th>
<th>SOT-23-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0 V ± 1.5%</td>
<td>S-1011C50-M6T1U4</td>
</tr>
<tr>
<td>6.0 V ± 1.5%</td>
<td>S-1011C60-M6T1U4</td>
</tr>
<tr>
<td>7.0 V ± 1.5%</td>
<td>S-1011C70-M6T1U4</td>
</tr>
<tr>
<td>8.0 V ± 1.5%</td>
<td>S-1011C80-M6T1U4</td>
</tr>
<tr>
<td>9.0 V ± 1.5%</td>
<td>S-1011C90-M6T1U4</td>
</tr>
<tr>
<td>10.0 V ± 1.5%</td>
<td>S-1011CA0-M6T1U4</td>
</tr>
</tbody>
</table>

Remark  Please contact our sales office for products with specifications other than the above.

4.3 S-1011 Series E type
Voltage detection: SENSE detection  
Output logic: Active "L"  
Hysteresis width: Available (5.0% typ.)  
Detection voltage: 5.0 V to 10.0 V

Table 5

<table>
<thead>
<tr>
<th>Detection Voltage</th>
<th>SOT-23-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0 V ± 1.5%</td>
<td>S-1011E50-M6T1U4</td>
</tr>
<tr>
<td>6.0 V ± 1.5%</td>
<td>S-1011E60-M6T1U4</td>
</tr>
<tr>
<td>7.0 V ± 1.5%</td>
<td>S-1011E70-M6T1U4</td>
</tr>
<tr>
<td>8.0 V ± 1.5%</td>
<td>S-1011E80-M6T1U4</td>
</tr>
<tr>
<td>9.0 V ± 1.5%</td>
<td>S-1011E90-M6T1U4</td>
</tr>
<tr>
<td>10.0 V ± 1.5%</td>
<td>S-1011EA0-M6T1U4</td>
</tr>
</tbody>
</table>

Remark  Please contact our sales office for products with specifications other than the above.

4.4 S-1011 Series G type
Voltage detection: SENSE detection  
Output logic: Active "L"  
Hysteresis width: Unavailable  
Detection voltage: 5.0 V to 10.0 V

Table 6

<table>
<thead>
<tr>
<th>Detection Voltage</th>
<th>SOT-23-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0 V ± 1.5%</td>
<td>S-1011G50-M6T1U4</td>
</tr>
<tr>
<td>6.0 V ± 1.5%</td>
<td>S-1011G60-M6T1U4</td>
</tr>
<tr>
<td>7.0 V ± 1.5%</td>
<td>S-1011G70-M6T1U4</td>
</tr>
<tr>
<td>8.0 V ± 1.5%</td>
<td>S-1011G80-M6T1U4</td>
</tr>
<tr>
<td>9.0 V ± 1.5%</td>
<td>S-1011G90-M6T1U4</td>
</tr>
<tr>
<td>10.0 V ± 1.5%</td>
<td>S-1011GA0-M6T1U4</td>
</tr>
</tbody>
</table>

Remark  Please contact our sales office for products with specifications other than the above.
4.5 S-1011 Series J type
Voltage detection: VDD detection  Output logic: Active "L"
Hysteresis width: Available (5.0% typ.)  Detection voltage: 3.6 V to 4.95 V

Table 7

<table>
<thead>
<tr>
<th>Detection Voltage</th>
<th>SOT-23-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.6 V ± 3.0%</td>
<td>S-1011J36-M6T1U4</td>
</tr>
<tr>
<td>4.2 V ± 2.5%</td>
<td>S-1011J42-M6T1U4</td>
</tr>
</tbody>
</table>

Remark  Please contact our sales office for products with specifications other than the above.

4.6 S-1011 Series L type
Voltage detection: VDD detection  Output logic: Active "L"
Hysteresis width: Unavailable  Detection voltage: 3.6 V to 4.95 V

Table 8

<table>
<thead>
<tr>
<th>Detection Voltage</th>
<th>SOT-23-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.6 V ± 3.0%</td>
<td>S-1011L36-M6T1U4</td>
</tr>
<tr>
<td>4.2 V ± 2.5%</td>
<td>S-1011L42-M6T1U4</td>
</tr>
</tbody>
</table>

Remark  Please contact our sales office for products with specifications other than the above.

4.7 S-1011 Series N type
Voltage detection: SENSE detection  Output logic: Active "L"
Hysteresis width: Available (5.0% typ.)  Detection voltage: 3.0 V to 4.95 V

Table 9

<table>
<thead>
<tr>
<th>Detection Voltage</th>
<th>SOT-23-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0 V ± 3.0%</td>
<td>S-1011N30-M6T1U4</td>
</tr>
<tr>
<td>3.3 V ± 3.0%</td>
<td>S-1011N33-M6T1U4</td>
</tr>
<tr>
<td>3.6 V ± 3.0%</td>
<td>S-1011N36-M6T1U4</td>
</tr>
<tr>
<td>4.2 V ± 2.5%</td>
<td>S-1011N42-M6T1U4</td>
</tr>
</tbody>
</table>

Remark  Please contact our sales office for products with specifications other than the above.

4.8 S-1011 Series Q type
Voltage detection: SENSE detection  Output logic: Active "L"
Hysteresis width: Unavailable  Detection voltage: 3.0 V to 4.95 V

Table 10

<table>
<thead>
<tr>
<th>Detection Voltage</th>
<th>SOT-23-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0 V ± 3.0%</td>
<td>S-1011Q30-M6T1U4</td>
</tr>
<tr>
<td>3.3 V ± 3.0%</td>
<td>S-1011Q33-M6T1U4</td>
</tr>
<tr>
<td>3.6 V ± 3.0%</td>
<td>S-1011Q36-M6T1U4</td>
</tr>
<tr>
<td>4.2 V ± 2.5%</td>
<td>S-1011Q42-M6T1U4</td>
</tr>
</tbody>
</table>

Remark  Please contact our sales office for products with specifications other than the above.
### Pin Configurations

1. **S-1011 Series A / C / J / L type (VDD detection product)**
   1. 1 **SOT-23-6**

   **Top view**

   ![Top view diagram](image)

   **Table 11**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Voltage input pin</td>
</tr>
<tr>
<td>2</td>
<td>NC(^1)</td>
<td>No connection</td>
</tr>
<tr>
<td>3</td>
<td>OUT</td>
<td>Voltage detection output pin</td>
</tr>
<tr>
<td>4</td>
<td>CP(^2)</td>
<td>Connection pin for release delay capacitor</td>
</tr>
<tr>
<td>5</td>
<td>VSS</td>
<td>GND pin</td>
</tr>
<tr>
<td>6</td>
<td>CN(^3)</td>
<td>Connection pin for detection delay capacitor</td>
</tr>
</tbody>
</table>

*1. The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

*2. Connect a capacitor between the CP pin and the VSS pin.
The release delay time can be adjusted according to the capacitance.
Moreover, the CP pin is available even when it is open.

*3. Connect a capacitor between the CN pin and the VSS pin.
The detection delay time can be adjusted according to the capacitance.
Moreover, the CN pin is available even when it is open.

2. **S-1011 Series E / G / N / Q type (SENSE detection product)**
   2. 1 **SOT-23-6**

   **Top view**

   ![Top view diagram](image)

   **Table 12**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Voltage input pin</td>
</tr>
<tr>
<td>2</td>
<td>SENSE</td>
<td>Detection voltage input pin</td>
</tr>
<tr>
<td>3</td>
<td>OUT</td>
<td>Voltage detection output pin</td>
</tr>
<tr>
<td>4</td>
<td>CP(^1)</td>
<td>Connection pin for release delay capacitor</td>
</tr>
<tr>
<td>5</td>
<td>VSS</td>
<td>GND pin</td>
</tr>
<tr>
<td>6</td>
<td>CN(^2)</td>
<td>Connection pin for detection delay capacitor</td>
</tr>
</tbody>
</table>

*1. Connect a capacitor between the CP pin and the VSS pin.
The release delay time can be adjusted according to the capacitance.
Moreover, the CP pin is available even when it is open.

*2. Connect a capacitor between the CN pin and the VSS pin.
The detection delay time can be adjusted according to the capacitance.
Moreover, the CN pin is available even when it is open.
### Absolute Maximum Ratings

*(Ta = +25°C unless otherwise specified)*

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Absolute Maximum Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage</td>
<td>$V_{DD} - V_{SS}$</td>
<td>$V_{SS} - 0.3$ to $V_{SS} + 45$</td>
<td>V</td>
</tr>
<tr>
<td>SENSE pin input voltage</td>
<td>$V_{SENSE}$</td>
<td>$V_{SS} - 0.3$ to $V_{SS} + 45$</td>
<td>V</td>
</tr>
<tr>
<td>CP pin input voltage</td>
<td>$V_{CP}$</td>
<td>$V_{SS} - 0.3$ to $V_{DO} + 0.3 \leq V_{SS} + 7.0$</td>
<td>V</td>
</tr>
<tr>
<td>CN pin input voltage</td>
<td>$V_{CN}$</td>
<td>$V_{SS} - 0.3$ to $V_{DO} + 0.3 \leq V_{SS} + 7.0$</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>$V_{OUT}$</td>
<td>$V_{SS} - 0.3$ to $V_{SS} + 45$</td>
<td>V</td>
</tr>
<tr>
<td>Output current</td>
<td>$I_{OUT}$</td>
<td>25</td>
<td>mA</td>
</tr>
<tr>
<td>Operation ambient temperature</td>
<td>$T_{opr}$</td>
<td>-40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td>-40 to +125</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

### Thermal Resistance Value

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction-to-ambient thermal resistance*1</td>
<td>$\theta_{ja}$</td>
<td>SOT-23-6</td>
<td>Board 1</td>
<td>–</td>
<td>159</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Board 2</td>
<td>–</td>
<td>124</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "**Thermal Characteristics**" for details of power dissipation and test board.
### Electrical Characteristics

1. **VDD detection product**

1.1 **S-1011 Series J / L type**

Table 15

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection voltage*1</td>
<td>(-V_{DET})</td>
<td>(3.6 \leq -V_{DET(S)} \leq 4.15) V</td>
<td>(-V_{DET(S)} \times 0.970)</td>
<td>(-V_{DET(S)} \times 1.030)</td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(4.2 \leq -V_{DET(S)} \leq 4.95) V</td>
<td>(-V_{DET(S)} \times 0.975)</td>
<td>(-V_{DET(S)} \times 1.025)</td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Hysteresis width*2</td>
<td>(V_{HYS})</td>
<td>J type</td>
<td>(3.6 \leq -V_{DET(S)} \leq 4.15) V</td>
<td>(-V_{DET} \times 0.010)</td>
<td>(-V_{DET} \times 0.100)</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(4.2 \leq -V_{DET(S)} \leq 4.95) V</td>
<td>(-V_{DET} \times 0.020)</td>
<td>(-V_{DET} \times 0.090)</td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>L type*2</td>
<td></td>
<td></td>
<td>(3.6 \leq -V_{DET(S)} \leq 4.95) V</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Current consumption</td>
<td>(I_{SS})</td>
<td>(V_{DD} = -V_{DET} - 0.1) V, (3.6 \leq -V_{DET} \leq 4.95) V</td>
<td>–</td>
<td>0.60</td>
<td>1.60</td>
<td>µA</td>
<td>2</td>
</tr>
<tr>
<td>Operation voltage</td>
<td>(V_{DD})</td>
<td>–</td>
<td>1.8</td>
<td>–</td>
<td>36.0</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Output current</td>
<td>(I_{OUT})</td>
<td>Output transistor Nch, (V_{OS} = 0.05) V</td>
<td>(V_{DD} = 2.9) V</td>
<td>0.33</td>
<td>–</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>Leakage current</td>
<td>(I_{LEAK})</td>
<td>Output transistor Nch, (V_{DD} = 30.0) V, (V_{OUT} = 30.0) V</td>
<td>–</td>
<td>–</td>
<td>2.0</td>
<td>µA</td>
<td>3</td>
</tr>
<tr>
<td>Detection delay time*4</td>
<td>(t_{RESET})</td>
<td>(C_{N} = 3.3) nF</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td>Release delay time*5</td>
<td>(t_{DELAY})</td>
<td>(C_{P} = 3.3) nF</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td>CP pin discharge ON resistance</td>
<td>(R_{CP})</td>
<td>(V_{DD} = 6.9) V, (V_{CP} = 0.5) V</td>
<td>0.52</td>
<td>–</td>
<td>2.2</td>
<td>kΩ</td>
<td>–</td>
</tr>
<tr>
<td>CN pin discharge ON resistance</td>
<td>(R_{CN})</td>
<td>(V_{DD} = 2.9) V, (V_{CN} = 0.5) V</td>
<td>1.0</td>
<td>–</td>
<td>5.0</td>
<td>kΩ</td>
<td>–</td>
</tr>
</tbody>
</table>

*1. \(-V_{DET}\): Actual detection voltage value, \(-V_{DET(S)}\): Set detection voltage value

*2. Hysteresis width is "unavailable", so release voltage = detection voltage.

*3. \(V_{OS}\): Drain-to-source voltage of the output transistor

*4. The time period from when the pulse voltage of \(-V_{DET(S)} + 0.5\) V \(\rightarrow\) \(-V_{DET(S)} - 0.5\) V is applied to the VDD pin to when \(V_{OUT}\) reaches \(V_{DD}/2\), after the power supply voltage (\(V_{DD}\)) reaches the release voltage once.

*5. The time period from when the pulse voltage of \(-V_{DET(S)} - 0.5\) V \(\rightarrow\) \(-V_{DET(S)} + 0.5\) V is applied to the VDD pin to when \(V_{OUT}\) reaches \(V_{DD}/2\).
## S-1011 Series A / C type

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection voltage*1</td>
<td>$-V_{DET}$</td>
<td>$5.0 \leq -V_{DET(S)} \leq 10.0$ V</td>
<td>$-V_{DET(S)} \times 0.985$</td>
<td>$-V_{DET(S)} \times 1.015$</td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Hysteresis width</td>
<td>$V_{HYS}$</td>
<td>A type</td>
<td>$-V_{DET}$</td>
<td>$-V_{DET}$</td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C type*2</td>
<td>–</td>
<td>–</td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Current consumption</td>
<td>$I_{SS}$</td>
<td>$V_{DD} = -V_{DET} - 0.1$ V, $5.0 \leq -V_{DET} \leq 10.0$ V</td>
<td>–</td>
<td>0.60</td>
<td>1.60</td>
<td>μA</td>
<td>2</td>
</tr>
<tr>
<td>Operation voltage</td>
<td>$V_{DD}$</td>
<td>–</td>
<td>1.8</td>
<td>–</td>
<td>36.0</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Output current</td>
<td>$I_{OUT}$</td>
<td>Output transistor Nch $V_{DS} = 0.05$ V</td>
<td>$V_{DD} = 4.5$ V</td>
<td>0.5</td>
<td>–</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>Leakage current</td>
<td>$I_{LEAK}$</td>
<td>Output transistor Nch $V_{DD} = 30.0$ V, $V_{OUT} = 30.0$ V</td>
<td>–</td>
<td>–</td>
<td>2.0</td>
<td>μA</td>
<td>3</td>
</tr>
<tr>
<td>Detection delay time*4</td>
<td>$t_{RESET}$</td>
<td>$C_{N} = 3.3$ nF</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td>Release delay time*5</td>
<td>$t_{DELAY}$</td>
<td>$C_{P} = 3.3$ nF</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td>CP pin discharge ON resistance</td>
<td>$R_{CP}$</td>
<td>$V_{DD} = 14.0$ V, $V_{CP} = 0.5$ V</td>
<td>0.30</td>
<td>–</td>
<td>2.60</td>
<td>kΩ</td>
<td>–</td>
</tr>
<tr>
<td>CN pin discharge ON resistance</td>
<td>$R_{CN}$</td>
<td>$V_{DD} = 4.5$ V, $V_{CN} = 0.5$ V</td>
<td>0.63</td>
<td>–</td>
<td>2.60</td>
<td>kΩ</td>
<td>–</td>
</tr>
</tbody>
</table>

*1. $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value
*2. Hysteresis width is “unavailable”, so release voltage = detection voltage.
*3. $V_{DS}$: Drain-to-source voltage of the output transistor
*4. The time period from when the pulse voltage of $-V_{DET(S)} + 1.0$ V → $-V_{DET(S)} - 1.0$ V is applied to the VDD pin to when $V_{OUT}$ reaches $V_{DD} / 2$, after the power supply voltage ($V_{DD}$) reaches the release voltage once.
*5. The time period from when the pulse voltage of $-V_{DET(S)} - 1.0$ V → $-V_{DET(S)} + 1.0$ V is applied to the VDD pin to when $V_{OUT}$ reaches $V_{DD} / 2$. 

---

*ABLIC Inc.*
2. SENSE detection product

2.1 S-1011 Series N / Q type

### Table 17

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection voltage (^*1)</td>
<td>(-V_{DET})</td>
<td>(V_{DD} = 16.0 \text{ V}) (-V_{DET(S)} \leq 4.15 \text{ V})</td>
<td>(-V_{DET(S)} \times 0.970)</td>
<td>(-V_{DET(S)} \times 1.030)</td>
<td>(-V_{DET(S)} \times 1.025)</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(4.2 \text{ V} \leq -V_{DET(S)} \leq 4.95 \text{ V})</td>
<td>(-V_{DET(S)} \times 0.975)</td>
<td>(-V_{DET(S)} \times 1.00)</td>
<td>(-V_{DET(S)} \times 1.020)</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Hysteresis width (^*2)</td>
<td>(V_{HYS})</td>
<td>(V_{DD} = 16.0 \text{ V}) (3.0 \text{ V} \leq -V_{DET(S)} \leq 4.15 \text{ V})</td>
<td>(-V_{DET} \times 0.010)</td>
<td>(-V_{DET} \times 0.050)</td>
<td>(-V_{DET} \times 0.090)</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(4.2 \text{ V} \leq -V_{DET(S)} \leq 4.95 \text{ V})</td>
<td>(-V_{DET} \times 0.020)</td>
<td>(-V_{DET} \times 0.050)</td>
<td>(-V_{DET} \times 0.090)</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Current consumption (^*3)</td>
<td>(I_{SS})</td>
<td>(V_{DD} = 16.0 \text{ V}, V_{SENSE} = -V_{DET} - 0.1 \text{ V}), (3.0 \text{ V} \leq -V_{DET} \leq 4.95 \text{ V})</td>
<td>–</td>
<td>0.55</td>
<td>1.55</td>
<td>(\mu\text{A})</td>
<td>2</td>
</tr>
<tr>
<td>Operation voltage</td>
<td>(V_{DD})</td>
<td>–</td>
<td>3.0</td>
<td>–</td>
<td>36.0</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Output current</td>
<td>(I_{OUT})</td>
<td>Output transistor Nch (V_{DS} = 0.05 \text{ V})</td>
<td>(V_{DD} = 5.0 \text{ V}, V_{SENSE} = 2.9 \text{ V})</td>
<td>0.5</td>
<td>–</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>Leakage current</td>
<td>(I_{LEAK})</td>
<td>Output transistor Nch (V_{DS} = 0.05 \text{ V})</td>
<td>(V_{DD} = 30.0 \text{ V}, V_{OUT} = 30.0 \text{ V}, V_{SENSE} = 30.0 \text{ V})</td>
<td>–</td>
<td>–</td>
<td>2.0</td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>Detection delay time (^*5)</td>
<td>(t_{RESET})</td>
<td>(C_N = 3.3 \text{ nF})</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td>Release delay time (^*6)</td>
<td>(t_{DELAY})</td>
<td>(C_P = 3.3 \text{ nF})</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td>SENSE pin resistance</td>
<td>(R_{SENSE})</td>
<td>–</td>
<td>6.8</td>
<td>–</td>
<td>275</td>
<td>M\text{\Omega}</td>
<td>2</td>
</tr>
<tr>
<td>CP pin discharge ON resistance</td>
<td>(R_{CP})</td>
<td>(V_{DD} = 3.0 \text{ V}, V_{SENSE} = 6.9 \text{ V}, V_{CP} = 0.5 \text{ V})</td>
<td>0.72</td>
<td>–</td>
<td>4.29</td>
<td>k\text{\Omega}</td>
<td>–</td>
</tr>
<tr>
<td>CN pin discharge ON resistance</td>
<td>(R_{CN})</td>
<td>(V_{DD} = 3.0 \text{ V}, V_{SENSE} = 2.9 \text{ V}, V_{CN} = 0.5 \text{ V})</td>
<td>0.72</td>
<td>–</td>
<td>4.29</td>
<td>k\text{\Omega}</td>
<td>–</td>
</tr>
</tbody>
</table>

\(^*1\) \(-V_{DET}\): Actual detection voltage value, \(-V_{DET(S)}\): Set detection voltage value

\(^*2\) Hysteresis width is “unavailable”, so release voltage = detection voltage.

\(^*3\) The current flowing through the SENSE pin resistance is not included.

\(^*4\) \(V_{DS}\): Drain-to-source voltage of the output transistor

\(^*5\) The time period from when the pulse voltage of \(-V_{DET(S)} + 0.5 \text{ V} \rightarrow -V_{DET(S)} - 0.5 \text{ V}\) is applied to the SENSE pin to when \(V_{OUT}\) reaches \(V_{DD} / 2\), after voltage of 16.0 V is applied to the VDD pin and the SENSE pin input voltage (\(V_{SENSE}\)) reaches the release voltage once.

\(^*6\) The time period from when voltage of 16.0 V is applied to the VDD pin and the pulse voltage of \(-V_{DET(S)} - 0.5 \text{ V} \rightarrow -V_{DET(S)} + 0.5 \text{ V}\) is applied to the SENSE pin to when \(V_{OUT}\) reaches \(V_{DD} / 2\).
### 2. 2 S-1011 Series E / G type

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection voltage*1</td>
<td>(-V_{DET})</td>
<td>(V_{DD} = 16.0 , V, 5.0 , V \leq -V_{DET}(S) \leq 10.0 , V)</td>
<td>(-V_{DET}(S) \times 0.985)</td>
<td>(-V_{DET}(S) \times 1.015)</td>
<td>(V)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Hysteresis width</td>
<td>(V_{HYS})</td>
<td>(V_{DD} = 16.0 , V)</td>
<td>(-V_{DET})</td>
<td>(-V_{DET})</td>
<td>(-V_{DET})</td>
<td>(V)</td>
<td>1</td>
</tr>
<tr>
<td>Current consumption*2</td>
<td>(I_{SS})</td>
<td>(V_{DD} = 16.0 , V, V_{SENSE} = -V_{DET} - 0.1 , V,) (5.0 , V \leq -V_{DET} \leq 10.0 , V)</td>
<td>(-)</td>
<td>0.55</td>
<td>1.55</td>
<td>(\mu A)</td>
<td>2</td>
</tr>
<tr>
<td>Operation voltage</td>
<td>(V_{DD})</td>
<td></td>
<td>3.0</td>
<td>(-)</td>
<td>36.0</td>
<td>(V)</td>
<td>1</td>
</tr>
<tr>
<td>Output current</td>
<td>(I_{OUT})</td>
<td>Output transistor Nch (V_{DS} = 0.05 , V) (V_{DD} = 5.0 , V, V_{SENSE} = 4.5 , V)</td>
<td>0.5</td>
<td>(-)</td>
<td>(-)</td>
<td>(mA)</td>
<td>3</td>
</tr>
<tr>
<td>Leakage current</td>
<td>(I_{LEAK})</td>
<td>Output transistor Nch (V_{DD} = 30.0 , V, V_{OUT} = 30.0 , V, V_{SENSE} = 30.0 , V)</td>
<td>(-)</td>
<td>(-)</td>
<td>2.0</td>
<td>(\mu A)</td>
<td>3</td>
</tr>
<tr>
<td>Detection delay time*5</td>
<td>(t_{RESET})</td>
<td>(C_N = 3.3 , nF)</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td>Release delay time*6</td>
<td>(t_{DELAY})</td>
<td>(C_P = 3.3 , nF)</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td>SENSE pin resistance</td>
<td>(R_{SENSE})</td>
<td></td>
<td>(-)</td>
<td>26.0</td>
<td>(-)</td>
<td>(M \Omega)</td>
<td>2</td>
</tr>
<tr>
<td>CP pin discharge ON resistance</td>
<td>(R_{CP})</td>
<td>(V_{DD} = 4.5 , V, V_{SENSE} = 14.0 , V, V_{CP} = 0.5 , V)</td>
<td>0.30</td>
<td>(-)</td>
<td>2.60</td>
<td>(k \Omega)</td>
<td>(-)</td>
</tr>
<tr>
<td>CN pin discharge ON resistance</td>
<td>(R_{CN})</td>
<td>(V_{DD} = 4.5 , V, V_{SENSE} = 4.5 , V, V_{CN} = 0.5 , V)</td>
<td>0.63</td>
<td>(-)</td>
<td>2.60</td>
<td>(k \Omega)</td>
<td>(-)</td>
</tr>
</tbody>
</table>

*1. \(-V_{DET}\): Actual detection voltage value, \(-V_{DET}(S)\): Set detection voltage value

*2. Hysteresis width is "unavailable", so release voltage = detection voltage.

*3. The current flowing through the SENSE pin resistance is not included.

*4. \(V_{DS}\): Drain-to-source voltage of the output transistor

*5. The time period from when the pulse voltage of \(-V_{DET}(S) + 1.0 \, V \rightarrow -V_{DET}(S) - 1.0 \, V\) is applied to the SENSE pin to when \(V_{OUT}\) reaches \(V_{DD} / 2\), after voltage of 16.0 V is applied to the VDD pin and the SENSE pin input voltage \(V_{SENSE}\) reaches the release voltage once.

*6. The time period from when voltage of 16.0 V is applied to the VDD pin and the pulse voltage of \(-V_{DET}(S) - 1.0 \, V \rightarrow -V_{DET}(S) + 1.0 \, V\) is applied to the SENSE pin to when \(V_{OUT}\) reaches \(V_{DD} / 2\).
Test Circuits

Figure 7  Test Circuit 1
(VDD detection product)

Figure 8  Test Circuit 1
(SENSE detection product)

Figure 9  Test Circuit 2
(VDD detection product)

Figure 10  Test Circuit 2
(SENSE detection product)

Figure 11  Test Circuit 3
(VDD detection product)

Figure 12  Test Circuit 3
(SENSE detection product)

Figure 13  Test Circuit 4
(VDD detection product)

Figure 14  Test Circuit 4
(SENSE detection product)
## Standard Circuits

1. **VDD detection product**

![Diagram for VDD detection product]

*1. The delay capacitor (C<sub>P</sub>) should be connected directly to the CP pin and the VSS pin.
*2. The delay capacitor (C<sub>N</sub>) should be connected directly to the CN pin and the VSS pin.

**Figure 15**

2. **SENSE detection product**

![Diagram for SENSE detection product]

*1. The delay capacitor (C<sub>P</sub>) should be connected directly to the CP pin and the VSS pin.
*2. The delay capacitor (C<sub>N</sub>) should be connected directly to the CN pin and the VSS pin.

**Figure 16**

**Caution** The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
**Explanation of Terms**

1. **Detection voltage (−VDET)**

   The detection voltage is a voltage at which the output in Figure 21 or Figure 22 turns to "L" (VDD detection product: VDD, SENSE detection product: VSENSE). The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum (−VDET min.) and the maximum (−VDET max.) is called the detection voltage range (Refer to Figure 17, Figure 19).

   Example: In −VDET = 5.0 V product, the detection voltage is either one in the range of 4.925 V ≤ −VDET ≤ 5.075 V. This means that some −VDET = 5.0 V product have −VDET = 4.925 V and some have −VDET = 5.075 V.

2. **Release voltage (+VDET)**

   The release voltage is a voltage at which the output in Figure 21 or Figure 22 turns to "H" (VDD detection product: VDD, SENSE detection product: VSENSE).

   The difference of detection voltage and release voltage is 5.0% typ.

   The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum (+VDET min.) and the maximum (+VDET max.) is called the release voltage range (Refer to Figure 18, Figure 20). The range is calculated from the actual detection voltage (−VDET) of a product.

   In the S-1011 Series C / G / L / Q type, the release voltage (+VDET) is the same value as the actual detection voltage (−VDET) of a product.

   Example: In −VDET = 6.0 V product, the release voltage is either one in the range of 6.0873 V ≤ +VDET ≤ 6.5772 V. This means that some −VDET = 6.0 V product have +VDET = 6.0873 V and some have +VDET = 6.5772 V.
3. Hysteresis width ($V_{HYS}$)

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point $B$ - the voltage at point $A = V_{HYS}$ in Figure 24 and Figure 28). Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

4. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector.
■ Operation

1. Basic operation

1.1 S-1011 Series A / J type

(1) When the power supply voltage (VDD) is the release voltage (+VDET) or higher, the Nch transistor is turned off to output VDD ("H") when the output is pulled up.

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is

\[ \frac{(R_A + R_C) \cdot VDD}{R_A + R_B + R_C} \].

(2) Even if VDD decreases to +VDET or lower, VDD is output when VDD is higher than the detection voltage (−VDET).

When VDD decreases to −VDET or lower (point A in Figure 24), the Nch transistor is turned on. And then VSS ("L") is output from the OUT pin after the elapse of the detection delay time (tRESET).

At this time, N1 is turned on, and the input voltage to the comparator is

\[ \frac{R_B \cdot VDD}{R_A + R_B} \].

(3) The output is unstable when VDD decreases to the IC's minimum operation voltage or lower. VDD is output when the output is pulled up.

(4) VSS is output by increasing VDD to the minimum operation voltage or higher. Even if VDD exceeds −VDET, VSS is output when VDD is lower than +VDET.

(5) When VDD increases to +VDET or higher (point B in Figure 24), the Nch transistor is turned off. And then VDD is output from the OUT pin after the elapse of the release delay time (tDELAY) when the output is pulled up.

![Figure 23 Operation of S-1011 Series A / J Type](image)

*1. Parasitic diode

### Figure 23 Operation of S-1011 Series A / J Type

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Release voltage (+VDET)</td>
</tr>
<tr>
<td>2</td>
<td>Detection voltage (−VDET)</td>
</tr>
<tr>
<td>3</td>
<td>Minimum operation voltage</td>
</tr>
<tr>
<td>4</td>
<td>Output from OUT pin</td>
</tr>
<tr>
<td>5</td>
<td>Hysteresis width (VHYS)</td>
</tr>
</tbody>
</table>

Remark When VDD is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

![Figure 24 Timing Chart of S-1011 Series A / J Type](image)
1.2 S-1011 Series C / L type

(1) When the power supply voltage \( V_{DD} \) is the release voltage \( \pm V_{DET} \) or higher, the Nch transistor is turned off to output \( V_{DD} \) ("H") when the output is pulled up.

At this time, the input voltage to the comparator is \( \frac{(R_B + R_C)}{R_A + R_B + R_C} \cdot V_{DD} \).

(2) When \( V_{DD} \) decreases to the detection voltage \( -V_{DET} \) or lower (point A in Figure 26), the Nch transistor is turned on. And then \( V_{SS} \) ("L") is output from the OUT pin after the elapse of the detection delay time (\( t_{RESET} \)).

(3) The output is unstable when \( V_{DD} \) decreases to the IC's minimum operation voltage or lower. \( V_{DD} \) is output when the output is pulled up.

(4) \( V_{SS} \) is output by increasing \( V_{DD} \) to the minimum operation voltage or higher.

(5) When \( V_{DD} \) increases to \( \pm V_{DET} \) or higher (point B in Figure 26), the Nch transistor is turned off. And then \( V_{DD} \) is output from the OUT pin after the elapse of the release delay time (\( t_{DELAY} \)) when the output is pulled up.

*1. Parasitic diode

Figure 25  Operation of S-1011 Series C / L Type

Figure 26  Timing Chart of S-1011 Series C / L Type

**Remark 1.** When \( V_{DD} \) is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

2. The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.
1.3 S-1011 Series E / N type

(1) When the power supply voltage (VDD) is the minimum operation voltage or higher, and the SENSE pin voltage (VSENSE) is the release voltage (+VDET) or higher, the Nch transistor is turned off to output VDD ("H") when the output is pulled up.

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is \( \frac{(R_B + R_C) \cdot V_{SENSE}}{R_A + R_B + R_C} \).

(2) Even if VSENSE decreases to +VDET or lower, VDD is output when VSENSE is higher than the detection voltage (−VDET).

When VSENSE decreases to −VDET or lower (point A in Figure 28), the Nch transistor is turned on. And then VSS ("L") is output from the OUT pin after the elapse of the detection delay time (tRESET).

At this time, N1 is turned on, and the input voltage to the comparator is \( \frac{R_B \cdot V_{SENSE}}{R_A + R_B} \).

(3) Even if VSENSE further decreases to the IC’s minimum operation voltage or lower, the output from the OUT pin is stable when VDD is minimum operation voltage or higher.

(4) Even if VSENSE exceeds −VDET, VSS is output when VSENSE is lower than +VDET.

(5) When VSENSE increases to +VDET or higher (point B in Figure 28), the Nch transistor is turned off. And then VDD is output from the OUT pin after the elapse of the release delay time (tDELAY) when the output is pulled up.

*1. Parasitic diode

Figure 27 Operation of S-1011 Series E / N Type

Figure 28 Timing Chart of S-1011 Series E / N Type
1.4 S-1011 Series G / Q type

(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage (+V_{DET}) or higher, the Nch transistor is turned off to output V_{DD} ("H") when the output is pulled up.

At this time, the input voltage to the comparator is \( \frac{(R_B + R_C) \cdot V_{SENSE}}{R_A + R_B + R_C} \).

(2) When V_{SENSE} decreases to the detection voltage (−V_{DET}) or lower (point A in Figure 30), the Nch transistor is turned on. And then V_{SS} ("L") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}).

(3) Even if V_{SENSE} further decreases to the IC’s minimum operation voltage or lower, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or higher.

(4) Even if V_{SENSE} increases, V_{SS} is output when V_{SENSE} is lower than +V_{DET}.

(5) When V_{SENSE} increases to +V_{DET} or higher (point B in Figure 30), the Nch transistor is turned off. And then V_{DD} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}) when the output is pulled up.

*1 Parasitic diode

![Figure 29 Operation of S-1011 Series G / Q Type](image)

**Figure 29** Operation of S-1011 Series G / Q Type

**Remark** The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.
2. SENSE pin

2.1 Error when detection voltage is set externally

The detection voltage for the S-1011 Series is 10.0 V max., however, in the SENSE detection product with \(-V_{\text{DET}} = 10.0 \text{ V}\), the detection voltage can be set externally by connecting a node that was resistance-divided by the resistor \(R_A\) and the resistor \(R_B\) to the SENSE pin as shown in Figure 31.

For conventional products without the SENSE pin, external resistor cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if external resistor is large, problems such as oscillation or larger error in the hysteresis width may occur.

In the S-1011 Series, \(R_A\) and \(R_B\) in Figure 31 are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance \(R_{\text{SENSE}}\) that will occur.

Although \(R_{\text{SENSE}}\) in the S-1011 Series is large (the S-1011 Series E / G type: 26 MΩ min., the S-1011 Series N / Q type: 6.8 MΩ min.) to make the error small, \(R_A\) and \(R_B\) should be selected such that the error is within the allowable limits.

2.2 Selection of \(R_A\) and \(R_B\)

In Figure 31, the relation between the external setting detection voltage \(V_{\text{DX}}\) and the actual detection voltage \((-V_{\text{DET}})\) is ideally calculated by the equation below.

\[
V_{\text{DX}} = -V_{\text{DET}} \times \left(1 + \frac{R_A}{R_B}\right) \quad \cdots (1)
\]

However, in reality there is an error in the current flowing through \(R_{\text{SENSE}}\).

When considering this error, the relation between \(V_{\text{DX}}\) and \(-V_{\text{DET}}\) is calculated as follows.

\[
V_{\text{DX}} = -V_{\text{DET}} \times \left(1 + \frac{R_A}{R_B || R_{\text{SENSE}}}\right)
\]

\[
= -V_{\text{DET}} \times \left(1 + \frac{R_A}{R_B \times R_{\text{SENSE}}}\right)
\]

\[
= -V_{\text{DET}} \times \left(1 + \frac{R_A}{R_B} + \frac{R_A}{R_{\text{SENSE}}} \times -V_{\text{DET}}\right) \quad \cdots (2)
\]

By using equations (1) and (2), the error is calculated as \(-V_{\text{DET}} \times \frac{R_A}{R_{\text{SENSE}}}\).

The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

\[
\frac{R_A \times R_B}{R_{\text{SENSE}} \times (R_A + R_B)} \times 100 \text{[%]} = \frac{R_A || R_B}{R_{\text{SENSE}}} \times 100 \text{[%]} \quad \cdots (3)
\]

As seen in equation (3), the smaller the resistance values of \(R_A\) and \(R_B\) compared to \(R_{\text{SENSE}}\), the smaller the error rate becomes.
Also, the relation between the external setting hysteresis width \( V_{\text{HX}} \) and the hysteresis width \( V_{\text{HYS}} \) is calculated by equation below. Error due to \( R_{\text{SENSE}} \) also occurs to the relation in a similar way to the detection voltage.

\[
V_{\text{HX}} = V_{\text{HYS}} \times \left( 1 + \frac{R_A}{R_B} \right)
\]  \( \cdots (4) \)

Figure 31 Detection Voltage External Setting Circuit

Caution 1. When externally setting the detection voltage, perform the operation with \( -V_{\text{DET}} = 10.0 \text{ V} \) product. Contact our sales office for details.

2. If the current flowing through \( R_B \) is set to 1 \( \mu \text{A} \) or less, the error may become larger.

3. If the parasitic resistance and parasitic inductance between \( V_{\text{DX}} \) – point A and point A – VDD pin are larger, oscillation may occur. Perform thorough evaluation using the actual application.

4. If \( R_A \) and \( R_B \) are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.
3. Delay circuit

The delay circuit has a function that adjusts the detection delay time \( t_{\text{RESET}} \) from when the power supply voltage \( (V_{\text{DD}}) \) or SENSE pin voltage \( (V_{\text{SENSE}}) \) reaches the detection voltage \( (-V_{\text{DET}}) \) or lower to when the output from OUT pin inverts.

It also has a function that adjusts the release delay time \( t_{\text{DELAY}} \) from when the power supply voltage \( (V_{\text{DD}}) \) or SENSE pin voltage \( (V_{\text{SENSE}}) \) reaches the release voltage \( (+V_{\text{DET}}) \) to when the output from OUT pin inverts.

\( t_{\text{RESET}} \) is determined by the delay coefficient, the delay capacitor \( (C_N) \) and the detection delay time when the CN pin is open \( (t_{\text{RESET}0}) \), and the \( t_{\text{DELAY}} \) is determined by the delay coefficient, the delay capacitor \( (C_P) \) and the release delay time when the CP pin is open \( (t_{\text{DELAY}0}) \). They are calculated by the equation below.

\[
\begin{align*}
t_{\text{RESET}} \ [\text{ms}] &= \text{Delay coefficient} \times C_N \ [\text{nF}] + t_{\text{RESET}0} \ [\text{ms}] \\
t_{\text{DELAY}} \ [\text{ms}] &= \text{Delay coefficient} \times C_P \ [\text{nF}] + t_{\text{DELAY}0} \ [\text{ms}]
\end{align*}
\]

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<tr>
<th>Operation Temperature</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
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<tr>
<td>Ta = +85°C</td>
<td>2.41</td>
<td>2.85</td>
<td>3.32</td>
</tr>
<tr>
<td>Ta = +25°C</td>
<td>2.41</td>
<td>2.86</td>
<td>3.30</td>
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<tr>
<td>Ta = −40°C</td>
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Table 20

<table>
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<tr>
<th>Operation Temperature</th>
<th>Detection Delay Time when CN Pin is Open ( (t_{\text{RESET}0}) )</th>
<th>Release Delay Time when CP Pin is Open ( (t_{\text{DELAY}0}) )</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Typ.</td>
<td>Typ.</td>
</tr>
<tr>
<td>Ta = −40°C to +85°C</td>
<td>0.35 ms</td>
<td>0.35 ms</td>
</tr>
</tbody>
</table>

Caution 1. Mounted board layout should be made in such a way that no current flows into or flows from the CN pin or CP pin since the impedance of the CN pin and CP pin are high, otherwise correct delay time cannot be provided.

2. There is no limit for the capacitance of \( C_N \) and \( C_P \) as long as the leakage current of the capacitor can be ignored against the built-in constant current value (approximately 300 nA). The leakage current may cause error in delay time. When the leakage current is larger than the built-in constant current, no detect or release takes place.

3. The above equation will not guarantee successful operation. Determine the capacitance of \( C_N \) and \( C_P \) through thorough evaluation including temperature characteristics in the actual usage conditions.

When using an X8R equivalent capacitor, refer to the "2. Detection delay time \( (t_{\text{RESET}}) \) vs. Temperature (Ta)”, "3. Detection delay time \( (t_{\text{RESET}}) \) vs. Power supply voltage \( (V_{\text{DD}}) \)”, "5. Release delay time \( (t_{\text{DELAY}}) \) vs. Temperature (Ta)” and "6. Release delay time \( (t_{\text{DELAY}}) \) vs. Power supply voltage \( (V_{\text{DD}}) \)” in “Reference Data” for details.
Usage Precautions

1. Feed-through current during detection and release

   In the S-1011 Series, the feed-through current flows at the time of detection and release. For this reason, if the input impedance is high, oscillation may occur due to voltage drop caused by the feed-through current.

   When using the S-1011 Series in configurations like those shown in Figure 32 and Figure 33, it is recommended that input impedance be set to 1 kΩ or less.

   Determine the impedance through thorough evaluation including temperature characteristics.
2. Power on and shut down sequence

SENSE detection products monitor SENSE pin voltage ($V_{\text{SENSE}}$) while power is being supplied to the VDD pin. Apply power in the order, the VDD pin then the SENSE pin. In addition, when shutting down VDD pin, shut down the SENSE pin first, and shut down the VDD pin after the detection delay time ($t_{\text{RESET}}$) has elapsed.

![Figure 34](image)

3. Falling power (reference)

Figure 35 shows the relation between $V_{\text{DD}}$ amplitude ($V_{P-P}$) and input voltage falling time ($t_f$) where the release status can be maintained when the VDD pin (VDD detection product) sharply drops to a voltage equal to or higher than the detection voltage ($-V_{\text{DET}}$) during release status.

![Figure 35](image)

Caution Figure 35 shows the input voltage conditions which can maintain the release status. If the voltage whose $V_{P-P}$ and $t_f$ are larger than these conditions is input to the VDD pin (VDD detection product), the OUT pin may change to a detection status.

*1. $V_{\text{IH}} = 36.0 \text{ V}$
*2. $V_{\text{IL}} = -V_{\text{DET(S)}} + 1.0 \text{ V}$
4. Detection delay time accuracy (reference)

Figure 37 and Figure 38 show the relation between $V_{DD}$ amplitude ($V_{P-P}$) and input voltage falling time ($t_F$) where the arbitrarily set detection delay time accuracy can be maintained when the VDD pin (VDD detection product) sharply drops.

Caution: Figure 37 and Figure 38 show the input voltage conditions which can maintain the detection delay time accuracy. If the voltage whose $V_{P-P}$ and $t_F$ are larger than these conditions is input to the VDD pin (VDD detection product), the desired detection delay time may not be achieved.
5. **V\text{DD}** drop during release delay time (reference)

Figure 40 and Figure 41 show the relation between pulse width (t\text{PW}) and V\text{DD} lower limit (V\text{DROP}) where a release signal can be output after the normal release delay time has elapsed when the VDD pin (VDD detection product) instantaneously drops to the detection voltage (−V\text{DET}) or lower and then increases to the release voltage (+V\text{DET}) or higher during release delay time.

![Figure 40](image1)

![Figure 41](image2)

Figure 42  VDD Pin Input Voltage Waveform

Caution 1. Figure 40 and Figure 41 show the input voltage conditions when a release signal is output after the normal release delay time has elapsed. When this is within the inhibited area, release may erroneously be executed before the delay time completes.

2. When the VDD pin voltage is within the inhibited areas shown in Figure 40 and Figure 41 during release delay time, input 0 V to the VDD pin then restart the S-1011 Series.
Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- Because the SENSE pin has a high impedance, malfunctions may occur due to noise. Be careful of wiring adjoining SENSE pin wiring in actual applications.

- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.
Characteristics (Typical Data)

1. Detection voltage (−VDET), Release voltage (+VDET) vs. Temperature (Ta)
   
   1.1 VDD detection product
   
   ![Graph of VDD detection product](image)

   1.2 SENSE detection product
   
   ![Graph of SENSE detection product](image)

2. Detection voltage (−VDET), Release voltage (+VDET) vs. Power supply voltage (VDD)
   
   2.1 SENSE detection product
   
   ![Graph of SENSE detection product](image)

3. Current consumption (I<sub>SS</sub>) vs. Power supply voltage (VDD)
   
   3.1 VDD detection product
   
   ![Graph of VDD detection product](image)

   3.2 SENSE detection product
   
   ![Graph of SENSE detection product](image)
4. Current consumption ($I_{SS}$) vs. Temperature ($T_a$)
   4.1 VDD detection product
   S-1011A50
   $V_{DD} = V_{DET} + 0.1 \, V$

   ![Graph of S-1011A50 VDD detection product]

   4.2 SENSE detection product
   S-1011E50
   $V_{DD} = 16.0 \, V$, $V_{SENSE} = V_{DET} + 0.1 \, V$

   ![Graph of S-1011E50 SENSE detection product]

5. Current consumption during detection delay ($I_{SS}$) vs. Temperature ($T_a$)
   5.1 VDD detection product
   S-1011A50
   $V_{CN} = 0.2 \, V$

   ![Graph of S-1011A50 VDD detection product]

   5.2 SENSE detection product
   S-1011E50
   $V_{DD} = 16.0 \, V$, $V_{CN} = 0.2 \, V$

   ![Graph of S-1011E50 SENSE detection product]

6. Current consumption during release delay ($I_{SS}$) vs. Temperature ($T_a$)
   6.1 VDD detection product
   S-1011A50
   $V_{CP} = 0.2 \, V$

   ![Graph of S-1011A50 VDD detection product]

   6.2 SENSE detection product
   S-1011E50
   $V_{DD} = 16.0 \, V$, $V_{CP} = 0.2 \, V$

   ![Graph of S-1011E50 SENSE detection product]
7. **Nch transistor output current (I\textsubscript{OUT}) vs. V\textsubscript{DS}\****

7.1 **SENSE detection product**

![Graph showing Nch transistor output current (I\textsubscript{OUT}) vs. V\textsubscript{DS} for different temperatures and power supply voltages](image1)

8. **Nch transistor output current (I\textsubscript{OUT}) vs. Power supply voltage (V\textsubscript{DD})\****

8.1 **VDD detection product**

![Graph showing Nch transistor output current (I\textsubscript{OUT}) vs. Power supply voltage (V\textsubscript{DD}) for different temperatures](image2)

8.2 **SENSE detection product**

![Graph showing Nch transistor output current (I\textsubscript{OUT}) vs. Power supply voltage (V\textsubscript{DD}) for different temperatures](image3)

**Remark**  
V\textsubscript{DS}: Drain-to-source voltage of the output transistor
9. Minimum operation voltage ($V_{OUT}$) vs. Power supply voltage ($V_{DD}$)

9.1 VDD detection product

S-1011A50

Pull-up to $V_{DD}$, Pull-up resistance: 100 kΩ

V_{OUT} [V] vs. V_{DD} [V] for different temperatures:

- $T_a = -40^\circ C$
- $T_a = +25^\circ C$
- $T_a = +85^\circ C$

S-1011A50

Pull-up to 16.0 V, Pull-up resistance: 100 kΩ

V_{OUT} [V] vs. V_{DD} [V] for different temperatures:

- $T_a = -40^\circ C$
- $T_a = +25^\circ C$
- $T_a = +85^\circ C$

9.2 SENSE detection product

S-1011E50

$V_{DD} = 3.0$ V,

Pull-up to $V_{DD}$, Pull-up resistance: 100 kΩ

V_{OUT} [V] vs. V_{SENSE} [V] for different temperatures:

- $T_a = -40^\circ C$
- $T_a = +25^\circ C$
- $T_a = +85^\circ C$

S-1011E50

$V_{DD} = 3.0$ V,

Pull-up to 16.0 V, Pull-up resistance: 100 kΩ

V_{OUT} [V] vs. V_{SENSE} [V] for different temperatures:

- $T_a = -40^\circ C$
- $T_a = +25^\circ C$
- $T_a = +85^\circ C$
10. Dynamic response vs. Output pin capacitance (C_{OUT}) (CP pin, CN pin; open)

10.1 VDD detection product

![Graph showing dynamic response vs. output pin capacitance for S-1011A50 at different temperatures.](image)

**Figure 43 Test Condition of Response Time**

**Figure 44 Test Circuit of Response Time**

Caution: The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

*1. V_{IH} = 36.0 V
*2. V_{IL} = 3.0 V

* \[ V_{DD} \times 50\% \]

* \[ V_{DD1} \times 50\% \]
Reference Data

1. Detection delay time ($t_{\text{RESET}}$) vs. CN pin capacitance ($C_N$) (Without output pin capacitance)
   1.1 VDD detection product

   ![Graph](image)

2. Detection delay time ($t_{\text{RESET}}$) vs. Temperature ($T_a$)
   2.1 VDD detection product

   ![Graph](image)

---

**Caution**
The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. Detection delay time ($t_{\text{RESET}}$) vs. Power supply voltage ($V_{\text{DD}}$)

3.1 SENSE detection product

![Graph showing $t_{\text{RESET}}$ vs. $V_{\text{DD}}$ with different $T_a$ values.]

**Input voltage**

V$_{\text{IH}}$ *1

**Output voltage**

V$_{\text{IL}}$ *2

V$_{\text{DD}}$

V$_{\text{SS}}$

V$_{\text{DET(S)}}$ = 1.0 V

*1. V$_{\text{IH}}$ = $V_{\text{DET(S)}}$ + 1.0 V

*2. V$_{\text{IL}}$ = $V_{\text{DET(S)}}$ - 1.0 V

Caution: The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
4. Release delay time \( (t_{\text{DELAY}}) \) vs. CP pin capacitance \( (C_P) \) (Without output pin capacitance)

4.1 VDD detection product

![Graph showing release delay time vs. CP pin capacitance](image)

5. Release delay time \( (t_{\text{DELAY}}) \) vs. Temperature \( (T_a) \)

5.1 VDD detection product

![Graph showing release delay time vs. temperature](image)

\*1. \( V_{\text{IH}} = +V_{\text{DET}} + 1.0 \text{ V} \)

\*2. \( V_{\text{IL}} = +V_{\text{DET}} - 1.0 \text{ V} \)

Figure 49 Test Condition of Release Delay Time

Figure 50 Test Circuit of Release Delay Time

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
6. Release delay time ($t_{\text{DELAY}}$) vs. Power supply voltage ($V_{\text{DD}}$)

6.1 SENSE detection product

![Graph showing $t_{\text{DELAY}}$ vs. $V_{\text{DD}}$ for different temperatures.]

Caution: The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
1. Microcomputer reset circuits

In microcomputers, when the power supply voltage is lower than the minimum operation voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the microcomputer may malfunction after that. Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.

Using the S-1011 Series which has the low minimum operation voltage, the high-accuracy detection voltage and the hysteresis width, reset circuits can be easily constructed as seen in Figure 53 and Figure 54.

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
Thermal Characteristics

1. SOT-23-6

![Figure 55 Power Dissipation of Package (When Mounted on Board)](image)

Table 21

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<thead>
<tr>
<th>Item</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Thermal resistance value ($\theta_{ja}$)</td>
<td>159°C/W</td>
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<tr>
<td>Size</td>
<td>114.3 mm × 76.2 mm × t1.6 mm</td>
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<tr>
<td>Material</td>
<td>FR-4</td>
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<tr>
<td>Number of copper foil layer</td>
<td>2</td>
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<tr>
<td>Copper foil layer</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Land pattern and wiring for testing: t0.070 mm</td>
</tr>
<tr>
<td>2</td>
<td>–</td>
</tr>
<tr>
<td>3</td>
<td>–</td>
</tr>
<tr>
<td>4</td>
<td>74.2 mm × 74.2 mm × t0.070 mm</td>
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<tr>
<td>Thermal via</td>
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</tbody>
</table>

Table 22

<table>
<thead>
<tr>
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<td>Thermal resistance value ($\theta_{ja}$)</td>
<td>124°C/W</td>
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<td>Size</td>
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*1. The board is same in SOT-23-3, SOT-23-5 and SOT-23-6.
No. MP006-A-P-SD-2.1

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ABLIC Inc.
No. MP006-A-C-SD-3.1

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ABLIC Inc.
Enlarged drawing in the central part

No. MP006-A-R-SD-2.1

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Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.

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10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.

11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.

12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.

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