

The ABLIC Inc. HDL6M05586 is an octal, 5-level RTZ, high-voltage, high-speed ultrasound pulser. The HDL6M05586 comprises logic interfaces, level translators, MOSFET gate drive buffers with floating voltage regulators, high-voltage, high-current MOSFETs, and active T/R switches.

### Functions

- Octal 5-level pulser with active T/R switch with 3-input per channel

### Features

- 0 to ±100V output voltage
- ±1.6A source and sink peak current for the 1<sup>st</sup> and 2<sup>nd</sup> high-voltage pulses ( $V_{PP1}/V_{NN1}, V_{PP2}/V_{NN2}$ )
- ±1.6A source and sink peak current for active ground clamp
- 250Ω (±0.1A) active ground clamp without blocking diode for anti-leakage (Analog SW type)
- Embedded floating voltage regulators
- Symmetrical positive and negative pulse waveforms for low 2<sup>nd</sup> order harmonic distortion
- Up to 200MHz LVDS/LVCMOS clock (transparent mode available)
- 12Ω active T/R switch with 2-bit turn-on timing control
- 20MHz output frequency @±60V output, 220pF load
- 1.8V to 5V CMOS logic interface
- Noise-cut diodes at each high-voltage output
- Embedded high-voltage clamp diodes
- 4-mode output current control for the 2<sup>nd</sup> high-voltage rail
- Automatic thermal protection with indicator
- Power-up/down reset function for free power sequencing and for fail-safe in abrupt power drop
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- 84-lead 10x10mm QFN package (RoHS compliant)

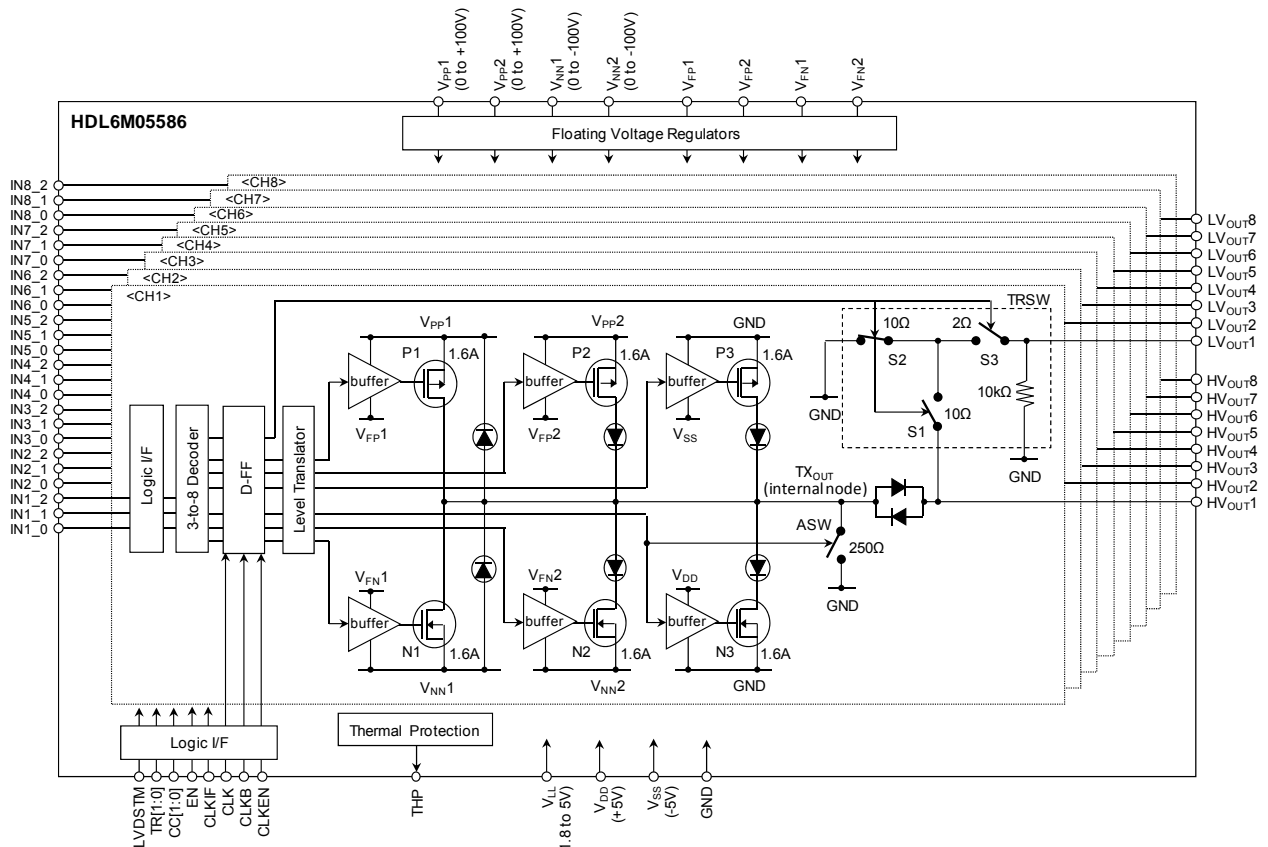


Fig.1 Block diagram

## 1. Absolute Maximum Ratings

T<sub>A</sub>=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Logic supply voltage	V <sub>LL</sub>	-0.4 to +7	V	
2	Positive supply voltage	V <sub>DD</sub>	-0.4 to +7	V	
3	Negative supply voltage	V <sub>SS</sub>	-7 to +0.4	V	
4	Positive high-voltage supplies	V <sub>PP1</sub> , V <sub>PP2</sub>	-0.5 to +105	V	
5	Negative high-voltage supplies	V <sub>NN1</sub> , V <sub>NN2</sub>	-105 to +0.5	V	
6	Positive high-voltage difference	(V <sub>PP1</sub> -V <sub>PP2</sub> )	-0.5 to +105	V	INx_[2:0]='001'
			-105 to +105	V	Other than above
7	Negative high-voltage difference	(V <sub>NN1</sub> -V <sub>NN2</sub> )	-105 to +0.5	V	INx_[2:0]='101'
			-105 to +105	V	Other than above
8	High-voltage outputs (x=1~8)	HV <sub>OUTX</sub>	-105 to +105	V	
9	Low-voltage outputs (x=1~8)	LV <sub>OUTX</sub>	-1 to +1	V	
10	THP (Thermal Protection) output	THP	-0.4 to +7	V	
11	All Logic input voltages (x=1~8)	INx_[2:0], EN, CLKEN, CLK, CLKB, CLKIF, CC[1:0], TR[1:0], LVDSTM	-0.4 to +7	V	
12	Operating junction temperature	T <sub>Jop</sub>	-20 to +150	°C	
13	Operating free-air Temperature	T <sub>A</sub>	0 to +75	°C	
14	Storage temperature	T <sub>STG</sub>	-55 to +150	°C	
15	Maximum power dissipation	P <sub>Dmax</sub>	4	W	

NOTE: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

## 2. Operating Supply Voltages, Logic Inputs, and Power sequencing

### 2.1 Operating Supply Voltages

Table 2 Operating Supply Voltages

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V <sub>LL</sub>	2.4	2.5 to 3.3	3.6	V	Clock mode
			1.7	1.8 to 5	V <sub>DD</sub>	V	Transparent mode
2	Positive supply voltage	V <sub>DD</sub>	4.75	5	5.25	V	
3	Negative supply voltage	V <sub>SS</sub>	-5.25	-5	-4.75	V	
4	Positive high-voltage supplies	V <sub>PP1</sub> , V <sub>PP2</sub>	0	-	100	V	
5	Negative high-voltage supplies	V <sub>NN1</sub> , V <sub>NN2</sub>	-100	-	0	V	
6	Positive high-voltage difference	(V <sub>PP1</sub> -V <sub>PP2</sub> )	0	-	100	V	
7	Negative high-voltage difference	(V <sub>NN1</sub> -V <sub>NN2</sub> )	-100	-	0	V	
8	IC substrate voltage *	V <sub>SUB</sub>	-	0	-	V	
9	V <sub>PPX</sub> , V <sub>NNX</sub> slew rate (x=1,2)	SR <sub>MAX</sub>	-	-	25	V/ms	

NOTE: \* The package exposed pad internally connected to the chip substrate must be soldered to the ground.

## 2.2 Logic Inputs

Clock (CLK) mode synchronizes data inputs INx\_[2:0] (x=1~8) with a differential LVDS/CMOS clock. Transparent (TP) mode without using clock is also available.

### CLK mode:

Set CLKEN=0. INx\_[2:0] are decoded, clocked, level-translated, then sent to high-voltage output stage.

Differential clock input has two modes as shown below.

- LVDS CLK mode: Set CLKIF=0. See Table 3 and 4 for the logic inputs, CLK, and CLKB.
- CMOS CLK mode: Set CLKIF=1. See Table 3 for all the logic inputs.

### TP mode:

Set CLKEN=CLKIF=1, CLK=CLKB=0. INx\_[2:0] are decoded, level-translated, then sent to high-voltage output stage. See Table 3 for all the logic inputs.

Table 3 Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level logic input voltage	V <sub>IH</sub>	0.8V <sub>LL</sub>	-	V <sub>LL</sub>	V	
2	Low-level logic input voltage	V <sub>IL</sub>	0	-	0.2V <sub>LL</sub>	V	
3	Logic input capacitance	C <sub>IN</sub>	-	3	-	pF	
4	Logic input high current *1	I <sub>IH</sub>	-10	-	10	μA	
5	Logic input low current *2	I <sub>IL</sub>	-10	-	10	μA	
6	Input rise/fall time	t <sub>r</sub> , t <sub>f</sub>	-	-	800	ps	CLK≥100MHz
			-	-	2.0	ns	CLK<100MHz
7	Input clock frequency	f <sub>CLK</sub>	-	-	200	MHz	CMOS CLK mode, CLK, CLKB,
8	Clock duty cycle	D <sub>CLK</sub>	40	50	60	%	f <sub>CLK</sub> =1/T, D <sub>CLK</sub> =τ/T, See Fig.3
9	Data setup time	t <sub>SU</sub>	1.4	-	-	ns	CLK mode
10	Data hold time	t <sub>HLD</sub>	1.4	-	-	ns	INx_[2:0] to CLK/CLKB, See Fig.3

NOTE:

\*1) TR[1:0] and LVDSTM have 50μA leakage at V<sub>LL</sub>=2.5V due to 50kΩ internal pull-down resistor.

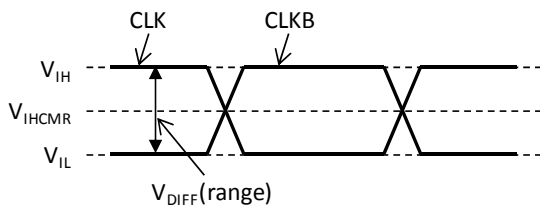
\*2) EN, CC[1:0], CLKEN, and CLKIF have 50μA leakage at V<sub>LL</sub>=2.5V due to 50kΩ internal pull-up resistor.

Table 4 LVDS Clock Inputs (CLK, CLKB)

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level input voltage	V <sub>IH</sub>	1.265	-	-	V	V <sub>IHCMR</sub> (Typ)+V <sub>DIFF</sub> (Min)/2
2	Low-level input voltage	V <sub>IL</sub>	-	-	1.135	V	V <sub>IHCMR</sub> (Typ)-V <sub>DIFF</sub> (Min)/2
3	Differential input voltage range	V <sub>DIFF</sub> (range)	0.13	0.35	0.49	±V	same as CLK,CLKB voltage swing See Fig.2
4	Differential input voltage peak to peak swing	V <sub>DIFF</sub> (p-p)	0.26	0.7	0.98	V <sub>pp</sub>	CLK-CLKB  differential peak-to-peak voltage swing, See Fig.2
5	Input voltage common mode range	V <sub>IHCMR</sub>	0.84	1.2	1.56	V	
6	Differential input impedance	R <sub>IN</sub>	85	100	115	Ω	LVDSTM=1
7	High-level input current	I <sub>IH</sub>	-	-	5.8	mA	
8	Low-level input current	I <sub>IL</sub>	-	-	5.8	mA	
9	Input rise/fall time	t <sub>r</sub> , t <sub>f</sub>	-	-	600	ps	20% to 80% of V <sub>DIFF</sub>
10	Input clock frequency	f <sub>CLK</sub>	-	-	200	MHz	LVDS CLK mode, CLK, CLKB,
11	Clock duty cycle	D <sub>CLK</sub>	40	50	60	%	f <sub>CLK</sub> =1/T, D <sub>CLK</sub> =τ/T, See Fig.3

NOTE: Please refer to table 3 for the logic inputs other than CLK, CLKB in LVDS CLK mode.

Differential input voltage range ( $V_{DIFF(range)}$ )



Differential input voltage peak to peak swing ( $V_{DIFF(p-p)}$ )

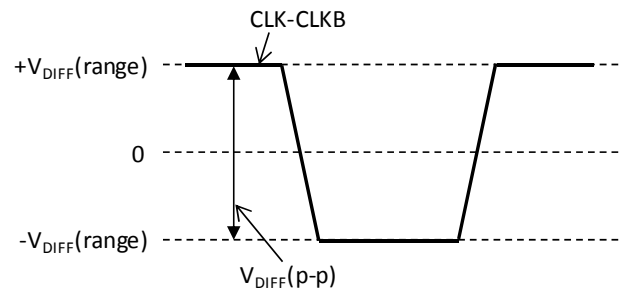


Fig.2 LVDS clock inputs

LVDS/CMOS CLK mode (CLKEN=0)

TP mode (CLKEN=1)

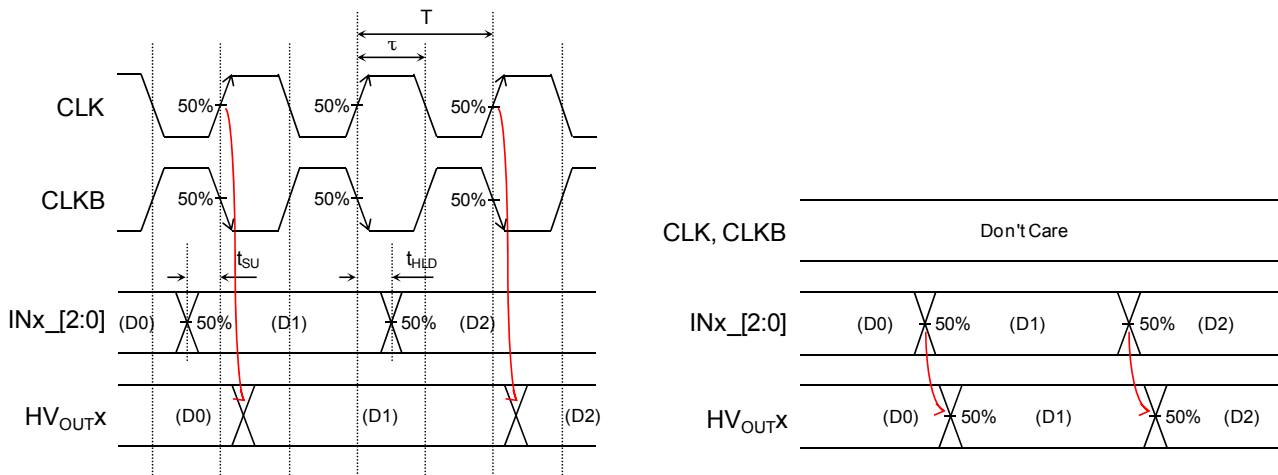


Fig.3 Setup/Hold Time

### 2.3 Power Supply Sequencing

Embedded low-voltage (LV) power-up/down reset function provides free power supply sequencing.

It also provides fail-safe system in abrupt LV power supply drop.

When any one of LV power supplies is turned off during operation, all internal circuits will be immediately reset, and both inputs and outputs will be disabled.

Once all LV power supplies are restored, both inputs and outputs will be enabled.

### 3. Typical Application Circuit

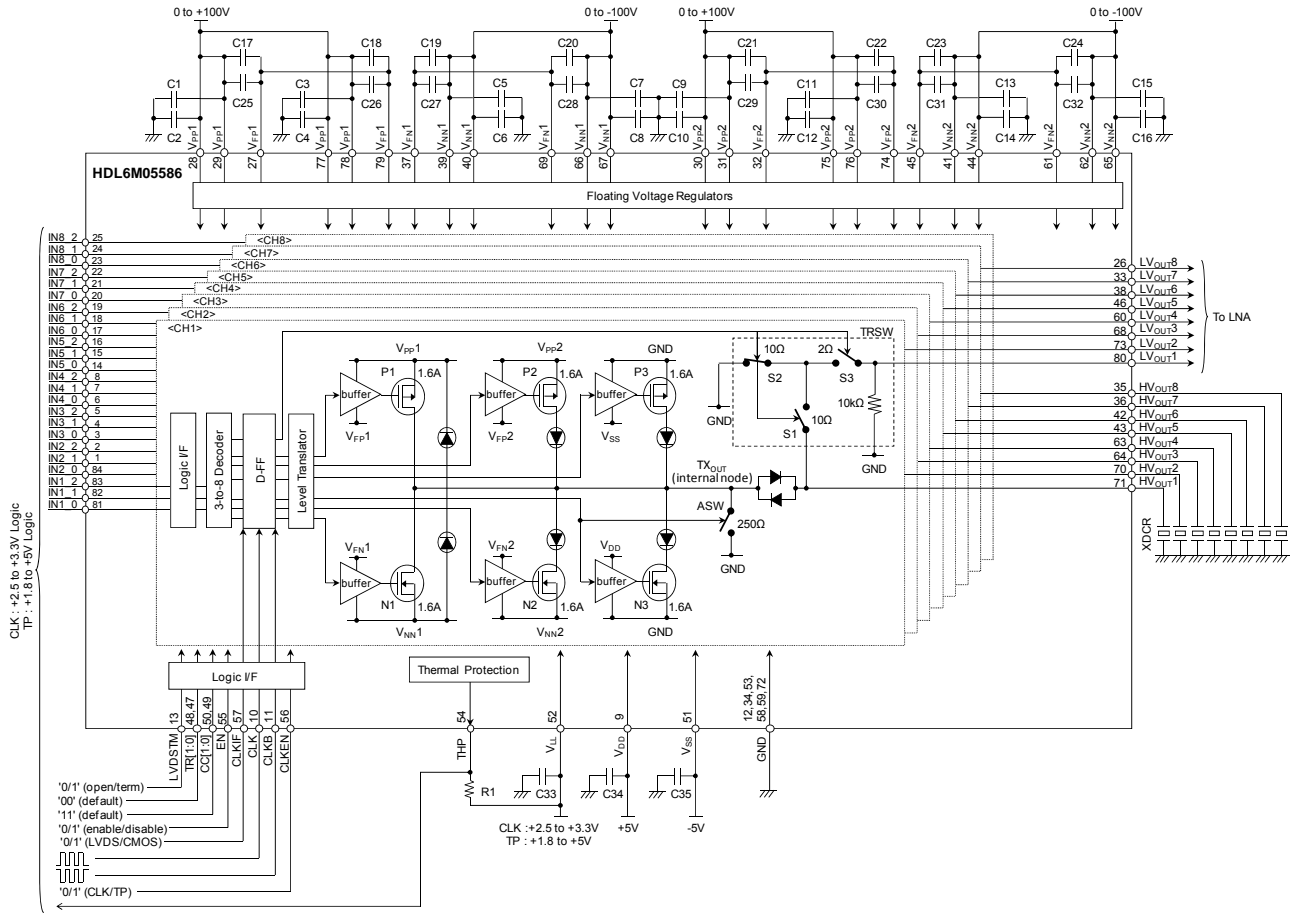


Fig.4 Typical Application Circuit

**Note:**

1. High-voltage power supply pins, V<sub>PPX</sub>/V<sub>NNX</sub> (x=1,2), can draw fast transient currents up to ±1.6A. Therefore, ceramic capacitors of ≥200V 0.1μF to 1μF (C1~16) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of ≥16V 10μF (C17~24), ≥16V 100nF (C25~32), and ≥16V 0.1μF to 1μF (C33~35) should also be connected between high-voltage power supply pins and corresponding floating voltage pins V<sub>FPX</sub>/V<sub>FNX</sub> (x=1,2), and low-voltage power supply pins for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.

## 4. Electrical Characteristics

### 4.1 Operating Supply Currents

Table 5 Operating Supply Currents

$V_{LL}=2.5V$ ,  $V_{DD}/V_{SS}=+/-5V$ ,  $T_A=25^{\circ}C$ ,  $CLK=CLKB=100MHz/0(CLKEN=0/1)$ ,  $TR[1:0]='00'$ ,  
 $HV_{OUT} load=220pF//200\Omega$ ,  $LV_{OUT} load=47pF//200\Omega$ , unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions	
			Min	Typ	Max			
1	$V_{LL}$ current	TP	-	0.03	-	mA	Quiescent current-1  EN=1(Disable) INX_[2:0]='000' Current mode 3 (CC[1:0]='11') $V_{PP1}/V_{NN1}=+/-100V$ $V_{PP2}/V_{NN2}=+/-100V$	
		LVDS CLK	-	0.13	-	mA		
		CMOS CLK	-	0.08	-	mA		
2	$V_{DD}$ current	TP	-	3.3	-	mA		
		LVDS CLK	-	3.3	-	mA		
		CMOS CLK	-	3.3	-	mA		
3	$V_{SS}$ current	$I_{SSQD}$	-	1.0	-	mA		
4	$V_{PP1}$ current	$I_{PP1QD}$	-	0.03	-	mA		
5	$V_{NN1}$ current	$I_{NN1QD}$	-	0.03	-	mA		
6	$V_{PP2}$ current	$I_{PP2QD}$	-	0.05	-	mA		
7	$V_{NN2}$ current	$I_{NN2QD}$	-	0.05	-	mA		
8	$V_{LL}$ current	TP	-	0.08	-	mA	Quiescent current-2  EN=0(Enable) INX_[2:0]='000' Current mode 3 (CC[1:0]='11') $V_{PP1}/V_{NN1}=+/-100V$ $V_{PP2}/V_{NN2}=+/-100V$	
		LVDS CLK	-	0.18	-	mA		
		CMOS CLK	-	0.13	-	mA		
9	$V_{DD}$ current	TP	-	4.2	-	mA		
		LVDS CLK	-	29	-	mA		
		CMOS CLK	-	27	-	mA		
10	$V_{SS}$ current	$I_{SSQE}$	-	1.6	-	mA		
11	$V_{PP1}$ current	$I_{PP1QE}$	-	0.15	-	mA		
12	$V_{NN1}$ current	$I_{NN1QE}$	-	0.15	-	mA		
13	$V_{PP2}$ current	$I_{PP2QE}$	-	0.17	-	mA		
14	$V_{NN2}$ current	$I_{NN2QE}$	-	0.17	-	mA		
15	$V_{LL}$ current	TP	-	0.18	-	mA		PW operating current  EN=0 Current mode 3 (CC[1:0]='11') 8-channel active Bipolar 3-level 2-cycle P1/N1-drive f=5MHz, PRT=200μs $V_{PP1}/V_{NN1}=+/-60V$ $V_{PP2}/V_{NN2}=+/-60V$
		LVDS CLK	-	0.18	-	mA		
		CMOS CLK	-	0.13	-	mA		
16	$V_{DD}$ current	TP	-	11	-	mA		
		LVDS CLK	-	37	-	mA		
		CMOS CLK	-	35	-	mA		
17	$V_{SS}$ current	$I_{SSPW}$	-	10	-	mA		
18	$V_{PP1}$ current	$I_{PP1PW}$	-	4.0	-	mA		
19	$V_{NN1}$ current	$I_{NN1PW}$	-	4.6	-	mA		
20	$V_{PP2}$ current	$I_{PP2PW}$	-	0.17	-	mA		
21	$V_{NN2}$ current	$I_{NN2PW}$	-	0.17	-	mA		

Table 5 Operating Supply Currents (continued)

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
22	V <sub>LL</sub> current	TP	I <sub>LLCW3</sub>	-	0.43	-	mA	CW operating current-1 EN=0 Current mode 3 (CC[1:0]='11') 8-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz V <sub>PP1</sub> /V <sub>NN1</sub> =+/-5V V <sub>PP2</sub> /V <sub>NN2</sub> =+/-5V
		LVDS CLK		-	0.53	-	mA	
		CMOS CLK		-	0.48	-	mA	
23	V <sub>DD</sub> current	TP	I <sub>DDCW3</sub>	-	39	-	mA	
		LVDS CLK		-	60	-	mA	
		CMOS CLK		-	58	-	mA	
24	V <sub>SS</sub> current		I <sub>SSCW3</sub>	-	26	-	mA	
25	V <sub>PP1</sub> current		I <sub>PP1CW3</sub>	-	0.15	-	mA	
26	V <sub>NN1</sub> current		I <sub>NN1CW3</sub>	-	0.15	-	mA	
27	V <sub>PP2</sub> current		I <sub>PP2CW3</sub>	-	171	-	mA	
28	V <sub>NN2</sub> current		I <sub>NN2CW3</sub>	-	173	-	mA	
29	V <sub>LL</sub> current	TP	I <sub>LLCW2</sub>	-	0.48	-	mA	CW operating current-2 EN=0 Current mode 2 (CC[1:0]='10') 8-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz V <sub>PP1</sub> /V <sub>NN1</sub> =+/-5V V <sub>PP2</sub> /V <sub>NN2</sub> =+/-5V
		LVDS CLK		-	0.58	-	mA	
		CMOS CLK		-	0.53	-	mA	
30	V <sub>DD</sub> current	TP	I <sub>DDCW2</sub>	-	35	-	mA	
		LVDS CLK		-	57	-	mA	
		CMOS CLK		-	55	-	mA	
31	V <sub>SS</sub> current		I <sub>SSCW2</sub>	-	23	-	mA	
32	V <sub>PP1</sub> current		I <sub>PP1CW2</sub>	-	0.15	-	mA	
33	V <sub>NN1</sub> current		I <sub>NN1CW2</sub>	-	0.15	-	mA	
34	V <sub>PP2</sub> current		I <sub>PP2CW2</sub>	-	164	-	mA	
35	V <sub>NN2</sub> current		I <sub>NN2CW2</sub>	-	166	-	mA	
36	V <sub>LL</sub> current	TP	I <sub>LLCW1</sub>	-	0.48	-	mA	CW operating current-3 EN=0 Current mode 1 (CC[1:0]='01') 8-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz V <sub>PP1</sub> /V <sub>NN1</sub> =+/-5V V <sub>PP2</sub> /V <sub>NN2</sub> =+/-5V
		LVDS CLK		-	0.58	-	mA	
		CMOS CLK		-	0.53	-	mA	
37	V <sub>DD</sub> current	TP	I <sub>DDCW1</sub>	-	31	-	mA	
		LVDS CLK		-	53	-	mA	
		CMOS CLK		-	51	-	mA	
38	V <sub>SS</sub> current		I <sub>SSCW1</sub>	-	19	-	mA	
39	V <sub>PP1</sub> current		I <sub>PP1CW1</sub>	-	0.15	-	mA	
40	V <sub>NN1</sub> current		I <sub>NN1CW1</sub>	-	0.15	-	mA	
41	V <sub>PP2</sub> current		I <sub>PP2CW1</sub>	-	153	-	mA	
42	V <sub>NN2</sub> current		I <sub>NN2CW1</sub>	-	155	-	mA	
43	V <sub>LL</sub> current	TP	I <sub>LLCW0</sub>	-	0.53	-	mA	CW operating current-4 EN=0 Current mode 0 (CC[1:0]='00') 8-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz V <sub>PP1</sub> /V <sub>NN1</sub> =+/-5V V <sub>PP2</sub> /V <sub>NN2</sub> =+/-5V
		LVDS CLK		-	0.63	-	mA	
		CMOS CLK		-	0.58	-	mA	
44	V <sub>DD</sub> current	TP	I <sub>DDCW0</sub>	-	26	-	mA	
		LVDS CLK		-	48	-	mA	
		CMOS CLK		-	46	-	mA	
45	V <sub>SS</sub> current		I <sub>SSCW0</sub>	-	15	-	mA	
46	V <sub>PP1</sub> current		I <sub>PP1CW0</sub>	-	0.15	-	mA	
47	V <sub>NN1</sub> current		I <sub>NN1CW0</sub>	-	0.15	-	mA	
48	V <sub>PP2</sub> current		I <sub>PP2CW0</sub>	-	131	-	mA	
49	V <sub>NN2</sub> current		I <sub>NN2CW0</sub>	-	133	-	mA	

## 4.2 Static Characteristics

Table 6 Static Characteristics

$V_{LL}=2.5V$ ,  $V_{DD}/V_{SS}=\pm 5V$ ,  $T_A=25^\circ C$ , unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	HV <sub>OUTX</sub> output voltage range	HV <sub>OUTX</sub>	-100	-	+100	V	
2	HV <sub>OUTX</sub> high-side peak current	I <sub>OH</sub>	-	1.6	-	A	P1 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V
			-	1.6	-	A	P2 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V Current mode 3 (CC[1:0]='11')
			-	1.28	-	A	P2 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V Current mode 2 (CC[1:0]='10')
			-	0.96	-	A	P2 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V Current mode 1 (CC[1:0]='01')
			-	0.64	-	A	P2 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V Current mode 0 (CC[1:0]='00')
3	HV <sub>OUTX</sub> high-side GND clamp peak current	I <sub>OHCL</sub>	-	1.6	-	A	N3 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V
4	HV <sub>OUTX</sub> low-side peak current	I <sub>OL</sub>	-	1.6	-	A	N1 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V
			-	1.6	-	A	N2 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V Current mode 3 (CC[1:0]='11')
			-	1.28	-	A	N2 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V Current mode 2 (CC[1:0]='10')
			-	0.96	-	A	N2 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V Current mode 1 (CC[1:0]='01')
			-	0.64	-	A	N2 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V Current mode 0 (CC[1:0]='00')
5	HV <sub>OUTX</sub> low-side GND clamp peak current	I <sub>OLCL</sub>	-	1.6	-	A	P3 active, V <sub>PP1</sub> /V <sub>NN1</sub> =V <sub>PP2</sub> /V <sub>NN2</sub> =±60V
6	HV <sub>OUTX</sub> high-side on-resistance	R <sub>ONH</sub>	-	15	-	Ω	P1 active, I <sub>OH</sub> =100mA
			-	15	-	Ω	P2 active, I <sub>OH</sub> =100mA Current mode 3 (CC[1:0]='11')
			-	17	-	Ω	P2 active, I <sub>OH</sub> =100mA Current mode 2 (CC[1:0]='10')
			-	20	-	Ω	P2 active, I <sub>OH</sub> =100mA Current mode 1 (CC[1:0]='01')
			-	30	-	Ω	P2 active, I <sub>OH</sub> =100mA Current mode 0 (CC[1:0]='00')
7	HV <sub>OUTX</sub> high-side GND clamp on-resistance	R <sub>ONHCL</sub>	-	15	-	Ω	N3 active, I <sub>OHCL</sub> =100mA
8	HV <sub>OUTX</sub> low-side on-resistance	R <sub>ONL</sub>	-	15	-	Ω	N1 active, I <sub>OL</sub> =100mA
			-	15	-	Ω	N2 active, I <sub>OL</sub> =100mA Current mode 3 (CC[1:0]='11')
			-	17	-	Ω	N2 active, I <sub>OL</sub> =100mA Current mode 2 (CC[1:0]='10')
			-	20	-	Ω	N2 active, I <sub>OL</sub> =100mA Current mode 1 (CC[1:0]='01')
			-	30	-	Ω	N2 active, I <sub>OL</sub> =100mA Current mode 0 (CC[1:0]='00')
9	HV <sub>OUTX</sub> low-side GND clamp on-resistance	R <sub>ONLCL</sub>	-	15	-	Ω	P3 active, I <sub>OLCL</sub> =100mA
10	HV <sub>OUTX</sub> off-capacitance	C <sub>HVOFF</sub>	-	34	-	pF	TX <sub>OUTX</sub> =GND, TRSW=off



### 4.3 Dynamic Characteristics

Table 7 Dynamic Characteristics

$V_{LL}=2.5V$ ,  $V_{DD}/V_{SS}=+/-5V$ ,  $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$ ,  $T_A=25^{\circ}C$ ,  $TR[1:0]='00'$ ,  $CC[1:0]='11'$ ,  
 $CLK=CLKB=100MHz/0(CLKEN=0/1)$ ,  $HV_{OUT}$  load= $220pF//200\Omega$ ,  $LV_{OUT}$  load= $47pF//200\Omega$ , unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions	
				Min	Typ	Max			
1	Output frequency		$f_{OUT}$	-	20	-	MHz		
2	Output rise propagation delay	TP mode	$t_{dr}$	-	28	-	ns	See Fig.5	
		CLK mode		-	36	-	ns		
3	Output fall propagation delay	TP mode	$t_{df}$	-	28	-	ns		
		CLK mode		-	36	-	ns		
4	Output rise propagation delay clamp	TP mode	$t_{drCL}$	-	28	-	ns		
		CLK mode		-	36	-	ns		
5	Output fall propagation delay clamp	TP mode	$t_{dfCL}$	-	28	-	ns		
		CLK mode		-	36	-	ns		
6	Propagation delay matching		$\Delta t_d$	-	±1	±3	ns		
7	Output rise time		$t_r$	-	19	-	ns		P1 active
				-	19	-	ns	P2 active, CC[1:0]='11'	
				-	23	-	ns	P2 active, CC[1:0]='10'	
				-	31	-	ns	P2 active, CC[1:0]='01'	
				-	44	-	ns	P2 active, CC[1:0]='00'	
		$t_{rCL}$	-	10	-	ns	P3 active		
8	Output fall time		$t_f$	-	19	-	ns	N1 active	
				-	19	-	ns	N2 active, CC[1:0]='11'	
				-	23	-	ns	N2 active, CC[1:0]='10'	
				-	31	-	ns	N2 active, CC[1:0]='01'	
				-	44	-	ns	N2 active, CC[1:0]='00'	
		$t_{fCL}$	-	10	-	ns	N3 active		
9	2 <sup>nd</sup> harmonic distortion		HD2	-	-40	-	dBc	Bipolar, 2-cyc, $f_{OUT}=5MHz$	
10	Pulse cancellation		HDPC	-	-40	-	dBc	See Fig.6	
			HDPC2	-	-40	-	dBc		
11	RMS output jitter		$t_j$	-	10	-	ps	Bipolar CW, $f_{OUT}=5MHz$ $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-5V$	
12	Crosstalk between channels		$X_{TLK}$	-	-70	-	dB	$f_{OUT}=5MHz$ , $10V_{p-p}$ , $HV_{OUT}$ load= $50\Omega$	
13	Output enable time	TP	$t_{EN}$	-	28	-	ns	See Fig.7	
		LVDS CLK		-	115	-	ns		
		CMOS CLK		-	140	-	ns		
14	Output disable time		$t_{DS}$	-	36	-	ns		
15	Clock mode enable time		$t_{CLKEN}$	-	36	-	ns		
16	Clock mode disable time		$t_{CLKDS}$	-	36	-	ns		

#### 4.4 Integrated Peripheral Circuits Characteristics

##### T/R Switch

Table 8 T/R Switch Characteristics

$V_{LL}=2.5V$ ,  $V_{DD}/V_{SS}=+/-5V$ ,  $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$ ,  $T_A=25^{\circ}C$ , unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions	
			Min	Typ	Max			
1	LV <sub>OUTX</sub> output voltage range	LV <sub>OUTX</sub>	-0.85	-	0.85	V		
2	TRSW on-resistance	R <sub>ONTR</sub>	-	12	-	Ω	HV <sub>OUTX</sub> =100mV, LV <sub>OUTX</sub> =0V	
3	TRSW on-capacitance	C <sub>ONTR</sub>	-	13	-	pF	LV <sub>OUTX</sub> =0V	
4	TRSW off-resistance on HV <sub>OUTX</sub>	R <sub>OFFTRHV</sub>	1	-	-	MΩ		
5	TRSW off-resistance on LV <sub>OUTX</sub>	R <sub>OFFTRLV</sub>	8	10	12	kΩ		
6	Spike voltage on HV <sub>OUTX</sub> and LV <sub>OUTX</sub>	V <sub>TRN</sub>	-	-	50	mV <sub>PP</sub>	50pF//200Ω load on HV <sub>OUTX</sub> 20pF//200Ω load on LV <sub>OUTX</sub>	
7	TRSW turn-on time	t <sub>dTRON</sub>	TR[1:0]='00'	-	300	-	ns	Logic input-to-ready for Rx signal See Fig.8
			TR[1:0]='01'	-	400	-	ns	
			TR[1:0]='10'	-	500	-	ns	
			TR[1:0]='11'	-	600	-	ns	
8	TRSW turn-off time	t <sub>dTROFF</sub>	-	50	100	ns	See Fig.8	
9	Tx setup time	t <sub>TXSU</sub>	100	-	-	ns	INx_[2:0]='100'(GND) for at least 100ns before Tx burst. See Fig.8	

##### Analog Switch

Table 9 Analog Switch Characteristics

$T_A=25^{\circ}C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	ASW on-resistance	R <sub>ONASW</sub>	-	250	-	Ω	

##### HV Blocking Diode

Table 10 Output HV Blocking Diode Characteristics

$T_A=25^{\circ}C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V <sub>FHVD</sub>	-	1.0	-	V	I <sub>F</sub> =100mA
			-	1.2	-	V	I <sub>F</sub> =200mA
2	Reverse voltage	V <sub>RHVD</sub>	200	-	-	V	I <sub>R</sub> =1μA

##### LV Noise-cut Diode

Table 11 Output LV Noise-cut Diode Characteristics

$T_A=25^{\circ}C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V <sub>FLVD</sub>	-	1.1	-	V	I <sub>F</sub> =100mA
			-	1.25	-	V	I <sub>F</sub> =200mA

Thermal Protection

Table 12 Thermal Protection Characteristics

$V_{LL}=2.5V$ ,  $V_{DD}/V_{SS}=+/-5V$ ,  $T_A=25^{\circ}C$ , unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	$V_{PUTHP}$	-	-	5.25	V	Open drain
2	THP output current	$I_{THP}$	-	1.0	-	mA	-
3	THP output low voltage	$V_{OLTHP}$	-	-	0.5	V	THP active, $V_{LL}=2.5V$ , $I_{THP}=1mA$
4	THP temperature threshold	$T_{THP}$	90	110	130	$^{\circ}C$	
5	THP reset hysteresis	$T_{HYSTHP}$	-	10	-	$^{\circ}C$	

### 5. Switching Time Diagram

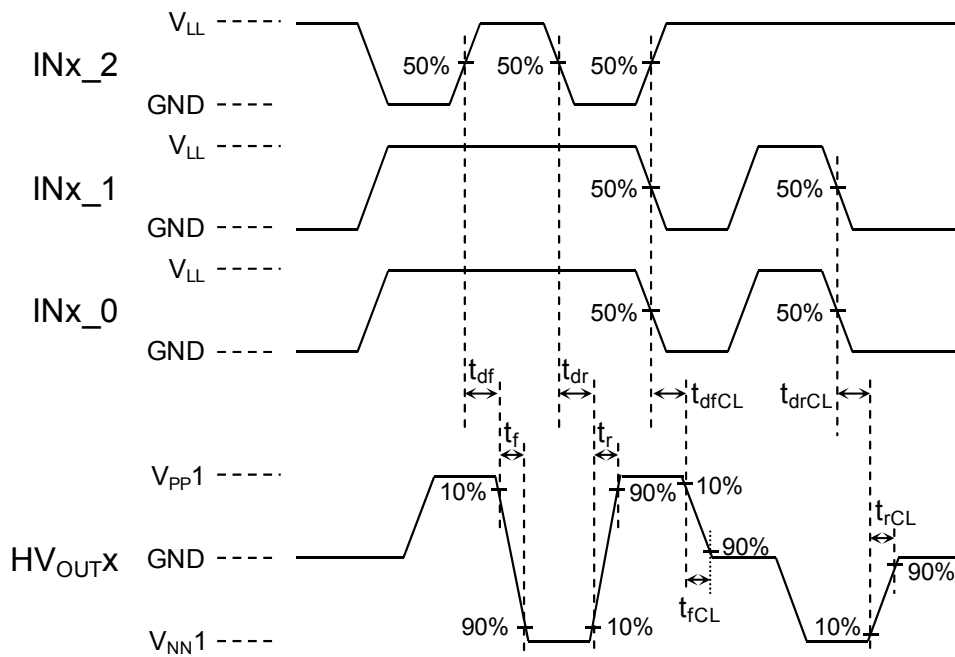
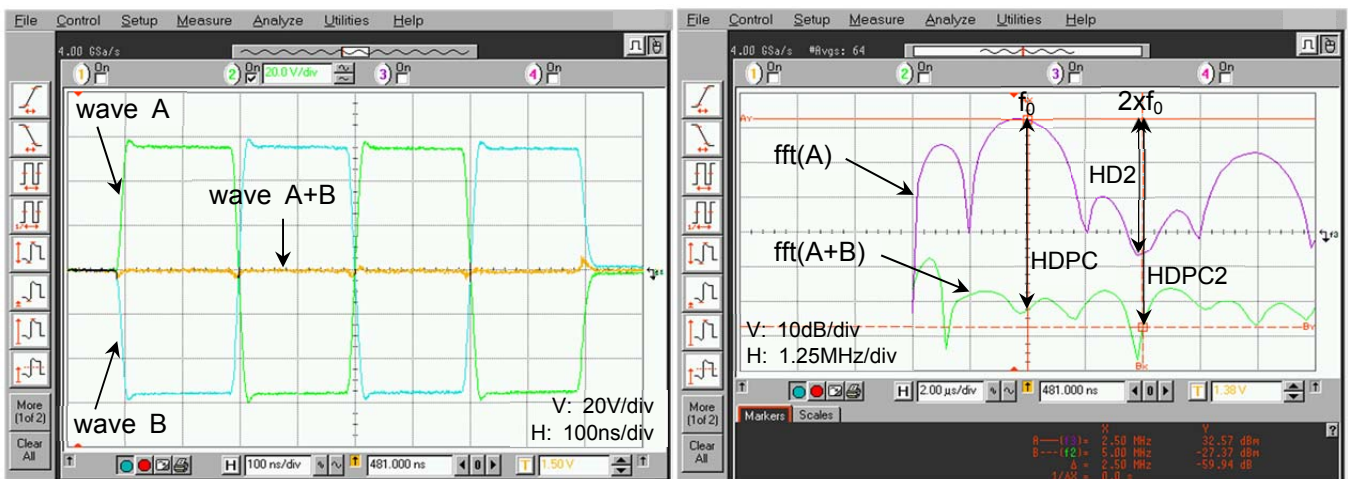


Fig.5 Propagation delay and Output rise/fall time



Example waveforms:  $V_{PP}/V_{NN} = \pm 60V$ ,  $f_0 = 2.5MHz$ , 2-cycle,  $HV_{OUT}$  load =  $220pF // 200\Omega$

Fig.6 2<sup>nd</sup> harmonic distortion and Pulse cancellation

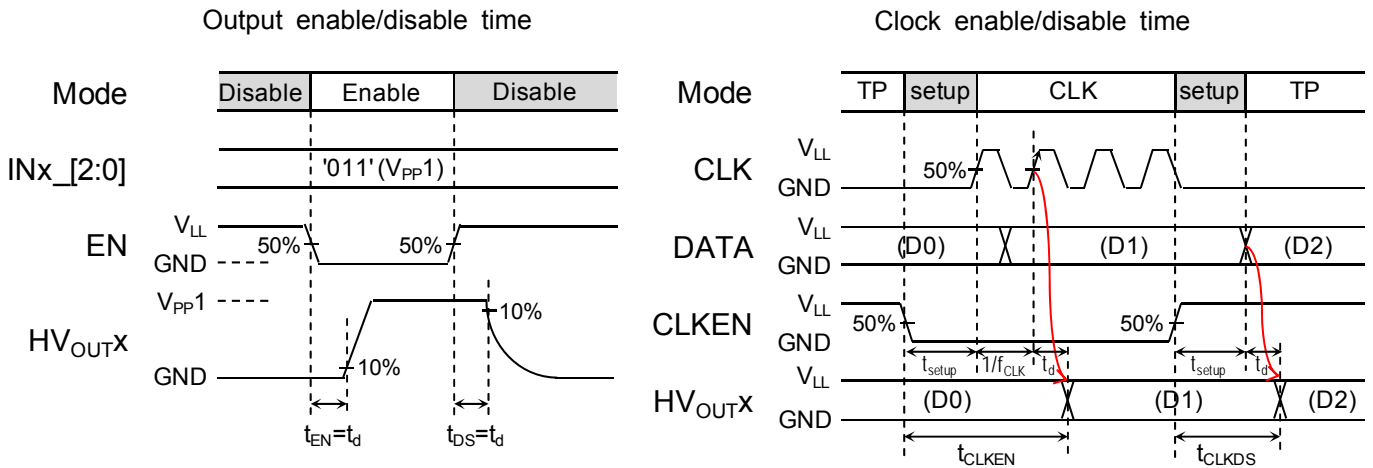


Fig.7 Output enable/disable and Clock enable/disable time

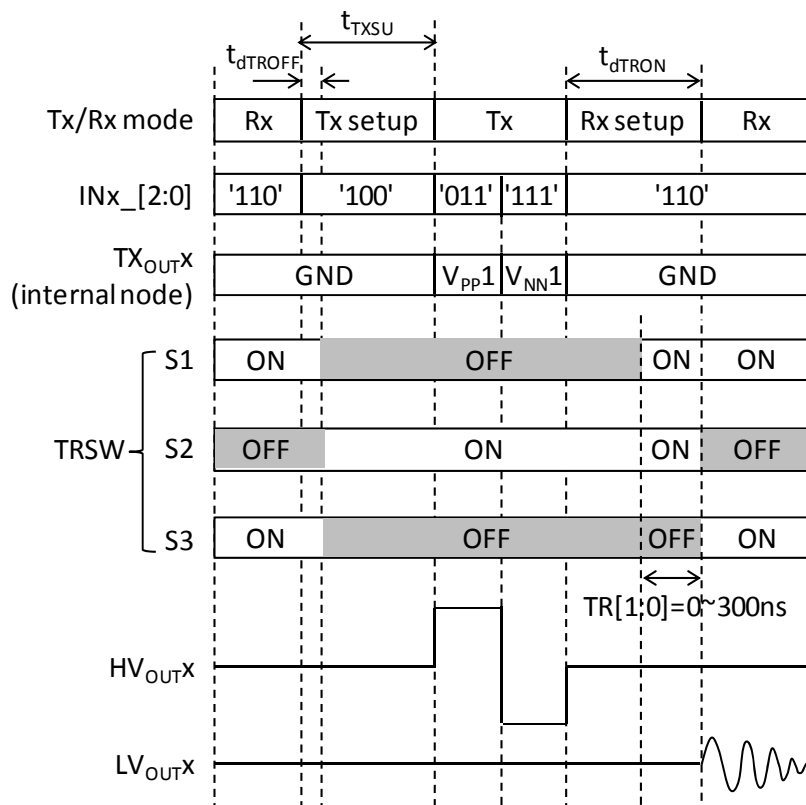


Fig.8 T/R Switch turn-on/off time

## 6. Truth Table and Mode Control table

Table 13 Truth table

Logic Inputs				Internal MOSFET state										Output state		
EN	INx_2	INx_1	INx_0	P1	N1	P2	N2	P3	N3	ASW	TRSW			TX <sub>OUTX</sub> (internal node)	LV <sub>OUTX</sub>	
				+HV1	-HV1	+HV2	-HV2	GND	GND	GND	S1	S2	S3			
0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	HiZ	10kΩ
0	0	0	1	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	+HV2	10kΩ
0	0	1	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	HiZ	HV <sub>OUTX</sub>
0	0	1	1	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	+HV1	10kΩ
0	1	0	0	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	GND	10kΩ
0	1	0	1	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	-HV2	10kΩ
0	1	1	0	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	OFF	GND	HV <sub>OUTX</sub>
0	1	1	1	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	-HV1	10kΩ
1	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	HiZ	10kΩ

Note: V<sub>PP1</sub>/ V<sub>NN1</sub>=+/-HV1, V<sub>PP2</sub>/ V<sub>NN2</sub>=+/-HV2, x=1~8

Table 14 P2/N2 drive current mode

Current Mode	CC1	CC0	I <sub>out</sub> [A]	
			P2	N2
0	0	0	0.64	0.64
1	0	1	0.96	0.96
2	1	0	1.28	1.28
3	1	1	1.6	1.6

Note:

Recommended mode is as follows:

- Current mode 2 or 3 for high-amplitude short cycle pulse waveforms, or for driving a heavy load
- Current mode 0 or 1 for low-amplitude long pulse train waveforms (e.g. CW), or for driving a light load

Table 15 TRSW S1-S2 turn-on overlap time control mode

TRSW Control Mode	TR1	TR0	S1-S2 ON
			overlap time [ns]
0	0	0	0 (default)
1	0	1	100
2	1	0	200
3	1	1	300

Note: Detailed switching time diagram is shown in Fig.8

## 7. Pin Configuration

Table 16 Pin Configuration

Pin#	Pin Name	I/O	Function
1	IN2_1	I	The 2 <sup>nd</sup> significant bit of logic input of channel 2
2	IN2_2	I	The most significant bit of logic input of channel 2
3	IN3_0	I	The least significant bit of logic input of channel 3
4	IN3_1	I	The 2 <sup>nd</sup> significant bit of logic input of channel 3
5	IN3_2	I	The most significant bit of logic input of channel 3
6	IN4_0	I	The least significant bit of logic input of channel 4
7	IN4_1	I	The 2 <sup>nd</sup> significant bit of logic input of channel 4
8	IN4_2	I	The most significant bit of logic input of channel 4
9	V <sub>DD</sub>	-	Positive low voltage power supply (+5V)
10	CLK	I	Positive clock input (up to 200MHz)
11	CLKB	I	Negative clock Input (up to 200MHz)
12	GND	-	Drive power ground (0V)
13	LV <sub>DSTM</sub>	I	Control of LVDS termination between CLK and CLKB, Hi=embedded 100Ω, Low=open (50kΩ internal pull-down resistor)
14	IN5_0	I	The least significant bit of logic input of channel 5
15	IN5_1	I	The 2 <sup>nd</sup> significant bit of logic input of channel 5
16	IN5_2	I	The most significant bit of logic input of channel 5
17	IN6_0	I	The least significant bit of logic input of channel 6
18	IN6_1	I	The 2 <sup>nd</sup> significant bit of logic input of channel 6
19	IN6_2	I	The most significant bit of logic input of channel 6
20	IN7_0	I	The least significant bit of logic input of channel 7
21	IN7_1	I	The 2 <sup>nd</sup> significant bit of logic input of channel 7
22	IN7_2	I	The most significant bit of logic input of channel 7
23	IN8_0	I	The least significant bit of logic input of channel 8
24	IN8_1	I	The 2 <sup>nd</sup> significant bit of logic input of channel 8
25	IN8_2	I	The most significant bit of logic input of channel 8
26	LV <sub>OUT8</sub>	O	Low voltage output of channel 8
27	V <sub>FP1</sub>	-	Built-in power supply for P-MOS (P1) gate drive
28	V <sub>PP1</sub>	-	Positive high voltage power supply 1 (0 to +100V)
29	V <sub>PP1</sub>	-	Positive high voltage power supply 1 (0 to +100V)
30	V <sub>PP2</sub>	-	Positive high voltage power supply 2 (0 to +100V)
31	V <sub>PP2</sub>	-	Positive high voltage power supply 2 (0 to +100V)
32	V <sub>FP2</sub>	-	Built-in power supply for P-MOS (P2) gate drive
33	LV <sub>OUT7</sub>	O	Low voltage output of channel 7
34	GND	-	Drive power ground (0V)
35	HV <sub>OUT8</sub>	O	High voltage output of channel 8
36	HV <sub>OUT7</sub>	O	High voltage output of channel 7
37	V <sub>FN1</sub>	-	Built-in power supply for N-MOS (N1) gate drive
38	LV <sub>OUT6</sub>	O	Low voltage output of channel 6
39	V <sub>NN1</sub>	-	Negative high voltage power supply 1 (0 to -100V)
40	V <sub>NN1</sub>	-	Negative high voltage power supply 1 (0 to -100V)
41	V <sub>NN2</sub>	-	Negative high voltage power supply 2 (0 to -100V)
42	HV <sub>OUT6</sub>	O	High voltage output of channel 6

Table 16 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
43	HV <sub>OUT5</sub>	O	High voltage output of channel 5
44	V <sub>NN2</sub>	-	Negative high voltage power supply 2 (0 to -100V)
45	V <sub>FN2</sub>	-	Built-in power supply for N-MOS (N2) gate drive
46	LV <sub>OUT5</sub>	O	Low voltage output of channel 5
47	TR0	I	Lower bit of control of T/R switch S1 and S2 turn-on overlap time (50kΩ internal pull-down resistor)
48	TR1	I	Upper bit of control of T/R switch S1 and S2 turn-on overlap time (50kΩ internal pull-down resistor)
49	CC0	I	Lower bit of control of P2/N2 drive current (50kΩ internal pull-up resistor)
50	CC1	I	Upper bit of control of P2/N2 drive current (50kΩ internal pull-up resistor)
51	V <sub>SS</sub>	-	Negative low voltage power supply (-5V)
52	V <sub>LL</sub>	-	Positive voltage supply of logic input interface (1.8 to 5V)
53	GND	-	Drive power ground (0V)
54	THP	O	Thermal protection output flag, open N-MOS drain
55	EN	I	Control of drive output enable, Hi=disable, Low=enable (50kΩ internal pull-up resistor)
56	CLKEN	I	Control of clock enable, Hi=clock disable, Low=clock enable (50kΩ internal pull-up resistor)
57	CLKIF	I	Control of clock interface, Hi=differential CMOS, Low=LVDS (50kΩ internal pull-up resistor)
58	GND	-	Drive power ground (0V)
59	GND	-	Drive power ground (0V)
60	LV <sub>OUT4</sub>	O	Low voltage output of channel 4
61	V <sub>FN2</sub>	-	Built-in power supply for N-MOS (N2) gate drive
62	V <sub>NN2</sub>	-	Negative high voltage power supply 2 (0 to -100V)
63	HV <sub>OUT4</sub>	O	High voltage output of channel 4
64	HV <sub>OUT3</sub>	O	High voltage output of channel 3
65	V <sub>NN2</sub>	-	Negative high voltage power supply 2 (0 to -100V)
66	V <sub>NN1</sub>	-	Negative high voltage power supply 1 (0 to -100V)
67	V <sub>NN1</sub>	-	Negative high voltage power supply 1 (0 to -100V)
68	LV <sub>OUT3</sub>	O	Low voltage output of channel 3
69	V <sub>FN1</sub>	-	Built-in power supply for N-MOS (N1) gate drive
70	HV <sub>OUT2</sub>	O	High voltage output of channel 2
71	HV <sub>OUT1</sub>	O	High voltage output of channel 1
72	GND	-	Drive power ground (0V)
73	LV <sub>OUT2</sub>	O	Low voltage output of channel 2
74	V <sub>FP2</sub>	-	Built-in power supply for P-MOS (P2) gate drive
75	V <sub>PP2</sub>	-	Positive high voltage power supply 2 (0 to +100V)
76	V <sub>PP2</sub>	-	Positive high voltage power supply 2 (0 to +100V)
77	V <sub>PP1</sub>	-	Positive high voltage power supply 1 (0 to +100V)
78	V <sub>PP1</sub>	-	Positive high voltage power supply 1 (0 to +100V)
79	V <sub>FP1</sub>	-	Built-in power supply for P-MOS (P1) gate drive
80	LV <sub>OUT1</sub>	O	Low voltage output of channel 1
81	IN1_0	I	The least significant bit of logic input of channel 1
82	IN1_1	I	The 2 <sup>nd</sup> significant bit of logic input of channel 1
83	IN1_2	I	The most significant bit of logic input of channel 1
84	IN2_0	I	The least significant bit of logic input of channel 2



8. Package Outline

Unit: mm

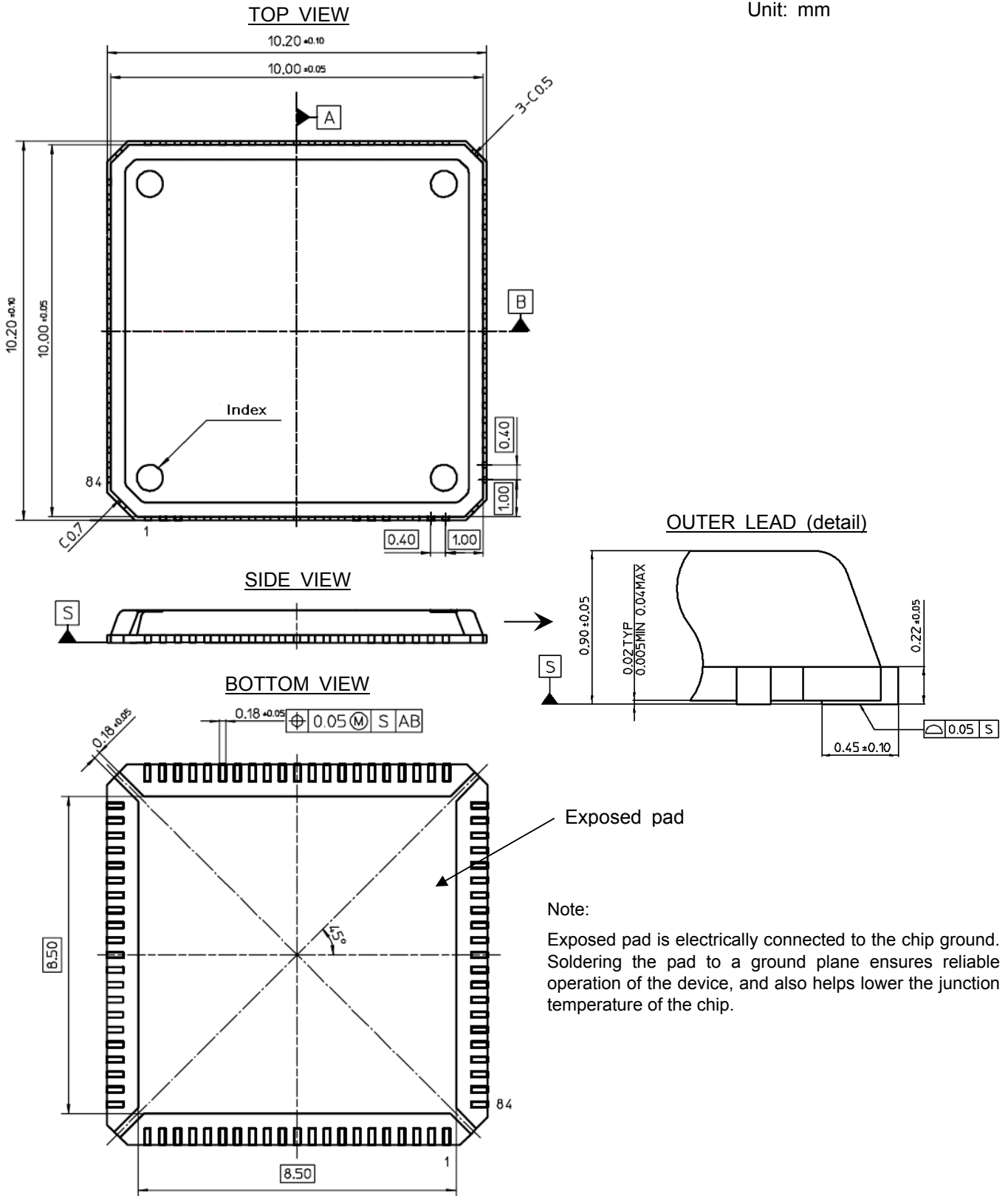
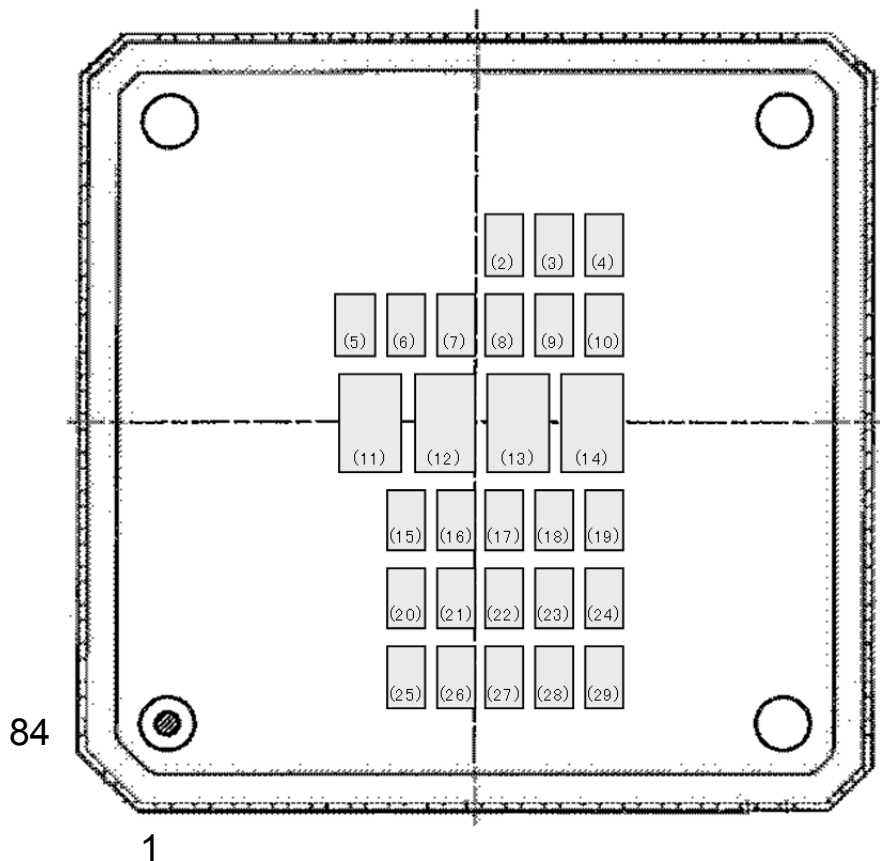


Fig.9 Package Outline (84-Lead QFN Package)

9. Package Marking



No.	Code
(2)	Year sealed : the last one digit of the year
(3)	Month sealed : A~M (exc. " I ") in the order of Jan. to Dec.
(4)	Week sealed : 1~5
(5)~(14)	HDL6M05586 (product name)
(15)~(24)	Quality control code
(25)~(29)	Country of origin

Fig.10 Package Marking

10. Transport Media, Quantity

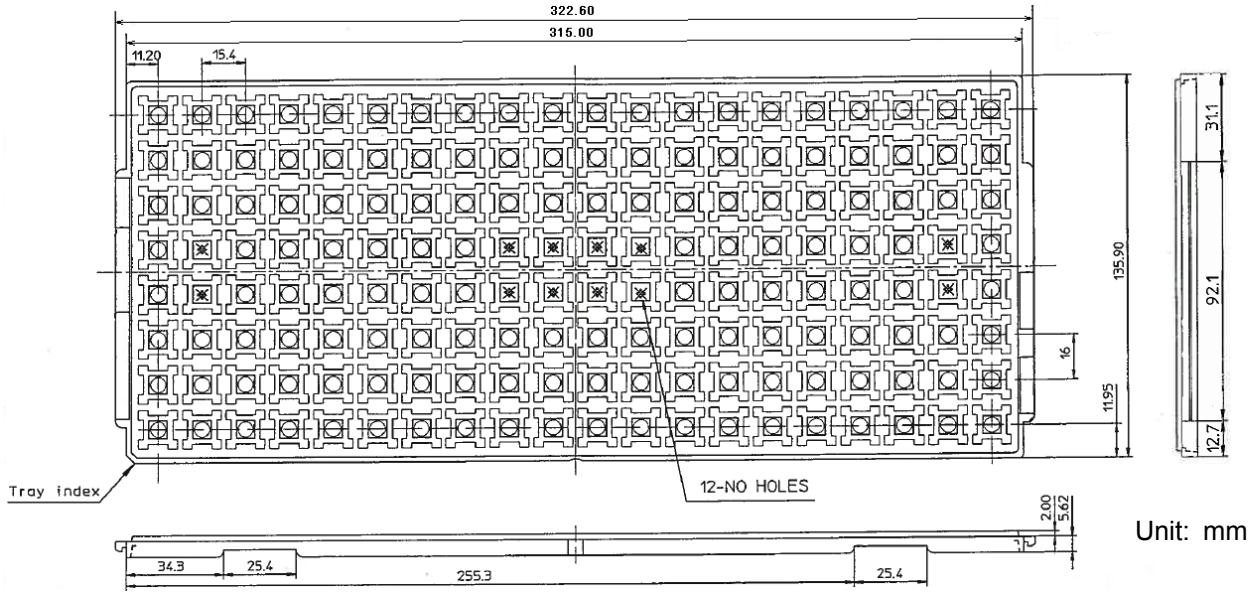


Fig.11 IC Tray Outline

1. Max 160 IC/Tray
2. 12 positions without holes (\*)
3. PPE containing carbon and static proof
4. Heat proof: 130°C, 24hr

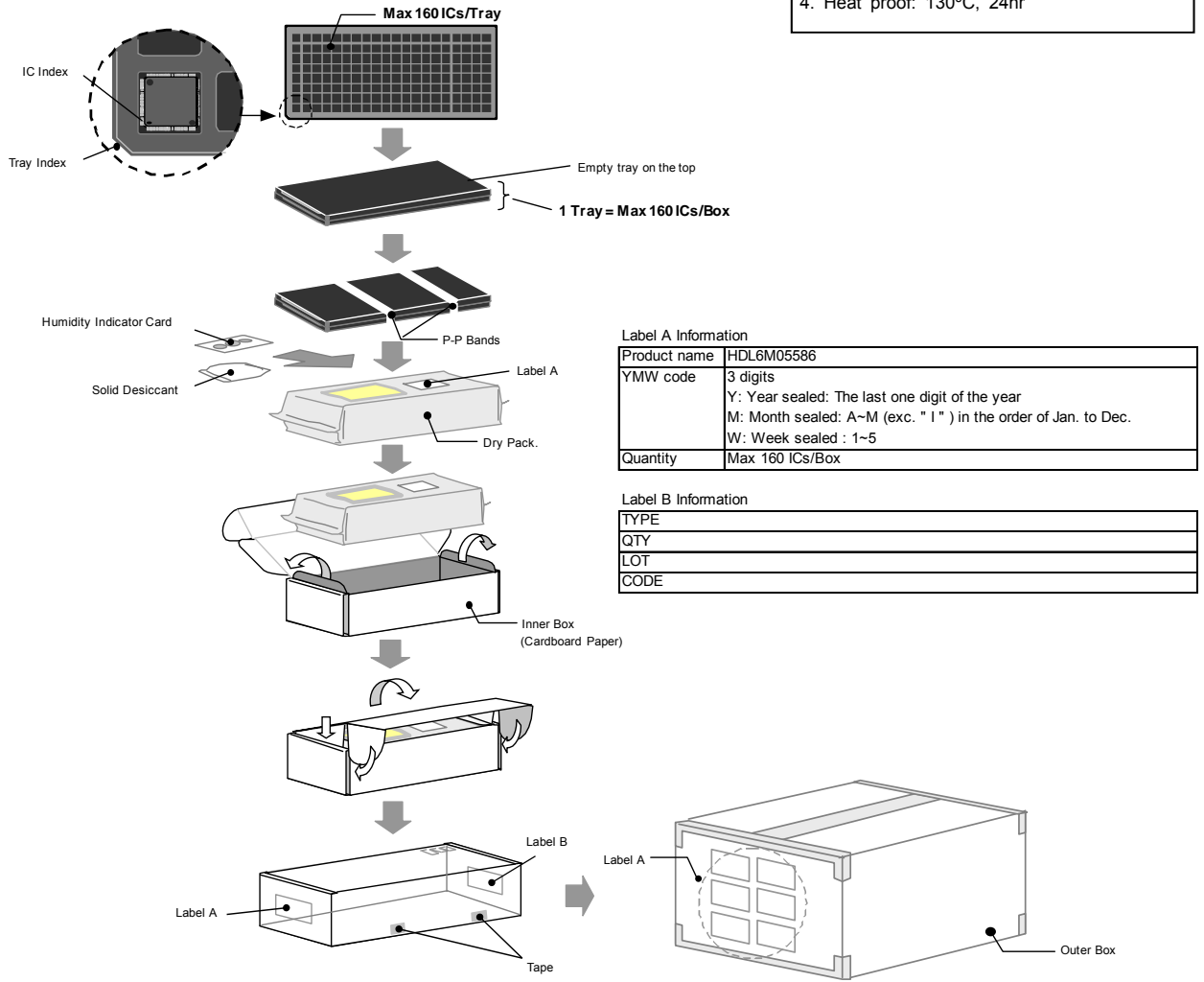


Fig.12 Transport Media, Quantity

## 11. Mounting, Storage

### 11.1 Mounting Pad Design Example

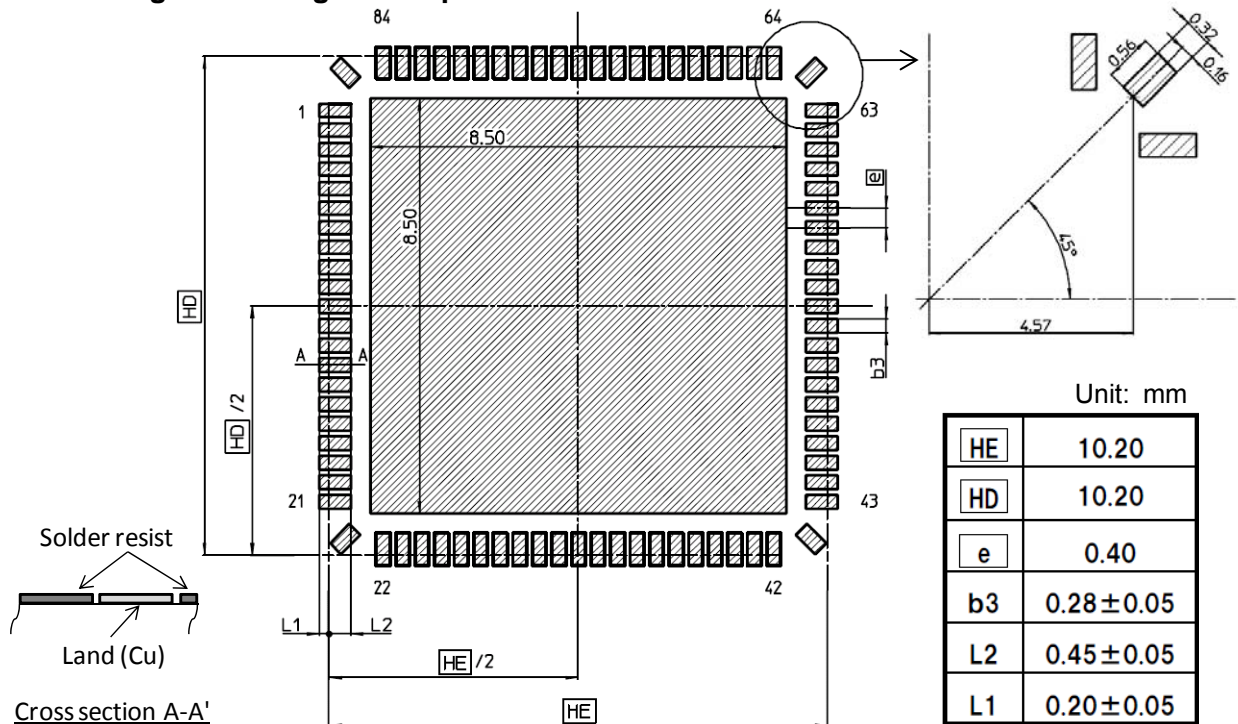


Fig.13 Mounting Pad Design Example

### 11.2 Storage Conditions

11.2.1 The storage location should be kept at 5 to 35 °C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

11.2.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125 °C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

### 11.3 Reflow Conditions

Typical full heating methods such as Infrared (IR), Hot air, and N2 reflow process are applicable. IR/Air reflow heating conditions are shown below.

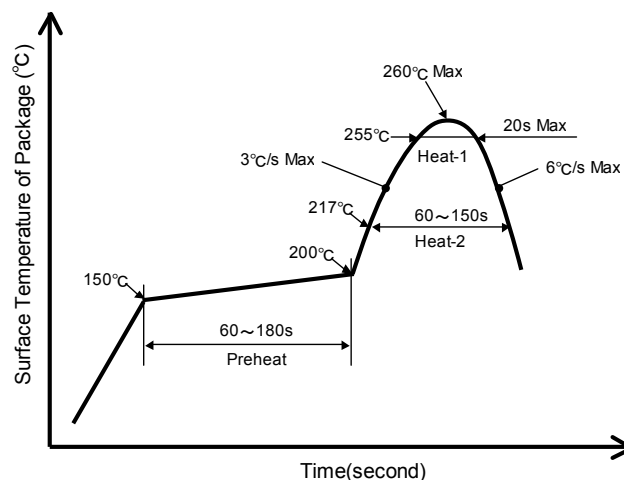


Fig.14 IR/Air Reflow Heating Conditions

## 12. Important Notice

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- 12.2 Should any claim be made within one month of product delivery about products’ failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before of such claim shall not be counted for such response.
- 12.3 ABLIC Inc. assumes no obligation or any way of compensation should any fault about customer products and applications using ABLIC Inc. products be found in marketplace. Only in such a case fault of ABLIC Inc. is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.
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### **13. Cautions**

- 13.1 Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).
  - 13.1.1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.
  - 13.1.2 Those who touch products such as work platform, machine, measurement/test equipment should be grounded.
  - 13.1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.
  - 13.1.4 Prevent friction with other materials made with high polymer.
  - 13.1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.
  - 13.1.6 Avoid dealing with or storing products in an extremely arid environment.
- 13.2 “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.
- 13.3 Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)
- 13.4 Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.
- 13.5 Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

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1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
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ABLIC Inc. is not responsible for damages caused by unauthorized or unspecified use of our products.
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10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
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12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
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