S-8594A/8594B/8595A/8595B Series

www.ablic.com

18 V INPUT, 1 A, SYNCHRONOUS STEP-DOWN SWITCHING REGULATOR

Rev.1.0_00

The S-8594/8595 Series is a step-down switching regulator developed using high withstand voltage CMOS process technologies.
This IC has high maximum operation voltage of 18 V and maintains high-accuracy FB pin voltage at ±1.0%. As suitable packages for high-density mounting, such as small-sized HSNT-8(2030), are adopted, this IC contributes to miniaturization of electronic equipment.
PWM control (S-8594 Series) or PWM / PFM switching control (S-8595 Series) can be selected as an option.
Since the S-8595 Series, which features PWM / PFM switching control, operates with PWM control under heavy load and automatically switches to PFM control under light load, it achieves high-efficiency operation in accordance with the device's status. Furthermore, our distinctive PWM / PFM switching control technology suppresses the ripple voltage to be generated in V_{OUT} while PFM control is in operation.
Since the S-8594/8595 Series has the built-in synchronous circuit, it achieves high efficiency easier compared with conventional step-down switching regulators. In addition, it has the built-in overcurrent protection circuit which protects the IC and coils from excessive load current as well as a thermal shutdown circuit which prevents damage from heat generation.

■ Features

- Input voltage: 4.0 V to 18.0 V
- Output voltage (externally set): 1.0 V to 12.0 V
- Output current: 1 A
- FB pin voltage accuracy: ±1.0%
- Efficiency: 91%
- Oscillation frequency: 2.2 MHz typ.
- Overcurrent protection function: 1.85 A typ. (pulse-by-pulse method)
- Thermal shutdown function: 170°C typ. (detection temperature)
- Short-circuit protection function: Hiccup control, Latch control
- 100% duty cycle operation:
- Soft-start function: 5.8 ms typ.
- Under voltage lockout function (UVLO): 3.35 V typ. (detection voltage)
- Input and output capacitors: Ceramic capacitor compatible
- Operation temperature range: Ta = −40°C to +105°C
- Lead-free (Sn 100%), halogen-free

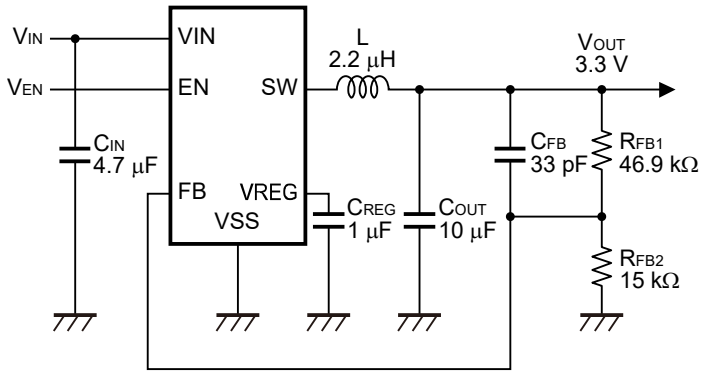
■ Applications

- Constant-voltage power supply for industrial equipment
- Constant-voltage power supply for home electric appliance

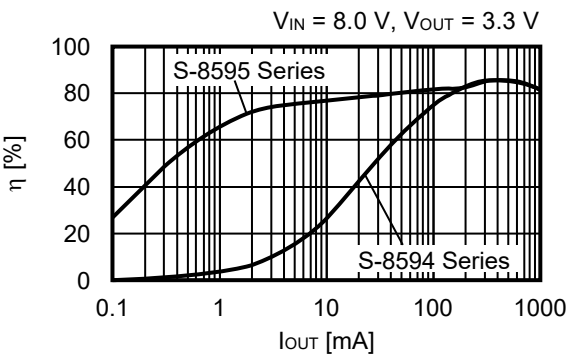
■ Packages

- HTMSOP-8
  (4.0 mm × 2.9 mm × t0.8 mm max.)
- HSNT-8(2030)
  (3.0 mm × 2.0 mm × t0.5 mm max.)

■ Typical Application Circuit

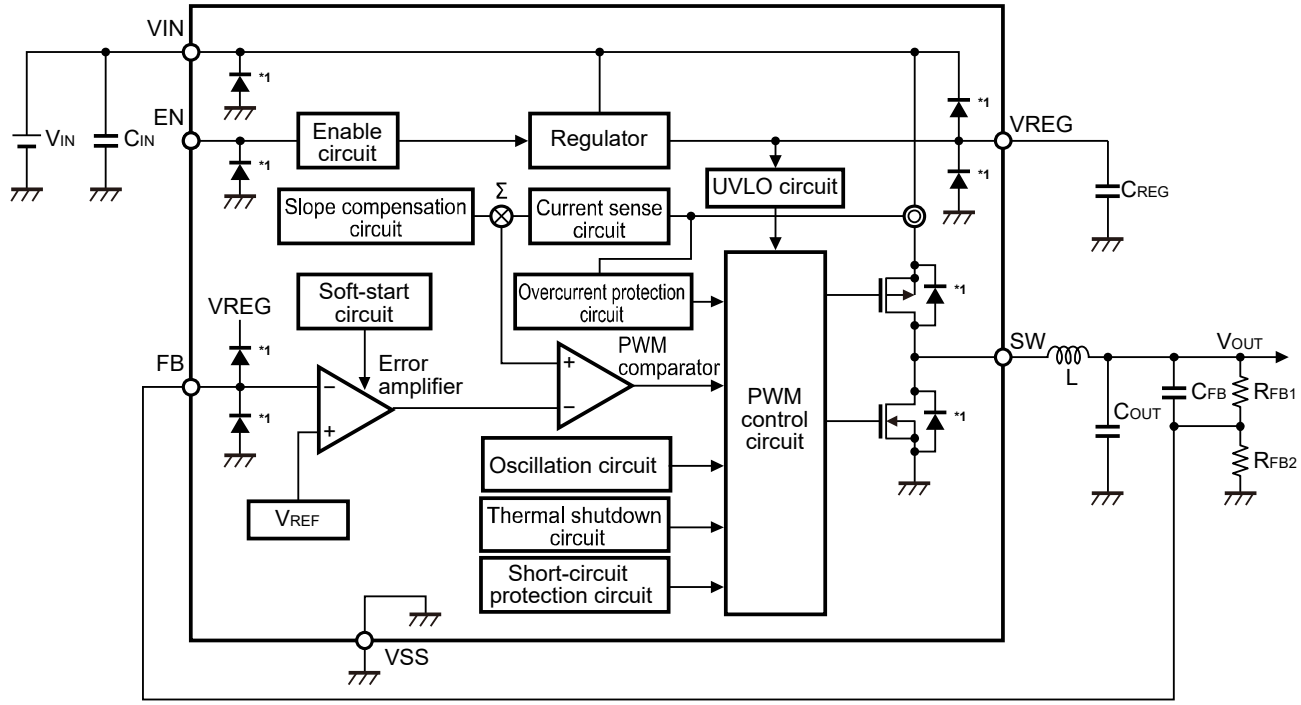


■ Efficiency



■ Block Diagrams

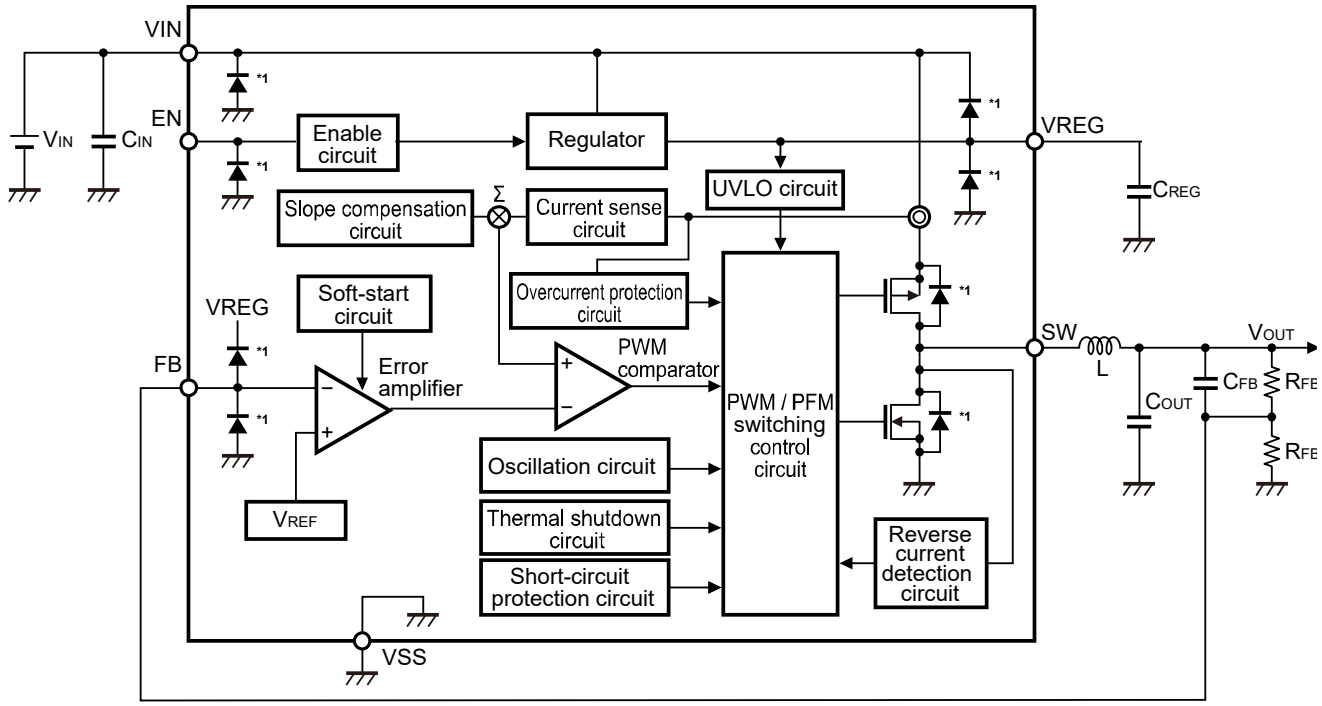
1. S-8594 Series (PWM control)



***1.** Parasitic diode

Figure 1

2. S-8595 Series (PWM / PFM switching control)

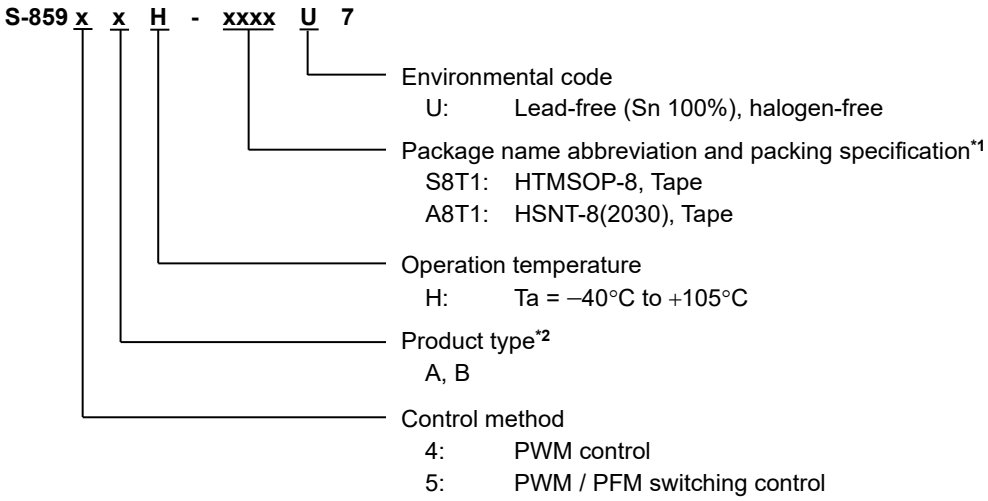


***1.** Parasitic diode

Figure 2

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** Refer to "**2. Function list of product types**".

2. Function list of product types

Table 1

Product Type	Oscillation Frequency	Short-circuit Protection Function
A	2.2 MHz	Hiccup control
B	2.2 MHz	Latch control

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
HTMSOP-8	FP008-A-P-SD	FP008-A-C-SD	FP008-A-R-SD	FP008-A-L-SD
HSNT-8(2030)	PP008-A-P-SD	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD

■ Pin Configurations

1. HTMSOP-8

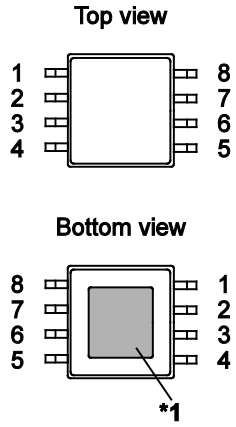


Figure 3

Table 3

Pin No.	Symbol	Description
1	VIN	Power supply pin
2	FB	Feedback pin
3	EN	Enable pin (active "H")
4	NC*2	No connection
5	NC*2	No connection
6	VREG*3	Internal power supply pin
7	VSS	GND pin
8	SW	External inductor connection pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.
***2.** The NC pin is electrically open.
The NC pin can be connected to the VIN pin or the VSS pin.
***3.** The VREG pin cannot supply load current outside.

2. HSNT-8(2030)

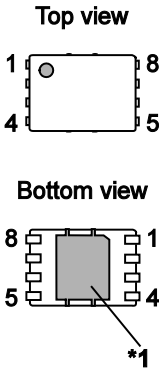


Figure 4

Table 4

Pin No.	Symbol	Description
1	VIN	Power supply pin
2	FB	Feedback pin
3	EN	Enable pin (active "H")
4	NC*2	No connection
5	NC*2	No connection
6	VREG*3	Internal power supply pin
7	VSS	GND pin
8	SW	External inductor connection pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.
***2.** The NC pin is electrically open.
The NC pin can be connected to the VIN pin or the VSS pin.
***3.** The VREG pin cannot supply load current outside.

■ Absolute Maximum Ratings

Table 5

(Unless otherwise specified: Ta = +25°C, V_{SS} = 0 V)

Item	Symbol	Absolute Maximum Ratings	Unit
VIN pin voltage	V_{IN}	V_{SS} − 0.3 to V_{SS} + 22	V
EN pin voltage	V_{EN}	V_{SS} − 0.3 to V_{SS} + 22	V
FB pin voltage	V_{FB}	V_{SS} − 0.3 to V_{REG} + 0.3 ≤ V_{SS} + 6.0	V
VREG pin voltage	V_{REG}	V_{SS} − 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 6.0	V
SW pin voltage	V_{SW}	V_{SS} − 2 to V_{IN} + 2 ≤ V_{SS} + 22 (< 20 ns)	V
		V_{SS} − 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 22	
Junction temperature	T_j	−40 to +125	°C
Operation ambient temperature	T_{opr}	−40 to +105	°C
Storage temperature	T_{stg}	−40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	HTMSOP-8	Board A	–	159	–	°C/W
			Board B	–	113	–	°C/W
			Board C	–	39	–	°C/W
			Board D	–	40	–	°C/W
			Board E	–	30	–	°C/W
		HSNT-8(2030)	Board A	–	181	–	°C/W
			Board B	–	135	–	°C/W
			Board C	–	40	–	°C/W
			Board D	–	42	–	°C/W
			Board E	–	32	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 7

(V_{IN} = 12 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Operating input voltage	V_{IN}	–		4.0	–	18.0	V
Current consumption during shutdown	I_{SSS}	V_{EN} = 0 V		–	0	1	μA
Current consumption during switching off	I_{SS}	V_{FB} = 1.0 V	S-8594 Series	–	175	260	μA
			S-8595 Series	–	68	120	μA
UVLO detection voltage	V_{UVLO-}	VREG pin voltage		3.1	3.35	3.6	V
UVLO release voltage	V_{UVLO+}	VREG pin voltage		3.2	3.45	3.7	V
FB pin voltage	V_{FB}	–		0.792	0.8	0.808	V
Oscillation frequency	f_{OSC}	–		1.98	2.2	2.42	MHz
Minimum ON time	t_{ON_MIN}	–		–	60	–	ns
Maximum duty ratio	MaxDuty	–		100	–	–	%
Soft-start wait time	t_{SSW}	Time until V_{OUT} starts rising, C_{REG} = 1 μF		0.30	0.58	0.90	ms
Soft-start time	t_{SS}	Time until V_{FB} reaches 90% after it starts rising		3.0	5.8	8.5	ms
High side power MOS FET on-resistance	R_{HFET}	I_{SW} = 50 mA		–	0.40	0.92	Ω
Low side power MOS FET on-resistance	R_{LFET}	I_{SW} = –50 mA		–	0.20	0.48	Ω
High side power MOS FET leakage current	I_{HSW}	V_{IN} = 18.0 V, V_{EN} = 0 V, V_{SW} = 0 V		–	0.01	1	μA
Low side power MOS FET leakage current	I_{LSW}	V_{IN} = 18.0 V, V_{EN} = 0 V, V_{SW} = 18.0 V		–	0.01	1	μA
Limit current	I_{LIM}	–		1.6	1.85	2.1	A
Thermal shutdown detection temperature	T_{SD}	Junction temperature		–	170	–	°C
Thermal shutdown release temperature	T_{SR}	Junction temperature		–	150	–	°C
High level input voltage	V_{SH}	EN pin		2.0	–	–	V
Low level input voltage	V_{SL}	EN pin		–	–	0.8	V
High level input current	I_{SH}	EN pin, V_{EN} = 2.0 V		–	–	1	μA
Low level input current	I_{SL}	EN pin, V_{EN} = 0 V		–0.5	–	0.5	μA
FB pin current	I_{FB}	FB pin, V_{FB} = 1.0 V		–0.06	–	0.06	μA

■ Operation

1. Overview of operation

The S-8594/8595 Series adopts the current mode control. The SW pin duty cycle is determined by comparing the error amplifier output signal to a current feedback signal with slope compensation added to the current which flows to the high side power MOS FET. Using the negative feedback loop configured, the error amplifier output signal is maintained at the value that V_{REF} and FB pin voltage (V_{FB}) will be equalized.

2. PWM control (S-8594 Series)

The S-8594 Series operates with the pulse width modulation method (PWM) regardless of the extent of load current and allows the switching frequency to stabilize.

3. PWM / PFM switching control (S-8595 Series)

The S-8595 Series automatically switches between PWM and pulse frequency modulation method (PFM) according to the load current. PFM control is selected when under light load, and the pulse will skip according to the load current. This reduces self-current consumption and improves efficiency when under light load.
In PFM control, the peak current, flows through an inductor, is set to 180 mA typ. in the IC. In addition, our distinctive PWM / PFM switching control technology suppresses the ripple voltage to be generated in V_{OUT} while PFM control is in operation.

4. Minimum ON time

ON time (t_{ON}) of the SW pin during current continuous mode can be calculated by the following expression.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{OSC}}$$

t_{ON} will be small when V_{IN} is high and V_{OUT} is low. Set the use conditions to realize t_{ON} > minimum ON time (t_{ON_MIN}). Although the maximum value of t_{ON_MIN} varies according to inductance, load current, and the conditions of V_{IN} and V_{OUT}, the value is 80 ns. When $t_{ON} < t_{ON\_MIN}$, the ripple voltage (ΔV_{OUT}) in V_{OUT} may increase by skipping a pulse during current continuous mode. In addition, when the S-8594/8595 Series changes to an overload status, the limit current (I_{LIM}) to protect the IC from overcurrent may increase. Sufficient evaluations under actual conditions are required.

5. 100% duty cycle operation

The high side power MOS FET allows for 100% duty cycle operation. Even when the input voltage is lowered up to the output voltage setting value, the high side power MOS FET is kept on and current can be supplied to the load. The output voltage at this time is the input voltage from which the voltage drop due to the direct resistance of the inductor and the on-resistance of the high side power MOS FET are subtracted.

6. Under voltage lockout function (UVLO)

The S-8594/8595 Series has a built-in UVLO circuit to prevent the IC from malfunctioning due to a transient status at power-on or a momentary drop in the supply voltage. When UVLO status is detected, the high side power MOS FET and low side power MOS FET will turn off, and the SW pin will change to "High-Z". For this reason, switching operation will stop. The soft-start function is reset if UVLO status is detected once and is restarted by releasing the UVLO status. Note that the other internal circuits operate normally, and the status is different from the disabled status.
Also, there is a hysteresis width for avoiding malfunctions due to generation of noise etc. in the input voltage.

7. EN pin

This pin starts and stops switching operation. When the EN pin is set to "L", the operation of all internal circuits, including the high side power MOS FET, is stopped, reducing current consumption. When not using the EN pin, connect it to the VIN pin. Since the EN pin is neither pulled down nor pulled up internally, do not use it in the floating status. The structure of the EN pin is shown in **Figure 5**, and the clamp circuit is internally connected. Refer to "**3. 1 High level input current (I_{SH}) vs. EN pin voltage (V_{EN})**" in "**■ Characteristics (Typical Data)**" for the input current of EN pin.

Table 8

EN Pin	Internal Circuit	V_{OUT}
"H"	Enable (normal operation)	Constant value*1
"L"	Disable (standby)	Pulled down to V_{SS}*2

***1.** The constant value is output due to the regulating based on the output voltage setting resistors (R_{FB1} and R_{FB2}).

***2.** V_{OUT} is pulled down to V_{SS} due to the output voltage setting resistors (R_{FB1} and R_{FB2}) and a load.

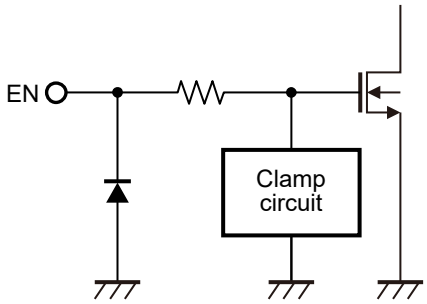


Figure 5

8. Thermal shutdown function

The S-8594/8595 Series has a built-in thermal shutdown circuit to limit overheating. When the junction temperature increases to 170°C typ., the thermal shutdown circuit becomes the detection status, and the switching operation is stopped. When the junction temperature decreases to 150°C typ., the thermal shutdown circuit becomes the release status, and the switching operation is restarted.

If the thermal shutdown circuit becomes the detection status due to self-heating, the switching operation is stopped and output voltage (V_{OUT}) decreases. For this reason, the self-heating is limited and the temperature of the IC decreases. The thermal shutdown circuit becomes release status when the temperature of the IC decreases, and the switching operation is restarted, thus the self-heating is generated again. Repeating this procedure makes the waveform of V_{OUT} into a pulse-like form. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously. Switching operation stopping and starting can be stopped by either setting the EN pin to "L", lowering the output current (I_{OUT}) to reduce internal power consumption, or decreasing the ambient temperature.

Table 9

Thermal Shutdown Circuit	V_{OUT}
Release: 150°C typ.*1	Constant value*2
Detection: 170°C typ.*1	Pulled down to V_{SS}*3

***1.** Junction temperature

***2.** The constant value is output due to the regulating based on the output voltage setting resistors (R_{FB1} and R_{FB2}).

***3.** V_{OUT} is pulled down to V_{SS} due to the output voltage setting resistors (R_{FB1} and R_{FB2}) and a load.

9. Overcurrent protection function

The overcurrent protection circuit monitors the current that flows through the high side power MOS FET and limits current to prevent thermal destruction of the IC due to an overload, magnetic saturation in the inductor, etc.
When a current exceeding the limit current (I_{LIM}) flows through the high side power MOS FET, the high side power MOS FET is turned off. When the next switching cycle starts, the high side power MOS FET is turned on. If the current value continues to remain at I_{LIM} or higher, the high side power MOS FET is turned off again, repeating this series of operation.
Meanwhile, when the current, which flows through the high side power MOS FET, falls to I_{LIM} or lower, the S-8594/8595 Series will return to the normal operation.
When the slope of inductor current is large, I_{LIM} may appear to increase due to the delay time of overcurrent protection circuit. This phenomenon tends to occur when low-inductance inductor is used or when the voltage different between V_{IN} and V_{OUT} is large.

10. Frequency foldback function

The frequency foldback function has FB pin voltage (V_{FB}) and oscillation frequency (f_{OSC}) to have a proportional relation when V_{FB} is 0.7 V typ. or lower. Refer to "**11. Short-circuit protection function**" for details.
The frequency foldback function in the S-8594 Series is set to invalid at start-up.

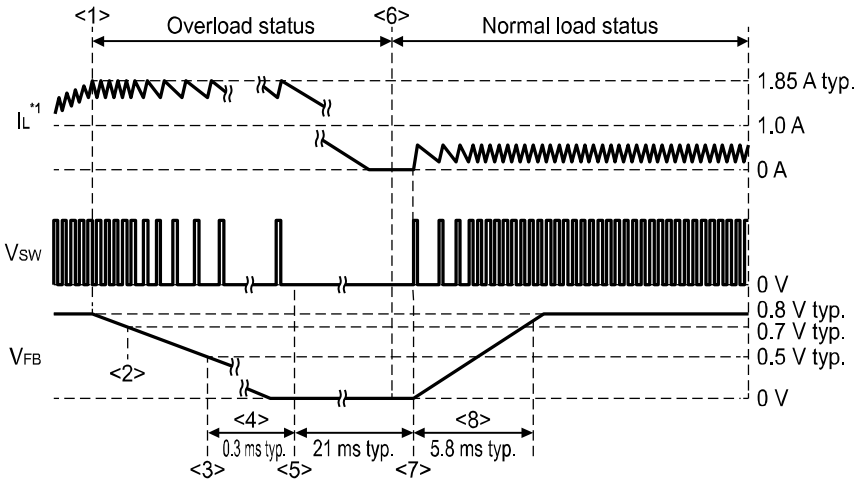
11. Short-circuit protection function

11. 1 Hiccup control

The S-8594/8595 Series A type has a built-in short-circuit protection function for Hiccup control.
Hiccup control is a method for periodically carrying out automatic recovery when the IC detects overcurrent and stops the switching operation.

11. 1. 1 When overload status is released

<1> Overcurrent detection
<2> After detection of the FB pin voltage (V_{FB}) < 0.7 V typ., frequency foldback function becomes valid.
<3> Detection of V_{FB} < 0.5 V typ.
<4> 0.3 ms elapse
<5> Switching operation stop (for 21 ms typ.)
<6> Overload status release
<7> The IC restarts, soft-start function starts.
In this case, it is unnecessary to input an external reset signal for restart.
<8> V_{FB} reaches 0.72 V typ. after 5.8 ms typ. elapses.

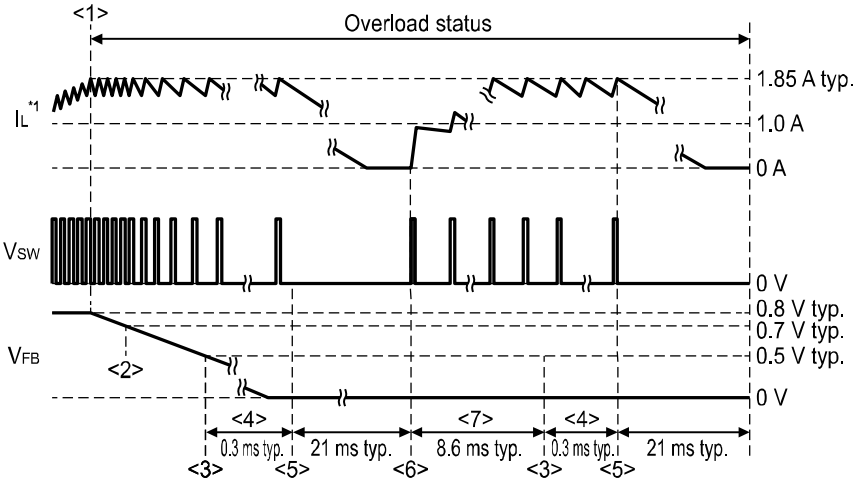


***1.** Inductor current

Figure 6

11. 1. 2 When overload status continues

<1> Overcurrent detection
<2> After detection of V_{FB} < 0.7 V typ., frequency foldback function becomes valid.
<3> Detection of V_{FB} < 0.5 V typ.
<4> 0.3 ms elapse
<5> Switching operation stop (for 21 ms typ.)
<6> The IC restarts, soft-start function starts.
<7> The status returns to <3> when overload status continues after 8.6 ms typ. elapses.



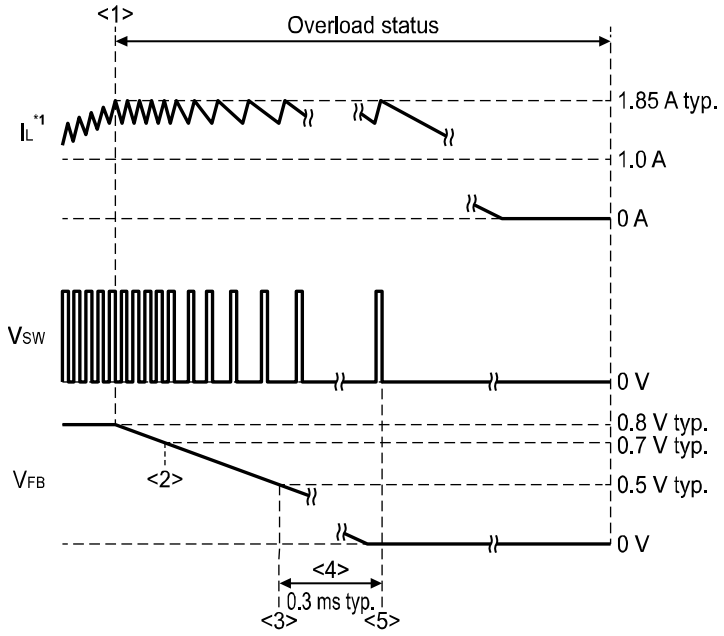
***1.** Inductor current

Figure 7

11. 2 Latch control

The S-8594/8595 Series B type has a built-in short-circuit protection function for Latch control.
Latch control is a method for maintaining the Latch status when the IC detects overcurrent and stops the switching operation.

<1> Overcurrent detection
<2> After detection of V_{FB} < 0.7 V typ., frequency foldback function becomes valid.
<3> Detection of V_{FB} < 0.5 V typ.
<4> 0.3 ms elapse
<5> Switching operation stop



***1.** Inductor current

Figure 8

In addition, Latch status is reset under the following conditions.

- At UVLO detection
- When the EN pin changes from "H" to "L".

12. Pre-bias compatible soft-start function

The S-8594/8595 Series has a built-in pre-bias compatible soft-start circuit.
If the pre-bias compatible soft-start circuit starts when electrical charge remains in the output voltage (V_{OUT}) as a result of power supply restart, etc., or when V_{OUT} is biased beforehand (pre-bias status), switching operation is stopped until the soft-start voltage exceeds the FB pin voltage (V_{FB}), and then V_{OUT} is maintained. If the soft-start voltage exceeds V_{FB}, switching operation will restart and V_{OUT} will rise to the output voltage setting value ($V_{OUT(S)}$). This allows $V_{OUT(S)}$ to be reached without lowering the pre-biased V_{OUT}.
In soft-start circuits which are not pre-bias compatible, a large current flows as a result of the discharge of the residual electric charge through the low side power MOS FET when switching operation starts, which could cause damage, however in a pre-bias compatible soft-start circuit, the IC is protected from the large current when switching operation starts, and it makes power supply design for the application circuit simpler.

In the S-8594/8595 Series, V_{OUT} reaches $V_{OUT(S)}$ gradually due to the soft-start circuit.
In the following cases, rush current and V_{OUT} overshoot are reduced.

- When the EN pin changes from "L" to "H".
- When UVLO operation is released.*1
- When thermal shutdown is released.*1
- At short-circuit recovery*1

***1.** In this case, the soft-start wait time is eliminated.

The soft-start circuit starts operating after "H" is input to the EN pin and the soft-start wait time (t_{SSW}) = 0.58 ms typ. elapses. The soft-start time (t_{SS}) is set to 5.8 ms typ.

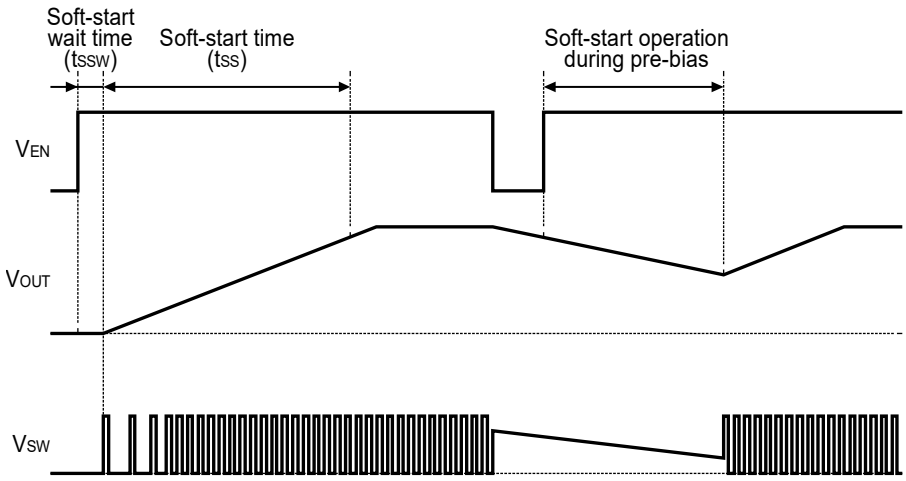


Figure 9

13. Internal power supply (V_{REG})

Some of the circuits in the IC operate using the VREG pin voltage (V_{REG}) as the power supply. To stabilize this internal power supply, a ceramic capacitor with 1 μF needs to be connected between the VREG pin and the VSS pin. To achieve low impedance, this capacitor should be placed as close to the IC as possible. Additionally, note that any external parts other than C_{REG} or any load must not connect to the VREG pin.

■ Typical Circuit

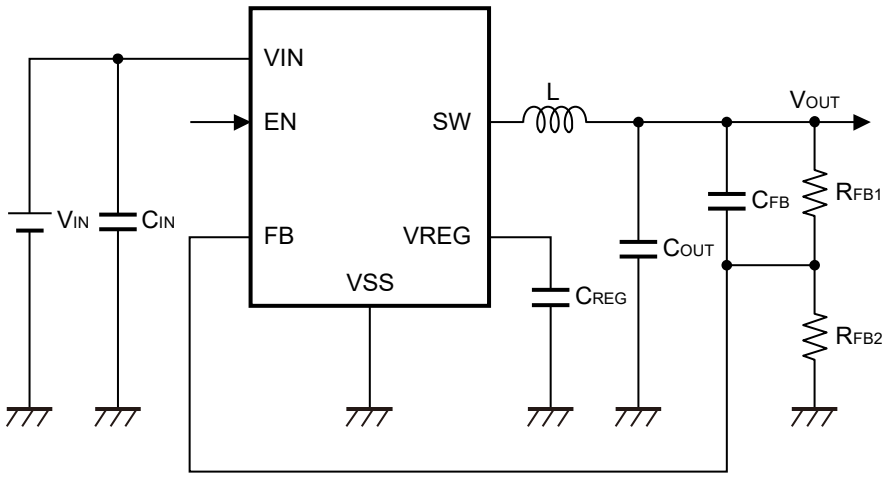


Figure 10

Caution The above connection diagram will not guarantee successful operation. Perform thorough evaluation using an actual application to set the constants.

■ External Parts Selection

The recommended values for each external part are shown in **Table 10**, and the recommended parts are shown in **Table 11** to **Table 15**. When selecting an input capacitor (C_{IN}), output capacitor (C_{OUT}), and internal power supply stabilized capacitor (C_{REG}), take into consideration the temperature range and DC bias characteristics of the capacitor to be used.

Table 10

V_{OUT}	C_{IN}	C_{OUT}	C_{FB}	C_{REG}	L	R_{FB1}	R_{FB2}
1.0 V	4.7 μF	10 μF	33 pF	1 μF	2.2 μH	3.75 kΩ	15 kΩ
2.5 V	4.7 μF	10 μF	33 pF	1 μF	2.2, 3.3 μH	31.9 kΩ	15 kΩ
3.3 V	4.7 μF	10 μF	33 pF	1 μF	2.2, 3.3 μH	46.9 kΩ	15 kΩ
5.0 V	4.7 μF	10 μF	33 pF	1 μF	3.3, 4.7 μH	84 kΩ	16 kΩ
12.0 V	4.7 μF	10 μF	33 pF	1 μF	4.7, 6.8 μH	210 kΩ	15 kΩ

Table 11 Recommended Capacitors (C_{IN}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	C2012X7R1E475K125AB	4.7 μF	25 V	2.0 mm × 1.25 mm × 1.25 mm
TDK Corporation	C2012X7R1H475K125AC	4.7 μF	50 V	2.0 mm × 1.25 mm × 1.25 mm
TDK Corporation	CGA5L3X7R1H475K160AB	4.7 μF	50 V	3.2 mm × 1.6 mm × 1.6 mm
Murata Manufacturing Co., Ltd.	GCM31CR71E475KA55	4.7 μF	25 V	3.2 mm × 1.6 mm × 1.6 mm

Table 12 Recommended Capacitors (C_{OUT}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	CGA4J3X7S1A106K125AB	10 μF	10 V	2.0 mm × 1.25 mm × 1.25 mm
TDK Corporation	CGA5L1X7R1C106K160AC	10 μF	16 V	3.2 mm × 1.6 mm × 1.6 mm
TDK Corporation	C2012X7S1E106K125AC	10 μF	25 V	2.0 mm × 1.25 mm × 1.25 mm
Murata Manufacturing Co., Ltd.	GCM188D70J106ME36	10 μF	6.3 V	1.6 mm × 0.8 mm × 0.8 mm

Table 13 Recommended Capacitor (C_{FB}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	CGA1A2C0G1H330J030BA	33 pF	50 V	0.6 mm × 0.3 mm × 0.3 mm

Table 14 Recommended Capacitors (C_{REG}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	C1608X7R1C105K080AC	1 μF	16 V	1.6 mm × 0.8 mm × 0.8 mm
Murata Manufacturing Co., Ltd.	GRM155C71A105KE11	1 μF	10 V	1.0 mm × 0.5 mm × 0.5 mm

Table 15 Recommended Inductors (L) List

Manufacturer	Part Number	Inductance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	TFM252012ALMA2R2MTAA	2.2 μH	20 V	2.5 mm × 2.0 mm × 1.2 mm
TDK Corporation	CLF5030NIT-2R2N-D	2.2 μH	–	5.0 mm × 5.3 mm × 2.7 mm
TDK Corporation	TFM322512ALMA3R3MTAA	3.3 μH	20 V	3.2 mm × 2.5 mm × 1.2 mm
TDK Corporation	CLF5030NIT-3R3N-D	3.3 μH	–	5.0 mm × 5.3 mm × 2.7 mm
TDK Corporation	CLF5030NIT-4R7N-D	4.7 μH	–	5.0 mm × 5.3 mm × 2.7 mm
TDK Corporation	CLF6045NIT-6R8N-D	6.8 μH	–	6.3 mm × 6.0 mm × 4.5 mm
Würth Elektronik GmbH & Co. KG	74438356022HT	2.2 μH	–	4.1 mm × 4.1 mm × 2.1 mm
Würth Elektronik GmbH & Co. KG	74438356033HT	3.3 μH	–	4.1 mm × 4.1 mm × 2.1 mm
Würth Elektronik GmbH & Co. KG	74438356047HT	4.7 μH	–	4.1 mm × 4.1 mm × 2.1 mm
TAIYO YUDEN CO.,LTD.	EST0645T4R7NDGA	4.7 μH	–	6.3 mm × 6.0 mm × 4.8 mm
TAIYO YUDEN CO.,LTD.	EST0645T6R8NDGA	6.8 μH	–	6.3 mm × 6.0 mm × 4.8 mm
MinebeaMitsumi Inc.	C5-K3LGA*1	4.7 μH	–	5.6 mm × 5.6 mm × 3.0 mm
MinebeaMitsumi Inc.	C5-K3LGA*1	6.8 μH	–	5.6 mm × 5.6 mm × 3.0 mm

***1.** 150°C compatible

1. Input capacitor (C_{IN})

C_{IN}, which has an effect to suppress the ripple voltage and switching noise to be generated in the power supply line, is used for the stable operation of IC. A ceramic capacitor with 4.7 μF or higher is recommended.

2. Output capacitor (C_{OUT})

C_{OUT} is used to smooth output voltage. The ripple voltage (ΔV_{OUT}) to be generated in V_{OUT} is inversely proportional to C_{OUT}. When selecting a capacitor whose ESR is sufficiently small, ΔV_{OUT} during current continuous mode is calculated by the following expression.

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times f_{OSC} \times C_{OUT}}$$

In addition, since C_{OUT} contributes to the stability of feedback loop, a ceramic capacitor with 10 μF or higher is recommended. When selecting a capacitor whose capacitance is extremely large, the overcurrent protection function may start the operation and cause a start-up failure. Therefore, select a capacitor with 200 μF or lower.

3. Inductor (L)

To suppress the intrinsic subharmonic oscillation in current mode control, the optimal L value needs to be selected. Considering the slope compensation in the IC, select an inductor from the range of 2.2 μH to 6.8 μH depending on V_{OUT}.

When selecting L, note the allowable current. If a current exceeding the allowable current flows through the inductor, magnetic saturation may occur, and there may be risks which substantially lower efficiency and damage the IC as a result of large current.
The ripple current (ΔI_L) and peak current (I_{PK}) flow through the inductor during current continuous mode are calculated by the following expressions respectively. Make sure I_{PK} will not exceed the allowable current of inductor.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{OSC} \times L \times V_{IN}}$$

$$I_{PK} = I_{OUT} + \frac{\Delta I_L}{2}$$

In order to maintain the allowable current of inductor even in cases V_{OUT} shorts to V_{SS} or other fault conditions occur, an inductor with 2.1 A or higher, the maximum value of I_{LIM}, needs to be selected.

4. Internal power supply stabilized capacitor (C_{REG})

C_{REG} is used to stabilize the operation of IC's internal power supply (V_{REG} = 4.5 V typ.) A ceramic capacitor with 1 μF is recommended.

5. Output voltage setting resistors (R_{FB1}, R_{FB2}), capacitor for phase compensation (C_{FB})

V_{OUT} can be set to any value using R_{FB1} and R_{FB2}. V_{OUT} can be calculated by the following expression substituting V_{FB} = 0.8 V typ. Note that if the R_{FB1} and R_{FB2} values are increased, the FB pin will more likely to be affected by noise. A resistor with approximately 15 kΩ is recommended for R_{FB2}.

$$V_{OUT} = \frac{(R_{FB1} + R_{FB2})}{R_{FB2}} \times 0.8$$

C_{FB} connected in parallel with R_{FB1} is a capacitor for phase compensation. Using R_{FB1} and C_{FB} to set the zero point (the phase feedback) allows the feedback loop to gain larger phase margin.
When selecting C_{FB}, refer to the following expressions. In addition, perform thorough evaluations with the actual applications to set the constants.

First, calculate the zero point frequency (f_Z) by the following expression.

$$f_Z = 3.94 \times \frac{1}{C_{OUT}} \times \frac{V_{FB}}{V_{OUT}}$$

Next, substitute R_{FB1} and f_Z gained by the above expression into the below expression to calculate C_{FB} value.

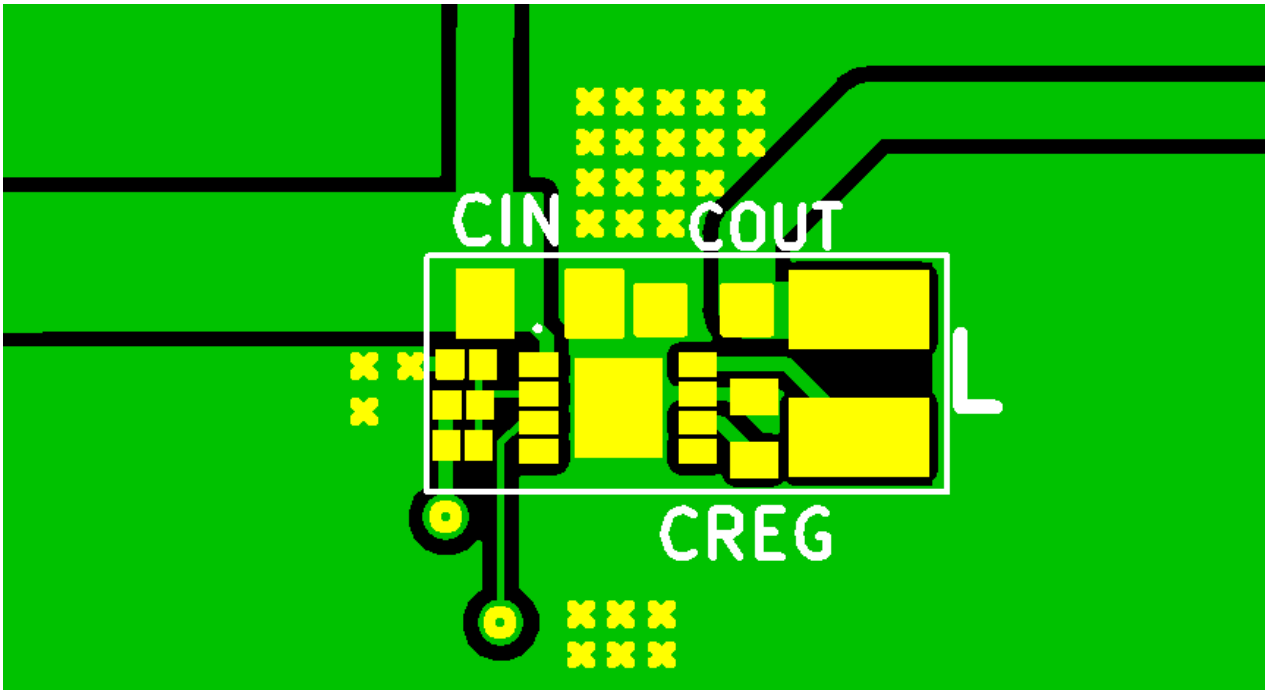
$$C_{FB} = \frac{1}{2 \times \pi \times R_{FB1} \times f_Z}$$

Caution Generally a switching regulator may cause oscillation depending on the selection of external parts. Perform thorough evaluations including the temperature characteristics with actual applications to confirm no oscillation occurs.

■ Board Layout Guidelines

Note the following cautions when determining the board layout for the S-8594/8595 Series.

- Place C_{IN} as close to the VIN pin and the VSS pin as possible. Prioritize the layout of C_{IN}.
- Place C_{REG} as close to the VREG pin and the VSS pin as possible.
- Mount C_{IN} and C_{REG} on the same surface layer as the IC. If they are connected through thermal vias, the impedance of the thermal vias may influence the operation, resulting in unstable condition.
- Make the wiring of the FB pin as short as possible. The parasitic capacitance of FB pin may affect the phase margin of feedback loop.
- Do not place the FB pin close to noise sources such as the wiring of SW pin to avoid unstable operations.
- Make the GND pattern as wide as possible.
- Place thermal vias in the GND pattern to ensure sufficient heat dissipation.
- Large current flows through the SW pin. Make the wiring area of the pattern to be connected to the SW pin small to minimize parasitic capacitance and emission noise.
- Make a short loop wiring of the SW pin → L → C_{OUT} → VSS pin. This is effective to reduce emission noise.
- Do not wire the SW pin pattern under the IC.



Total size 9.0 mm × 4.1 mm = 36.9 mm^2

Figure 11 Reference Board Pattern

Caution The above pattern diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to determine the pattern.

■ Precautions

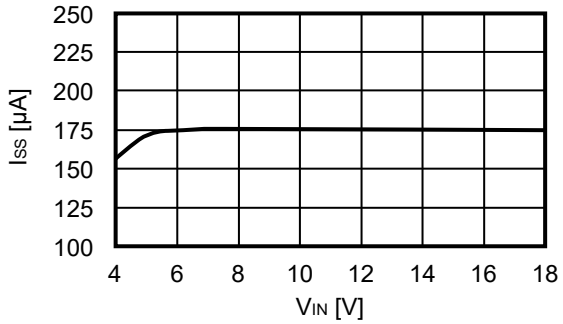
- Mount external capacitors and inductors as close as possible to the IC, and make single GND.
- Characteristic ripple voltage and spike noise occur in the IC containing switching regulators. Moreover rush current flows at the time of a power supply injection. Because these largely depend on the inductor, the capacitor and impedance of power supply to be used, fully check them using an actually mounted model.
- The 4.7 μF capacitor connected between the VIN pin and the VSS pin is a bypass capacitor. It stabilizes the power supply in the IC, and thus effectively works for stable switching regulator operation. Allocate the bypass capacitor as close to the IC as possible, prioritized over other parts.
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- The power dissipation of the IC greatly varies depending on the size and material of the board to be connected. Perform sufficient evaluation using an actual application before designing.
- ABLIC Inc. assumes no responsibility for the way in which this IC is used on products created using this IC or for the specifications of that product, nor does ABLIC Inc. assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Japan or in other countries.

■ Characteristics (Typical Data)

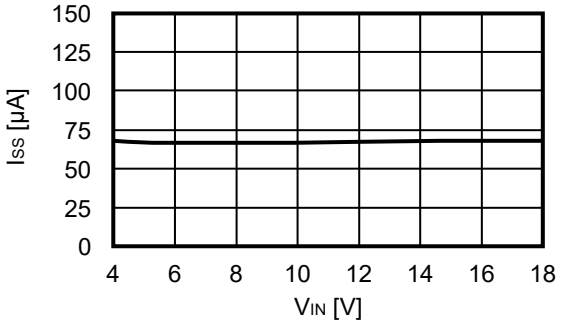
1. Example of major power supply dependence characteristics (Ta = +25°C)

1. 1 Current consumption during switching off (I_{SS}) vs. Input voltage (V_{IN})

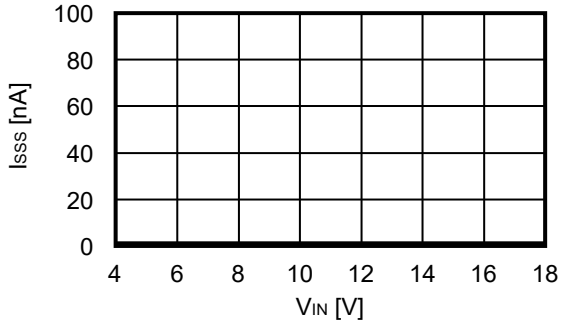
1. 1. 1 S-8594 Series



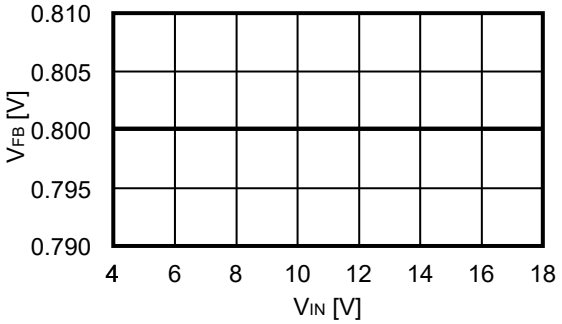
1. 1. 2 S-8595 Series



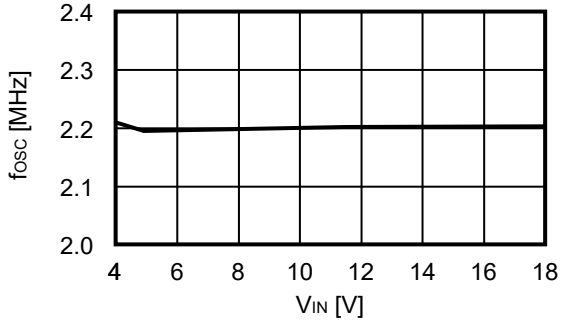
1. 2 Current consumption during shutdown (I_{SSS}) vs. Input voltage (V_{IN})



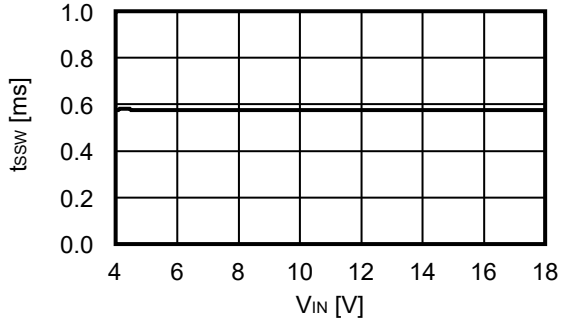
1. 3 FB pin voltage (V_{FB}) vs. Input voltage (V_{IN})



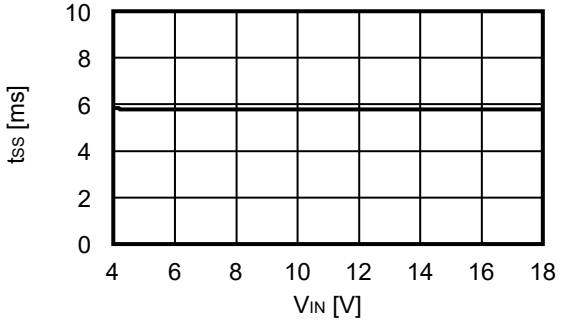
1. 4 Oscillation frequency (f_{OSC}) vs. Input voltage (V_{IN})



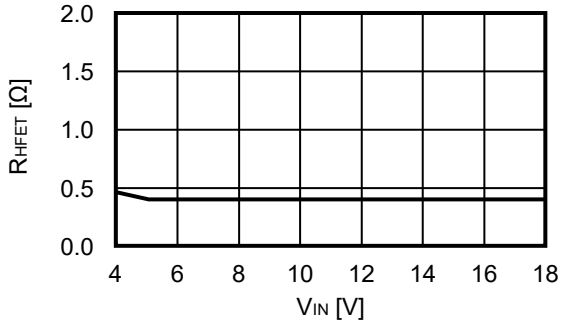
1. 5 Soft-start wait time (t_{SSW}) vs. Input voltage (V_{IN})



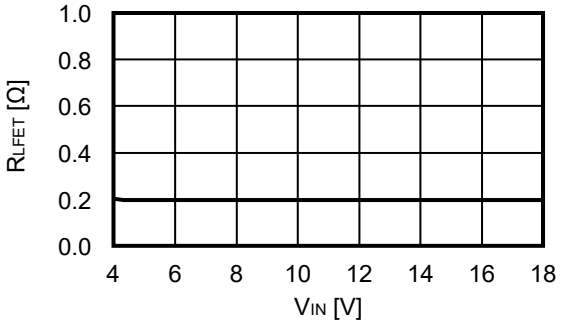
1. 6 Soft-start time (t_{SS}) vs. Input voltage (V_{IN})



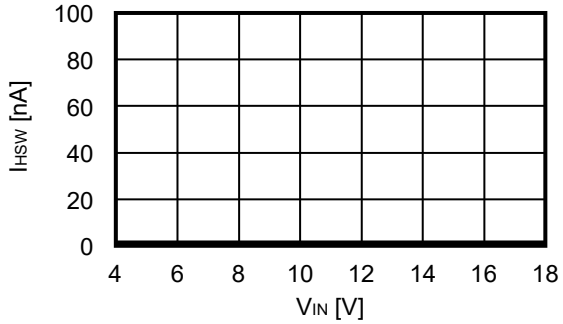
1. 7 High side power MOS FET on-resistance (R_{HFET}) vs. Input voltage (V_{IN})



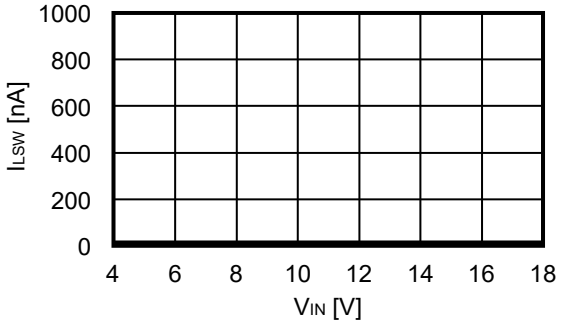
1. 8 Low side power MOS FET on-resistance (R_{LFET}) vs. Input voltage (V_{IN})



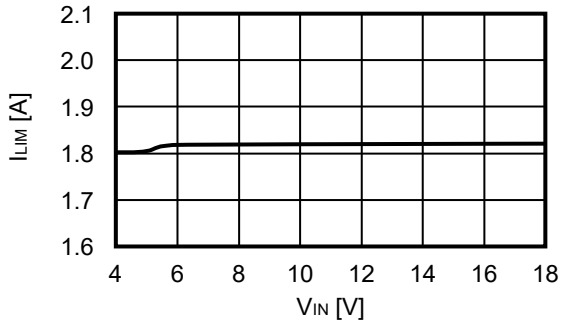
1. 9 High side power MOS FET leakage current (I_{HSW}) vs. Input voltage (V_{IN})



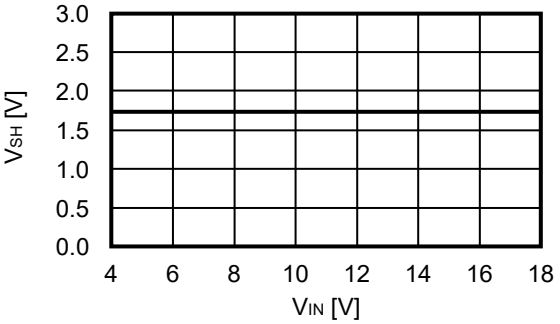
1. 10 Low side power MOS FET leakage current (I_{LSW}) vs. Input voltage (V_{IN})



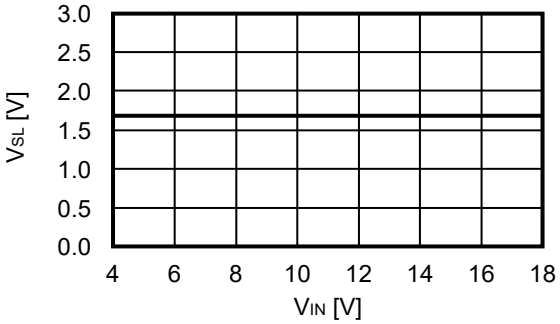
1. 11 Limit current (I_{LIM}) vs. Input voltage (V_{IN})



1. 12 High level input voltage (V_{SH}) vs. Input voltage (V_{IN})



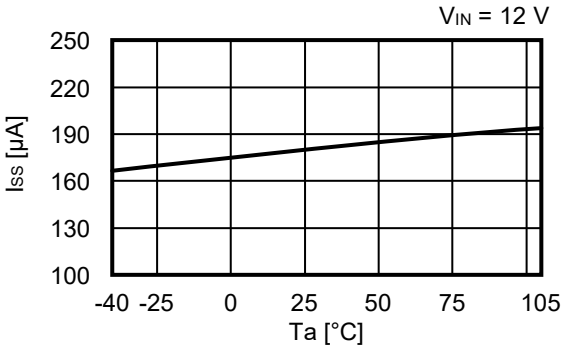
1. 13 Low level input voltage (V_{SL}) vs. Input voltage (V_{IN})



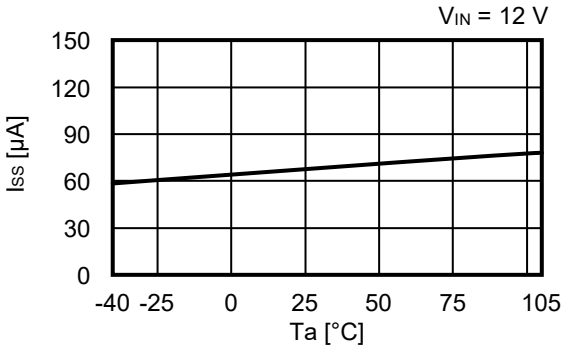
2. Example of major temperature characteristics (Ta = –40°C to +105°C)

2. 1 Current consumption during switching off (I_{SS}) vs. Temperature (Ta)

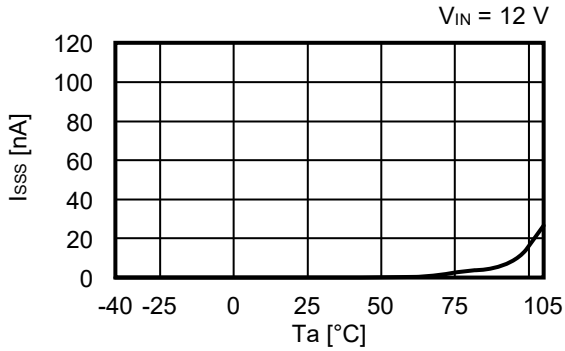
2. 1. 1 S-8594 Series



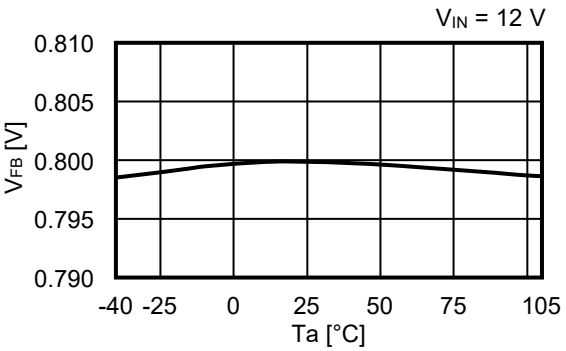
2. 1. 2 S-8595 Series



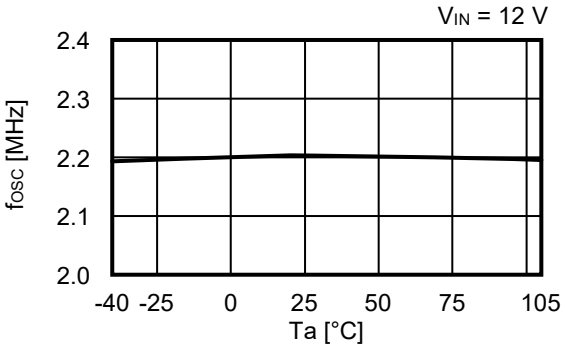
2. 2 Current consumption during shutdown (I_{SSS}) vs. Temperature (Ta)



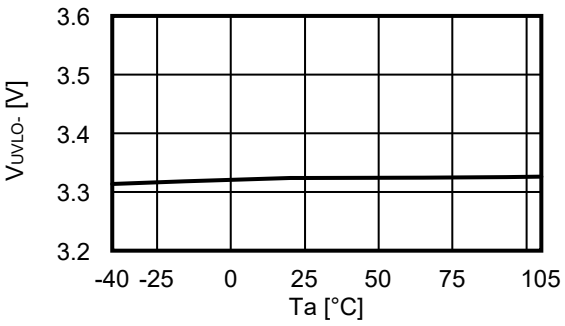
2. 3 FB pin voltage (V_{FB}) vs. Temperature (Ta)



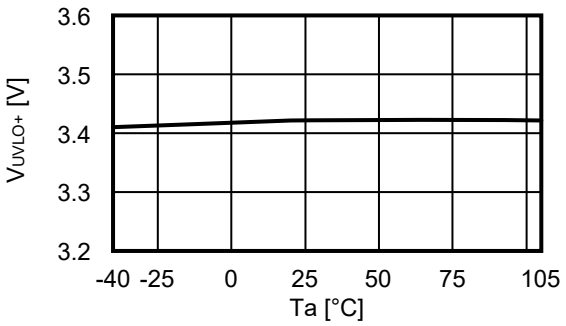
2. 4 Oscillation frequency (f_{OSC}) vs. Temperature (Ta)



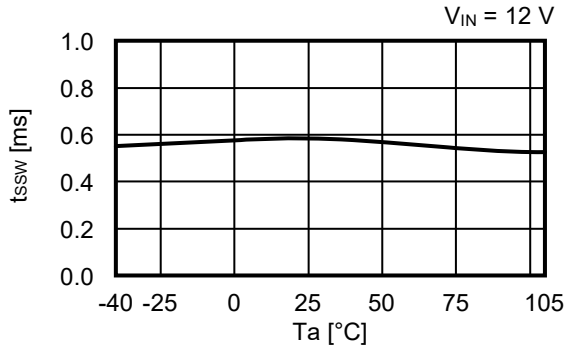
2. 5 UVLO detection voltage (V_{UVLO-}) vs. Temperature (Ta)



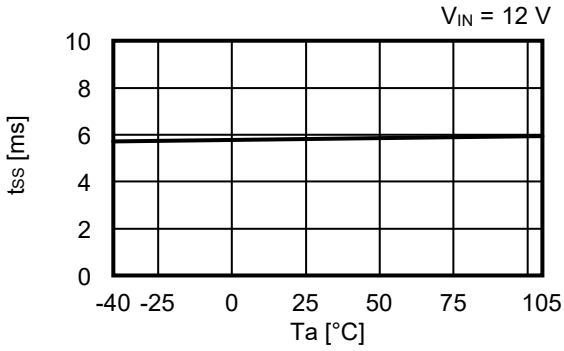
2. 6 UVLO release voltage (V_{UVLO+}) vs. Temperature (Ta)



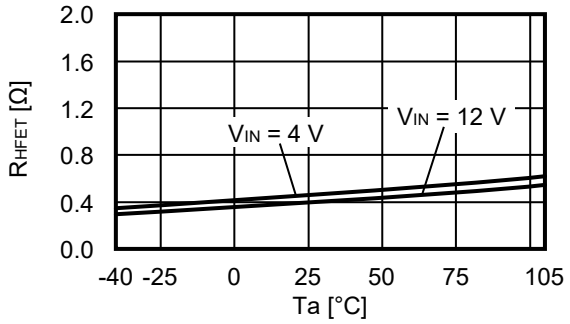
2. 7 Soft-start wait time (t_{SSW}) vs. Temperature (Ta)



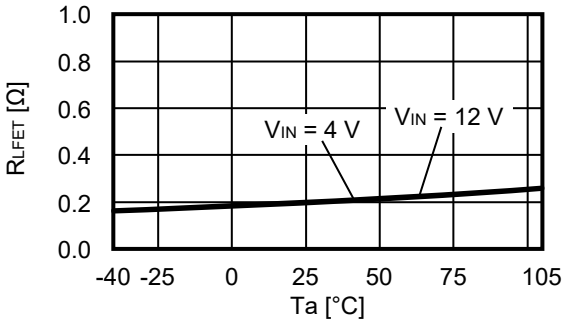
2. 8 Soft-start time (t_{SS}) vs. Temperature (Ta)



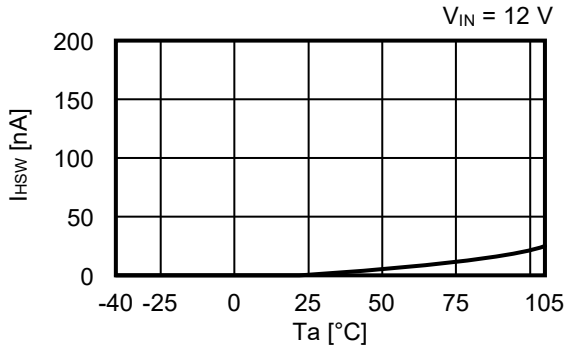
2. 9 High side power MOS FET on-resistance (R_{HFET}) vs. Temperature (Ta)



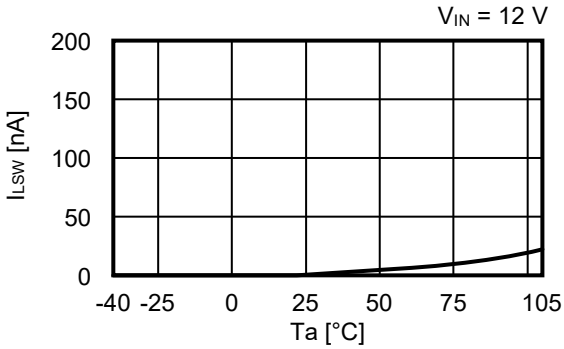
2. 10 Low side power MOS FET on-resistance (R_{LFET}) vs. Temperature (Ta)



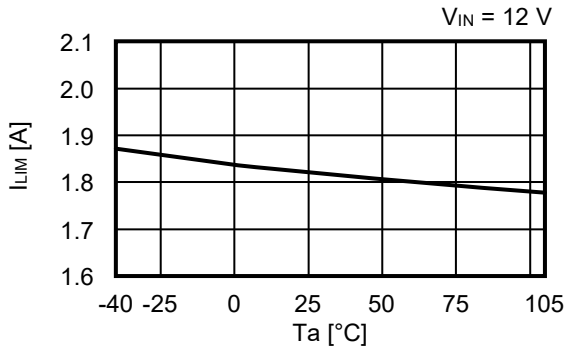
2. 11 High side power MOS FET leakage current (I_{HSW}) vs. Temperature (Ta)



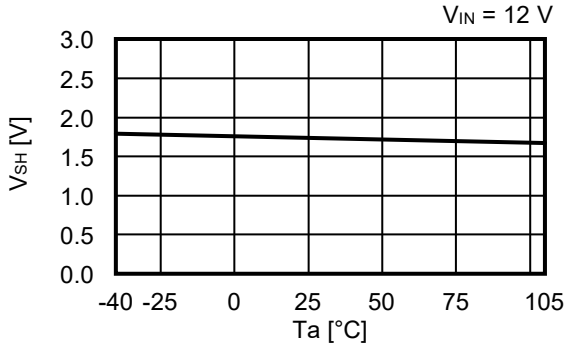
2. 12 Low side power MOS FET leakage current (I_{LSW}) vs. Temperature (Ta)



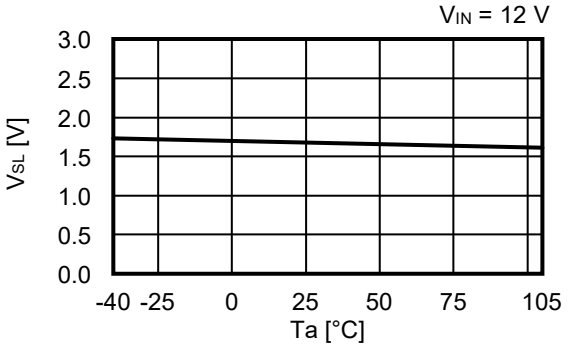
2. 13 Limit current (I_{LIM}) vs. Temperature (Ta)



2. 14 High level input voltage (V_{SH}) vs. Temperature (Ta)

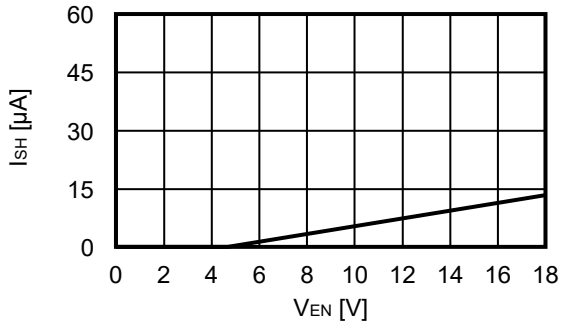


2. 15 Low level input voltage (V_{SL}) vs. Temperature (Ta)



3. EN pin characteristics (Ta = +25°C)

3. 1 High level input current (I_{SH}) vs. EN pin voltage (V_{EN})



4. Transient response characteristics

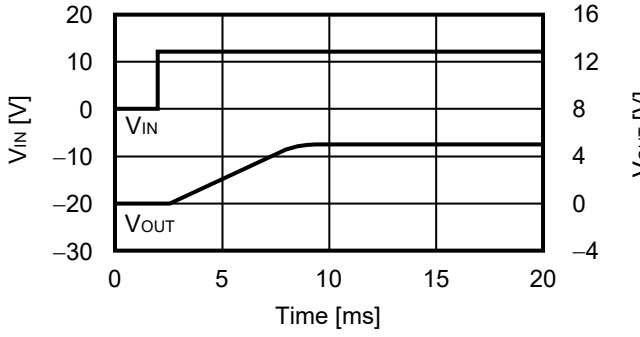
The external parts shown in **Table 16** are used in "**4. Transient response characteristics**".

Table 16

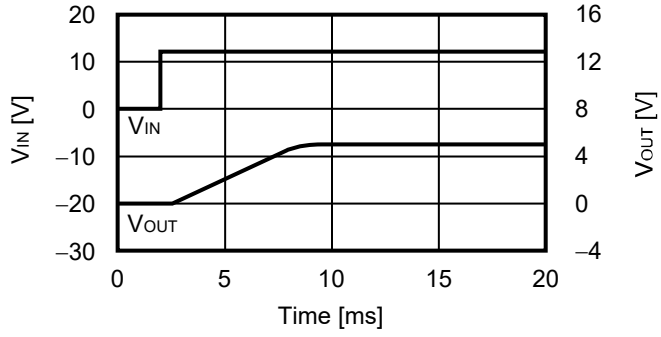
Element Name	Constant	Manufacturer	Part Number
Inductor	3.3 µH	TDK Corporation	TFM322512ALMA3R3MTAA
Input capacitor	4.7 µF	TDK Corporation	CGA5L3X7R1H475K160AB
Output capacitor	10 µF	TDK Corporation	CGA5L1X7R1C106K160AC

4. 1 Power-on (V_{OUT} = 5.0 V, V_{IN} = V_{EN} =0 V → 12 V, Ta = +25°C)

4. 1. 1 I_{OUT} = 1 mA

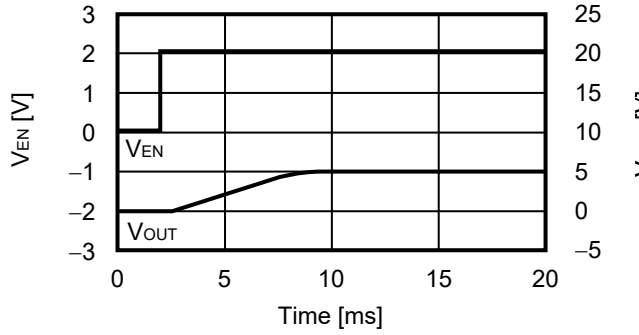


4. 1. 2 I_{OUT} = 1 A

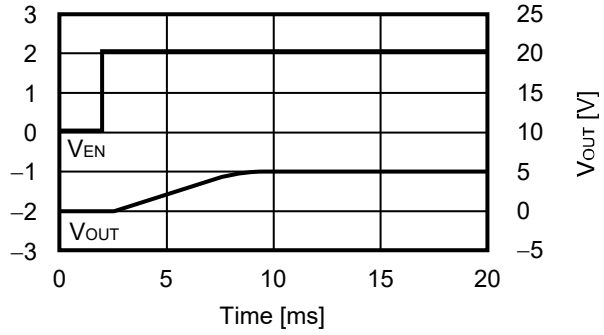


4. 2 Transient response characteristics of EN pin
(V_{OUT} = 5.0 V, V_{IN} = 12 V, V_{EN} = 0 V → 2.0 V, Ta = +25°C)

4. 2. 1 I_{OUT} = 1 mA

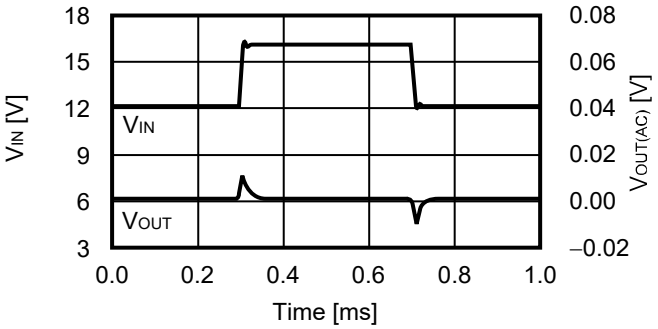


4. 2. 2 I_{OUT} = 1 A

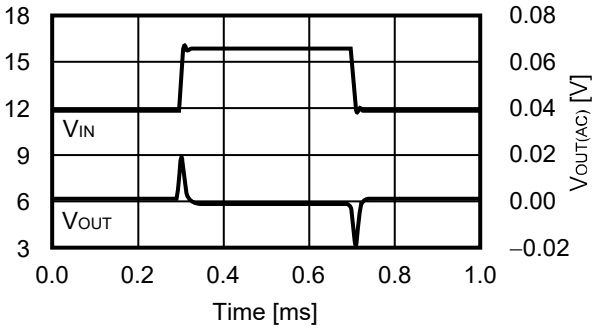


4. 3 Power supply fluctuation (V_{OUT} = 5.0 V, V_{IN} = 12 V → 16 V→ 12 V, Ta = +25°C)

4. 3. 1 I_{OUT} = 1 mA

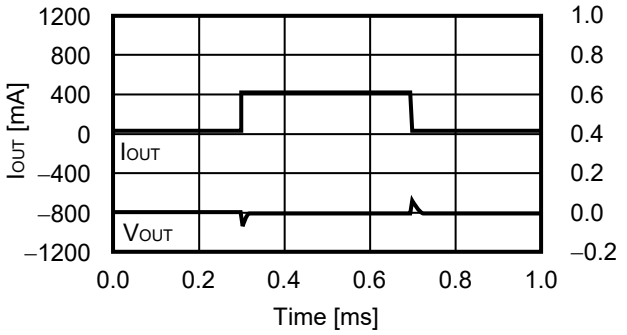


4. 3. 2 I_{OUT} = 1 A

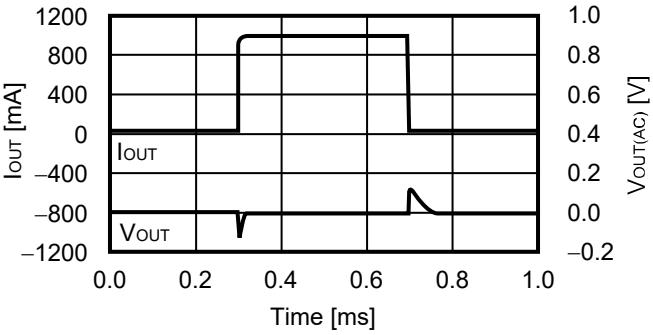


4. 4 Load fluctuation (V_{OUT} = 5.0 V, Ta = +25°C)

4. 4. 1 I_{OUT} = 10 mA → 400 mA → 10 mA



4. 4. 2 I_{OUT} = 10 mA → 1000 mA → 10 mA



■ Reference Data

The external parts shown in **Table 17** are used in "■ **Reference Data**".

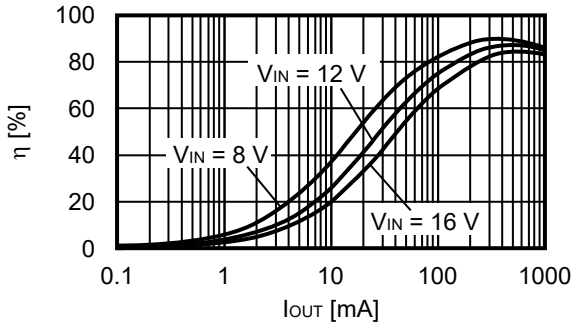
Table 17

Condition	Inductor (L)	Input Capacitor (C_{IN})	Output Capacitor (C_{OUT})
<1>	TFM322512ALMA3R3MTAA (3.3 μH) TDK Corporation	CGA5L3X7R1H475K160AB (4.7 μF) TDK Corporation	CGA5L1X7R1C106K160AC (10 μF) TDK Corporation
<2>	TFM252012ALMA2R2MTAA (2.2 μH) TDK Corporation	CGA5L3X7R1H475K160AB (4.7 μF) TDK Corporation	CGA5L1X7R1C106K160AC (10 μF) TDK Corporation

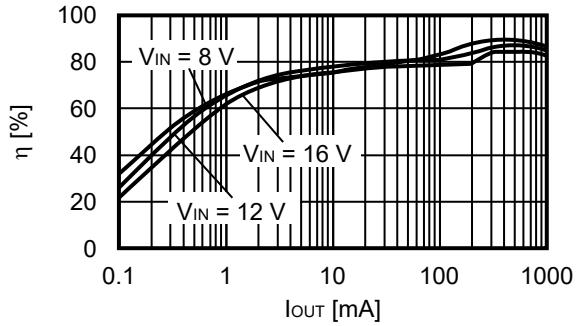
1. V_{OUT} = 5.0 V (External parts: Condition<1>)

1. 1 Efficiency (η) vs. Output current (I_{OUT})

1. 1. 1 S-8594 Series

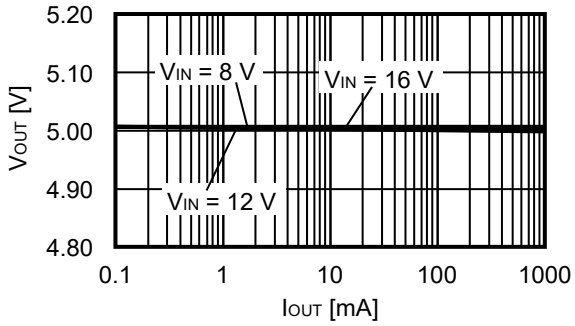


1. 1. 2 S-8595 Series

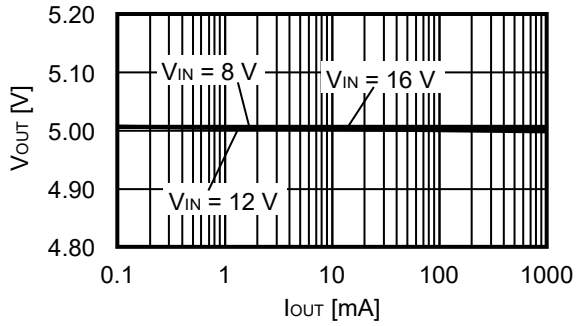


1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})

1. 2. 1 S-8594 Series

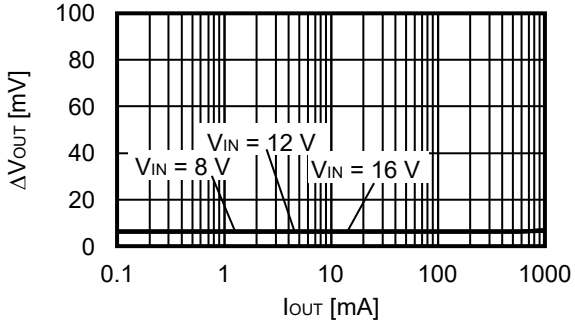


1. 2. 2 S-8595 Series

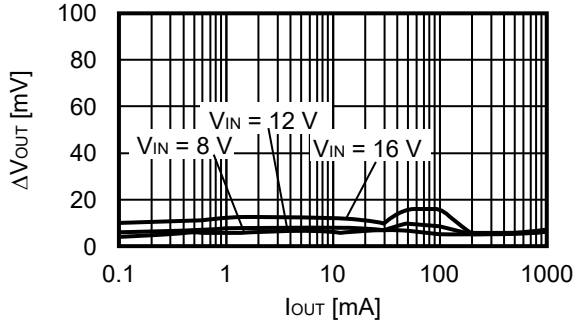


1. 3 Ripple voltage (ΔV_{OUT}) vs. Output current (I_{OUT})

1. 3. 1 S-8594 Series



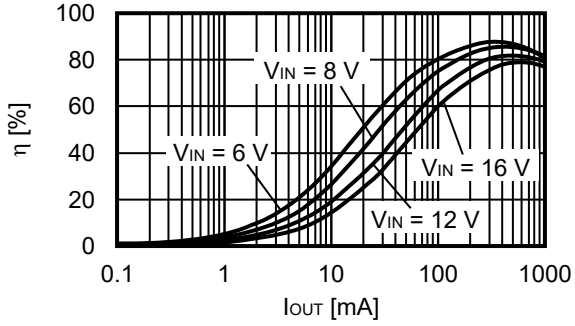
1. 3. 2 S-8595 Series



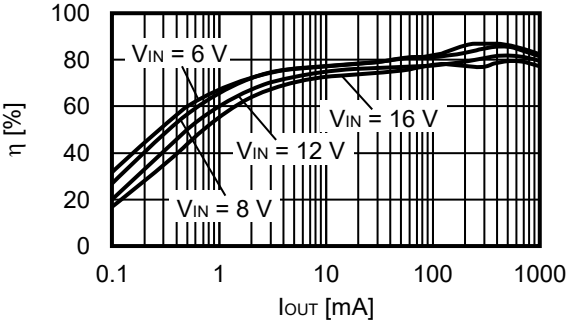
2. V_{OUT} = 3.3 V (External parts: Condition<2>)

2. 1 Efficiency (η) vs. Output current (I_{OUT})

2. 1. 1 S-8594 Series

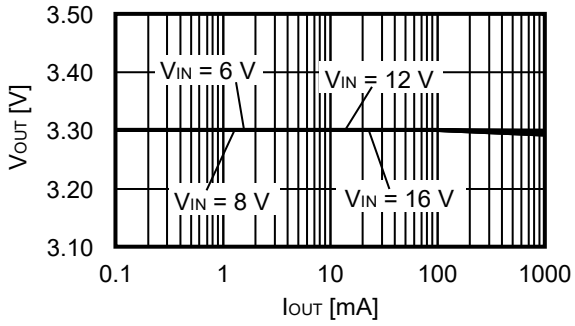


2. 1. 2 S-8595 Series

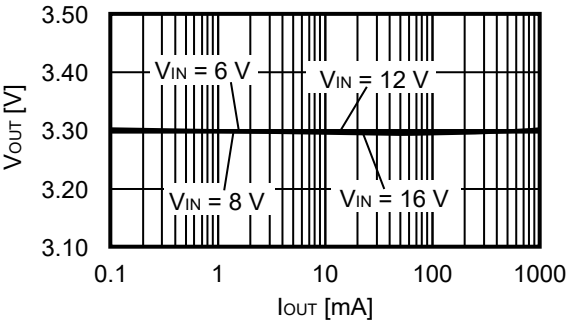


2. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})

2. 2. 1 S-8594 Series

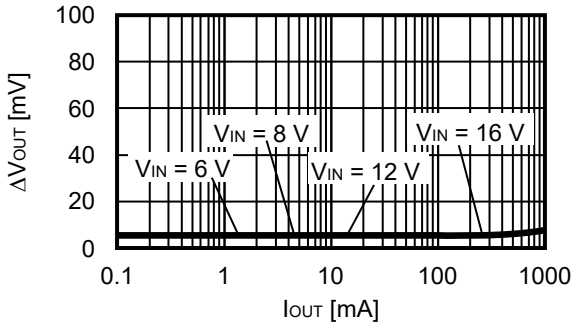


2. 2. 2 S-8595 Series

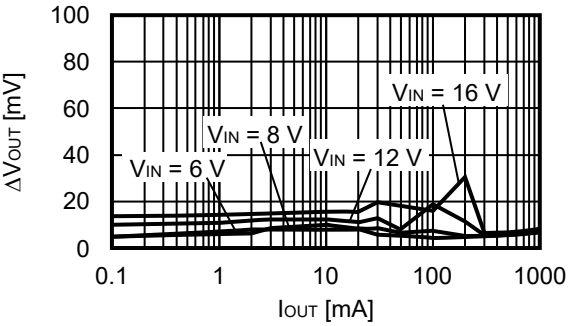


2. 3 Ripple voltage (ΔV_{OUT}) vs. Output current (I_{OUT})

2. 3. 1 S-8594 Series

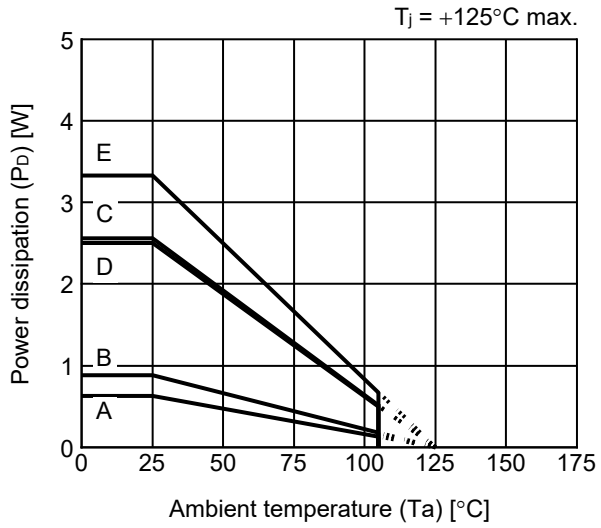


2. 3. 2 S-8595 Series



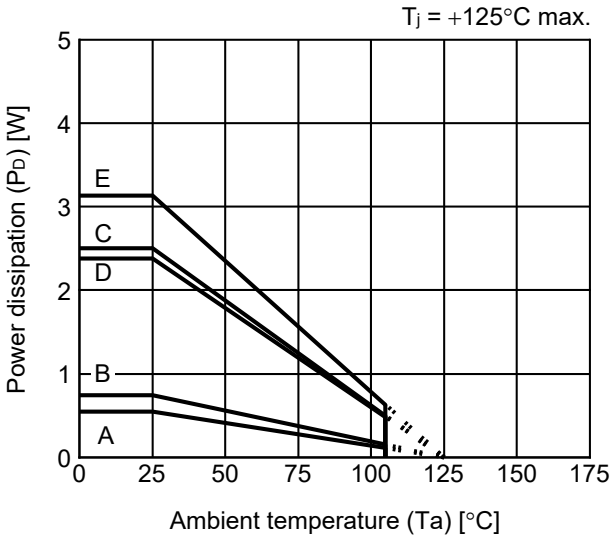
■ Power Dissipation

HTMSOP-8



Board	Power Dissipation (P_D)
A	0.63 W
B	0.88 W
C	2.56 W
D	2.50 W
E	3.33 W

HSNT-8(2030)

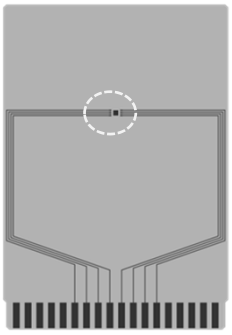


Board	Power Dissipation (P_D)
A	0.55 W
B	0.74 W
C	2.50 W
D	2.38 W
E	3.13 W

HTMSOP-8 Test Board

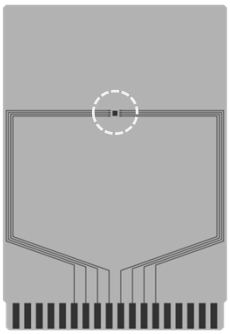
IC Mount Area

(1) Board A



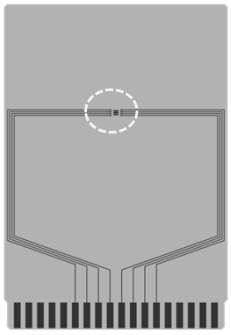
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

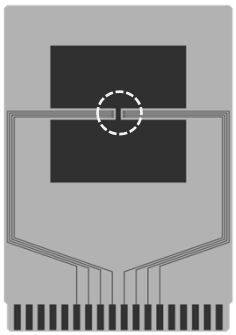
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HTMSOP8-A-Board-SD-1.0

HTMSOP-8 Test Board

IC Mount Area

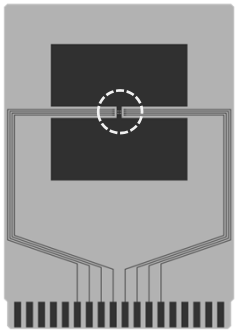
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



enlarged view

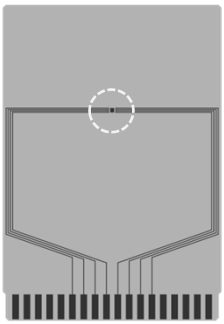
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HTMSOP8-A-Board-SD-1.0

HSNT-8(2030) Test Board

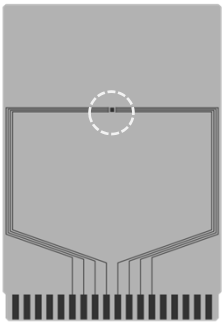
IC Mount Area

(1) Board A



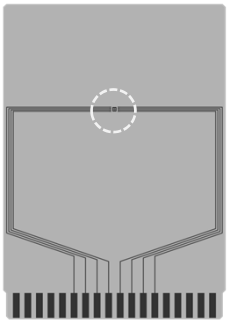
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

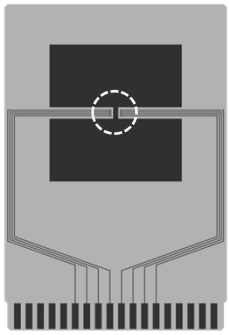
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-A-Board-SD-2.0

HSNT-8(2030) Test Board

IC Mount Area

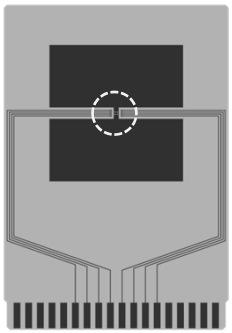
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

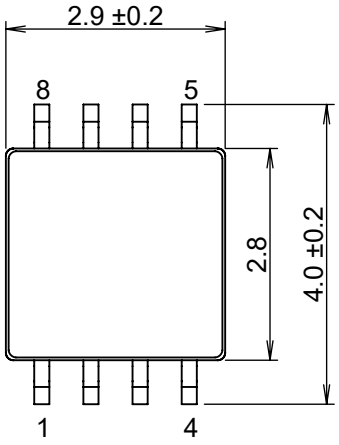
(5) Board E

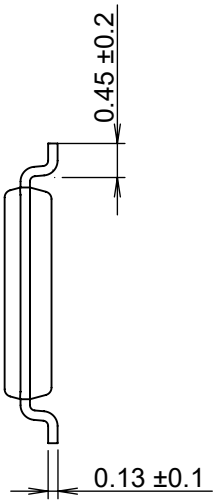


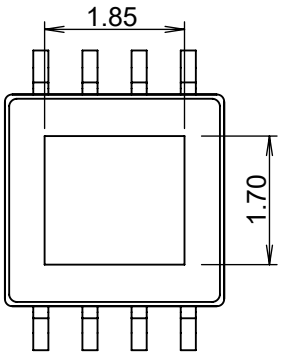
enlarged view

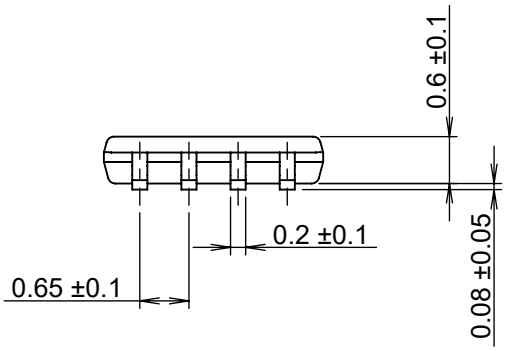
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-A-Board-SD-2.0



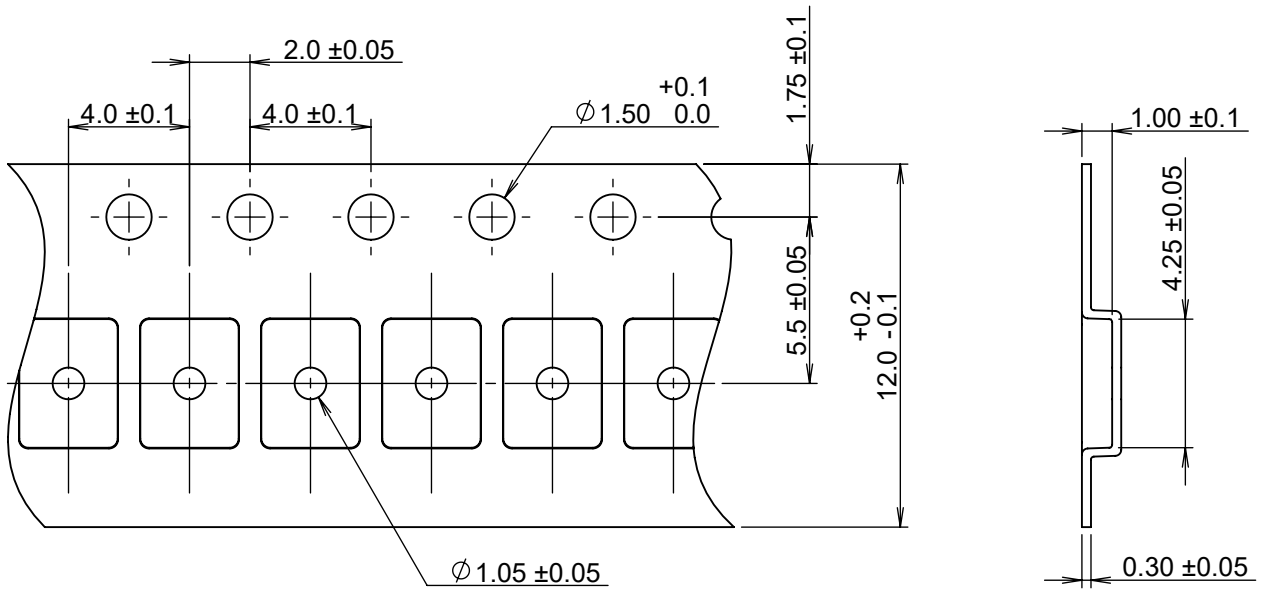


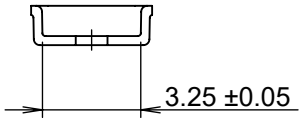


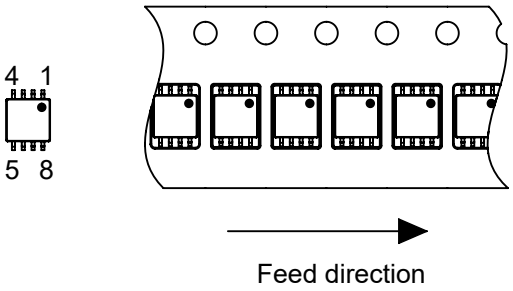


No. FP008-A-P-SD-2.0

TITLE	HTMSOP8-A-PKG Dimensions
No.	FP008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

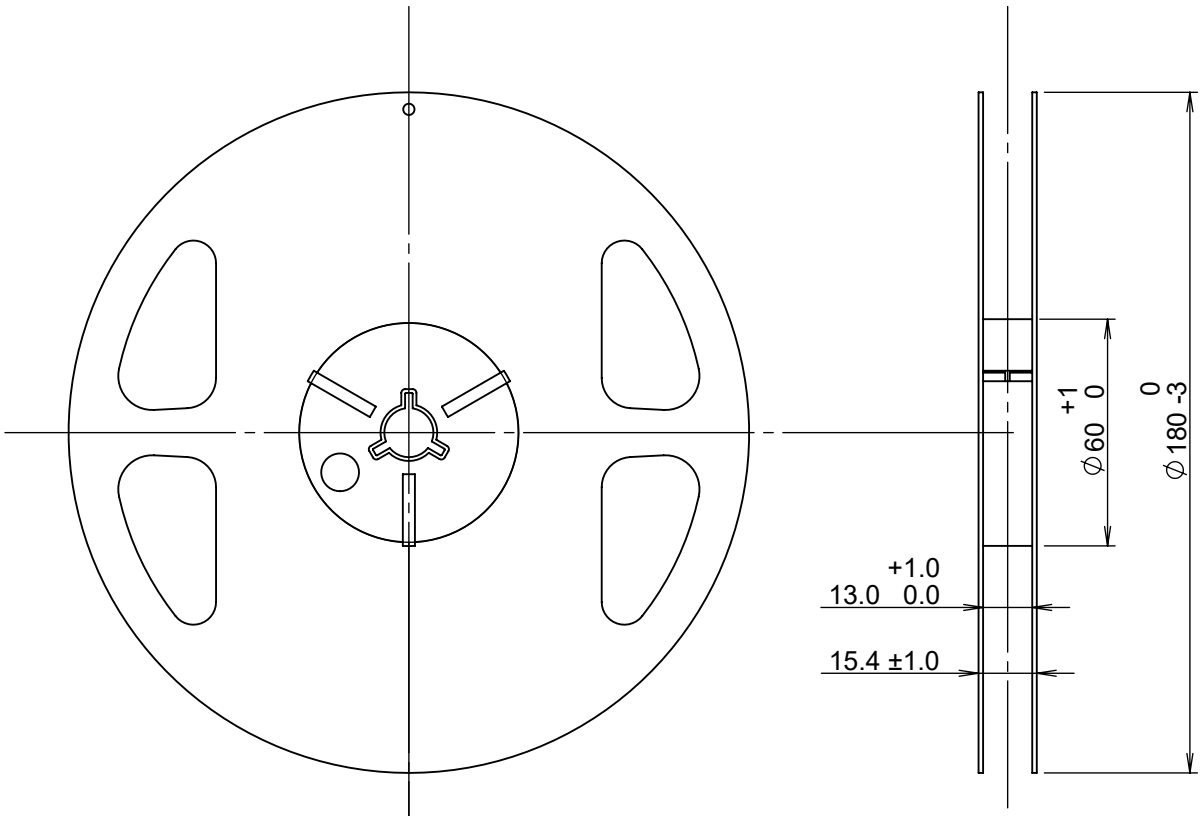




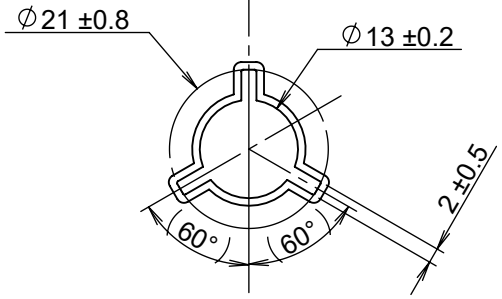


No. FP008-A-C-SD-1.0

TITLE	HTMSOP8-A-Carrier Tape
No.	FP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

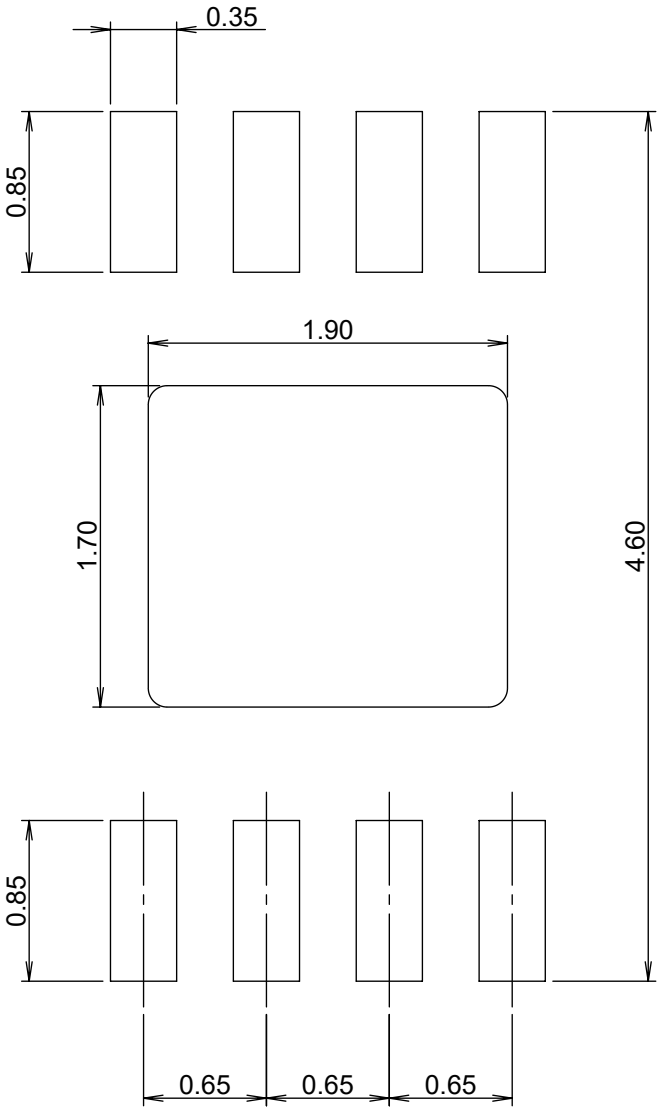


Enlarged drawing in the central part



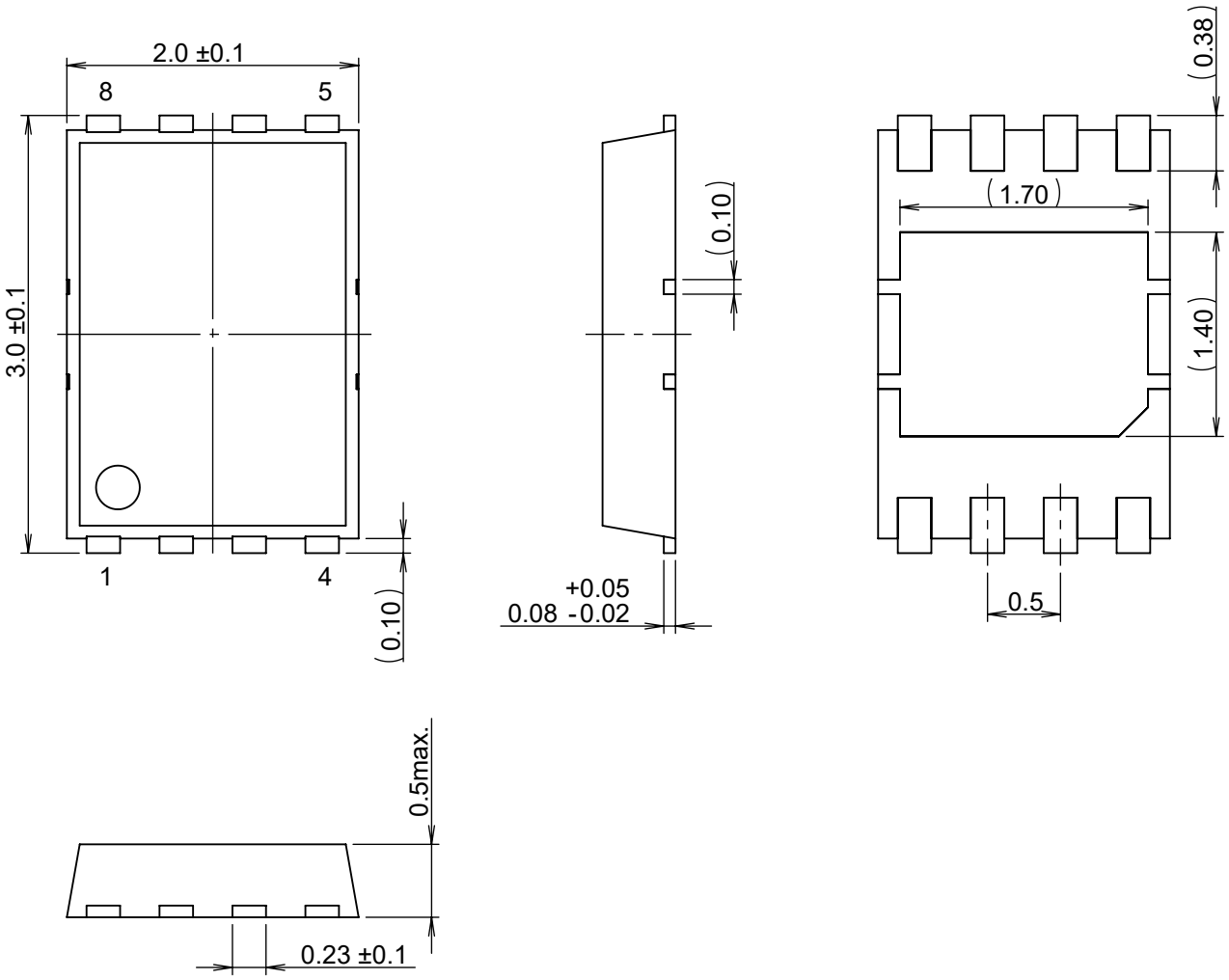
No. FP008-A-R-SD-2.0

TITLE	HTMSOP8-A-Reel		
No.	FP008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



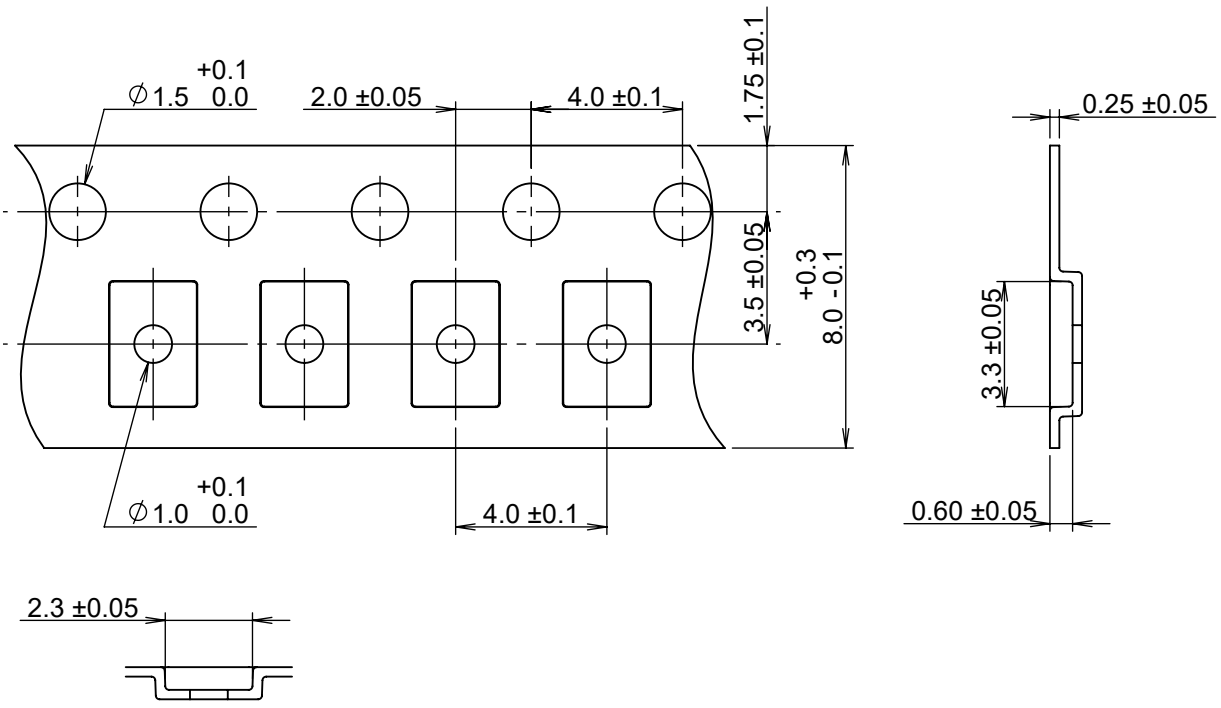
No. FP008-A-L-SD-2.0

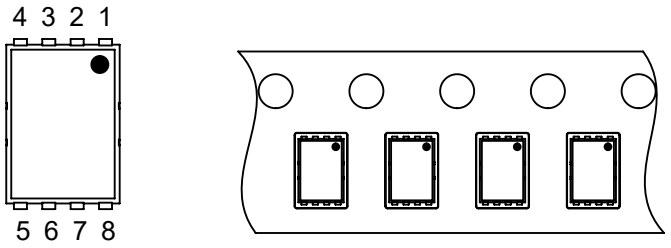
TITLE	HTMSOP8-A -Land Recommendation
No.	FP008-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. PP008-A-P-SD-3.0

TITLE	HSNT-8-A-PKG Dimensions
No.	PP008-A-P-SD-3.0
ANGLE	
UNIT	mm
ABLIC Inc.	

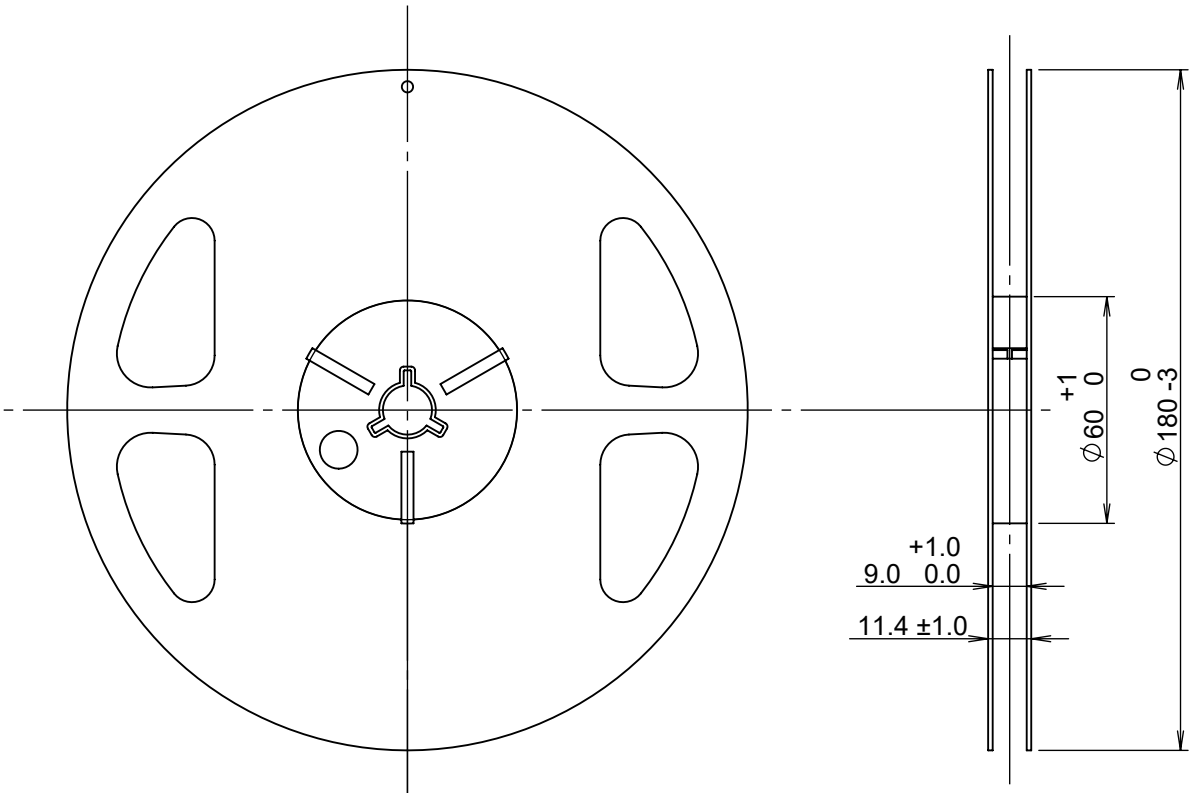




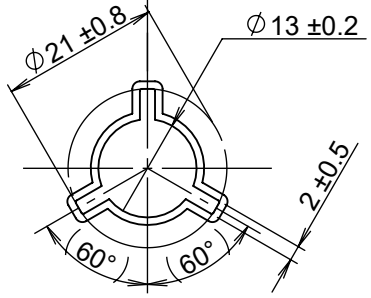
Feed direction

No. PP008-A-C-SD-1.0

TITLE	HSNT-8-A-Carrier Tape
No.	PP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

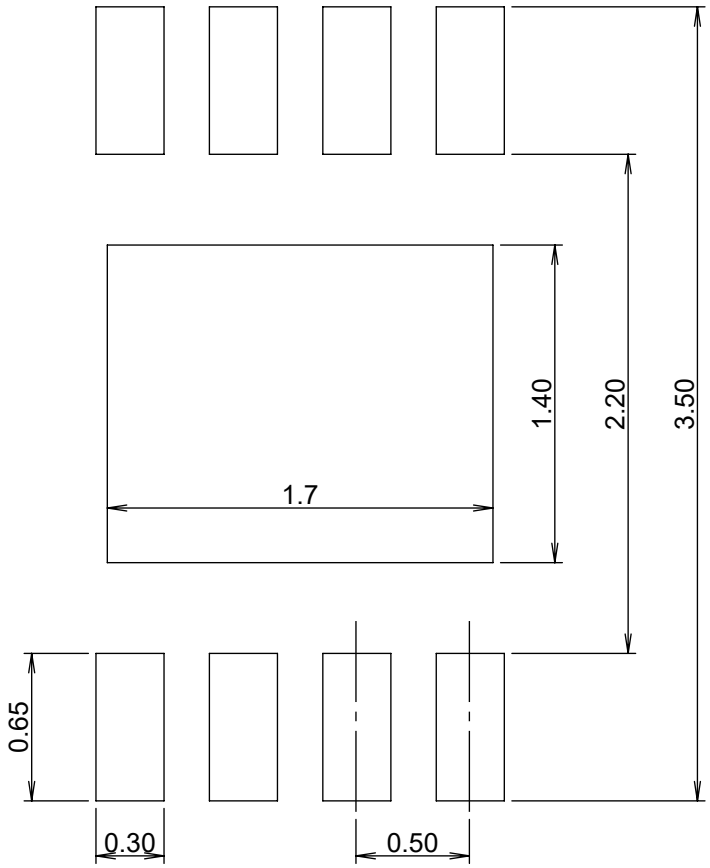


Enlarged drawing in the central part



No. PP008-A-R-SD-2.0

TITLE	HSNT-8-A-Reel		
No.	PP008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



No. PP008-A-L-SD-2.0

TITLE	HSNT-8-A -Land Recommendation
No.	PP008-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07