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PROGRAMMABLE, FAST-RESPONSE, LINEAR HALL EFFECT SENSOR IC

This IC, developed by CMOS technology, is a programmable fast-response linear Hall effect sensor IC. It provides an analog output voltage proportional to the magnetic flux density based on the VREF pin voltage.
The IC has a built-in non-volatile memory and a 2-wire serial interface that allow flexible switching functions and trimming adjustments. Switching functions are available for the reference voltage operation mode, reference voltage output, output voltage polarity, frequency bandwidth, and thermal shutdown. High-precision trimming adjustments are available for sensitivity, sensitivity thermal drift, output offset voltage, and reference voltage output.
Because of its fast response, it is ideal for current sensor applications such as monitoring instantaneous overcurrent.

■ Features

- Output response time: 2.5 µs max. (frequency bandwidth 400 kHz)
- Analog voltage output proportional to magnetic flux density:
  Operates with VREF pin voltage reference, non-linearity ±0.5% max.
  High resistance to power supply noise due to non-ratiometric operation
- Built-in non-volatile memory: 2-wire serial interface enables switching of IC functions and trimming adjustment
- Built-in thermal shutdown circuit: Detection temperature 170°C typ.
- Switching functions
  - Reference voltage operation mode: Reference voltage output mode*1, reference voltage input mode
  - Reference voltage output: 0.50 V, 1.50 V, 1.65 V, 2.50 V*1
  - Output voltage polarity: Normal polarity*1, opposite polarity
  - Frequency bandwidth: 100 kHz, 200 kHz, 400 kHz*1
  - Thermal shutdown: Available*1, unavailable
- Trimming adjustment
  - Sensitivity: 6 V/T to 180 V/T (130 V/T typ.*1), 0.3% step max.
  - Sensitivity thermal drift: -500 ppm/°C to +500 ppm/°C (0 ppm/°C typ.*1), 25 ppm/°C step typ.
  - Output offset voltage: 1.5 mV step max.
  - Reference voltage output: 4.0 mV step max.
- Power supply voltage range: V_{DD} = 4.5 V to 5.5 V
- Current consumption: I_{DD} = 19 mA typ.
- Operation temperature range: Ta = -40°C to +125°C
- Lead-free (Sn 100%), halogen-free

***1.** Initial settings at shipment

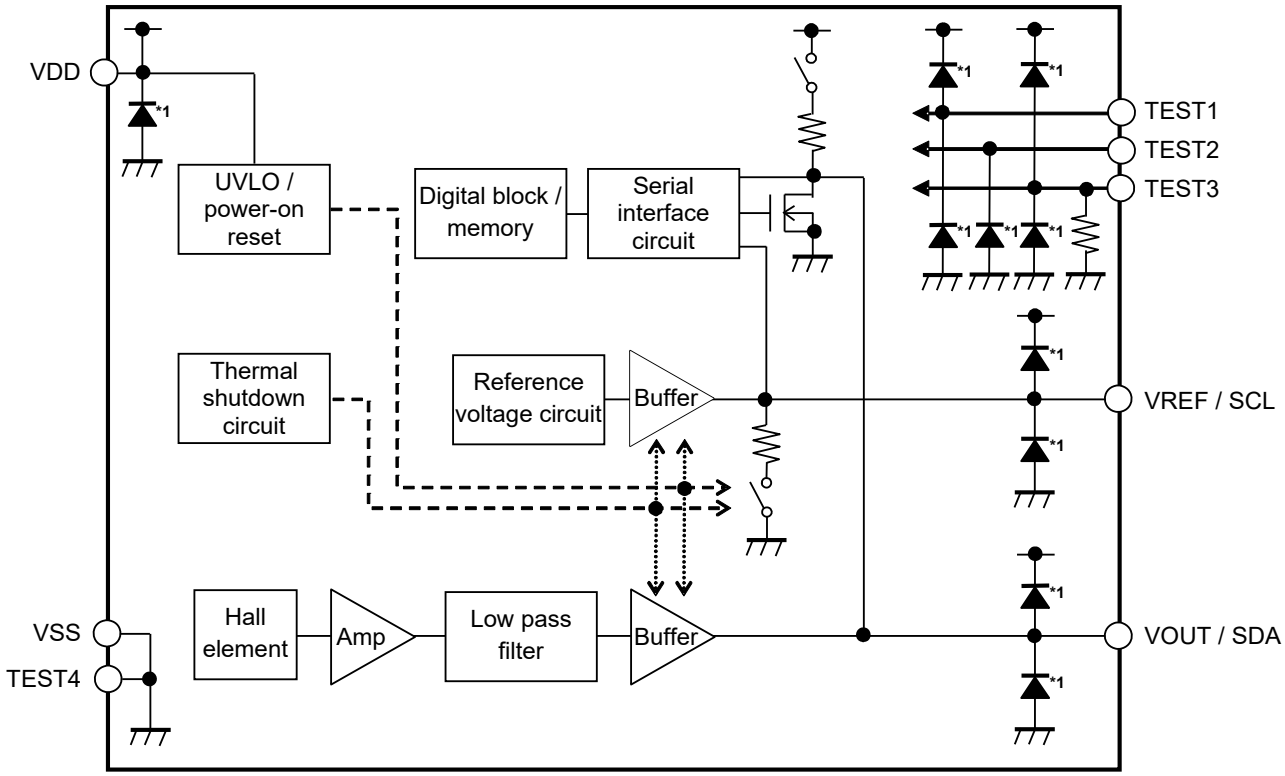
■ Application

- Magnetic core current sensor
- Linear position detection
- Rotation detection

■ Package

- TMSOP-8

■ Block Diagram

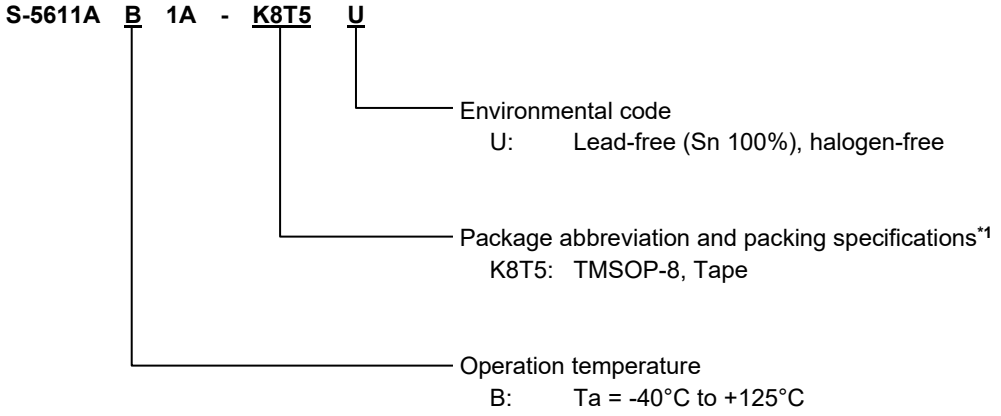


***1.** Parasitic diode

Figure 1

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	Package
S-5611AB1A-K8T5U	TMSOP-8

■ Pin Configurations

1. TMSOP-8

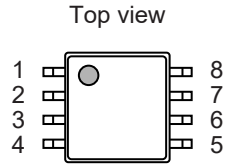


Figure 2

Table 3

Pin No.	Symbol	Description	
1	VREF / SCL*1	VREF	Reference voltage I/O pin
		SCL	Serial clock input pin
2	VOUT / SDA*2	VOUT	Output pin
		SDA	Serial data I/O pin
3	VSS	GND pin	
4	TEST4*3	Test 4 pin	
5	VDD	Power supply pin	
6	TEST1*4	Test 1 pin	
7	TEST2*4	Test 2 pin	
8	TEST3*4	Test 3 pin	

***1.** The VREF / SCL pin combines the reference voltage I/O pin and the serial clock input pin.
***2.** The VOUT / SDA pin combines the output pin and the serial data I/O pin.
***3.** The TEST4 pin is shorted to the VSS pin (refer to **Figure 1**). Set the TEST4 pin open in use.
***4.** Set the TEST1 pin, the TEST2 pin, and the TEST3 pin open in use.

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	VDD	V_{SS} - 0.3 to V_{SS} + 6.5	V
Input / output voltage	V_{REF}	VREF / SCL	V_{SS} - 0.3 to V_{DD} + 0.3	V
	V_{SCL}	VREF / SCL	V_{SS} - 0.3 to V_{DD} + 0.3	V
	V_{OUT}	VOUT / SDA	V_{SS} - 0.3 to V_{DD} + 0.3	V
	V_{SDA}	VOUT / SDA	V_{SS} - 0.3 to V_{DD} + 0.3	V
	$V_{I/O}$	TEST1, TEST3	V_{SS} - 0.3 to V_{DD} + 0.3	V
		TEST2	V_{SS} - 0.3 to V_{SS} + 1.98	V
Junction temperature	T_j	-	-40 to +175	°C
Operation ambient temperature	T_{opr}	-	-40 to +125	°C
Storage temperature	T_{stg}	-	-40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TMSOP-8	Board A	-	160	-	°C/W
			Board B	-	133	-	°C/W
			Board C	-	-	-	°C/W
			Board D	-	-	-	°C/W
			Board E	-	-	-	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Linear Hall effect sensor operation

1. 1 Power supply characteristics

Table 6

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V, V_{REF} = 2.5 V, S = 130 V/T, B = 0 mT, default value*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	-	4.5	5.0	5.5	V	-
Current consumption	I_{DD}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)	-	19	22	mA	1
UVLO release voltage	V_{UVLOR}	-	4.15	4.30	4.45	V	1
UVLO detection voltage	V_{UVLOD}	-	3.95	4.10	4.25	V	1
UVLO hysteresis voltage	$V_{UVLOHYS}$	-	-	0.2	-	V	-
UVLO detection delay time*2	t_{DELAY_UVLOD}	-	-	1.0	-	ms	-
Power-on reset threshold voltage	V_{PON}	-	-	2.90	-	V	-
Power-off threshold voltage	V_{POFF}	-	-	2.80	-	V	-
Power-on reset hysteresis voltage	V_{PHYS}	-	-	0.10	-	V	-
Thermal shutdown detection temperature	T_{SD}	Junction temperature	-	170	-	°C	-
Thermal shutdown release temperature	T_{SR}	Junction temperature	-	155	-	°C	-
Start up time*3	t_{PON}	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF	-	0.9	1.0	ms	-

***1.** The function settings and trimming adjustments of the IC are in the initial settings at the time of shipment.
***2.** Refer to "**3. 1 Low power supply voltage detection circuit**" in "**■ Operation**".
***3.** Refer to "**2. 12 Start up time**" in "**■ Operation**".

1. 2 Magnetic characteristics

Table 7

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V, V_{REF} = 2.5 V, S = 130 V/T, B = 0 mT, default value*1 unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Maximum magnetic flux density*2, 3	B_{MAX}	At minimum magnetic sensitivity setting		±350	-	-	mT	1
Sensitivity linearity error*4	LIN	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-0.5	-	0.5	%	1
Sensitivity*5	S	Initial settings at shipment		-	130	-	V/T	-
Sensitivity programming range	S_{RNG}	-		6	-	180	V/T	1
Sensitivity programming step	S_{STEP}	Formula A (S@n + 1 [LSB] - S@n [LSB]) / S@0 [LSB]		-	0.08	0.15	%	1
		Formula B (S@n + 1 [LSB] - S@n [LSB]) / S@n [LSB]		-	0.18	0.30	%	1
Sensitivity thermal drift*6	TCS	Ta = -40°C to +125°C (Tj = -40°C to +150°C)		-200	0	200	ppm/°C	1
Sensitivity thermal drift programming range	TCS_{RNG}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-500	-	500	ppm/°C	1
Sensitivity thermal drift programming step	TCS_{STEP}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-	25	-	ppm/°C	-
Output response time*7	t_{RSP_OUT}	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, B = 10 mT, time from B 90% to V_{OUT} 90%	f_{BW} = 400 kHz	-	1.25	2.50	µs	1
			f_{BW} = 200 kHz	-	2.50	3.75	µs	1
			f_{BW} = 100 kHz	-	5.00	6.00	µs	1
Output reaction time*7	t_{RAC_OUT}	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, B = 10 mT, time from B 10% to V_{OUT} 10%	f_{BW} = 400 kHz	-	0.75	1.75	µs	1
			f_{BW} = 200 kHz	-	1.25	2.00	µs	1
			f_{BW} = 100 kHz	-	2.00	3.00	µs	1
Output settling time*2, 7	t_{SET_OUT}	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, B = 10 mT, time from V_{OUT} 10% to stabilization within 3% of V_{OUT} steady status	f_{BW} = 400 kHz	-	2.5	5.0	µs	1
			f_{BW} = 200 kHz	-	4.0	6.5	µs	1
			f_{BW} = 100 kHz	-	5.5	8.0	µs	1
Output overshoot*2, 7	OS	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, B = 10 mT, overshoot against V_{OUT} steady status		-	-	10	%	1
Frequency bandwidth	f_{BW}	Initial settings at shipment, C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, frequency with a magnetic sensitivity of -3 dB		-	400	-	kHz	-
Frequency bandwidth programming range	f_{BWRNG}	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, frequency with a magnetic sensitivity of -3 dB		-	400	-	kHz	-
				-	200	-	kHz	-
				-	100	-	kHz	-

***1.** The function settings and trimming adjustments of the IC are in the initial settings at the time of shipment.
***2.** This item is guaranteed by design.
***3.** Refer to "**2. 6 Maximum magnetic flux density**" in "**■ Operation**".
***4.** Refer to "**2. 7 Sensitivity linearity error**" in "**■ Operation**".
***5.** Refer to "**2. 4 Sensitivity**" in "**■ Operation**".
***6.** Refer to "**2. 5 Sensitivity thermal drift**" in "**■ Operation**".
***7.** Refer to "**2. 11 Output reaction**" in "**■ Operation**".

Remark The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

1. 3 Output voltage characteristics

Table 8

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V, V_{REF} = 2.5 V, S = 130 V/T, B = 0 mT, default value*1 unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Output offset voltage*2	V_{OFF}	Initial settings at shipment		-	0	-	mV	1
Output offset voltage programming range	V_{OFFRNG}	-		-100	-	100	mV	1
Output offset voltage programming step	$V_{OFFSTEP}$	-		-	0.6	1.5	mV	1
Output offset voltage thermal drift*3	T_{CVOFF}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-0.075	0	0.075	mV/°C	1
Output voltage "H"	V_{OUT_H}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		4.85	-	-	V	1
Output voltage "L"	V_{OUT_L}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-	-	0.15	V	1
Output source current	I_{OUT_SOC}	V_{OUT} = V_{SS}		17	22	27	mA	2
Output sink current	I_{OUT_SNK}	V_{OUT} = V_{DD}		17	22	27	mA	2
Output resistance	R_{OUT}	I_{OUT} = ±1.25 mA, Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-	1	4	Ω	3
Output pin load resistance	R_{LOUT}	Connected between the VOUT pin and the VSS pin, Ta = -40°C to +125°C (T_j = -40°C to +150°C)		2	-	-	kΩ	-
Output pin load capacitance	C_{LOUT}	Connected between the VOUT pin and the VSS pin, Ta = -40°C to +125°C (T_j = -40°C to +150°C)		0	4.7	6.0	nF	-
Input magnetic flux density referred noise voltage	B_{NOISE}	f = 10 kHz		-	0.09	-	$\mu T/\sqrt{Hz}$	-
Output noise voltage	V_{NOISE_RMS}	S = 30 V/T	f_{BW} = 400 kHz	-	1.89	-	mV_{rms}	-
			f_{BW} = 200 kHz	-	1.40	-	mV_{rms}	-
			f_{BW} = 100 kHz	-	1.08	-	mV_{rms}	-

***1.** The function settings and trimming adjustments of the IC are in the initial settings at the time of shipment.

***2.** Refer to "**2. 8 Output offset voltage**" in "**■ Operation**".

***3.** Refer to "**2. 9 Output offset voltage thermal drift**" in "**■ Operation**".

1. 4 Reference voltage characteristics

Table 9

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V, V_{REF} = 2.5 V, S = 130 V/T, B = 0 mT, default value*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Reference voltage output mode							
Reference voltage output	V_{REF}	Initial settings at shipment	2.48	2.50	2.52	V	1
Reference voltage programming range	V_{REFRNG}	V_{REF} = 2.50 V	-	2.50	-	V	1
		V_{REF} = 1.65 V	-	1.65	-	V	1
		V_{REF} = 1.50 V	-	1.50	-	V	1
		V_{REF} = 0.50 V	-	0.50	-	V	1
Reference voltage programming step	$V_{REFSTEP}$	V_{REF} = 2.50 V	-	2.5	4.0	mV	1
Reference voltage thermal drift*2	T_{CVREF}	V_{REF} = 2.5 V / 1.65 V / 1.5 V, Ta = -40°C to +125°C (Tj = -40°C to +150°C)	-100	0	100	ppm/°C	1
		V_{REF} = 0.5 V, Ta = -40°C to +125°C (Tj = -40°C to +150°C)	-150	0	150	ppm/°C	1
Reference voltage source current	I_{REF_SOC}	V_{REF} = V_{SS}	0.30	0.36	0.50	mA	4
Reference voltage sink current	I_{REF_SNK}	V_{REF} = V_{DD}	10.0	12.0	14.0	mA	4
Reference voltage output resistance	R_{REF}	I_{REF} = ±12.5 μA, Ta = -40°C to +125°C (T_j = -40°C to +150°C)	160	200	280	Ω	5
Reference voltage output pin load resistance	R_{LREF}	Connected between the VREF pin and the VSS pin, Ta = -40°C to +125°C (T_j = -40°C to +150°C)	200	-	-	kΩ	-
Reference voltage output pin load capacitance	C_{LREF}	Connected between the VREF pin and the VSS pin, Ta = -40°C to +125°C (T_j = -40°C to +150°C)	-	47	-	nF	-
Reference voltage input mode							
Reference voltage input	V_{REFIN}	-	0.50	-	2.65	V	5
Reference voltage input leakage current	I_{IN_REF}	V_{REF} = 0 V to 2.65 V	-	0.1	-	μA	-

***1.** The function settings and trimming adjustments of the IC are in the initial settings at the time of shipment.

***2.** Refer to "**2. 10 Reference voltage thermal drift**" in "**■ Operation**".

2. Serial communication operations

2. 1 Pin capacitance

Table 10

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL pin input capacitance	C_{IN_SCL}	-	-	1	-	pF
SDA pin I/O capacitance	C_{I/O_SDA}	-	-	1	-	pF

2. 2 Memory characteristics

Table 11

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Endurance	N_W	-		1000	-	-	cycle / word*1
Data retention	-	365 days, 24 hours*2	T_j = +25°C	15	-	-	year
			T_j = +125°C	10	-	-	year
			T_j = +150°C	3	-	-	year
			T_j = +175°C	1	-	-	year

***1.** For each address (Word: 8-bit)

***2.** In the case where temperature changes occur over time, such as in a temperature cycle, this is the accumulated value of the time the IC is at high temperature.

2. 3 DC Electrical Characteristics

Table 12

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH_SCL}, V_{IH_SDA}	SCL pin*1, SDA pin	0.7 × V_{DD}	-	V_{DD} + 0.3	V
Low level input voltage	V_{IL_SCL}, V_{IL_SDA}	SCL pin, SDA pin	-0.3	-	0.3 × V_{DD}	V
Input leakage current	I_{IH_SCL}	SCL pin, V_{SCL} = V_{DD}	-	0.1	1.0	µA
	I_{IL_SCL}	SCL pin, V_{SCL} = V_{SS}	-	0.1	1.0	µA
	I_{IH_SDA}	SDA pin, V_{SDA} = V_{DD}	-	0.1	1.0	µA
Pull-up resistor*2	R_{PU_SDA}	SDA pin	320	380	460	Ω
Low level output current	I_{OL_SDA}	SDA pin, V_{SDA} = 0.6 V	8	12	-	mA

***1.** The voltage at the SCL pin is also used to leave from the serial communication operation mode.
Refer to "**1. 2. 2 Exiting serial communication operation mode**" in "**■ Operation**" for details.

***2.** Current flows through the pull-up resistor during the period when the SDA pin is set to "L" during serial communication operation mode.

Note that this increases the amount of current consumed from the VDD pin by the current of $\frac{V_{DD}}{R_{PU\_SDA}}$ [A] in addition to the current consumption (I_{DD}) of the linear Hall effect sensor operation mode.

2. 4 AC Electrical Characteristics

2. 4. 1 Output load = 100 pF (SCL clock frequency ≤ 400 kHz)

Table 13 Measurement Conditions

Input pulse voltage	0.2 × V_{DD} to 0.8 × V_{DD}
Input pulse rising / falling time	20 ns or less
Output judgment voltage	0.3 × V_{DD} to 0.7 × V_{DD}
Output load	100 pF

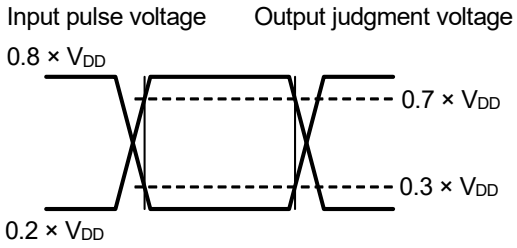


Figure 3 Input / Output Waveform during AC Measurement

Table 14

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	-	-	400	kHz
SCL clock time "L"	t_{LOW}	1300	-	-	ns
SCL clock time "H"	t_{HIGH}	600	-	-	ns
SCL, SDA rising time*1	t_R	-	-	300	ns
SCL, SDA falling time*1	t_F	-	-	300	ns
Data input setup time	$t_{SU.DAT}$	100	-	-	ns
Data input hold time	$t_{HD.DAT}$	0	-	-	ns
Data output delay time	t_{AA}	100	-	1100	ns
Data output hold time	t_{DH}	50	-	-	ns
Start condition setup time	$t_{SU.STA}$	600	-	-	ns
Start condition hold time	$t_{HD.STA}$	600	-	-	ns
Stop condition setup time	$t_{SU.STO}$	600	-	-	ns
Bus release time	t_{BUF}	13	-	-	ms
Noise suppression time	t_I	-	50	-	ns

***1.** This item is guaranteed by design.

2. 4. 2 Output load = 4.7 nF (SCL clock frequency ≤ 100 kHz)

Table 15 Measurement Conditions

Input pulse voltage	0.2 × V_{DD} to 0.8 × V_{DD}
Input pulse rising / falling time	1.0 µs or less
Output judgment voltage	0.3 × V_{DD} to 0.7 × V_{DD}
Output load	4.7 nF

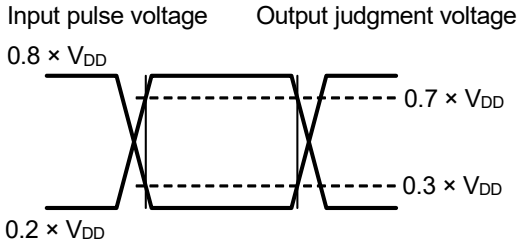


Figure 4 Input / Output Waveform during AC Measurement

Table 16

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	-	-	100	kHz
SCL clock time "L"	t_{LOW}	5.7	-	-	µs
SCL clock time "H"	t_{HIGH}	2.3	-	-	µs
SCL, SDA rising time*1	t_R	-	-	1.0	µs
SCL, SDA falling time*1	t_F	-	-	1.0	µs
Data input setup time	$t_{SU.DAT}$	0.25	-	-	µs
Data input hold time	$t_{HD.DAT}$	0	-	-	µs
Data output delay time	t_{AA}	0.1	-	5.45	µs
Data output hold time	t_{DH}	0.05	-	-	µs
Start condition setup time	$t_{SU.STA}$	4.0	-	-	µs
Start condition hold time	$t_{HD.STA}$	4.0	-	-	µs
Stop condition setup time	$t_{SU.STO}$	4.0	-	-	µs
Bus release time	t_{BUF}	13	-	-	ms
Noise suppression time	t_I	-	50	-	ns

***1.** This item is guaranteed by design.

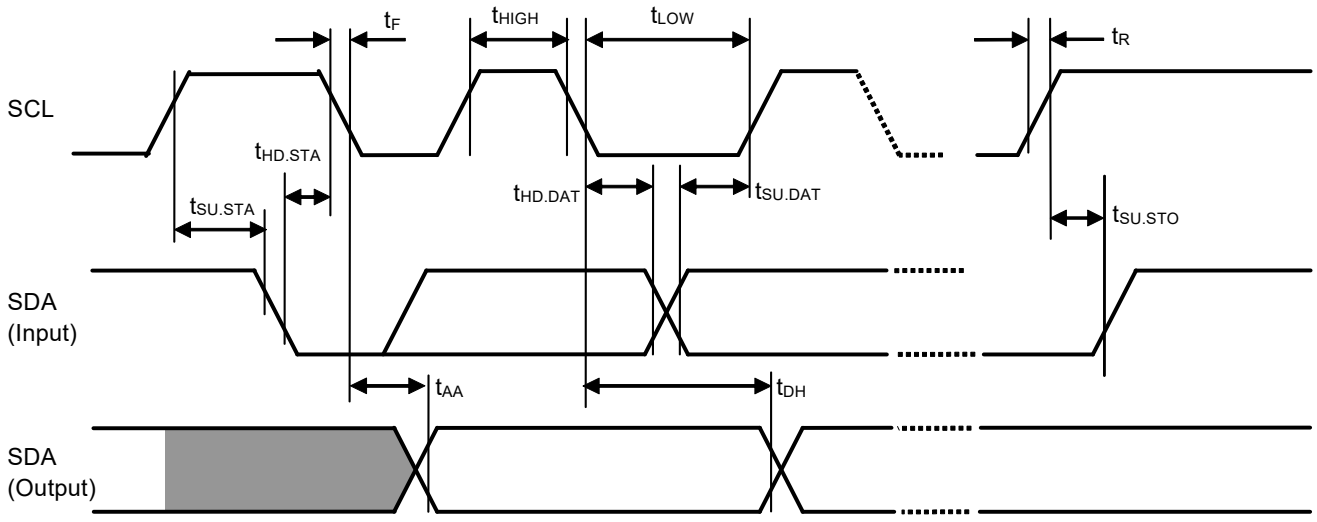


Figure 5 Bus Timing

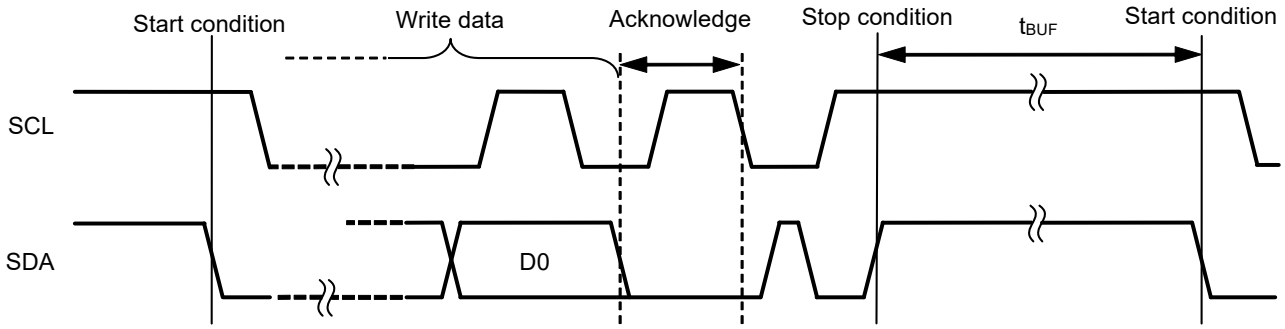


Figure 6 Write Cycle Timing

■ Test Circuits

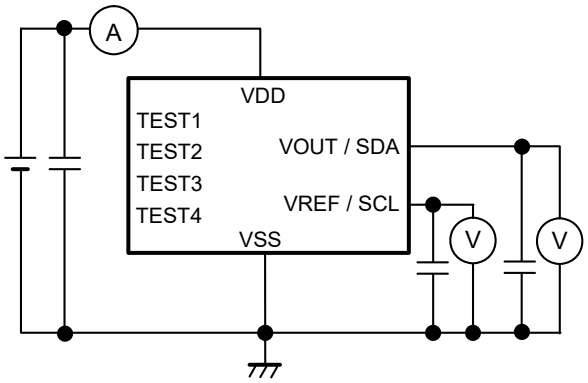


Figure 7 Test Circuit 1

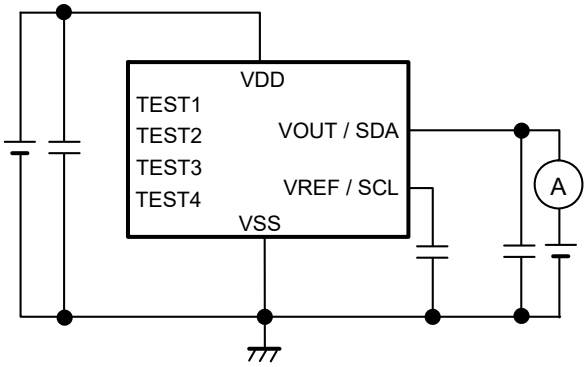


Figure 8 Test Circuit 2

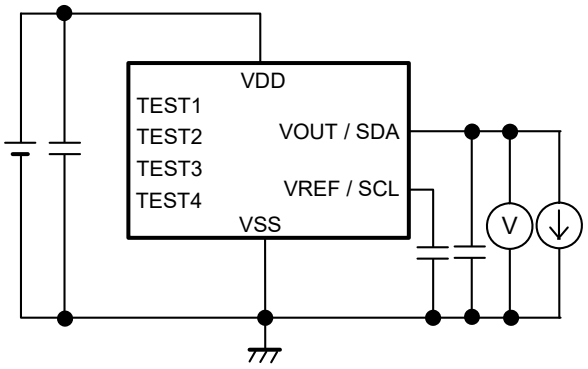


Figure 9 Test Circuit 3

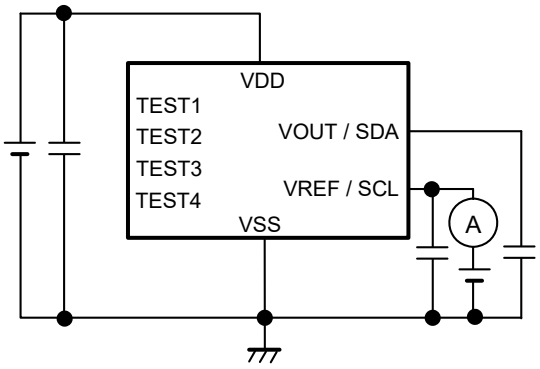


Figure 10 Test Circuit 4

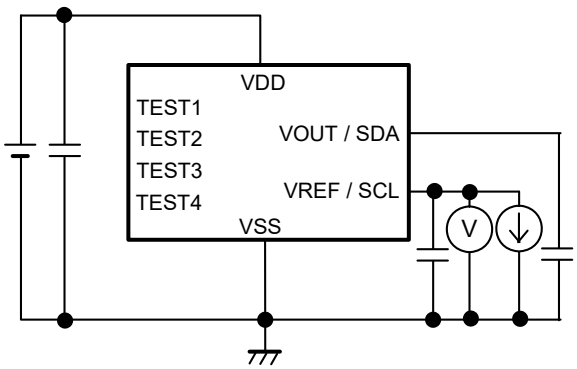


Figure 11 Test Circuit 5

■ Standard Circuits

1. Reference voltage output mode

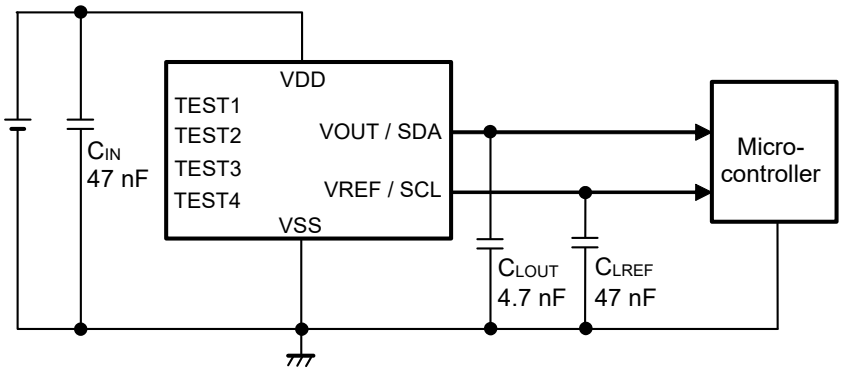


Figure 12 Standard Circuit (Reference Voltage Output Mode)

2. Reference voltage input mode

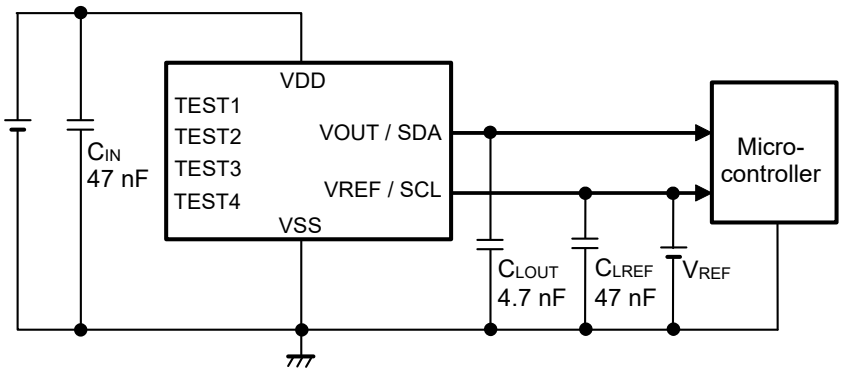


Figure 13 Standard Circuit (Reference Voltage Input Mode)

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Pin Functions

1. VDD pin

The VDD pin is used to apply positive supply voltage. Set a bypass capacitor of 47 nF or more between the VDD pin and the VSS pin for stabilization.

2. VREF / SCL pin

The VREF pin also serves as the SCL pin. In linear Hall effect sensor operation mode, it functions as the VREF pin, and in serial communication operation mode, it functions as the SCL pin.

In linear Hall effect sensor operation mode, it outputs or inputs the reference voltage. The built-in non-volatile memory allows switching between reference voltage output mode and reference voltage input mode. When operating in reference voltage output mode, connect a 47 nF capacitor (C_{LREF}) between the VREF pin and the VSS pin to ensure stable operation.

In serial communication operation mode, the master device inputs a serial clock to write/read data to the built-in non-volatile memory. Since the signals are processed at a rising or falling edge of the SCL clock, pay attention to the rising and falling time and comply with the specification.

3. VOUT / SDA pin

The VOUT pin also serves as the SDA pin. In linear Hall effect sensor operation mode, it functions as the VOUT pin, and in serial communication operation mode, it functions as the SDA pin.

In linear Hall effect sensor operation mode, this pin outputs a voltage according to the magnetic flux density applied to the IC. Connect a 47 nF capacitor (C_{LOUT}) between the VOUT pin and the VSS pin to ensure stable operation.

In serial communication operation mode, serial data is transferred in both directions and written to / read from the built-in non-volatile memory. It consists of a signal input pin and an Nch open-drain output pin and has a built-in resistor that pulls up to the V_{DD} potential.

■ Operation

1. Operation mode

This IC has two operation modes: linear Hall effect sensor operation mode and serial communication operation mode.
In the linear Hall effect sensor operation mode, it outputs an analog signal voltage proportional to the magnetic flux density with respect to the reference voltage output (V_{REF}). This is the normal operating mode for this IC.
In serial communication operation mode, IC functions can be switched, and trimming adjustments can be made by writing settings to the built-in non-volatile memory via a 2-wire serial interface. This is the operating mode to perform trimming adjustments before using this IC.

The conditions for switching to each operation mode are shown below.

1. 1 Entering linear Hall effect sensor operation mode

When the power supply voltage is turned on, if the VREF / SCL pin is left open or a load is connected between the VREF / SCL pin and the VSS pin, this IC will enter the linear hall effect sensor operation mode.
When the power supply voltage is raised, this IC resets its internal state. In this case, the VOUT / SDA pin and the VREF / SCL pin change to high impedance. When the power supply voltage reaches the UVLO release voltage (V_{UVLOR}), the trimming code is read from the built-in non-volatile memory. After that, the circuit starts operating, the VOUT / SDA pin voltage and the VREF / SCL pin voltage rise, and the device enters linear Hall effect sensor operation mode.

1. 2 Entering and exiting serial communication operation mode

1. 2. 1 Entering serial communication operation mode

Figure 14 shows how to enter serial communication operation mode. When the power supply voltage is applied to the VREF / SCL pin at the same time as the power supply voltage is turned on, this IC enters serial communication operation mode.
When the power supply voltage is raised, this IC resets its internal state. In this case, the VOUT / SDA pin and the VREF / SCL pin change to high impedance. When the power supply voltage reaches the UVLO release voltage (V_{UVLOR}), if the VREF / SCL pin voltage is higher than 0.8 × V_{DD} typ., the condition for entering serial communication operation mode is met. After the trimming code is read from the built-in non-volatile memory, the VOUT / SDA pin and VREF / SCL pin maintain high impedance output, and this IC enters serial communication operation mode. After entering serial communication operation mode, sending a command to start communication according to the serial communication protocol enables writing to and reading from the built-in non-volatile memory.

1. 2. 2 Exiting serial communication operation mode

Figure 14 shows how to exit the serial communication operation mode.
After entering the serial communication operation mode, if the VREF / SCL pin voltage is reduced to less than 0.8 × V_{DD} typ. without a start condition being input, this IC will exit the serial communication operation mode and enter the linear Hall effect sensor operation mode. To re-enter serial communication mode, the power supply voltage must be restarted.

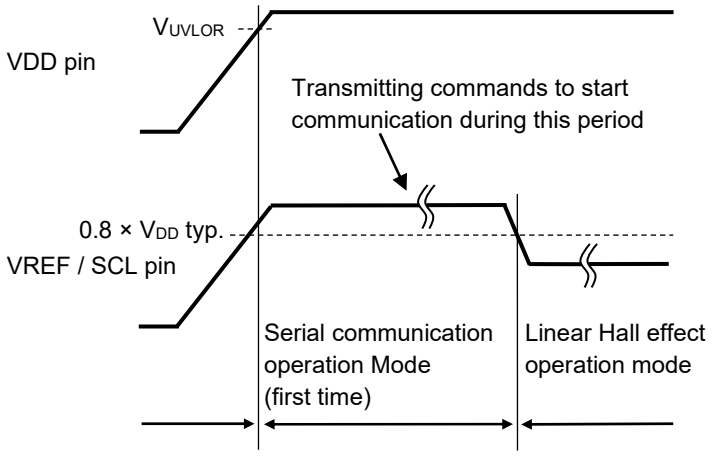


Figure 14

1. 2. 3 Re-entering serial communication operation mode when entering a keyword

Figure 15 shows how to re-enter serial communication operation mode when a keyword is entered.
When this IC is initially in serial communication mode, writing a specified code to the keyword register makes it possible to re-enter serial communication mode without having to cycle the power supply voltage. The serial communication operation mode can be re-entered by setting the VREF / SCL pin voltage higher than 0.8 × V_{DD} typ.

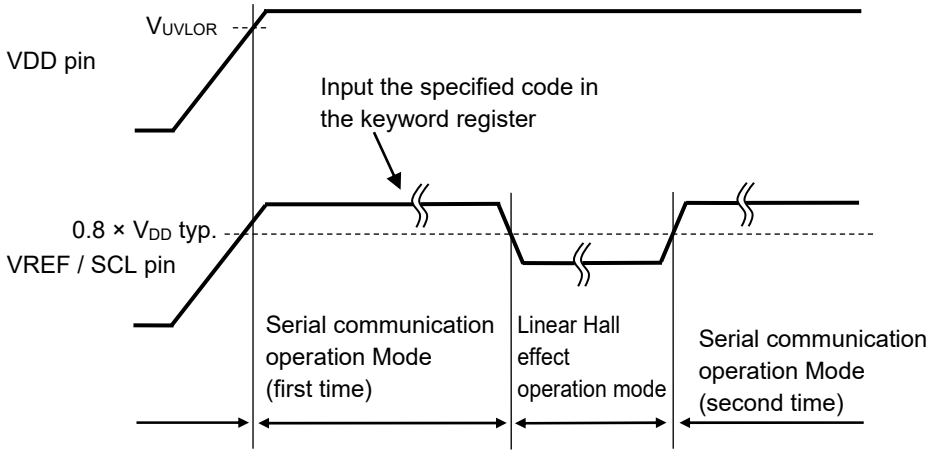


Figure 15

1. 2. 4 Timeout function

This IC has a timeout function from the serial communication operation mode.
In serial communication operation mode, when a start condition is input, if the VREF / SCL pin voltage is below 0.8 × V_{DD} typ. for 1 ms typ. or more, this IC leaves the serial communication operation mode and enters the linear Hall effect sensor operation mode.
If the above timeout occurs before or during a write to the keyword register, the power supply voltage must be restarted in order to re-enter serial communications operation mode.

2. Linear Hall effect sensor operation

2. 1 Direction of applied magnetic flux

This IC outputs a voltage according to the magnetic flux density perpendicular to the marking surface.

Figure 16 shows direction in which magnetic flux is being applied.
When the magnetic field lines pass from the bottom to the top of the IC, in other words, when the south pole is brought close from the top, the direction is considered to be positive.

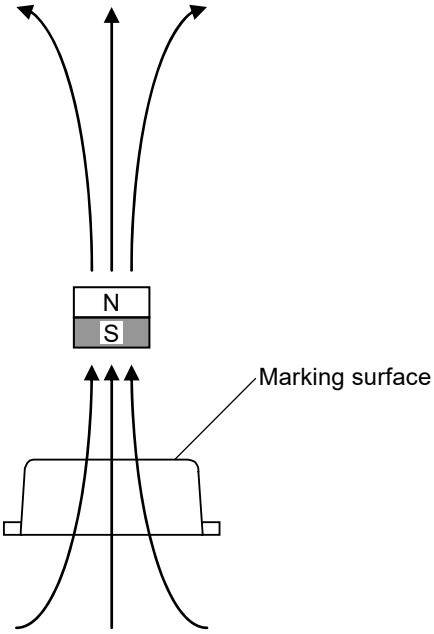


Figure 16

2. 2 Position of Hall sensor

Figure 17 shows the position of Hall sensor.
The Hall sensor is located in the area indicated by the dotted line in the center of the package.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

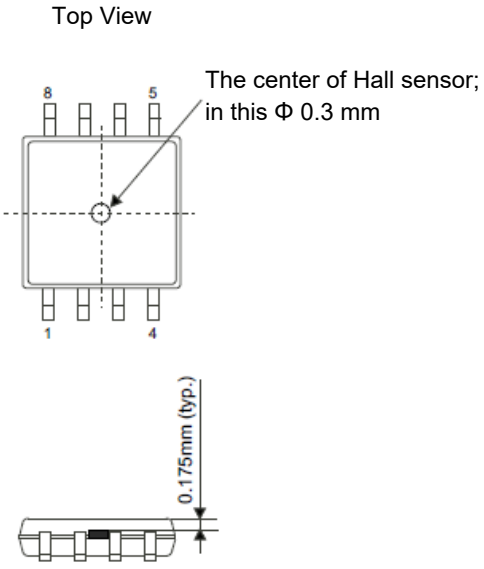


Figure 17

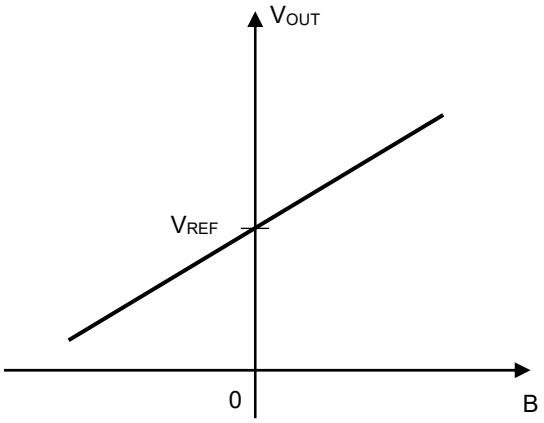
2. 3 Output voltage characteristics

This IC outputs an analog signal voltage that is proportional to the magnetic flux density based on the reference voltage output (V_{REF}).
The analog signal voltage is determined by the magnetic flux density (B) and sensitivity (S), and can be expressed by the following equation when the output offset voltage (V_{OFF}) is 0 mV. The ± sign in the formula changes depending on the output signal polarity.

$$V_{OUT}\ [V] = \pm(B \times S) + V_{REF}$$

Figure 18 shows the output voltage characteristics.
When magnetic flux density (B) = 0, $V_{OUT} = V_{REF}$. When the output signal polarity is positive, increasing the magnetic flux density (B) in the + direction causes V_{OUT} to increase with V_{REF} as the reference. When the output signal polarity is reversed, increasing the magnetic flux density (B) in the + direction causes V_{OUT} to decrease with V_{REF} as the reference.
The output signal polarity can be changed using the built-in non-volatile memory.

(1) Positive polarity



(2) Reverse polarity

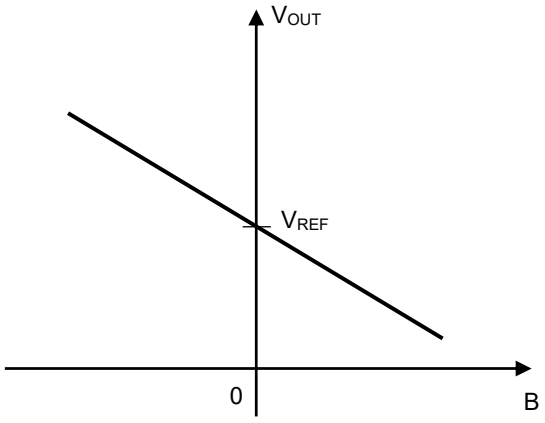


Figure 18

2. 4 Sensitivity

Figure 19 shows the relationship between the magnetic flux density (B) and output voltage (V_{OUT}). Sensitivity (S) is the slope of the output voltage (V_{OUT}) versus the magnetic flux density (B). The Sensitivity is calculated by the following formula from the output voltage = V_{OUT1} when the magnetic flux density = B_1 and the output voltage = V_{OUT2} when the magnetic flux density = B_2.

$$S\ [V/T] = (V_{OUT1} - V_{OUT2}) \div (B_1 - B_2)$$

The Sensitivity (S) can be adjusted by trimming using the built-in non-volatile memory.

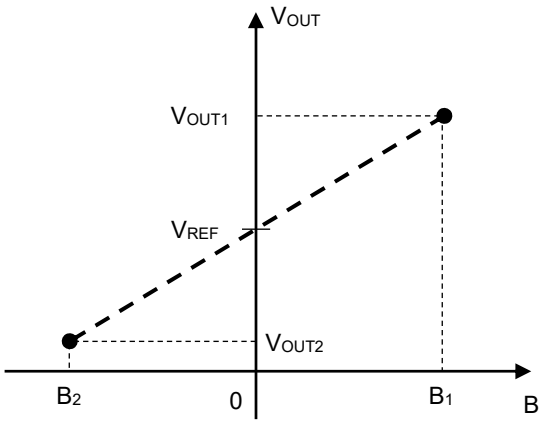


Figure 19

Remark Positive polarity

2. 5 Sensitivity thermal drift

Figure 20 shows the temperature dependency in the sensitivity.
The sensitivity thermal drift (TCS) is the slope of the line connecting the sensitivity (S_{TLOW}) at low temperature (T_{LOW}, Ta = -40°C) and the sensitivity (S_{THIGH}) at high temperature (T_{HIGH}, Ta = +125°C or T_j = +150°C). If the sensitivity at Ta = +25°C is S_{T25}, it is calculated using the following formula.

$$TCS\ [ppm/°C] = (S_{THIGH} - S_{TLOW}) \div S_{T25} \div (T_{HIGH} - T_{LOW}) \times 10^6$$

The TCS can be trimmed using the built-in non-volatile memory.

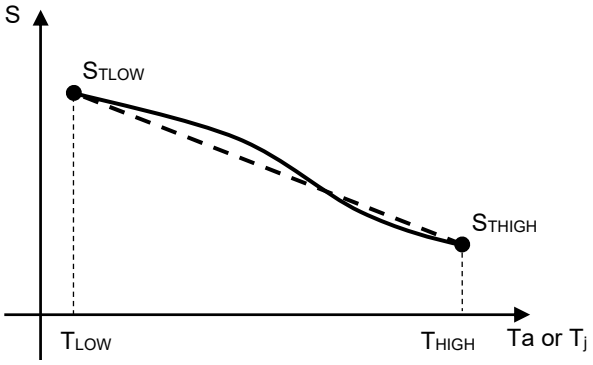


Figure 20

2. 6 Maximum magnetic flux density

Figure 21 shows the relationship between the magnetic flux density (B) and the output voltage (V_{OUT}).
The maximum magnetic flux density (B_{MAX}) is the minimum magnetic flux density at which the output voltage (V_{OUT}) reaches V_{DD} - 0.15 V or 0.15 V at the set sensitivity (S). When the output offset voltage (V_{OFF}) is 0 mV, it is calculated using the following formula.

$$B_{MAX}\ [mT] = \text{min. } \{ (V_{DD} - 0.15 - V_{REF}) \div S, (V_{REF} - 0.15) \div S \}$$

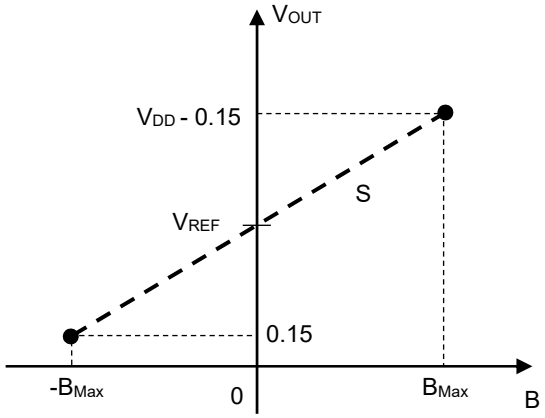


Figure 21

Remark Positive polarity

2. 7 Sensitivity linearity error

Figure 22 shows an explanatory diagram of sensitivity linearity error (LIN).
LIN is the error between the actual output voltage and the straight line that connects the output voltage (V_{OUTP}) when magnetic flux density = $+B_{LIN}$ and the output voltage (V_{OUTM}) when magnetic flux density = $-B_{LIN}$. When the output offset voltage (V_{OFF}) is 0 mV, it is calculated using the following formula.

$$LIN\ [\%] = \Delta V_{OUTX} \div (V_{OUTP} - V_{OUTM}) \times 100$$

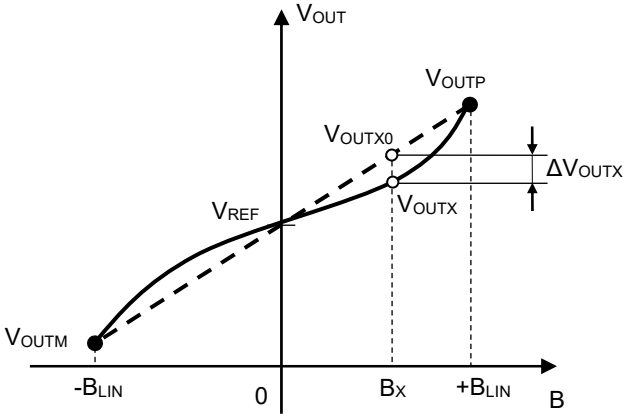


Figure 22

Remark Positive polarity

2. 8 Output offset voltage

Figure 23 shows an explanatory diagram of the output offset voltage (V_{OFF}).
The output voltage when magnetic flux density (B) = 0 mT is V_{OUT0}. Ideally, V_{OUT0} will match the reference voltage output (V_{REF}), but in reality a voltage error occurs. This voltage error is called the output offset voltage (V_{OFF}). V_{OFF} is calculated by the following formula.

$$V_{OFF} = V_{OUT0} - V_{REF}$$

The output offset voltage (V_{OFF}) can be adjusted by trimming using the built-in non-volatile memory.

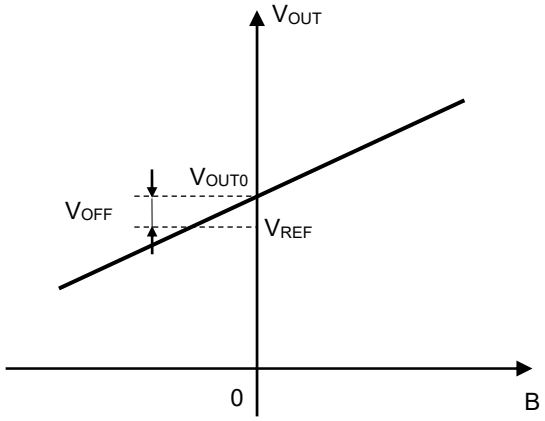


Figure 23

Remark Positive polarity

2. 9 Output offset voltage thermal drift

Figure 24 shows the temperature dependency in the output offset voltage.
The output offset voltage thermal drift (T_{CVOFF}) is the slope of the line connecting the output offset voltage (V_{OFF_TLOW}) at low temperature (T_{LOW}, Ta = -40°C) and the output offset voltage (V_{OFF_THIGH}) at high temperature (T_{HIGH}, Ta = +125°C or T_j = +150°C).
T_{CVOFF} is calculated by the following formula.

$$T_{CVOFF}\ [mV/°C] = (V_{OFF\_THIGH} - V_{OFF\_TLOW}) \div (T_{HIGH} - T_{LOW})$$

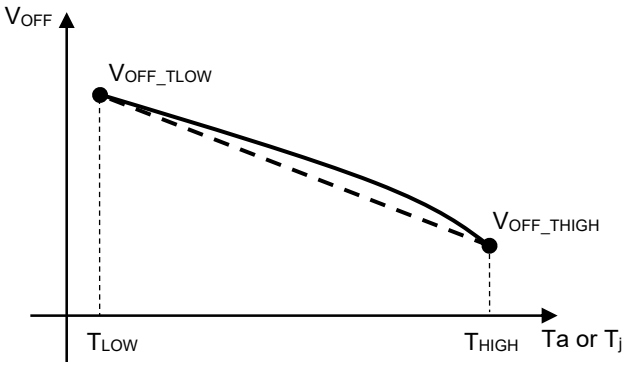


Figure 24

2. 10 Reference voltage thermal drift

Figure 25 shows the temperature dependency in the reference voltage.
The reference voltage thermal drift (T_{CVREF}) is the slope of the line connecting the reference voltage (V_{REF_TLOW}) at low temperature (T_{LOW}, Ta = -40°C) and the reference voltage (V_{REF_THIGH}) at high temperature (T_{HIGH}, Ta = +125°C or T_j = +150°C). If the reference voltage at Ta = +25°C is V_{REF_T25}, it is calculated using the following formula.

$$T_{CVREF}\ [ppm/°C] = (V_{REF\_TMAX} - V_{REF\_TLOW}) \div V_{REF\_T25} \div (T_{HIGH} - T_{LOW}) \times 10^6$$

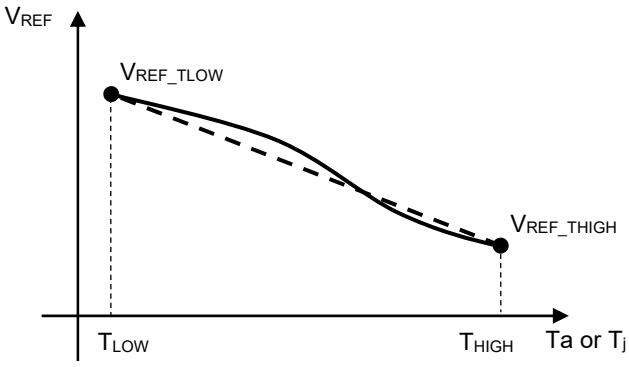


Figure 25

2. 11 Output response

Figure 26 shows the response waveform of the output voltage (V_{OUT}) when the magnetic flux density (B) is raised from 10% to 90% within 1 µs.
In the steady status after a sufficient amount of time has passed since magnetic flux density (B) was applied, the output voltage (V_{OUT}) is B × S + V_{REF}. In this case, the output reaction time (t_{RAC_OUT}) is the time from when the magnetic flux density reaches B × 0.1 to when the output voltage reaches B × S × 0.1 + V_{REF}. The output response time (t_{RSP_OUT}) is the time from when the magnetic flux density reaches B × 0.9 to when the output voltage reaches B × S × 0.9 + V_{REF}. The output settling time (t_{SET_OUT}) is the time it takes for the output voltage to settle within B × S × (1 ± 0.03) + V_{REF} after it reaches B × S × 0.1 + V_{REF}.
The rate at which the output voltage rises above the steady status value when it starts up is called the output overshoot (OS). If the maximum output voltage during startup is V_{OUT_MAX}, OS is calculated using the following formula.

$$OS\ [\%] = \{V_{OUT\_MAX} - (B \times S + V_{REF})\} \div (B \times S) \times 100$$

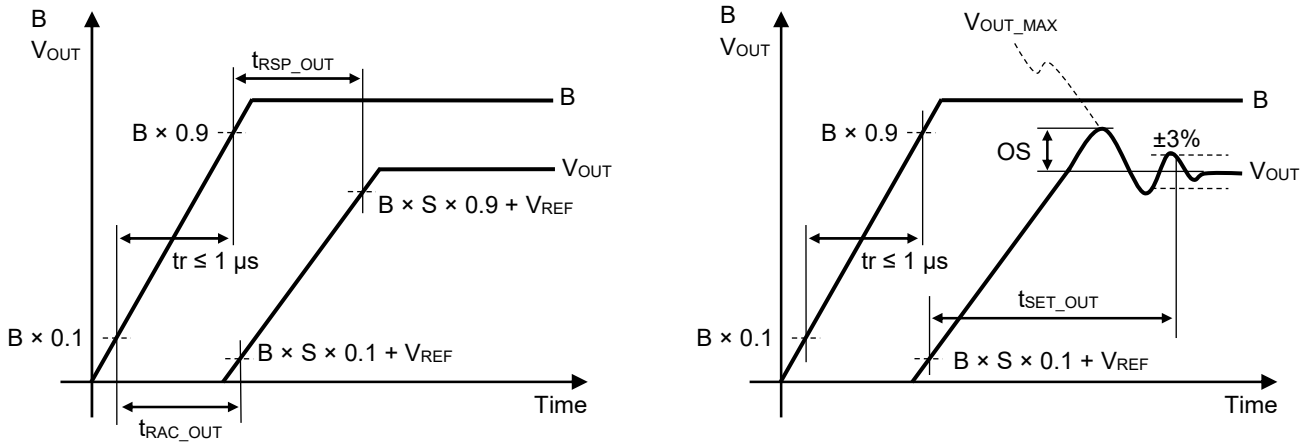


Figure 26

2. 12 Start up time

Figure 27 shows the rising waveform of the output voltage (V_{OUT}) in response to a rise in the power supply voltage.
When the power supply voltage is raised, this IC resets its internal state. At this time, the VOUT pin and VREF pin become high impedance outputs. After that, when the power supply voltage reaches the UVLO release voltage (V_{UVLOR}), the trimming code is read from the built-in non-volatile memory, and the circuit starts operating. When the circuit starts operating, the VOUT pin voltage and VREF pin voltage begin to rise.
In the reference voltage output mode, the start-up time (t_{PON}) is the time from when the power supply voltage reaches V_{DD} min. to when the output voltage reaches V_{REF} × 0.9.

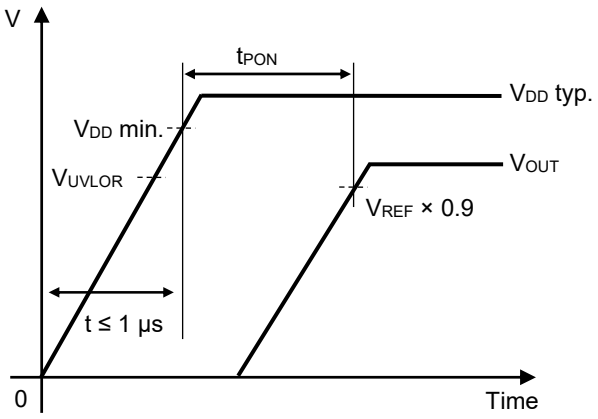


Figure 27

3. Protection function

3. 1 Low power supply voltage detection circuit

This IC has a built-in low power supply voltage detection circuit (UVLO). If the power supply voltage drops below the UVLO detection voltage (V_{UVLOD}) while the linear Hall effect sensor is operating, there will be no change in IC operation as long as the power supply voltage returns to the UVLO release voltage (V_{UVLOR}) or higher in less than 1 ms typ. However, if the power supply voltage falls below V_{UVLOD} for 1 ms typ. or more, the IC stops operating, the VOUT pin becomes a high-impedance output, and the VREF pin becomes V_{SS} (pulled down to V_{SS} by a 10 kΩ resistor). After that, when the power supply voltage returns to V_{UVLOR} or higher, the device goes through the same operations as when the power supply was started and then returns to the normal operating status. However, if the power supply voltage falls below the power-off threshold voltage (V_{POFF}), the IC stops operating regardless of the elapsed time, the VOUT pin becomes a high-impedance output, and the VREF pin becomes V_{SS} (pulled down to V_{SS} by a 10 kΩ resistor). The above operation is the same in both reference voltage output mode and reference voltage input mode (refer to **Table 17** and **Table 18**).

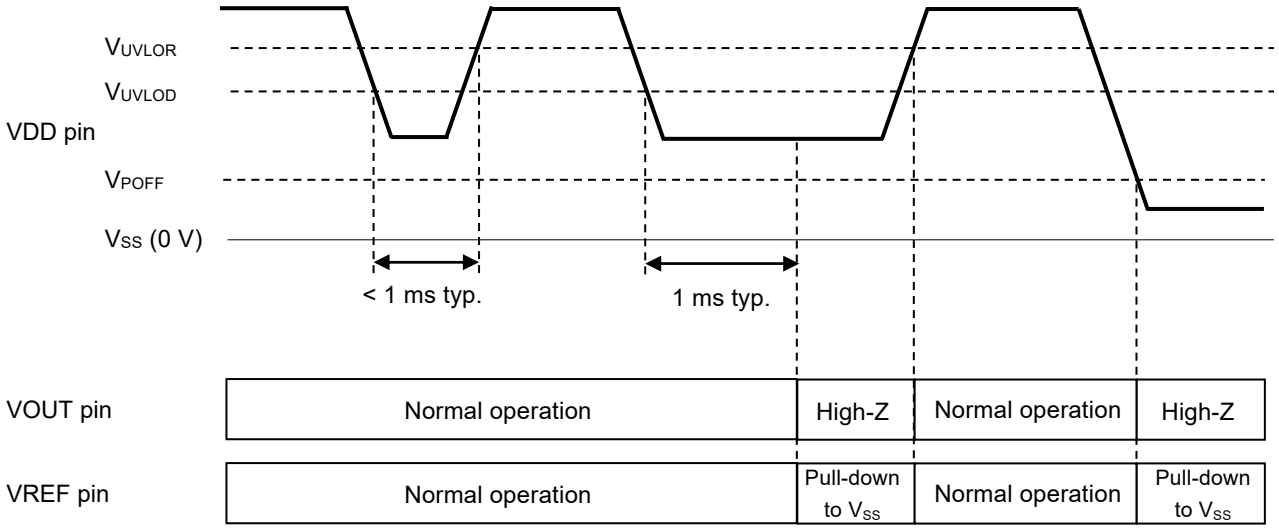


Figure 28 Low Power Supply Voltage Detection

3. 2 Thermal shutdown circuit

This IC has a built-in thermal shutdown circuit to limit overheating. When the junction temperature increases to 170°C typ. during the linear Hall effect sensor IC operation, the thermal shutdown circuit becomes the detection status, and the operation is stopped. When the junction temperature decreases to 155°C typ., the thermal shutdown circuit becomes the release status, and the operation is restarted. If the thermal shutdown circuit detects an overheat, it is necessary to reduce the current output from the VOUT pin or VREF pin, lower the ambient temperature, or improve the heat dissipation of the board on which the IC is mounted. Note that if the thermal shutdown circuit continues to maintain the detection status, physical damage such as product deterioration may occur. The above operation is the same in both reference voltage output mode and reference voltage input mode (refer to **Table 17** and **Table 18**).

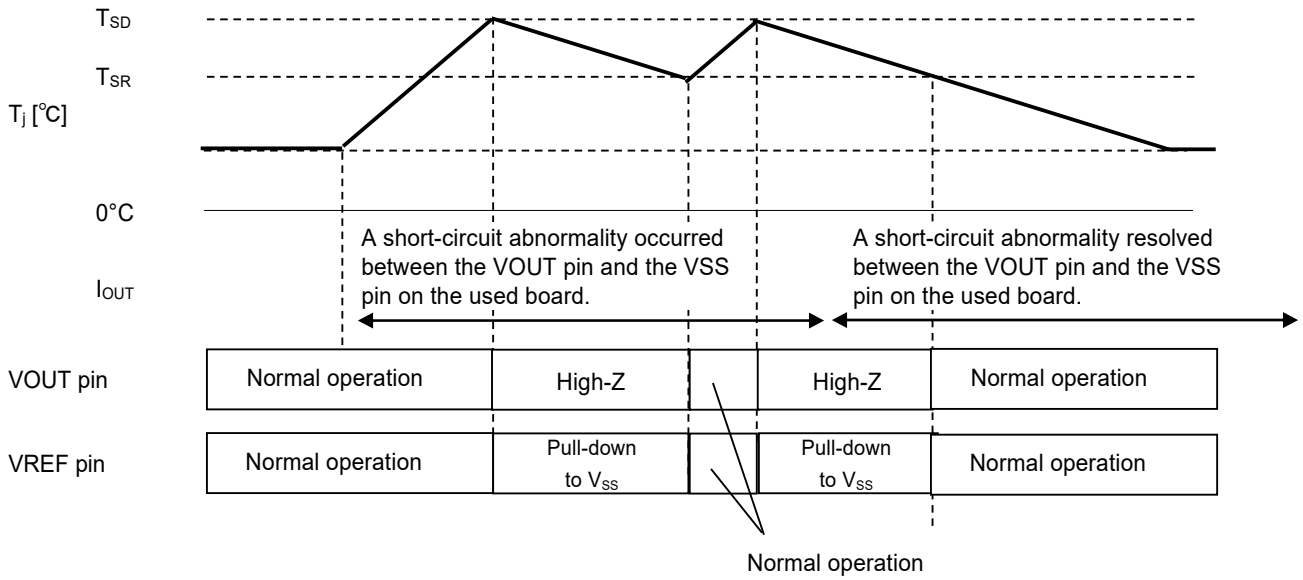


Figure 29 Thermal Shutdown Detection

Table 17 Reference Voltage Output Mode

Pin	Normal Operation	During Low Power Supply Voltage Detection	During Thermal Shutdown Detection	During Serial Communication
VOUT / SDA	Voltage output	High-Z	High-Z	V_{DD} (pull-up 380 Ω typ.)*1
VREF / SCL	Voltage output	V_{SS} (pull-down 10 kΩ typ.)	V_{SS} (pull-down 10 kΩ typ.)	High-Z*1

Table 18 Reference Voltage Input Mode

Pin	Normal Operation	During Low Power Supply Voltage Detection	During Thermal Shutdown Detection	During Serial Communication
VOUT / SDA	Voltage output	High-Z	High-Z	V_{DD} (pull-up 380 Ω typ.)*1
VREF / SCL	High-Z	V_{SS} (pull-down 10 kΩ typ.)	V_{SS} (pull-down 10 kΩ typ.)	High-Z*1

***1.** If the low power supply voltage detection (UVLO) status or thermal shutdown status is detected during serial communication operation, the VOUT / SDA pin remains at V_{DD} (pull-up 380 Ω typ.), and the VREF / SCL pin remains at high impedance.

Caution If the heat dissipation of the application is not good, self-heating cannot be restricted immediately, and the IC may be destroyed. The actual application should be evaluated carefully to verify that there is no problem.

4. Serial communication operation

When this IC is turned on in serial communication operation mode, it is possible to switch IC functions and adjust trimming by programming the built-in non-volatile memory via the 2-wire serial interface.

4. 1 Start condition

Start is identified by a "H" to "L" transition of the SDA pin while the SCL pin is stable at "H". Every operation begins from a start condition.

4. 2 Stop condition

Stop is identified by a "L" to "H" transition of the SDA pin while the SCL pin is stable at "H".
If a stop condition is received during a read sequence, the read operation is aborted and communication ends.
If a stop condition is received during a write sequence, the input of write data is ended.

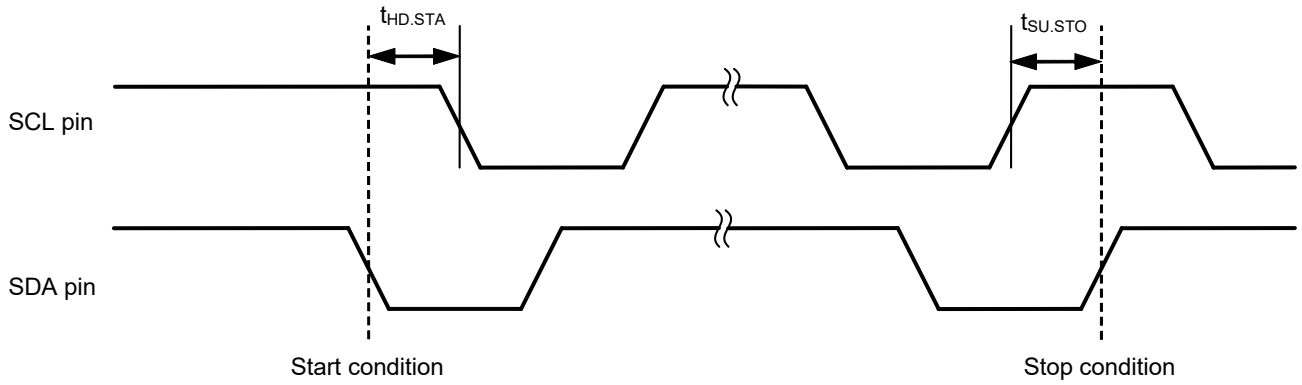


Figure 30 Start / Stop Conditions

4. 3 Data transmission

Changing the SDA pin while the SCL pin is "L", data is transmitted.
Changing the SDA pin while the SCL pin is "H", a start or stop condition is recognized.

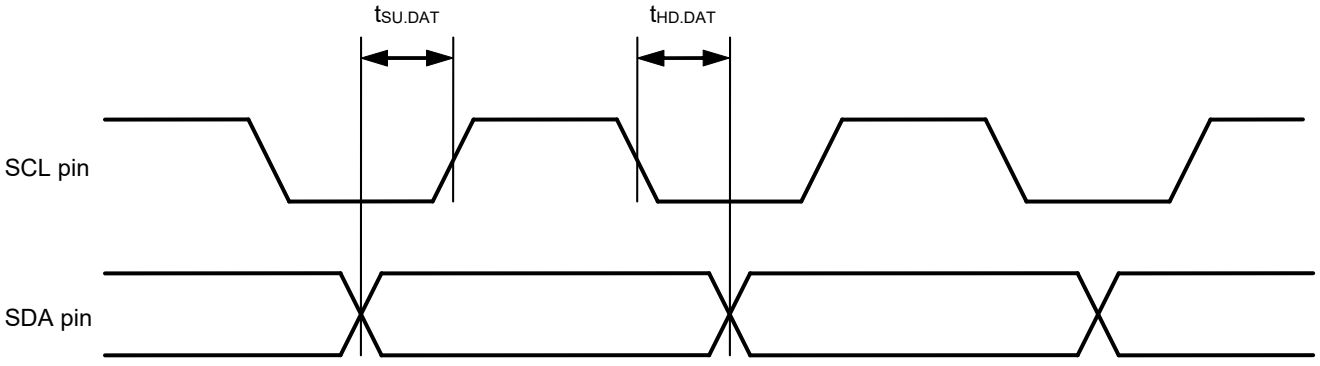


Figure 31 Data Transmission Timing

4. 4 Acknowledge

The unit of data transmission is 8 bits. Subsequently, during the 9th clock cycle, the slave device on the system bus receiving the data sets the SDA pin to “L” and returns acknowledge that it has received the data.

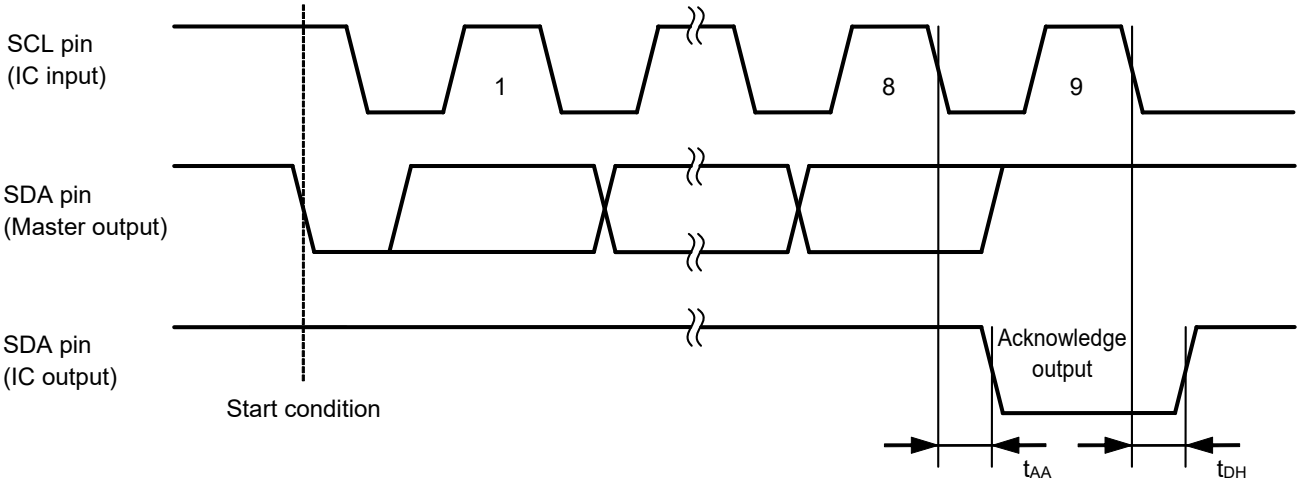


Figure 32 Acknowledge Output Timing

4. 5 Device addressing

To start communication, the master device on the system generates a start condition to the slave device. Next, the master device sends 7-bit device address and a 1-bit read / write instruction code on to the SDA bus.

The higher 7 bits of the device address are the "Device Code", and are fixed to "1100 000 b".
The lower 1 bit of the device address is called the "Read / Write Instruction Code", "0 b" indicates a write operation and "1 b" indicates a read operation.

If the device address sent from the master matches, this IC returns an acknowledge during the 9th clock cycle.

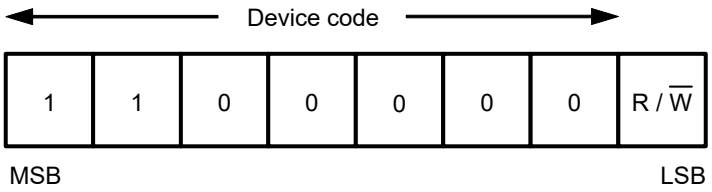


Figure 33 Device Address

4. 6 Write

4. 6. 1 Byte write

When this IC receives a 7-bit device address and a read / write instruction code set to "0", following a start condition, this IC generates an acknowledge.
This IC then receives an 8-bit pointer and responds with an acknowledge. After this IC receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the address specified by the pointer.
During the write cycle all operations are forbidden and no acknowledge is generated.

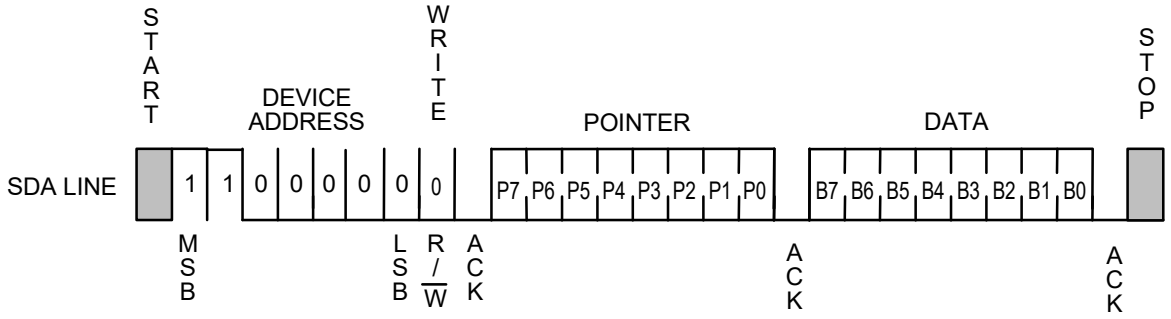


Figure 34 Byte Write

4. 6. 2 Multi-byte write

Its basic process to transmit data is as same as byte write, but it operates multi-byte write by sequentially receiving 8-bit write data.
When this IC receives a 7-bit device address and a read / write instruction code set to "0", following a start condition, it generates an acknowledge.
This IC then receives an 8-bit pointer and responds with an acknowledge. After this IC receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data, and generates an acknowledge. This IC repeats reception of 8-bit write data and generation of acknowledge in succession.
The contents of the address counter inside this IC are incremented by 1 from the address specified by the pointer each time 8-bit write data is received. If the address specified by the pointer is 0x00-0x1E, it will increment by 1 and wrap around to 0x00 when it reaches 0x1E.
Finally, when a stop condition is received, the write operation of the write data starting from the address specified by the pointer begins.

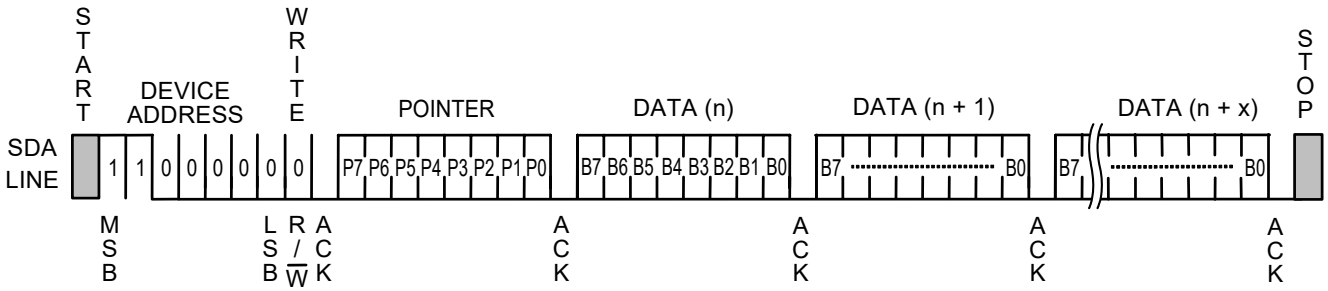


Figure 35 Multi-byte Write

4. 7 Read

4. 7. 1 Current address read

Either in writing or in reading this IC holds the address last specified by the pointer. The address is maintained when the instruction transmission is not interrupted, and the address is maintained as long as the power voltage does not decrease less than the operating voltage. Therefore, if the master device recognizes the address value of this IC, it can read data from the current address value without specifying the address. This is called "Current Address Read".
In the following the address counter in this IC is assumed to be "n".
When this IC receives a 7-bit device address and a read / write instruction code set to "1" following a start condition, it responds with an acknowledge. Next an 8-bit data at the address "n" is sent from this IC synchronous to the SCL clock. The address counter is incremented and the content of the address counter becomes n + 1. The master device outputs stop condition not an acknowledge, the reading of this IC is ended.

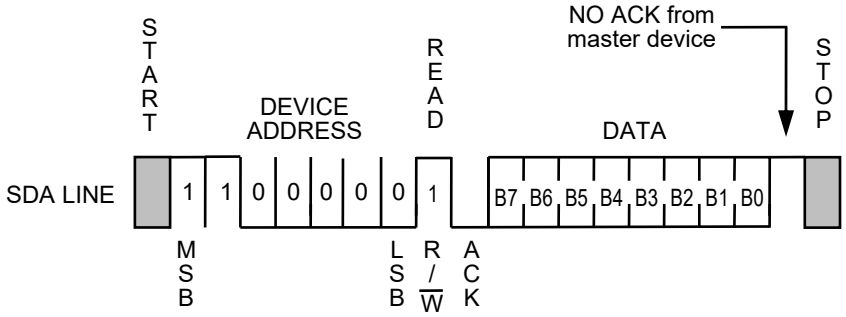


Figure 36 Current Address Read

4. 7. 2 Random read

Random read is used to read the data at an arbitrary memory address.
A dummy write is performed to load the address into the address counter.
When this IC receives a 7-bit device address and a read / write instruction code set to "0" following a start condition, it responds with an acknowledge. This IC then receives an 8-bit pointer byte and responds with an acknowledge. The address is loaded to the address counter in this IC by these operations.
Reception of write data does not follow in a dummy write whereas reception of write data follows in write.
Since the address is loaded into the address counter by dummy write, the master device can read the data starting from the arbitrary address by transmitting a new start condition and performing the same operation in the current address read. That is, when this IC receives a 7-bit device address and a read / write instruction code set to "1", following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from this IC in synchronous to the SCL clock.
The master device outputs stop condition not an acknowledge, the reading of this IC is ended.

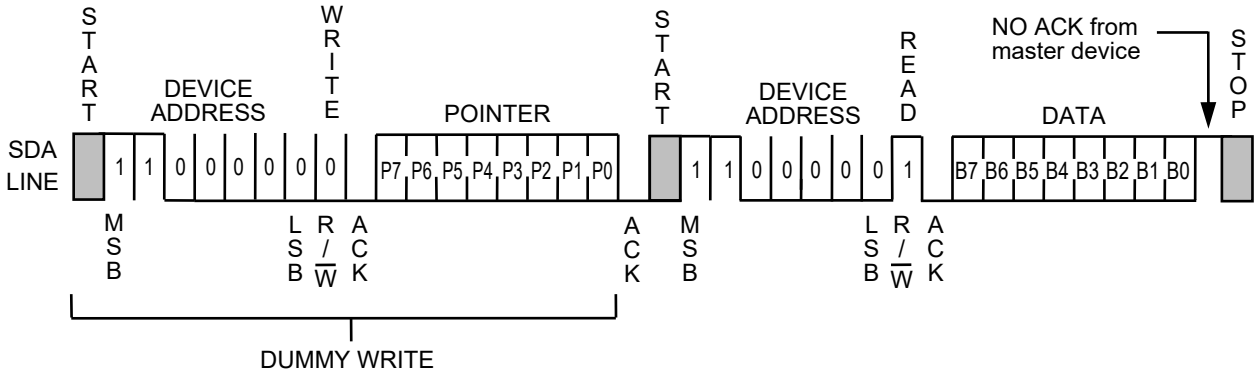


Figure 37 Random Read

4. 7. 3 Sequential read

When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition both in current address read and random read, it responds with an acknowledge.
When an 8-bit data is output from this IC synchronous to the SCL clock, the address counter is automatically incremented.
When the master device responds with an acknowledge, the data at the next address is transmitted. Response with an acknowledge by the master device has the address counter in this IC incremented and makes it possible to read data in succession. If the address specified by the pointer is 0x00-0x1E, it is incremented, and when it reaches 0x1E, it returns to 0x00. If the address specified by the pointer is between 0x40 and 0x5E, it will be incremented, and when it reaches 0x5E it will return to 0x40.
The master device outputs stop condition not an acknowledge, the reading of this IC is ended.

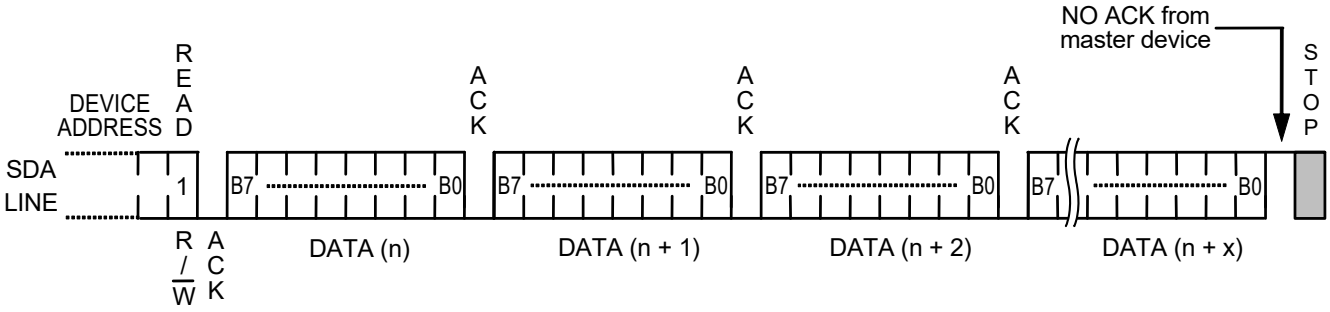


Figure 38 Sequential Read

■ Usage

1. A pull-up resistor to SDA pin and SCL pin

The SDA pin has a built-in pull-up resistor, so there is no need to pull it up.
The SCL pin do not have a built-in pull-up resistor. In case that the SCL pin of this IC is connected to the Nch open-drain output pin of the master device, connect the SCL pin with a pull-up resistor. As well, in case the SCL pin of this IC is connected to the tri-state output pin of the master device, connect the SCL pin with a pull-up resistor in order not to set it in "High-Z". This prevents this IC from error caused by an uncertain output (High-Z) from the tri-state pin when resetting the master device during the voltage drop. Remove this pull-up resistor in linear Hall effect sensor operation mode.

2. Equivalent circuits of SCL pin and SDA pin

The equivalent circuit of the SCL pin and SDA pin of this IC is shown below.

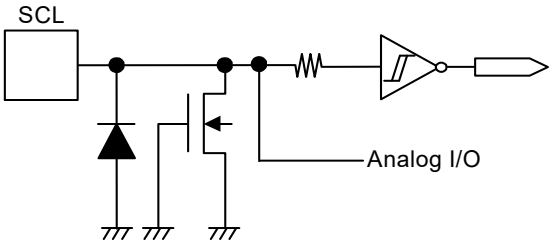


Figure 39 SCL Pin

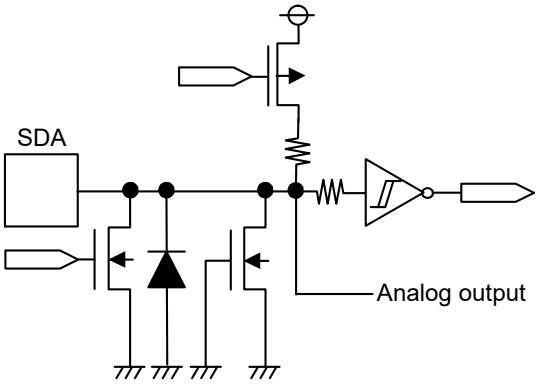


Figure 40 SDA Pin

3. Acknowledge check

This IC has an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the master device and this IC. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check with the master device.

4. SDA pin and SCL pin noise suppression time

This IC includes a built-in low-pass filter at the SDA pin and the SCL pin to suppress noise, and it can remove noise with a pulse width of 50 ns typ. or less.

5. Operation when input stop condition during input write data

If a stop condition is input to this IC while write data is being input, that data will become invalid because no ACK has been returned with that data input. However, in the case of a multi-byte write, if there is data input for which an ACK has been returned for one or more addresses, that data input will be valid.
Refer to **Figure 41** regarding details.

Since a write operation is executed immediately after the stop condition is input, new write data input is invalid for a maximum of 13 ms.

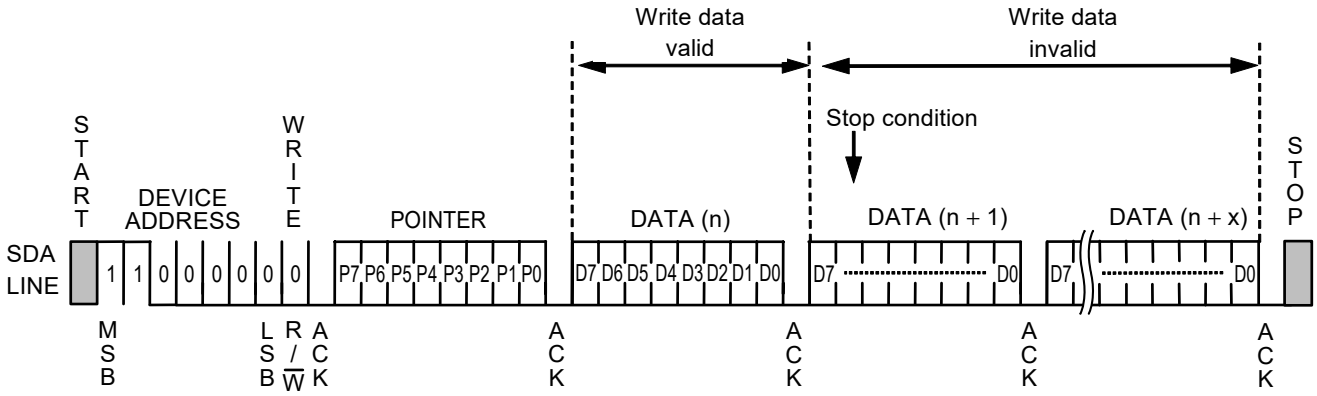


Figure 41 Write Operation by Inputting Stop Condition during Write

6. Operation when input start condition during input write data

When a start condition is input while inputting write data, this IC operates in the same way as when a stop condition is input while inputting write data. In this case it is treated as a restart.

■ Register

1. Register mapping

The register mapping of this IC is shown in **Table 19**.

Table 19 Register Mapping

Address	R/W	Function	Data [7:0]							
			B7	B6	B5	B4	B3	B2	B1	B0
00 h to 08 h	R/W	A: Holding equipment number, manufacturing date, etc.	A							
09 h to 0B h	R	B: Output offset voltage thermal drift adjustment data (Output voltage characteristics: positive polarity)	B							
0C h to 0E h	R	B: Output offset voltage thermal drift adjustment data (Output voltage characteristics: reverse polarity)								
0F h	R	C: Sensitivity thermal drift programming step correction data	C							
10 h	R/W	D: Output offset voltage adjustment	D							
11 h	R/W	E: Coarse sensitivity adjustment	-	-	-	E				
12 h	R/W	E: Coarse sensitivity adjustment	-	-	-	-	-	-	-	E
13 h	R/W	F: Thermal shutdown enabled / disabled	-	-	-	-	-	-	-	F
14 h	R/W	G: Fine adjustment of sensitivity	G							
15 h	R/W	H: Output signal polarity selection I: Sensitivity thermal drift adjustment	-	I						H
16 h	R/W	J: Reference voltage output selection K: Reference voltage output mode / input mode selection	-	-	-	J	K	-	J	
17 h	R/W	L: Fine adjustment of reference voltage output	-	-	L					
19 h	R/W	M: Output offset voltage thermal drift adjustment D: Output offset voltage adjustment	D		-	M				
1A h	R/W	G: Fine adjustment of sensitivity N: Frequency bandwidth selection	N		-	-	-	G		
1F h	R/W	O: Write protect enabled / disabled	-	-	-	-	-	-	-	O
CF h	W	P: Keyword register	P							

Remark -: Don't care

2. Configuration of registers

2. 1 Keyword register

Register access can be enabled or disabled by entering a specified code in the keyword register.
After entering serial communication operation mode, this IC's registers can be accessed by writing "1100 1101 b" to the keyword register.
When using the write protect function, enter "0101 1110 b" instead of the above keywords. For details about the write protection, refer to "**2. 9 Write protect enabled / disabled (WP)**".

Table 20 Keyword Register

Address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
CF h	W	Keyword register							

CF h								Keyword Register
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	0	0	1	1	0	1	Register access valid (addresses other than "1F h" can be accessed)
0	1	0	1	1	1	1	0	When write protect function is used, register access is enabled (only address "1F h" can be accessed)

Remark 1. Initial settings at shipment: 0000 0000 b (register access invalid)
2. Address "CF h" is volatile memory.

2. 2 Product information

This is an area where product-specific information such as the equipment number and manufacturing date can be stored.

Table 21 Product Information

Address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
00 h	R/W	Holding equipment number, manufacturing date, etc.							
01 h	R/W								
02 h	R/W								
03 h	R/W								
04 h	R/W								
05 h	R/W								
06 h	R/W								
07 h	R/W								
08 h	R/W								

Remark Initial settings at shipment: 0000 0000 b

2. 3 Trimming adjustment data

This is the area to store information required for adjusting the sensitivity thermal characteristics and the output offset voltage thermal drift.

Table 22 Trimming Adjustment Data

Address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
09 h	R	Output offset voltage thermal drift adjustment data (output voltage characteristics: positive polarity)							
0A h	R								
0B h	R								
0C h	R	Output offset voltage thermal drift adjustment data (output voltage characteristics: reverse polarity)							
0D h	R								
0E h	R								
0F h	R	Sensitivity thermal drift programming step correction data							

Remark Initial settings at shipment: optimal trimming adjustment code is written before shipping

2. 4 Adjustment of magnetic characteristics

Used to select sensitivity, sensitivity thermal drift, and output voltage polarity.

Table 23 Magnetic Characteristics Adjustment

Address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
11 h	R/W	-	-	-	SENSE_COARSE				
12 h	R/W	-	-	-	-	-	-	-	SENSE_ COARSE
14 h	R/W	SENSE_FINE							
15 h	R/W	-	SENSE_TC						SENSE_ REV
1A h	R/W	FBW_SEL*1		-	-	-	-	SENSE_FINE	

***1.** Refer to "**2. 7 Frequency bandwidth selection (FBW_SEL)**".

Remark -: Don't care

2. 4. 1 Coarse adjustment of sensitivity (SENSE_COARSE)

Coarsely adjust the sensitivity by changing SENSE_COARSE.

Table 24 Sensitivity Coarse Adjustment

11 h								12 h								Sensitivity Coarse Adjustment (Typ.)
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0	
-	-	-	0	0	0	0	0	-	-	-	-	-	-	-	0	5600 times (75 dB)
-	-	-	0	0	0	0	0	-	-	-	-	-	-	-	1	2800 times (69 dB)
-	-	-	0	0	1	0	0	-	-	-	-	-	-	-	1	1400 times (63 dB)
-	-	-	0	0	1	1	0	-	-	-	-	-	-	-	1	700 times (57 dB)
-	-	-	0	0	1	1	1	-	-	-	-	-	-	-	1	350 times (51 dB)
-	-	-	1	0	1	1	1	-	-	-	-	-	-	-	1	175 times (45 dB)
-	-	-	1	1	1	1	1	-	-	-	-	-	-	-	1	87.5 times (39 dB)

Remark 1. Initial settings at shipment: 0000 0000 b (address "11 h"), 0000 0001 b (address "12 h")
2. -: Don't care

2. 4. 2 Fine adjustment of sensitivity (SENSE_FINE)

Fine tune the sensitivity by changing SENSE_FINE.

Table 25 Sensitivity Fine Adjustment

1A h								14 h								Correction Value	Sensitivity Fine Adjustment (Typ.)
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0		
		-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0.00%
		-	-	-	-	0	0	0	0	0	0	0	0	0	1	-1	-0.08%
		-	-	-	-	0	0	0	0	0	0	0	0	1	0	-2	-0.16%
	*1	-	-	-	-	0	0	0	0	0	0	0	0	1	1	-3	-0.24%
		. . .						. . .								. . .	. . .
		-	-	-	-	1	1	1	1	1	1	1	1	1	0	-1022	. . .
		-	-	-	-	1	1	1	1	1	1	1	1	1	1	-1023	. . .

***1.** Refer to "**2. 7 Frequency bandwidth selection (FBW_SEL)**".

Remark 1. Initial settings at shipment: optimal trimming adjustment code is written before shipping
2. -: Don't care

2. 4. 3 Output signal polarity selection (SENSE_REV)

Select the output voltage polarity by changing SENSE_REV.

Table 26 Output Voltage Polarity Selection

15 h								Output Voltage Polarity
B7	B6	B5	B4	B3	B2	B1	B0	
-	***1**						0	Positive polarity
-							1	Reverse polarity

***1.** Refer to "**2. 4. 4 Adjustment of sensitivity thermal drift (SENSE_TC)**".

Remark 1. Initial settings at shipment: 0000 0000 b
2. -: Don't care

2. 4. 4 Adjustment of sensitivity thermal drift (SENSE_TC)

Adjust the sensitivity thermal drift by changing SENSE_TC.

Table 27 Sensitivity Thermal Drift Adjustment

15 h								Correction Value	Sensitivity Thermal Drift (Typ.)
B7	B6	B5	B4	B3	B2	B1	B0		
-	0	1	1	1	1	1	***1**	-31	· · ·
-	0	1	1	1	1	0		-30	· · ·
· · ·								· · ·	· · ·
-	0	0	0	0	1	1		-3	-75 ppm/°C
-	0	0	0	0	1	0		-2	-50 ppm/°C
-	0	0	0	0	0	1		-1	-25 ppm/°C
-	0	0	0	0	0	0	***1**	0	0 ppm/°C
-	1	0	0	0	0	1		+1	+25 ppm/°C
-	1	0	0	0	1	0		+2	+50 ppm/°C
-	1	0	0	0	1	1		+3	+75 ppm/°C
· · ·								· · ·	· · ·
-	1	1	1	1	1	0	***1**	+30	· · ·
-	1	1	1	1	1	1		+31	· · ·

***1.** Refer to "**2. 4. 3 Output signal polarity selection (SENSE_REV)**".

Remark 1. Initial settings at shipment: 0000 0000 b
2. -: Don't care

2. 5 Adjustment of output voltage characteristics

Used to adjust the output offset voltage, enable / disable the output offset voltage adjustment range change function, and the output offset voltage temperature characteristics.

Table 28 Output Voltage Characteristics Adjustment

Address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
10 h	R/W	VOUT_OFF							
19 h	R/W	VOUT_OFF		-	VOUT_OFF_TC*1				

***1.** Used to adjust the output offset voltage thermal drift. Contact our sales representatives for details.

Remark -: Don't care

2. 5. 1 Output offset voltage adjustment (VOUT_OFF)

Adjust the output offset voltage by changing VOUT_OFF.

Table 29 Output Offset Voltage Adjustment

10 h								19 h								Correction Value	Output Offset Voltage Adjustment (Typ.)
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0		
0	1	1	1	1	1	1	1	1	*1	-	*2					+255	Setting inhibited
0	1	1	1	1	1	1	1	0		-						+254	· · ·
0	1	1	1	1	1	1	0	1		-						+253	· · ·
0	1	1	1	1	1	1	0	0		-						+252	· · ·
· · ·								· · ·								· · ·	· · ·
0	0	0	0	0	0	0	1	1	*1	-	*2					+3	+1.8 mV
0	0	0	0	0	0	0	1	0		-						+2	+1.2 mV
0	0	0	0	0	0	0	0	1		-						+1	+0.6 mV
0	0	0	0	0	0	0	0	0		-						0	0.0 mV
1	1	1	1	1	1	1	1	1		-						-1	-0.6 mV
1	1	1	1	1	1	1	1	0		-						-2	-1.2 mV
1	1	1	1	1	1	1	0	1		-						-3	-1.8 mV
· · ·								· · ·								· · ·	· · ·
1	0	0	0	0	0	1	0	0	*1	-	*2					-252	· · ·
1	0	0	0	0	0	0	1	1		-						-253	· · ·
1	0	0	0	0	0	0	1	0		-						-254	· · ·

***1.** Refer to "**Table 30 Expanding Output Offset Voltage Adjustment Range**".
***2.** Refer to **Table 28**.

Remark 1. Initial settings at shipment: optimal trimming adjustment code is written before shipping
2. -: Don't care

The output offset voltage adjustment range can be expanded more widely.

Table 30 Expanding Output Offset Voltage Adjustment Range

19 h								Output Offset Voltage Adjustment Range Expansion
B7	B6	B5	B4	B3	B2	B1	B0	
*1	0	-	*2					Adjustment range expansion off
	1	-						Adjustment range expansion on

***1.** Refer to "**Table 29 Output Offset Voltage Adjustment**".
***2.** Refer to **Table 28**.

Remark 1. Initial settings at shipment: B6 = 0
2. -: Don't care

2. 6 Adjustment of reference voltage characteristics

Used to select the reference voltage, select the reference voltage output mode / input mode, and fine-tune the reference voltage.

Table 31 Adjustment of Reference Voltage Characteristics

Address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
16 h	R/W	-	-	-	VREF_SEL	VREF_EXT	-	VREF_SEL	
17 h	R/W	-	-	VREF_FINE					

Remark -: Don't care

2. 6. 1 Selection of reference voltage output mode / input mode (VREF_EXT)

By changing VREF_EXT, the reference voltage output mode and reference voltage input mode can be selected.

Table 32 Reference Voltage Output Mode and Reference Voltage Input Mode Selection

16 h								Reference Voltage Mode
B7	B6	B5	B4	B3	B2	B1	B0	
-	-	-	***1**	0	-	***1**		Reference voltage output mode
-	-	-		1	-			Reference voltage input mode

***1.** Refer to "**2. 6. 2 Reference voltage output selection (VREF_SEL)**".

Remark 1. Initial settings at shipment: 0000 0000 b
2. -: Don't care

2. 6. 2 Reference voltage output selection (VREF_SEL)

In reference voltage output mode, changing VREF_SEL changes the reference voltage output.

Table 33 Reference Voltage Output Selection

16 h								Reference Voltage Output (Typ.)
B7	B6	B5	B4	B3	B2	B1	B0	
-	-	-	0	***1**	-	0	0	2.50 V
-	-	-	0		-	0	1	1.65 V
-	-	-	1		-	1	0	1.50 V
-	-	-	1		-	1	1	0.50 V

***1.** Refer to "**2. 6. 1 Selection of reference voltage output mode / input mode (VREF_EXT)**".

Caution Settings other than those listed above are prohibited.

Remark 1. Initial settings at shipment: 0000 0000 b
2. -: Don't care

2. 6. 3 Fine adjustment of reference voltage output (VREF_FINE)

In reference voltage output mode, changing VREF_FINE fine-tunes the reference voltage output.

Table 34 Fine Adjustment of Reference Voltage Output

17 h								Correction Value	Reference Voltage Output Fine Adjustment (Typ.)			
B7	B6	B5	B4	B3	B2	B1	B0		V_{REF} = 2.50 V	V_{REF} = 1.65 V	V_{REF} = 1.50 V	V_{REF} = 0.50 V
-	-	0	0	0	0	0	0	0	0 mV	0 mV	0 mV	0 mV
-	-	0	0	0	0	0	1	+1	+2.5 mV	+1.7 mV	+1.5 mV	+0.5 mV
-	-	0	0	0	0	1	0	+2	+5.0 mV	+3.3 mV	+3.0 mV	+1.0 mV
-	-	0	0	0	0	1	1	+3	+7.5 mV	+5.0 mV	+4.5 mV	+1.5 mV
. . .								. . .	. . .	. . .	. . .	. . .
-	-	1	1	1	1	0	1	+61	. . .	. . .	. . .	. . .
-	-	1	1	1	1	1	0	+62	. . .	. . .	. . .	. . .
-	-	1	1	1	1	1	1	+63	. . .	. . .	. . .	. . .

Remark 1. Initial settings at shipment: optimal trimming adjustment code is written before shipping
2. -: Don't care

2. 7 Frequency bandwidth selection (FBW_SEL)

Changing FBW_SEL changes the frequency bandwidth.

Table 35 Frequency Bandwidth Selection

Address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
1A h	R/W	FBW_SEL		-	-	-	-	SENSE_FINE*1	

1A h								Frequency Bandwidth (Typ.)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	-	-	-	-	*1		400 kHz
0	1	-	-	-	-			200 kHz
1	0	-	-	-	-			100 kHz

***1.** Refer to "**2. 4. 2 Fine adjustment of sensitivity (SENSE_FINE)**".

Caution Settings other than those listed above are prohibited.

Remark 1. Initial settings at shipment: [B7, B6] = [0, 0]
2. -: Don't care

2. 8 Thermal shutdown available / unavailable (TSD_EN)

Select thermal shutdown available / unavailable by changing TSD_EN.

Table 36 Thermal Shutdown Available / Unavailable Selection

Address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
13 h	R/W	-	-	-	-	-	-	-	TSD_EN

13 h								Thermal Shutdown
B7	B6	B5	B4	B3	B2	B1	B0	
-	-	-	-	-	-	-	0	Unavailable
-	-	-	-	-	-	-	1	Available

Remark 1. Initial settings at shipment: 0000 0001 b
2. -: Don't care

2. 9 Write protect enabled / disabled (WP)

By changing the WP, you can select whether to enable or disable the write protection.
Enabling the write protection prevents accidental storage of data in the built-in non-volatile memory. Therefore, it is used when finalizing the test process, but using this function is not mandatory.
When the write protection is enabled, writing to non-volatile memory is not possible.
The enable / disable of the write protection can be written only when "0101 1110 b" is input to address CF h (refer to "**2. 1 Keyword register**").

Table 37 Write Protect Enable / Disable Selection

Address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
1F h	R/W	-	-	-	-	-	-	-	WP

1F h								Write Protect
B7	B6	B5	B4	B3	B2	B1	B0	
-	-	-	-	-	-	-	0	Disabled
-	-	-	-	-	-	-	1	Enabled

Remark 1. Initial settings at shipment: 0000 0000 b
2. -: Don't care

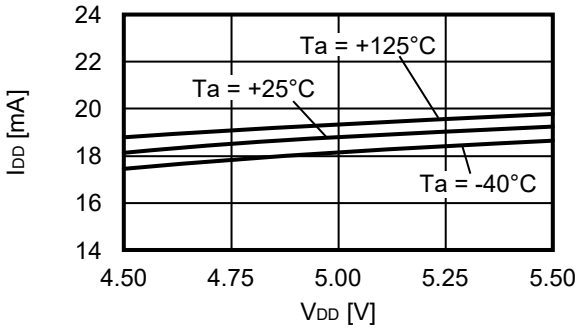
■ Precautions

- Do not operate these ICs in excess of the absolute maximum ratings. Attention should be paid to the power supply voltage, especially. The surge voltage which exceeds the absolute maximum ratings can cause latch-up and malfunction. Perform operations after confirming the detailed operation condition in the data sheet.
- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes. When the IC is used under the environment where the power supply voltage rapidly changes, it is recommended to judge the output voltage of the IC by reading it multiple times.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- The application conditions for the power supply voltage and the output resistor should not exceed the power dissipation.
- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.
- Since the package heat radiation differs according to the conditions of the application, perform thorough evaluation with actual applications to confirm no problems occur.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

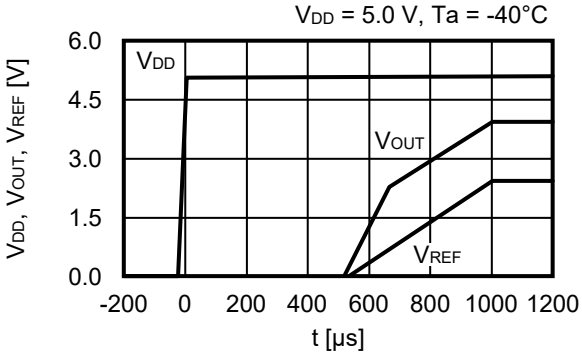
■ Characteristics (Typical Data)

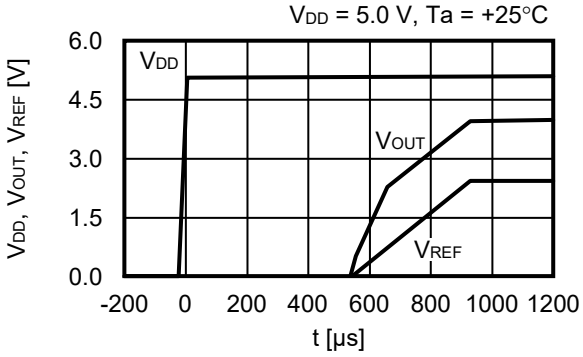
1. Power supply characteristics

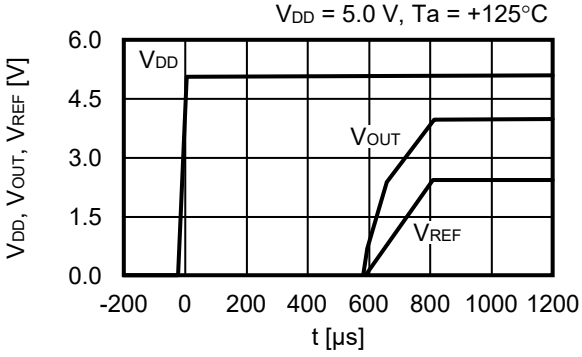
1. 1 Current consumption



1. 2 Start up time

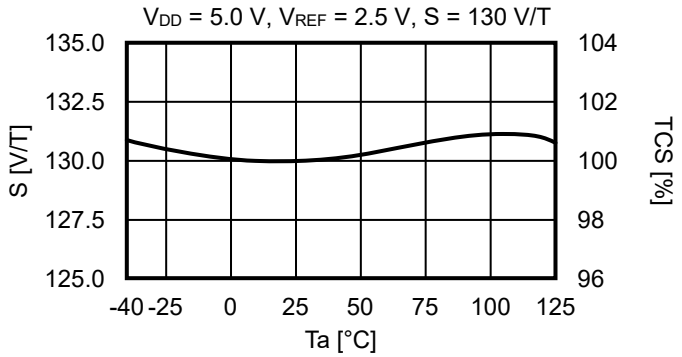




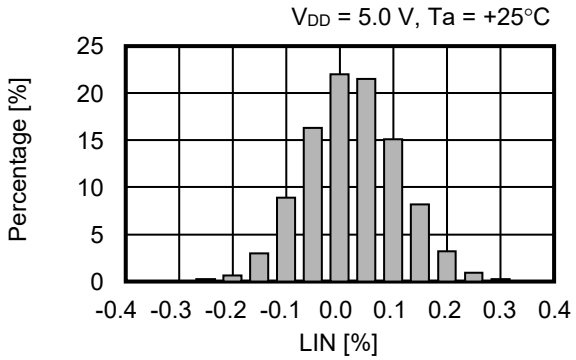


2. Magnetic characteristics

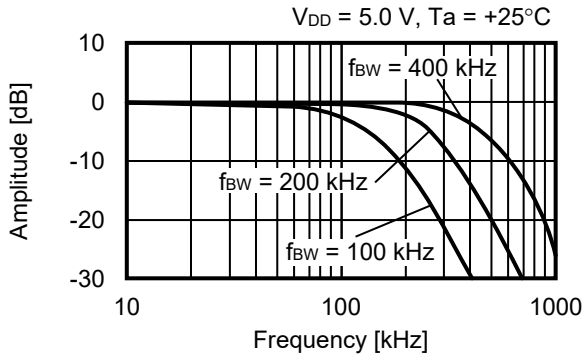
2. 1 Sensitivity



2. 2 Sensitivity linearity error

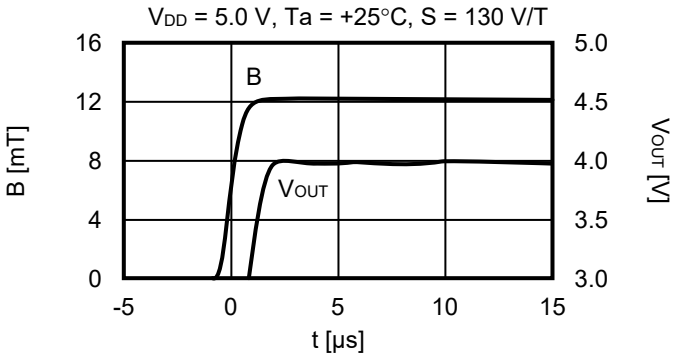


2. 3 Frequency bandwidth

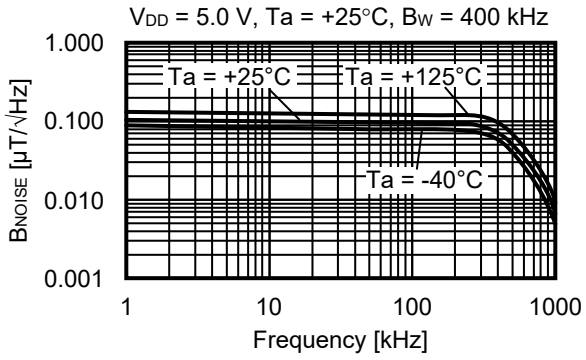


3. Output voltage characteristics

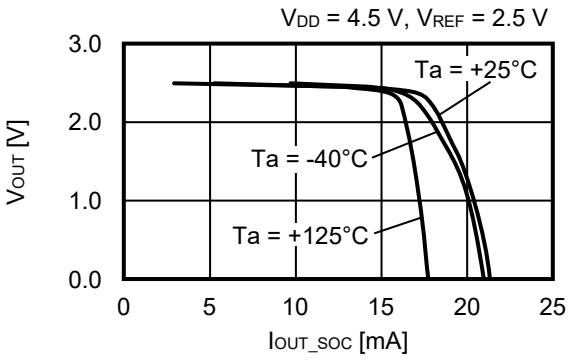
3. 1 Response waveform

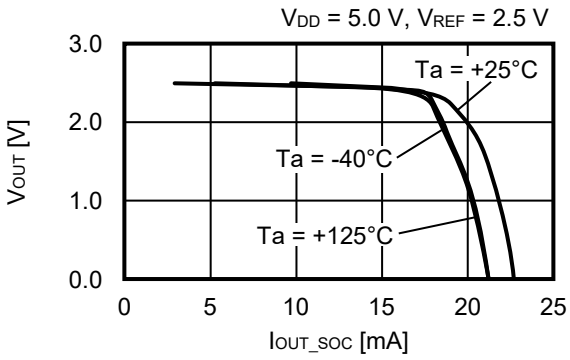


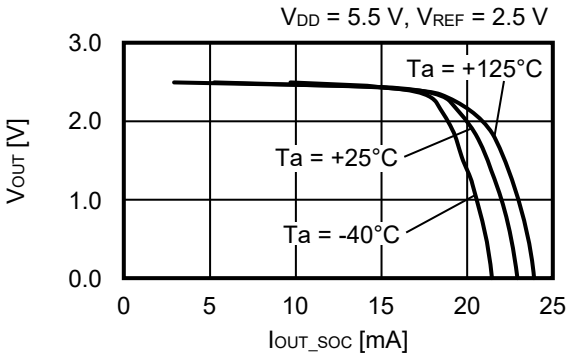
3. 2 Input magnetic flux density referred noise voltage



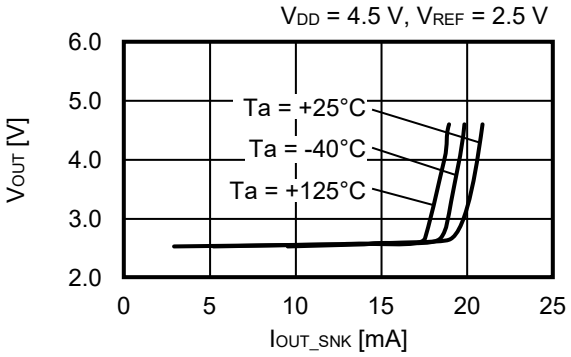
3. 3 Output source current

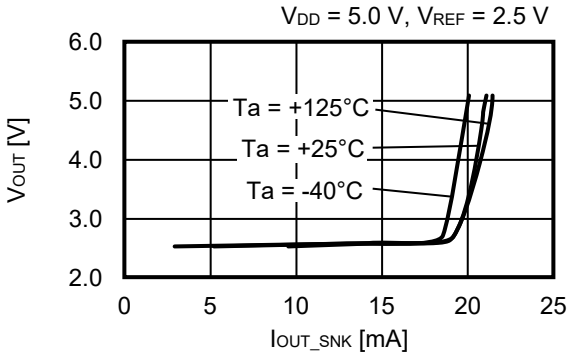


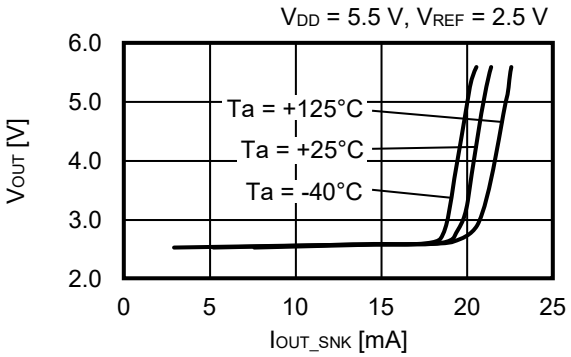




3. 4 Output sink current

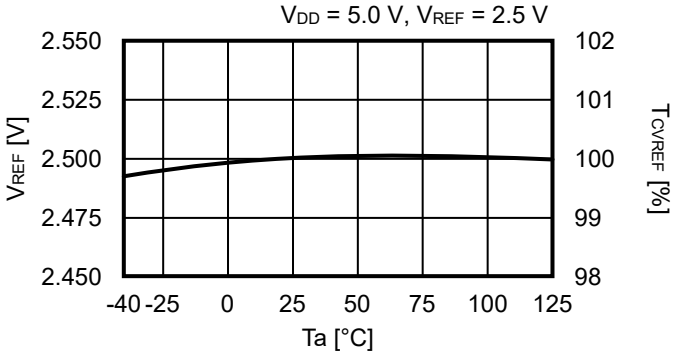




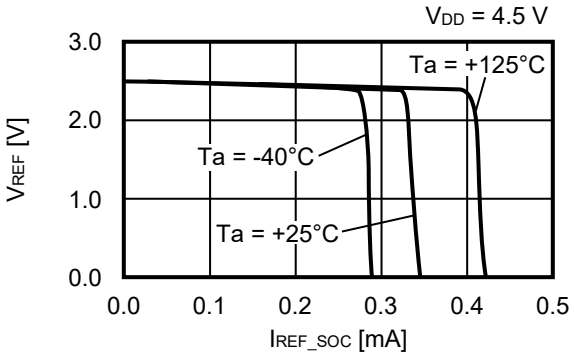


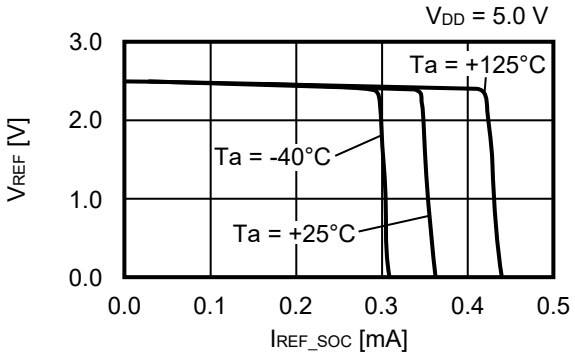
4. Reference voltage characteristics

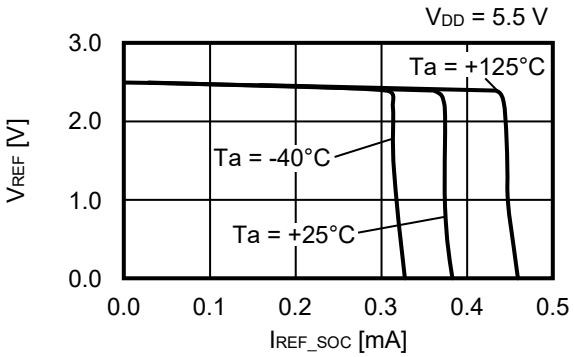
4. 1 Reference voltage output



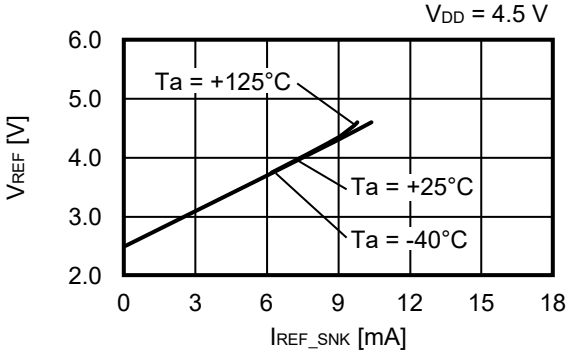
4. 2 Reference voltage source current (V_{REF} = 2.5 V)

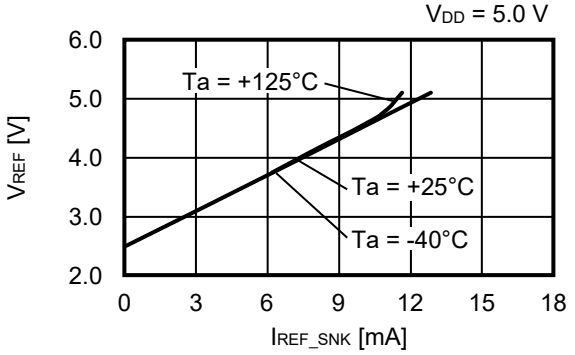


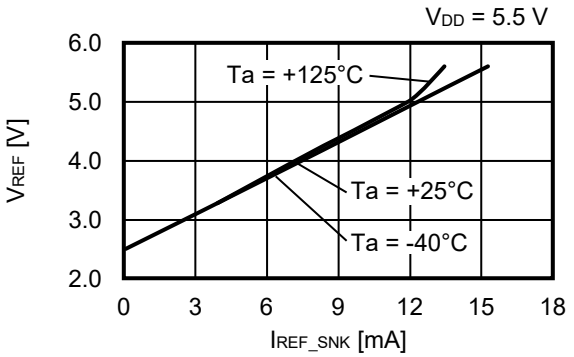




4. 3 Reference voltage sink current (V_{REF} = 2.5 V)

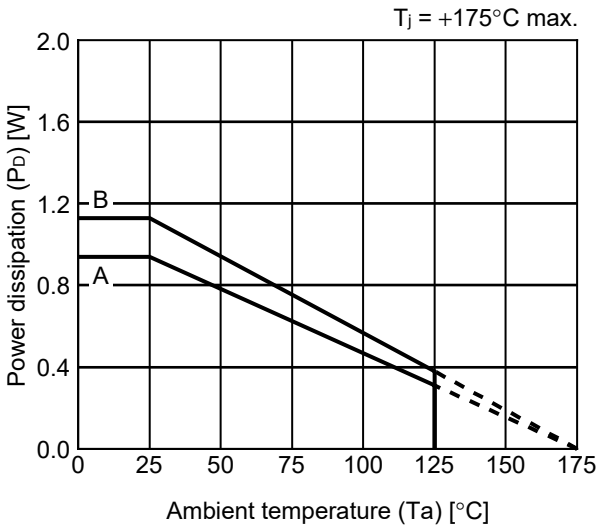






■ Power Dissipation

TMSOP-8

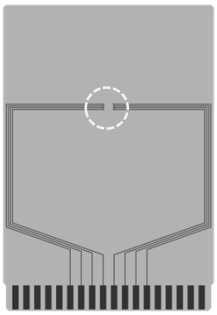


Board	Power Dissipation (P_D)
A	0.94 W
B	1.13 W
C	-
D	-
E	-

TMSOP-8 Test Board

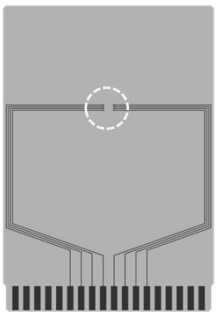
(1) Board A

IC Mount Area



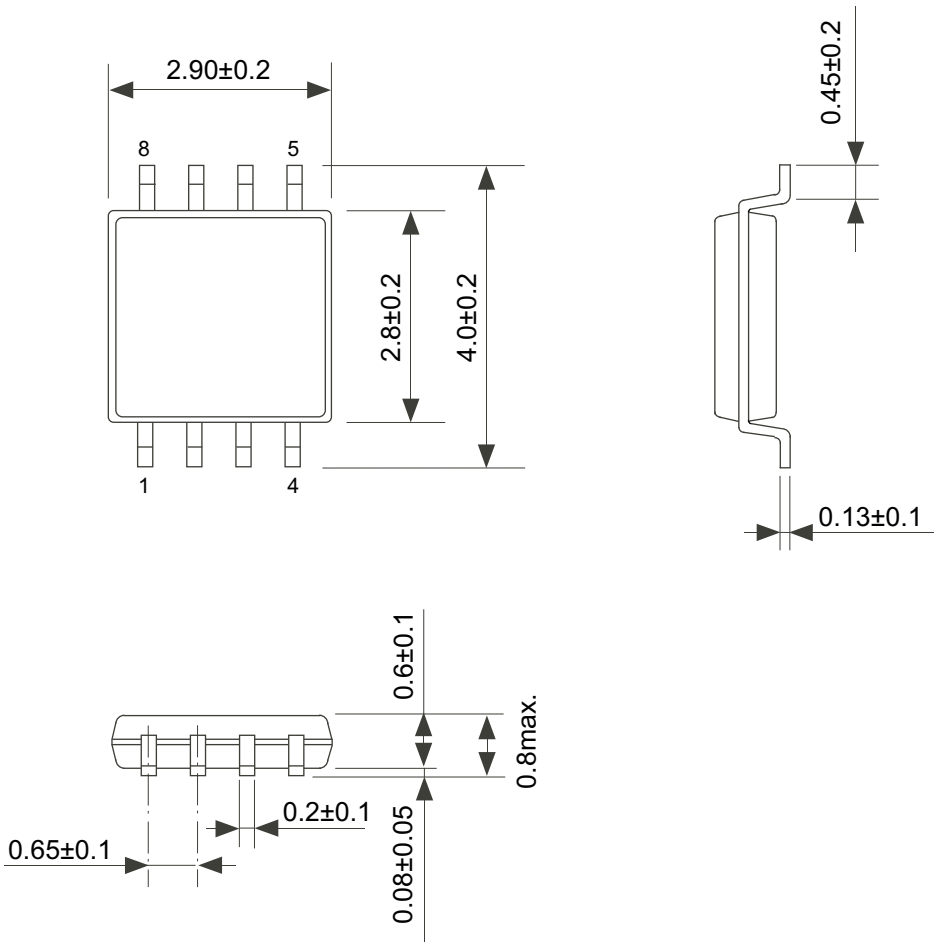
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

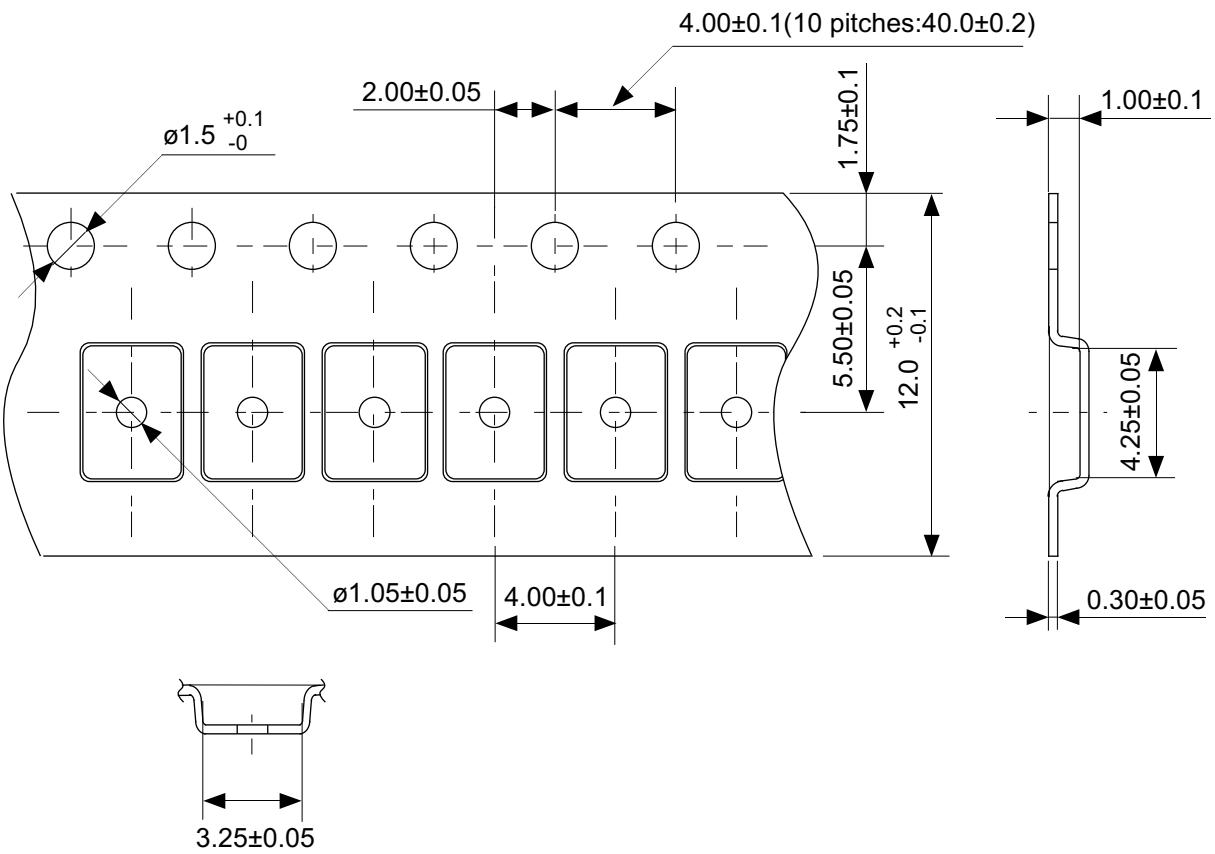
No. TMSOP8-A-Board-SD-1.0

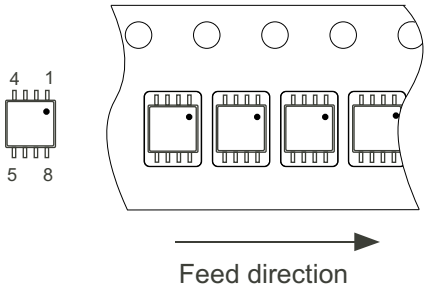


No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm

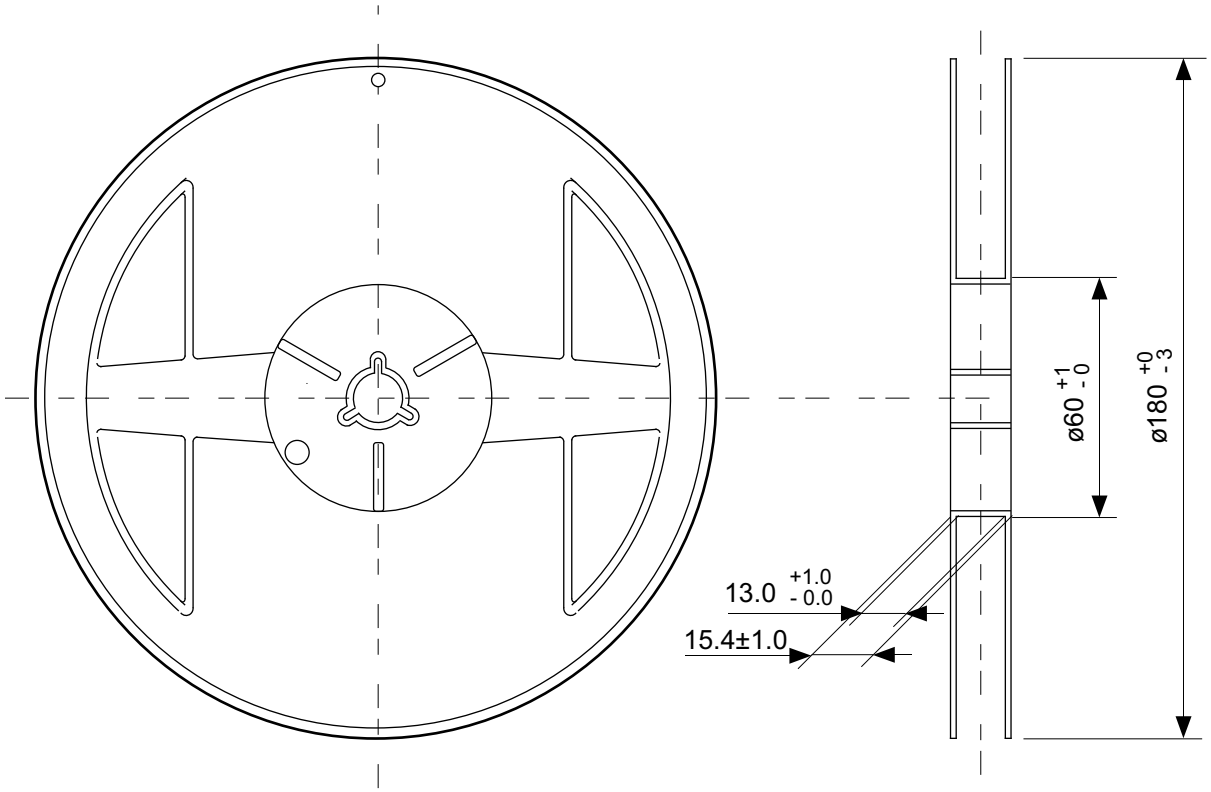
ABLIC Inc.



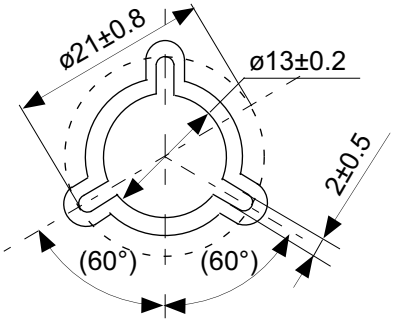


No. FM008-A-C-SD-3.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-3.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-2.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
	ABLIC Inc.		

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2.4-2019.07