S-5791/92 B Series

125°C OPERATION, HIGH-WITHSTAND VOLTAGE, HIGH-SPEED, 2D DUAL HALL EFFECT LATCH IC

www.ablic.com

Rev.1.0_00

This IC, developed by CMOS technology, is a 2D dual Hall effect latch IC that operates with high temperature, high-withstand voltage and high speed.
The output voltage level changes when this IC detects the intensity level of magnetic flux density and a polarity change. Using this IC with a magnet makes it possible to detect the rotational speed and direction in various devices.
Uses a small SOT-23-5 package or ultra-thin (t0.50 mm max.) HSNT-6(2025) package, allowing for device high-density mounting.

ABLIC Inc. offers a "magnetic simulation service" that provides the ideal combination of magnets and our Hall effect ICs for customer systems. Our magnetic simulation service will reduce prototype production, development period and development costs. In addition, it will contribute to optimization of parts to realize high cost performance.
For more information regarding our magnetic simulation service, contact our sales representatives.

■ Features

- Output type*1: Rotational speed and direction output / Quadrature output
- Detection axis*1: X and Y-Axis / Z and X-Axis / Z and Y-Axis
- Output logic*1 (Rotational speed and direction output): V_{OUT1} = "L" in forward rotation / V_{OUT1} = "H" in forward rotation
- Output logic*1 (Quadrature output): $V_{OUT1,2}$ = "L" at S pole detection / $V_{OUT1,2}$ = "H" at S pole detection
- Output form*1: Nch open-drain output / Nch driver + built-in pull-up resistor (10 kΩ typ.)
- Magnetic sensitivity*1: B_{OP} = 0.8 mT typ. / B_{OP} = 2.0 mT typ. / B_{OP} = 6.0 mT typ.
- Output delay time: t_D = 8.4 µs typ.
- Power supply voltage range*2: V_{DD} = 3.8 V to 26.0 V
- Built-in regulator
- Built-in output current limit circuit
- Operation temperature range: Ta = -40°C to +125°C
- Lead-free (Sn 100%), halogen-free

■ Applications

- Household appliances
- Industrial motor-related equipment
- Industrial equipment
- Residential equipment

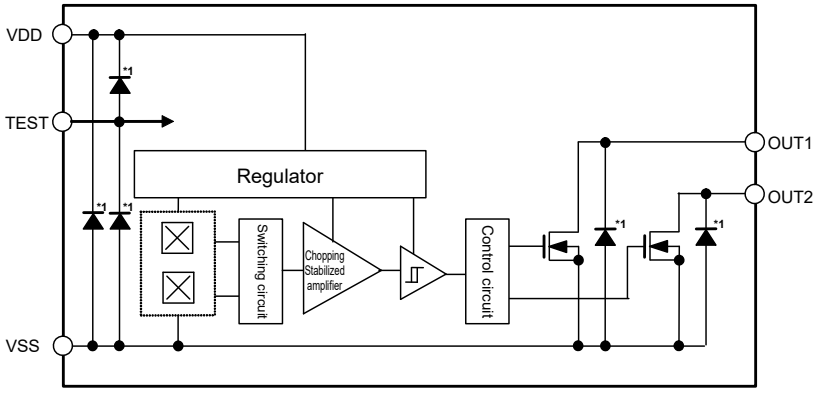
■ Packages

- SOT-23-5
- HSNT-6(2025)

***1.** The option can be selected.
***2.** V_{DD} = 3.8 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (10 kΩ typ.)

■ Block Diagrams

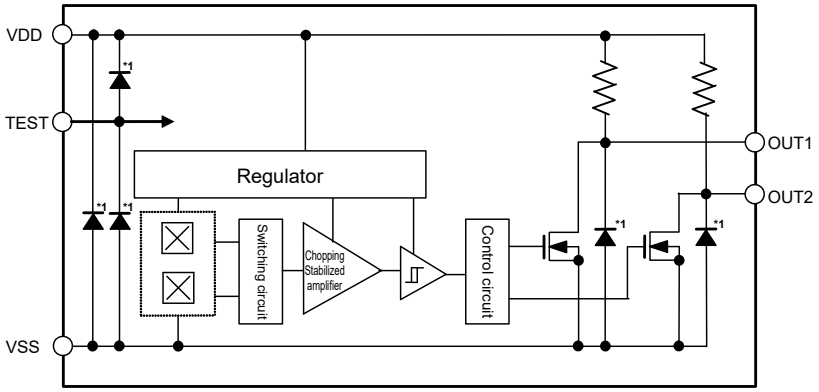
1. Nch open-drain output product



***1.** Parasitic diode

Figure 1

2. Nch driver + built-in pull-up resistor product



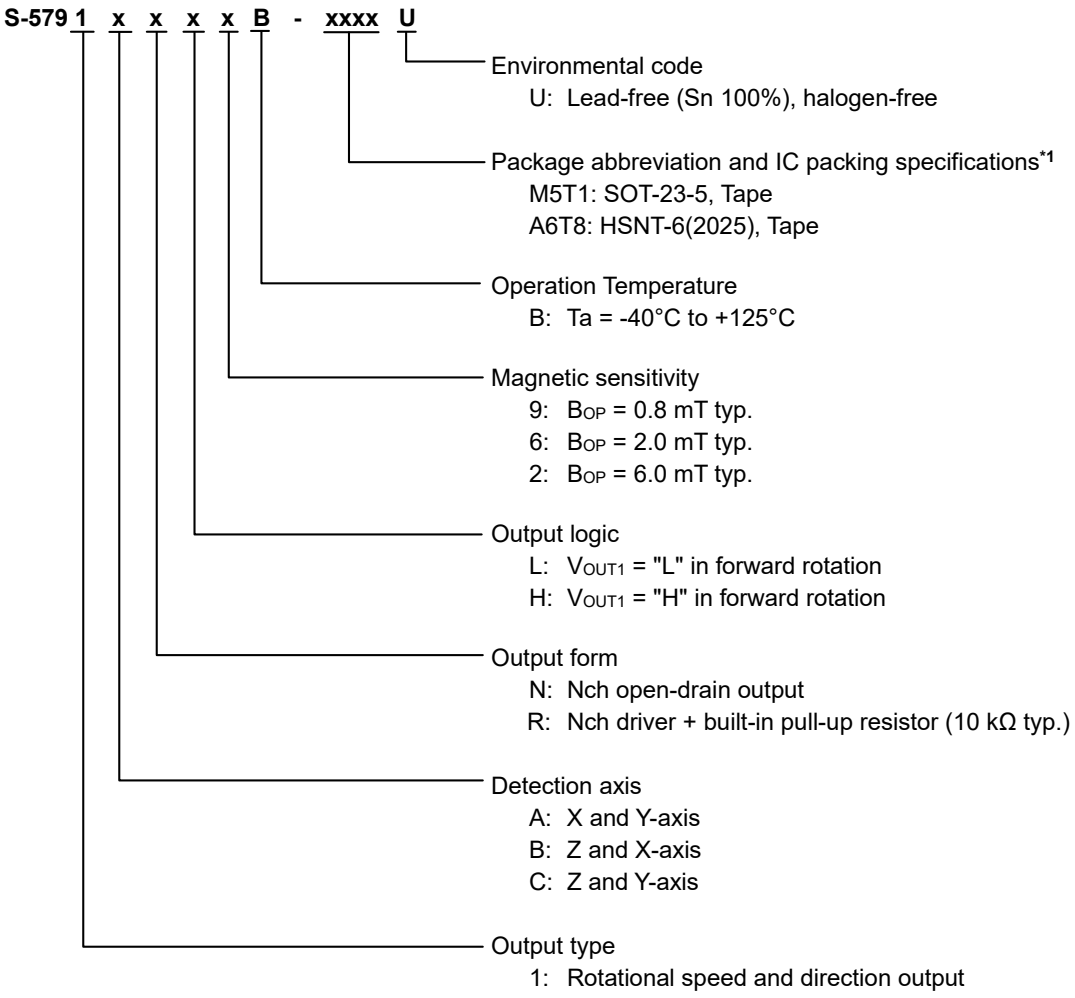
***1.** Parasitic diode

Figure 2

■ Product Name Structure

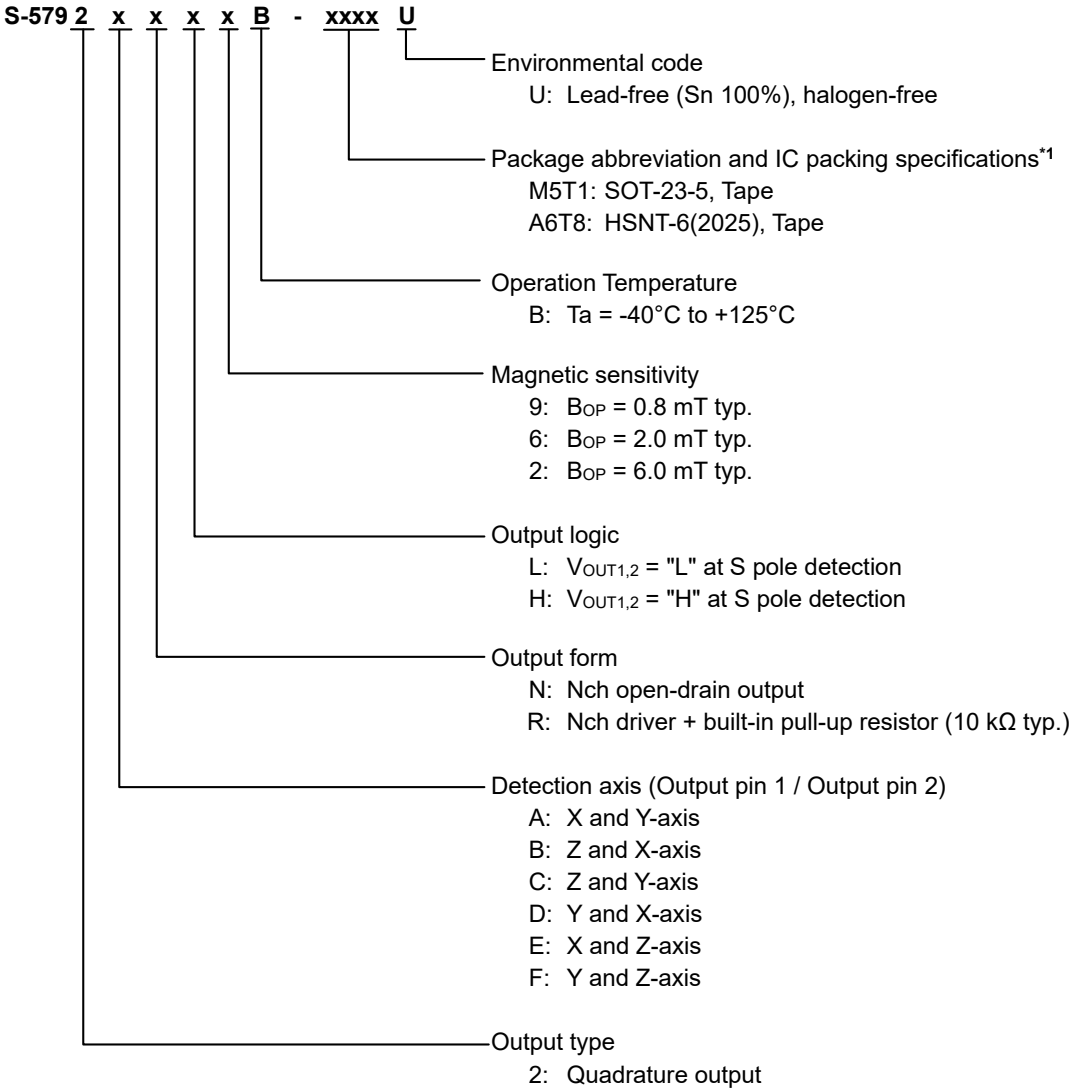
1. Product name

1. 1 S-5791xxxxB Series



***1.** Refer to the tape drawing.

1. 2 S-5792xxxxB Series



***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land	Stencil Opening
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	-	-
HSNT-6(2025)	PJ006-B-P-SD	PJ006-B-C-SD	PJ006-B-R-SD	PJ006-B-LM-SD	PJ006-B-LM-SD

3. Product name list

3. 1 SOT-23-5

3. 1. 1 Nch open-drain output product (V_{DD} = 3.8 V to 26.0 V)

Table 2

Product Name	Output Type	Detection Axis	Output Logic	Magnetic Sensitivity (B_{OP})
S-5792ANL6B-M5T1U	Quadrature output	X and Y-axis	$V_{OUT1,2}$ = "L" at S pole detection	2.0 mT typ.
S-5792ANL9B-M5T1U	Quadrature output	X and Y-axis	$V_{OUT1,2}$ = "L" at S pole detection	0.8 mT typ.
S-5792BNL6B-M5T1U	Quadrature output	Z and X-axis	$V_{OUT1,2}$ = "L" at S pole detection	2.0 mT typ.
S-5792CNL6B-M5T1U	Quadrature output	Z and Y-axis	$V_{OUT1,2}$ = "L" at S pole detection	2.0 mT typ.
S-5792CNL9B-M5T1U	Quadrature output	Z and Y-axis	$V_{OUT1,2}$ = "L" at S pole detection	0.8 mT typ.

Remark Please contact our sales representatives for products other than the above.

3. 2 HSNT-6(2025)

3. 2. 1 Nch open-drain output product (V_{DD} = 3.8 V to 26.0 V)

Table 3

Product Name	Output Type	Detection Axis	Output Logic	Magnetic Sensitivity (B_{OP})
S-5792ANL6B-A6T8U	Quadrature output	X and Y-axis	$V_{OUT1,2}$ = "L" at S pole detection	2.0 mT typ.
S-5792ANL9B-A6T8U	Quadrature output	X and Y-axis	$V_{OUT1,2}$ = "L" at S pole detection	0.8 mT typ.
S-5792CNL6B-A6T8U	Quadrature output	Z and Y-axis	$V_{OUT1,2}$ = "L" at S pole detection	2.0 mT typ.
S-5792CNL9B-A6T8U	Quadrature output	Z and Y-axis	$V_{OUT1,2}$ = "L" at S pole detection	0.8 mT typ.

Remark Please contact our sales representatives for products other than the above.

■ Pin Configurations

1. SOT-23-5

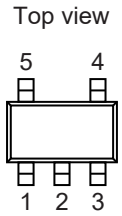


Figure 3

Table 4

Pin No.	Symbol	Description
1	OUT2	Output pin 2
2	VSS	GND pin
3	OUT1	Output pin 1
4	VDD	Power supply pin
5	TEST*1	Test pin

***1.** Connect the TEST pin to the VSS pin.

2. HSNT-6(2025)

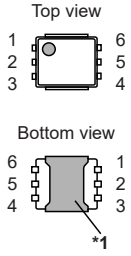


Figure 4

Table 5

Pin No.	Symbol	Description
1	OUT1	Output pin1
2	VSS	GND pin
3	OUT2	Output pin 2
4	TEST*2	Test pin
5	NC*3	No connection
6	VDD	Power supply pin

***1.** Connect the heatsink of backside at shadowed area to the board, and set electric potential open or GND. However, do not use it as the function of electrode.
***2.** Connect the TEST pin to the VSS pin.
***3.** The NC pin is electrically open. The NC pin can be connected to the VDD pin or the VSS pin.

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage	Nch open-drain output product	V_{DD}	V_{SS} - 0.3 to V_{SS} + 28	V
	Nch driver + built-in pull-up resistor (10kΩ typ.) product		V_{SS} - 0.3 to V_{SS} + 9.0	V
Output current		I_{OUT}	±10	mA
Output voltage	Nch open-drain output product	V_{OUT}	V_{SS} - 0.3 to V_{SS} + 28	V
	Nch driver + built-in pull-up resistor (10kΩ typ.) product		V_{SS} - 0.3 to V_{DD} + 0.3	V
TEST pin voltage		V_{TEST}	V_{SS} - 0.3 to V_{SS} + 3.6	V
Operation ambient temperature		T_{opr}	-40 to +125	°C
Storage temperature		T_{stg}	-40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SOT-23-5	Board A	-	192	-	°C/W
			Board B	-	160	-	°C/W
			Board C	-	-	-	°C/W
			Board D	-	-	-	°C/W
			Board E	-	-	-	°C/W
		HSNT-6(2025)	Board A	-	180	-	°C/W
			Board B	-	128	-	°C/W
			Board C	-	43	-	°C/W
			Board D	-	44	-	°C/W
			Board E	-	36	-	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Nch open-drain output product

Table 8

(Ta = +25°C, V_{DD} = 12.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	-	3.8	12.0	26.0	V	-
Current consumption	I_{DD}	-	-	3.5	5.2	mA	1
Low level output voltage	V_{OL}	I_{OUT} = 5 mA, $V_{OUT1,2}$ = "L"	-	-	0.4	V	2
Leakage current	I_{LEAK}	$V_{OUT1,2}$ = "H", $V_{OUT1,2}$ = 26.0 V	-	-	10	μA	3
Output limit current	I_{OM}	$V_{OUT1,2}$ = "L", $V_{OUT1,2}$ = 26.0 V	11	-	35	mA	3
Output delay time*1	t_D	-	-	8.4	11.8	μs	-
Chopping frequency	f_C	-	-	714	-	kHz	-
Start up time*1	t_{PON}	-	-	50	100	μs	4
Output rise time*1	t_R	C = 20 pF, R = 820 Ω	-	-	1.0	μs	5
Output fall time*1	t_F	C = 20 pF, R = 820 Ω	-	-	1.0	μs	5

***1.** This item is guaranteed by design.

2. Nch driver + built-in pull-up resistor (10 kΩ typ.) product

Table 9

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	-	3.8	5.0	5.5	V	-
Current consumption	I_{DD}	$V_{OUT1,2}$ = "H"	-	3.5	5.2	mA	1
Low level output voltage	V_{OL}	I_{OUT} = 0 mA, $V_{OUT1,2}$ = "L"	-	-	0.4	V	2
High level output voltage	V_{OH}	I_{OUT} = 0 mA, $V_{OUT1,2}$ = "H"	V_{DD} × 0.9	-	-	V	2
Output limit current	I_{OM}	$V_{OUT1,2}$ = "L", V_{DD} = $V_{OUT1,2}$ = 5.0 V	11	-	35	mA	3
Output delay time*1	t_D	-	-	8.4	11.8	μs	-
Chopping frequency	f_C	-	-	714	-	kHz	-
Start up time*1	t_{PON}	-	-	50	100	μs	4
Output rise time*1	t_R	C = 20 pF	-	-	10.0	μs	5
Output fall time*1	t_F	C = 20 pF	-	-	1.0	μs	5
Pull-up resistor	R_L	-	7.5	10	12.5	kΩ	-

***1.** This item is guaranteed by design.

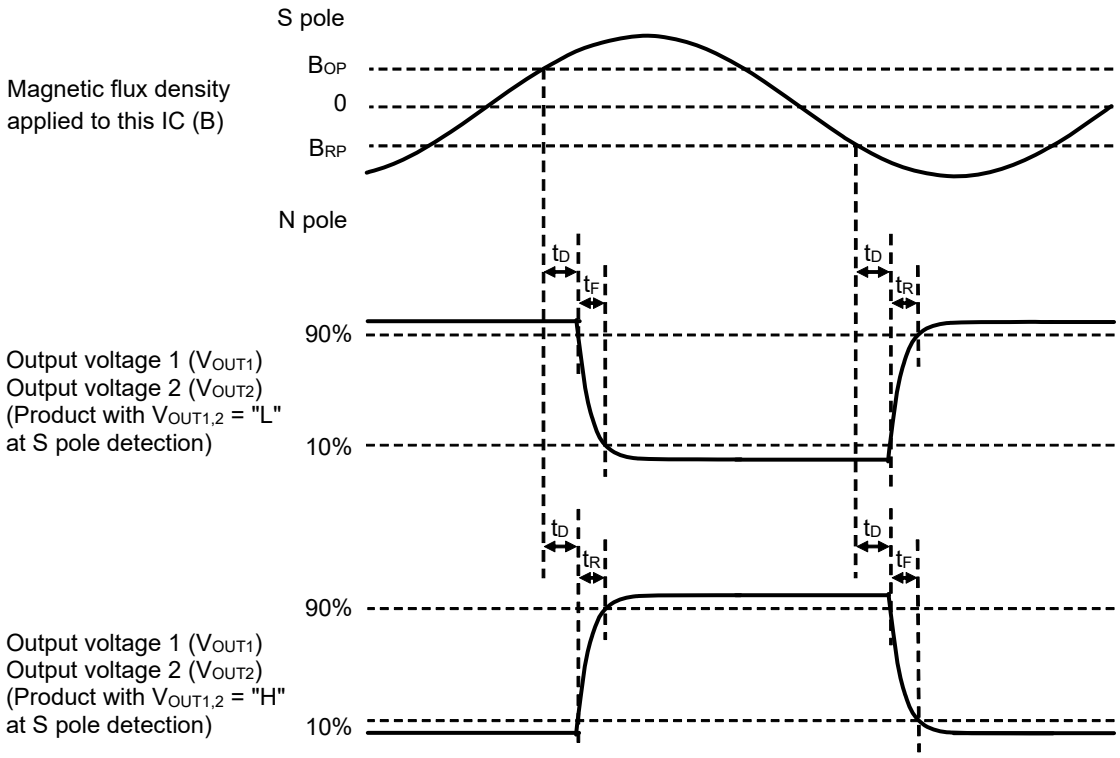


Figure 5 Operation Timing

■ Magnetic Characteristics

1. Product with B_{OP} = 0.8 mT typ.

Table 10

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
OUT1 operation point*1	S pole	B_{OP1}	-	-0.4	0.8	2.4	mT	4
OUT1 release point*2	N pole	B_{RP1}	-	-2.4	-0.8	0.4	mT	4
OUT1 hysteresis width*3		B_{HYS1}	$B_{HYS1} = B_{OP1} - B_{RP1}$	-	1.6	-	mT	4
OUT2 operation point*1	S pole	B_{OP2}	-	-0.4	0.8	2.4	mT	4
OUT2 release point*2	N pole	B_{RP2}	-	-2.4	-0.8	0.4	mT	4
OUT2 hysteresis width*3		B_{HYS2}	$B_{HYS2} = B_{OP2} - B_{RP2}$	-	1.6	-	mT	4

2. Product with B_{OP} = 2.0 mT typ.

Table 11

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
OUT1 operation point*1	S pole	B_{OP1}	-	0.5	2.0	4.0	mT	4
OUT1 release point*2	N pole	B_{RP1}	-	-4.0	-2.0	-0.5	mT	4
OUT1 hysteresis width*3		B_{HYS1}	$B_{HYS1} = B_{OP1} - B_{RP1}$	-	4.0	-	mT	4
OUT2 operation point*1	S pole	B_{OP2}	-	0.5	2.0	4.0	mT	4
OUT2 release point*2	N pole	B_{RP2}	-	-4.0	-2.0	-0.5	mT	4
OUT2 hysteresis width*3		B_{HYS2}	$B_{HYS2} = B_{OP2} - B_{RP2}$	-	4.0	-	mT	4

3. Product with B_{OP} = 6.0 mT typ.

Table 12

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
OUT1 operation point*1	S pole	B_{OP1}	-	3.0	6.0	9.0	mT	4
OUT1 release point*2	N pole	B_{RP1}	-	-9.0	-6.0	-3.0	mT	4
OUT1 hysteresis width*3		B_{HYS1}	$B_{HYS1} = B_{OP1} - B_{RP1}$	-	12.0	-	mT	4
OUT2 operation point*1	S pole	B_{OP2}	-	3.0	6.0	9.0	mT	4
OUT2 release point*2	N pole	B_{RP2}	-	-9.0	-6.0	-3.0	mT	4
OUT2 hysteresis width*3		B_{HYS2}	$B_{HYS2} = B_{OP2} - B_{RP2}$	-	12.0	-	mT	4

***1.** B_{OP}: Operation point
B_{OP} is the value of magnetic flux density when the output voltage ($V_{OUT1,2}$) changes after the magnetic flux density applied to this IC by the magnet (S pole) is increased (by moving the magnet closer).
$V_{OUT1,2}$ retains the status until a magnetic flux density of the N pole higher than B_{RP} is applied.

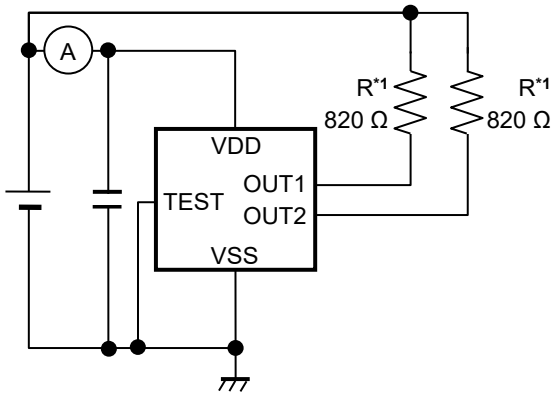
***2.** B_{RP}: Release point
B_{RP} is the value of magnetic flux density when the output voltage ($V_{OUT1,2}$) changes after the magnetic flux density applied to this IC by the magnet (N pole) is decreased (the magnet is moved further away).
$V_{OUT1,2}$ retains the status until a magnetic flux density of the S pole higher than B_{OP} is applied.

***3.** B_{HYS}: Hysteresis width
B_{HYS} is the difference between B_{OP} and B_{RP}.

Caution **Due to limitation of the power dissipation, these values may not be satisfied. Attention should be paid to the power dissipation when using in high temperature operation environments.**

Remark The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

■ Test Circuits



*1. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

Figure 6 Test Circuit 1

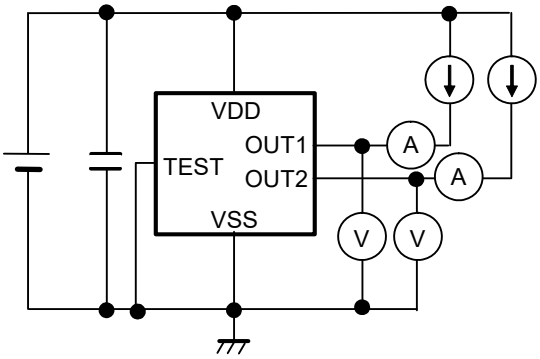


Figure 7 Test Circuit 2

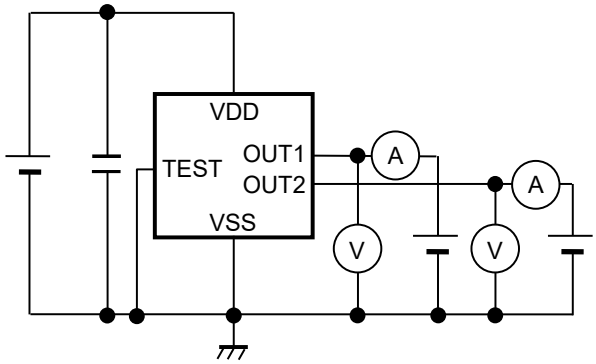
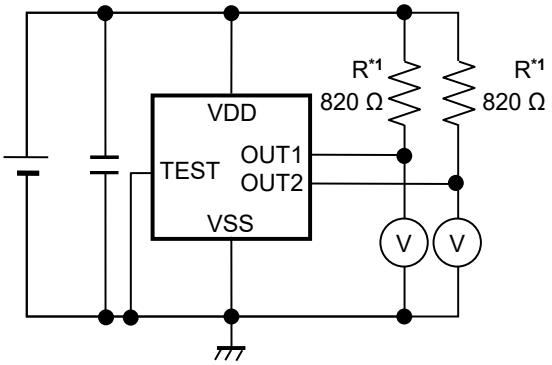
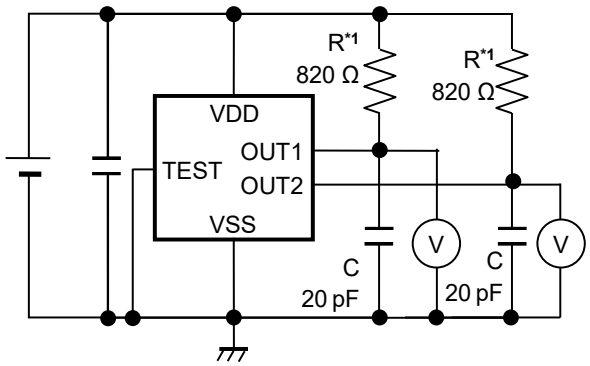


Figure 8 Test Circuit 3



*1. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

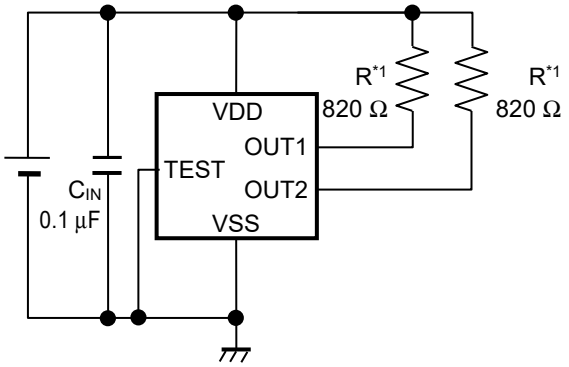
Figure 9 Test Circuit 4



*1. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

Figure 10 Test Circuit 5

■ Standard Circuit



***1**. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

Figure 11

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Operation

1. Direction of applied magnetic flux

Figure 12 and **Figure 13** show the direction in which the magnetic flux is applied. The Z-axis is defined as the direction perpendicular to the package marking surface, while the X-axis and Y-axis are defined as the directions perpendicular to the sides of the package. The direction of application where the IC side becomes the S pole is defined as the positive, and the direction of application where the IC side becomes the N pole is defined as the negative. This IC can detect two out of the three axes: X, Y, and Z.

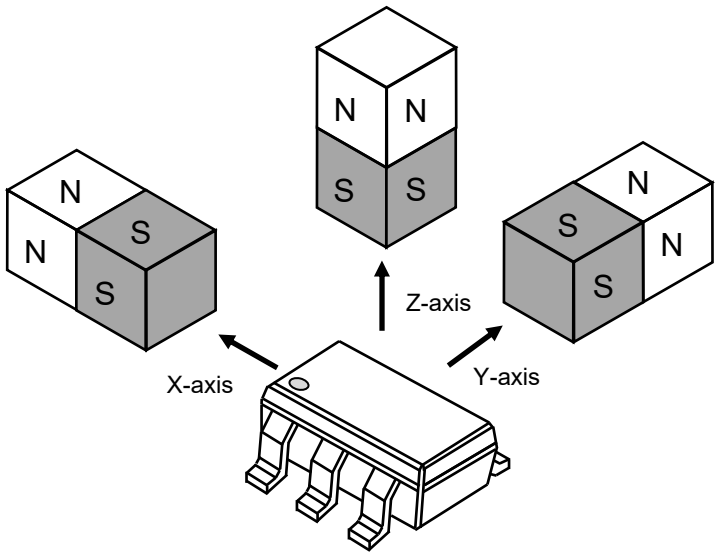


Figure 12 SOT-23-5

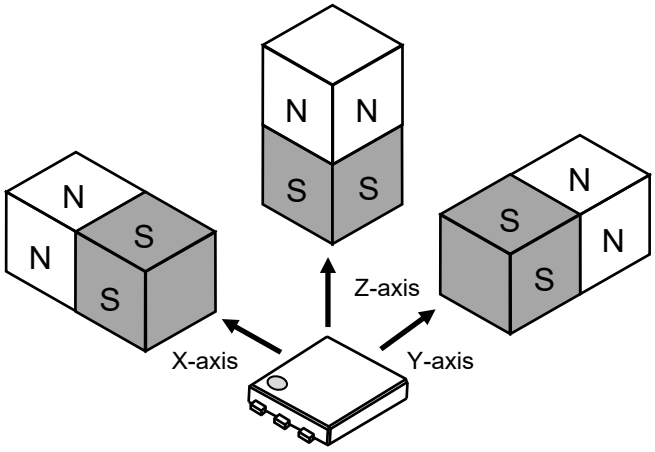


Figure 13 HSNT-6(2025)

2. Position of Hall sensor

Figure 14 and **Figure 15** show the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

2. 1 SOT-23-5

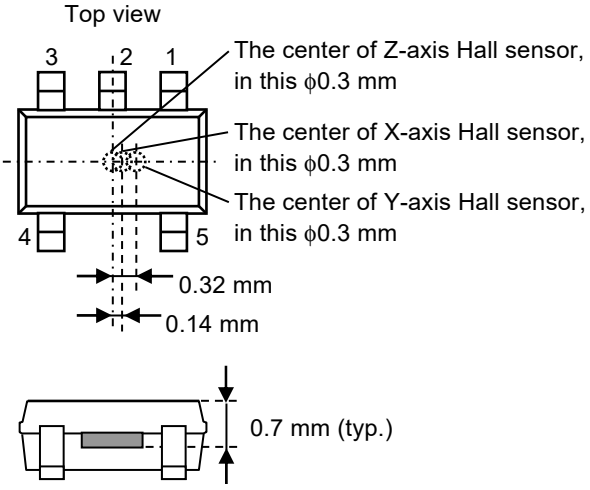


Figure 14

2. 2 HSNT-6(2025)

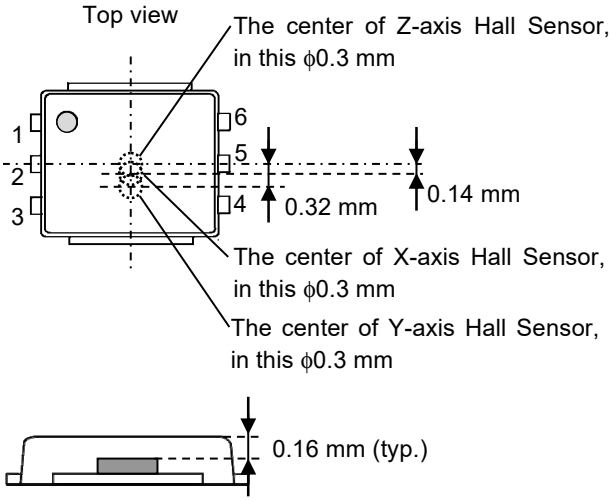


Figure 15

3. Basic operation

This IC changes the output voltage ($V_{OUT1,2}$) according to the level of the magnetic flux density (N pole or S pole) and a polarity change applied by a magnet.

3. 1 Product with quadrature output, $V_{OUT1,2}$ = "L" at S pole detection

When the S pole of a magnet approaches the IC from the positive direction of each axis X, Y, and Z as shown in **Figure 12** and **Figure 13**, and the magnetic flux density of the S pole exceeds the operation point (B_{OP}), $V_{OUT1,2}$ changes from "H" to "L". When the N pole of a magnet approaches the IC from the positive direction, and the magnetic flux density of the N pole exceeds the release point (B_{RP}), $V_{OUT1,2}$ changes from "L" to "H". When $B_{RP} < B < B_{OP}$, $V_{OUT1,2}$ retains the level.
Figure 16 shows the relationship between the magnetic flux density and $V_{OUT1,2}$.

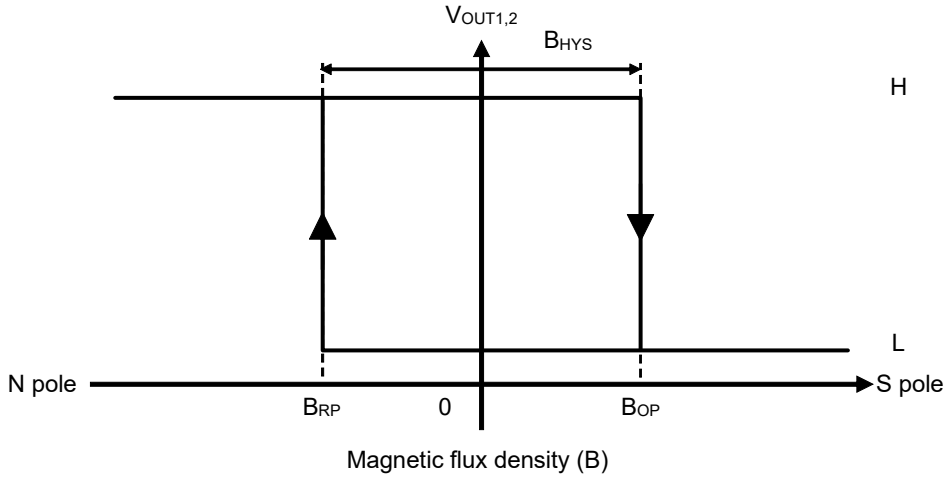


Figure 16

3. 2 Product with quadrature output, $V_{OUT1,2}$ = "H" at S pole detection

When the S pole of a magnet approaches the IC from the positive direction of each axis X, Y, and Z as shown in **Figure 12** and **Figure 13**, and the magnetic flux density of the S pole exceeds the operation point (B_{OP}), $V_{OUT1,2}$ changes from "L" to "H". When the N pole of a magnet approaches the IC from the positive direction, and the magnetic flux density of the N pole exceeds the release point (B_{RP}), $V_{OUT1,2}$ changes from "H" to "L". When $B_{RP} < B < B_{OP}$, $V_{OUT1,2}$ retains the level.
Figure 17 shows the relationship between the magnetic flux density and $V_{OUT1,2}$.

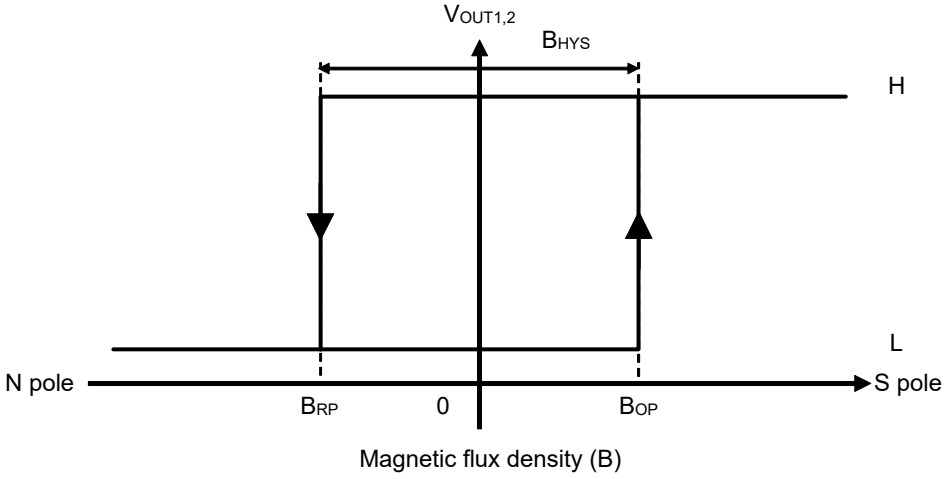


Figure 17

4. Magnetic flux density response timing chart

Figure 18 shows the timing chart for product with quadrature output, $V_{OUT1,2}$ = "L" at S pole detection.

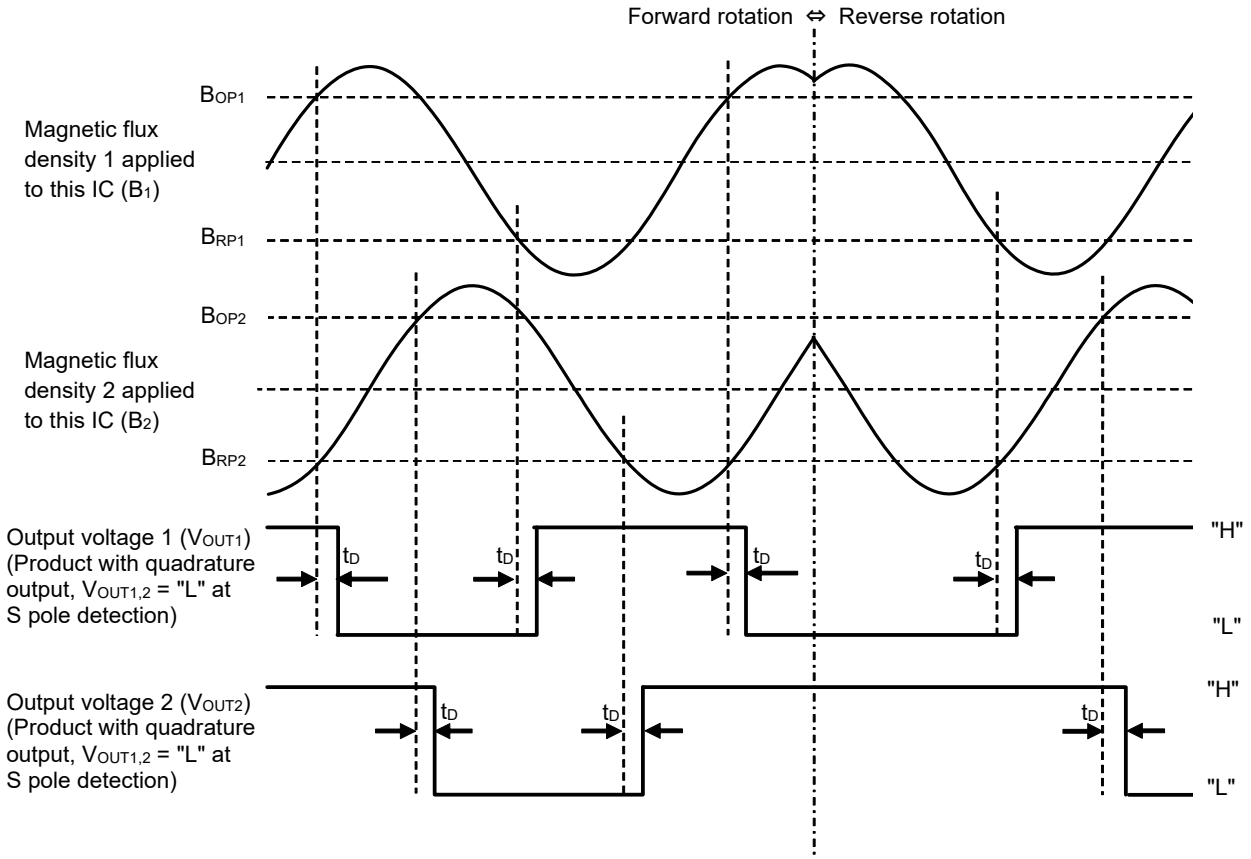


Figure 18

Figure 19 shows the timing chart for product with rotational speed and direction output, V_{OUT1} = "L" in forward rotation.

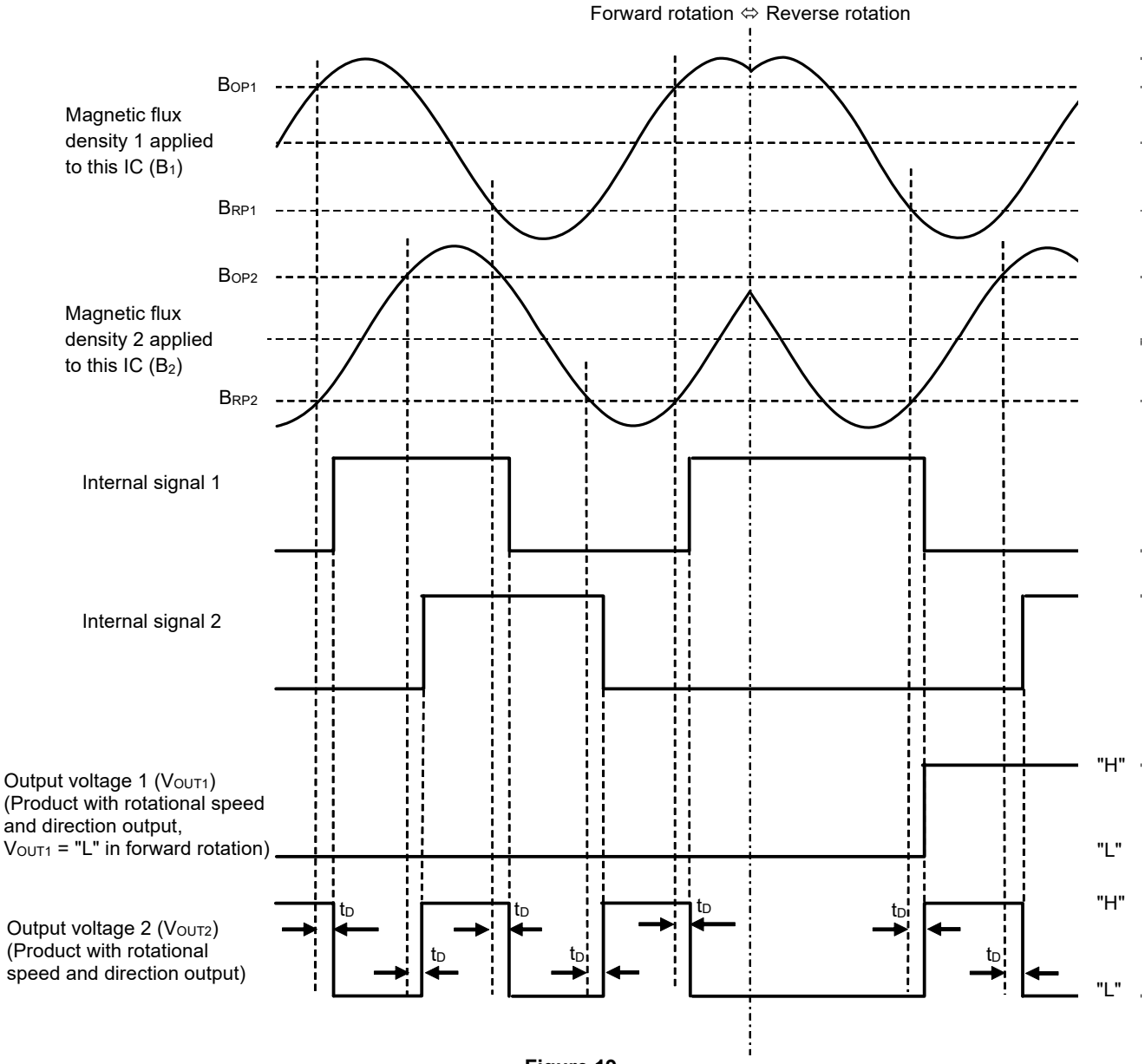


Figure 19

5. Power-on operation

The output voltages (V_{OUT1}, V_{OUT2}) of this IC immediately after power-on is "H". After the start up time (t_{PON}) is passed, if the magnetic flux density (B_1, B_2) is below the operation point ($B_1 < B_{OP1}$, $B_2 < B_{OP2}$), the output voltages corresponding to B_1 and B_2 (V_{OUT1}, V_{OUT2}) retain "H". When the magnetic flux density exceeds the operation point ($B_1 > B_{OP1}$, $B_2 > B_{OP2}$), the output voltages corresponding to B_1 and B_2 (V_{OUT1}, V_{OUT2}) are change to the predetermined output voltage according to the strength of the magnetic flux density and the polarity change.

■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low, and provide bypass capacitance between the power supplies if necessary.

- Note that the IC may malfunction if the power supply voltage rapidly changes. When the IC is used under the environment where the power supply voltage rapidly changes, it is recommended to judge the output voltage of the IC by reading it multiple times.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- Although this IC has a built-in output current limit circuit, it may suffer physical damage such as product deterioration under the environment where the absolute maximum ratings are exceeded.

- The application conditions for the power supply voltage, the pull-up voltage, and the pull-up resistor should not exceed the power dissipation.

- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.

- Since the package heat radiation differs according to the conditions of the application, perform thorough evaluation with actual applications to confirm no problems occur.

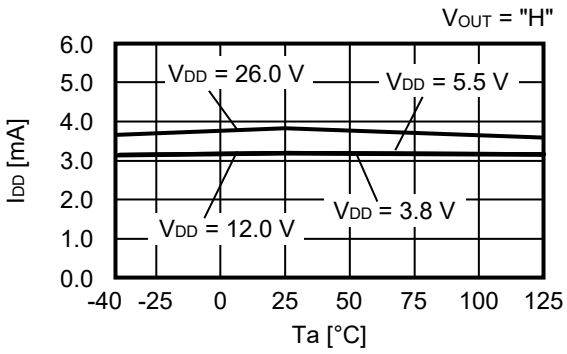
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

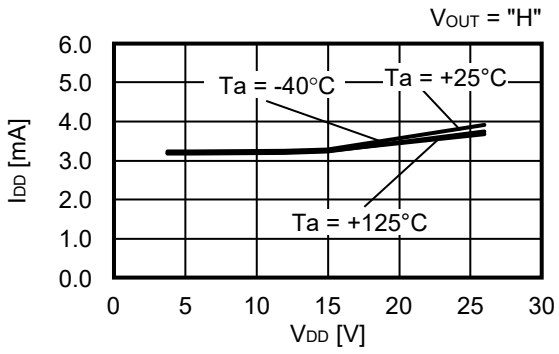
1. Electrical characteristics

1. 1 S-579xxxxxB

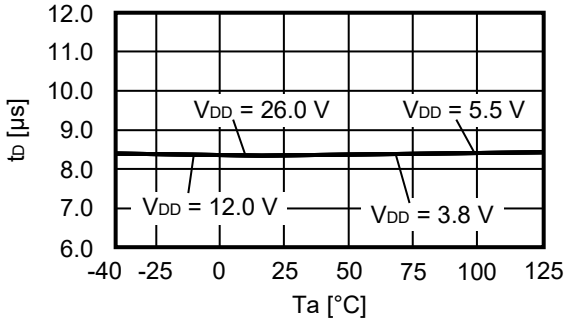
1. 1. 1 Current consumption (I_{DD}) vs. Temperature (Ta)



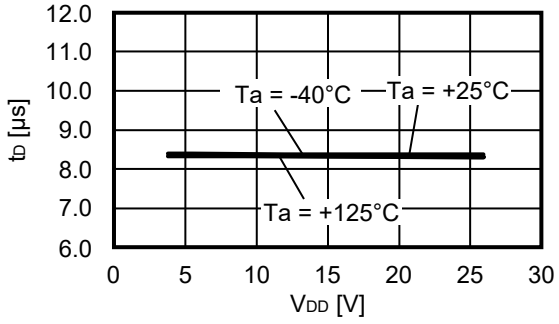
1. 1. 2 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



1. 1. 3 Output delay time (t_D) vs. Temperature (Ta)



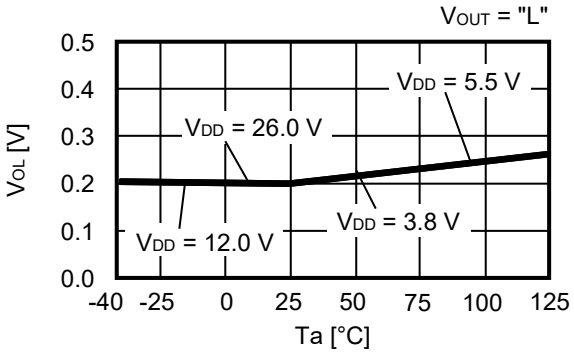
1. 1. 4 Output delay time (t_D) vs. Power supply voltage (V_{DD})



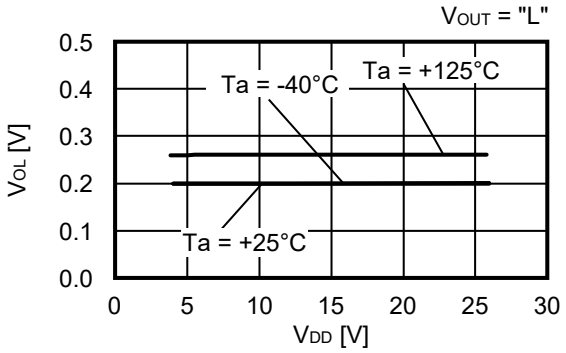
Caution V_{DD} = 3.8 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (10 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.

1. 2 S-579xxNxxB

1. 2. 1 Low level output voltage (V_{OL}) vs. Temperature (Ta)

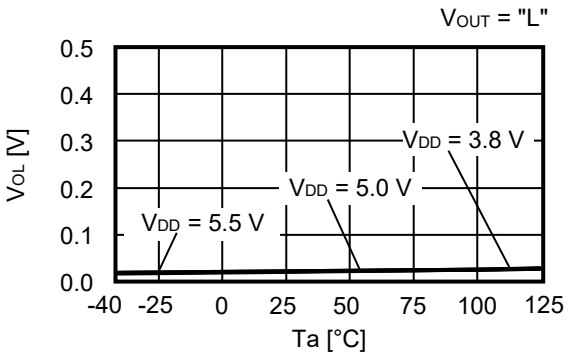


1. 2. 2 Low level output voltage (V_{OL}) vs. Power supply voltage (V_{DD})

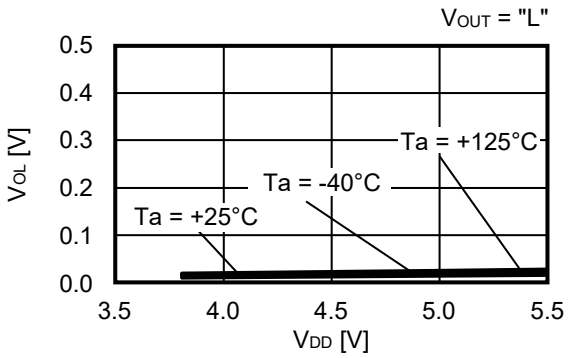


1. 3 S-579xxRxxB

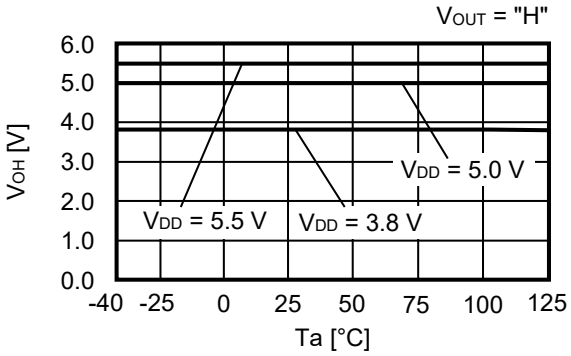
1. 3. 1 Low level output voltage (V_{OL}) vs. Temperature (Ta)



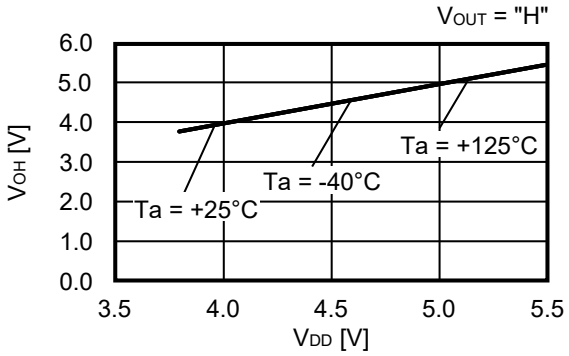
1. 3. 2 Low level output voltage (V_{OL}) vs. Power supply voltage (V_{DD})



1. 3. 3 High level output voltage (V_{OH}) vs. Temperature (Ta)



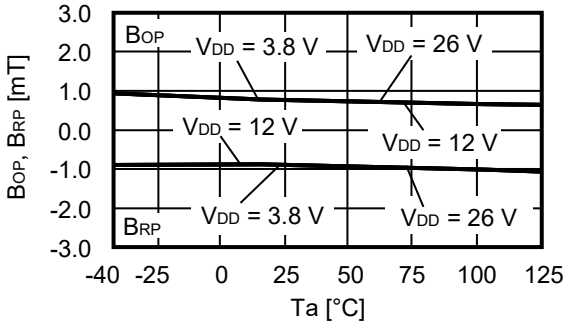
1. 3. 4 High level output voltage (V_{OH}) vs. Power supply voltage (V_{DD})



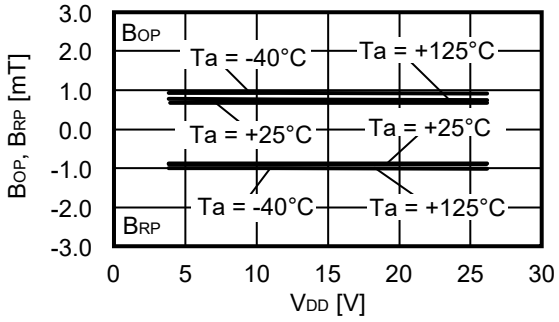
2. Magnetic Characteristics

2. 1 S-579xxxx9B-M5T1U

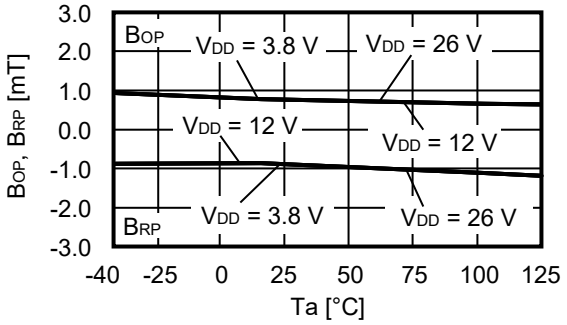
2. 1. 1 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



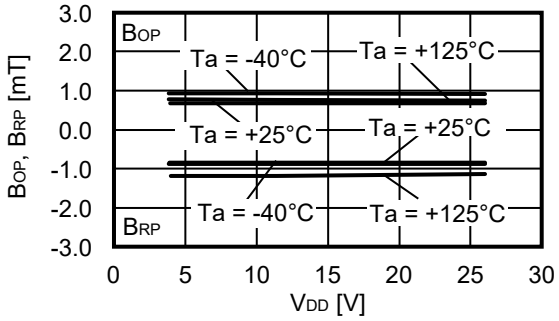
2. 1. 2 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



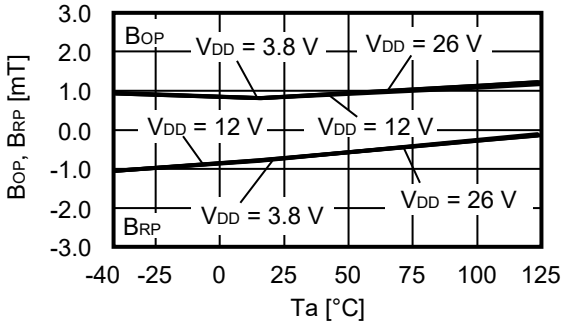
2. 1. 3 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



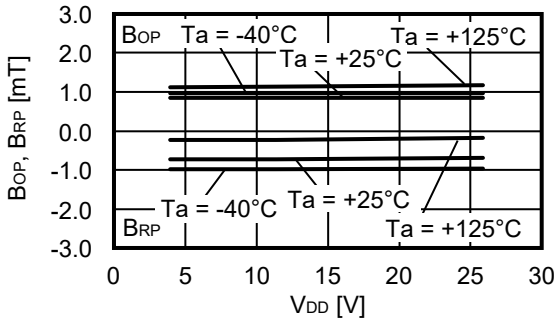
2. 1. 4 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



2. 1. 5 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



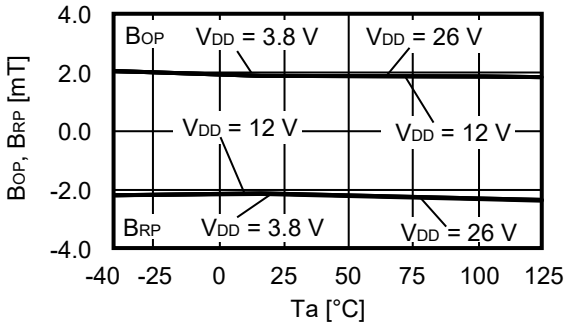
2. 1. 6 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



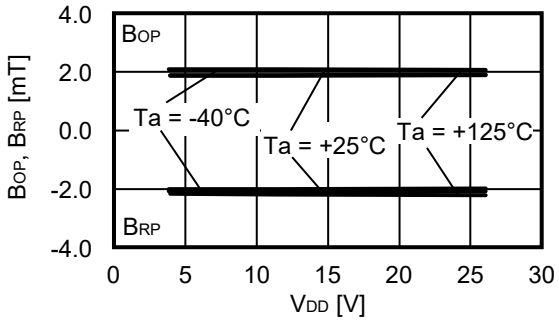
Caution V_{DD} = 3.8 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (10 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.

2. 2 S-579xxxx6B-M5T1U

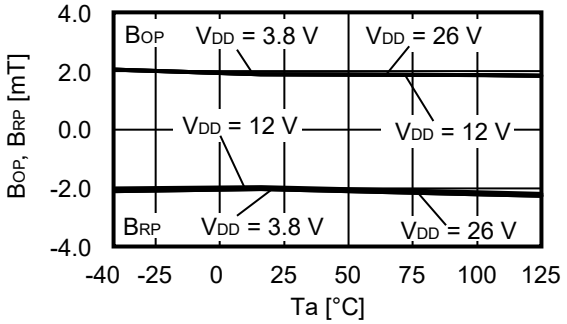
2. 2. 1 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



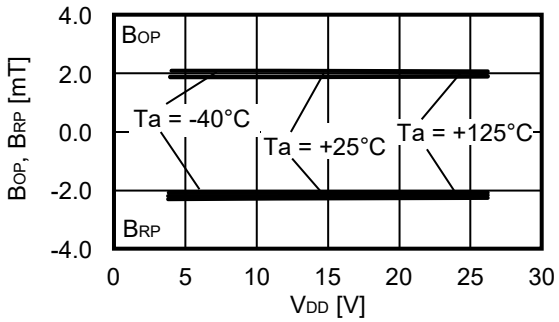
2. 2. 2 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



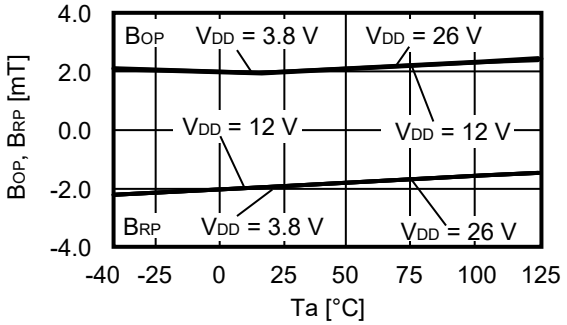
2. 2. 3 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



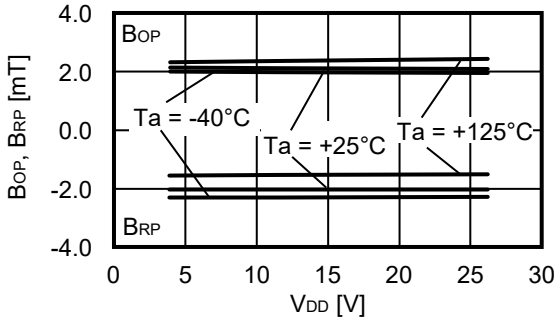
2. 2. 4 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



2. 2. 5 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



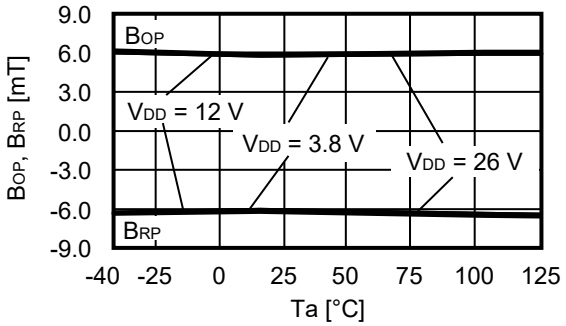
2. 2. 6 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



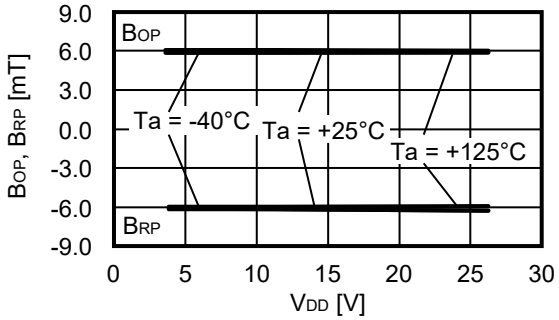
Caution **V_{DD} = 3.8 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (10 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

2. 3 S-579xxxx2B-M5T1U

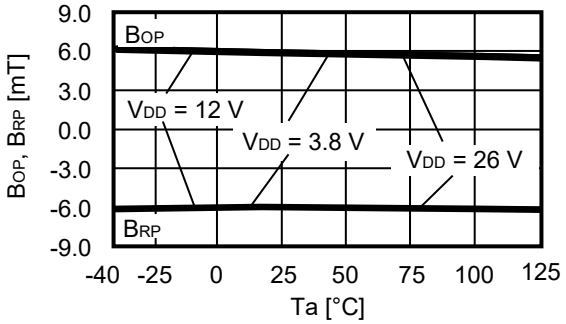
2. 3. 1 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



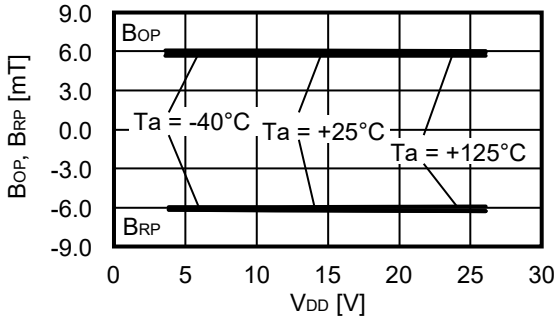
2. 3. 2 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



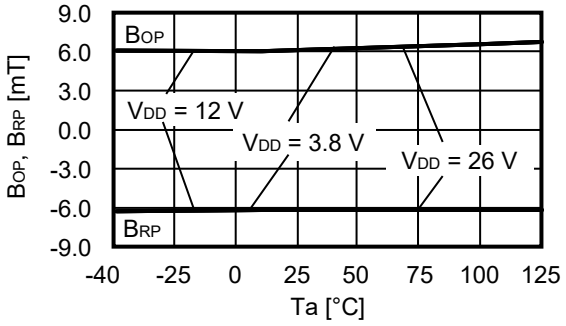
2. 3. 3 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



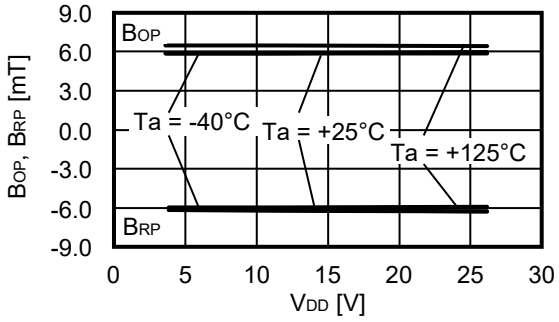
2. 3. 4 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



2. 3. 5 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



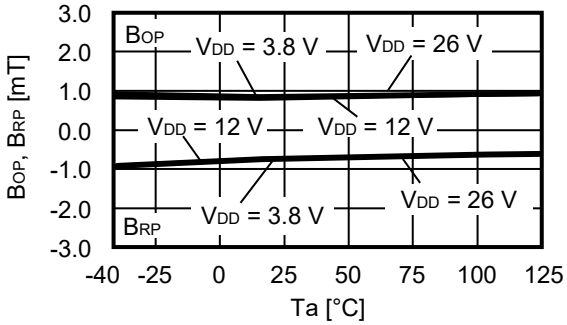
2. 3. 6 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



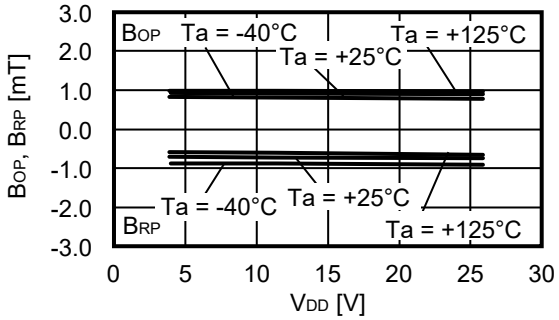
Caution **V_{DD} = 3.8 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (10 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

2. 4 S-579xxxx9B-A6T8U

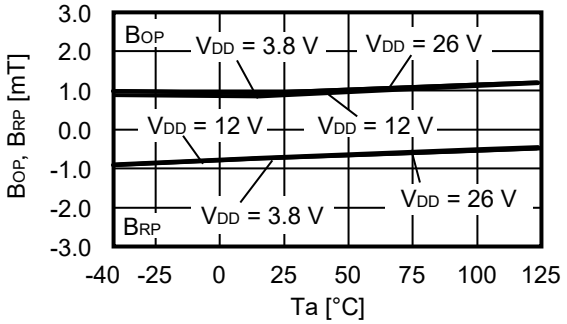
2. 4. 1 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



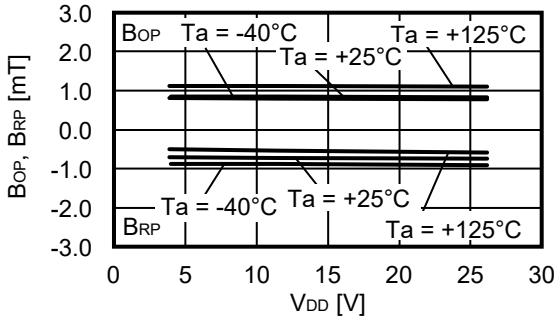
2. 4. 2 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



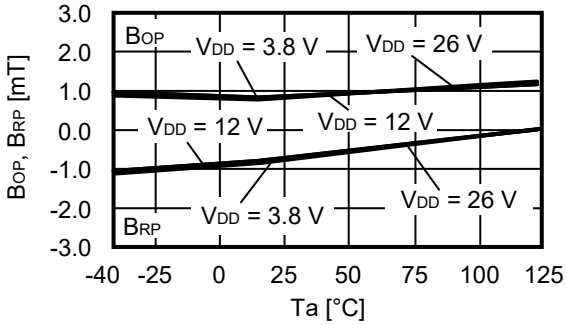
2. 4. 3 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



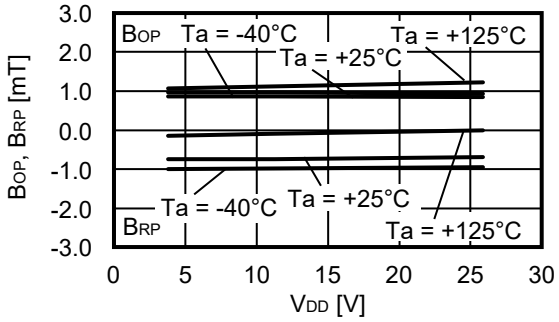
2. 4. 4 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



2. 4. 5 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



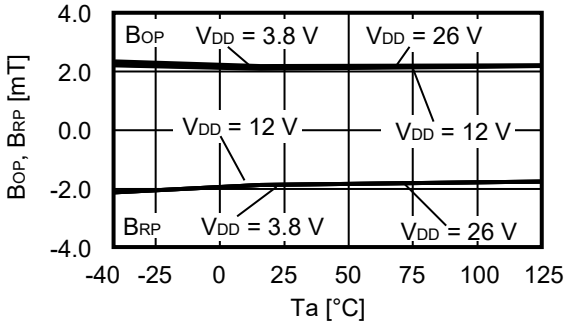
2. 4. 6 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



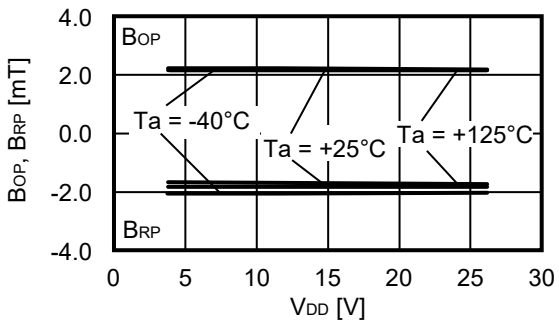
Caution **V_{DD} = 3.8 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (10 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

2. 5 S-579xxxx6B-A6T8U

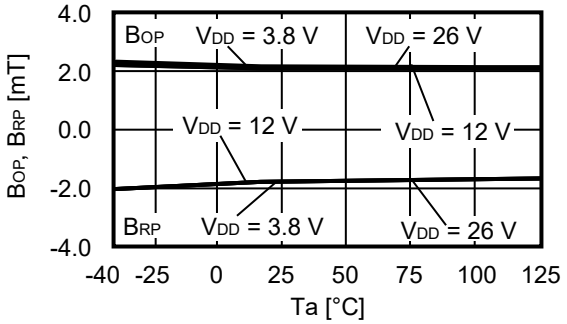
2. 5. 1 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



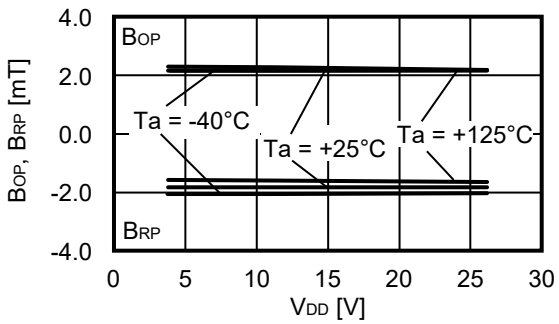
2. 5. 2 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



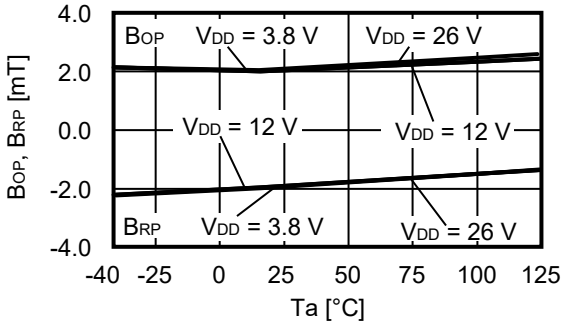
2. 5. 3 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



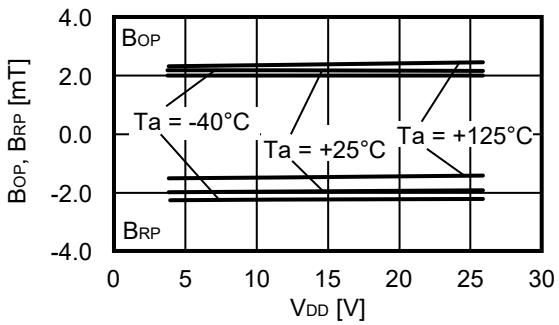
2. 5. 4 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



2. 5. 5 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



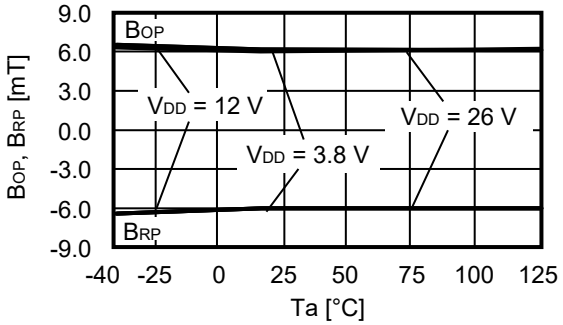
2. 5. 6 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



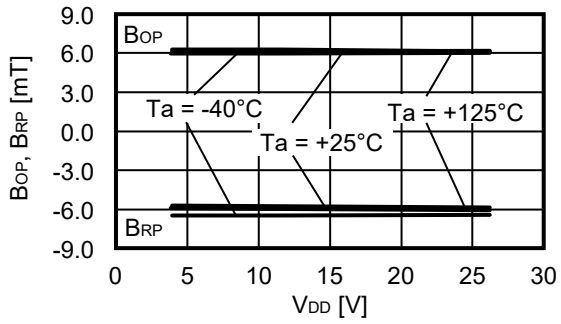
Caution **V_{DD} = 3.8 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (10 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

2. 6 S-579xxxx2B-A6T8U

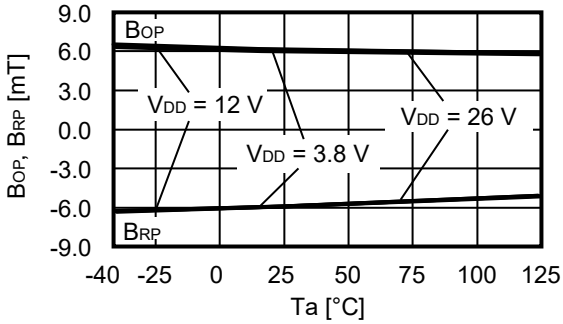
2. 6. 1 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



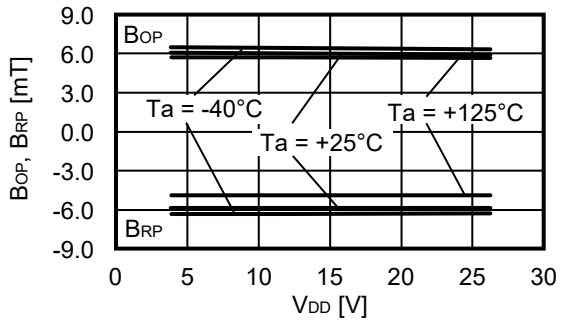
2. 6. 2 Z-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



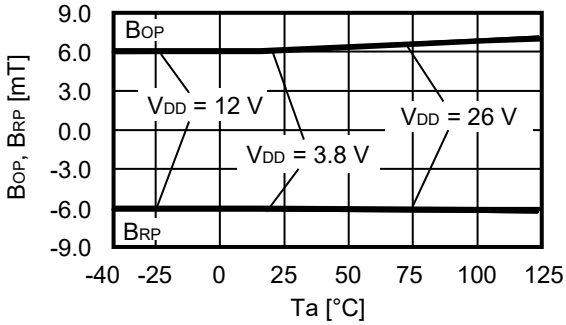
2. 6. 3 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



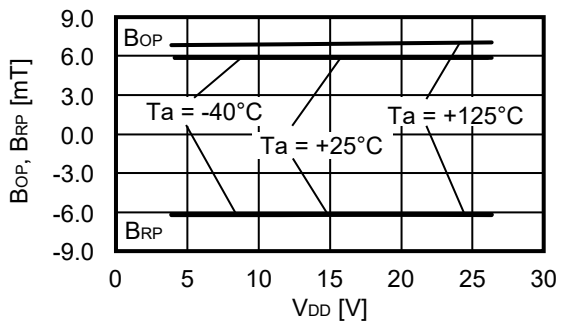
2. 6. 4 X-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



2. 6. 5 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



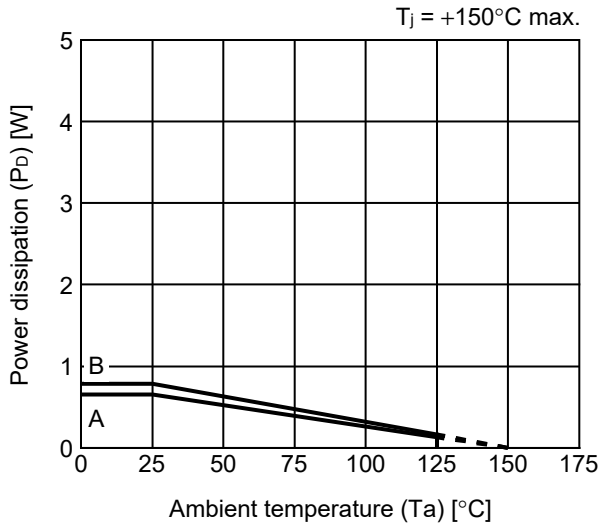
2. 6. 6 Y-axis: Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



Caution **V_{DD} = 3.8 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (10 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

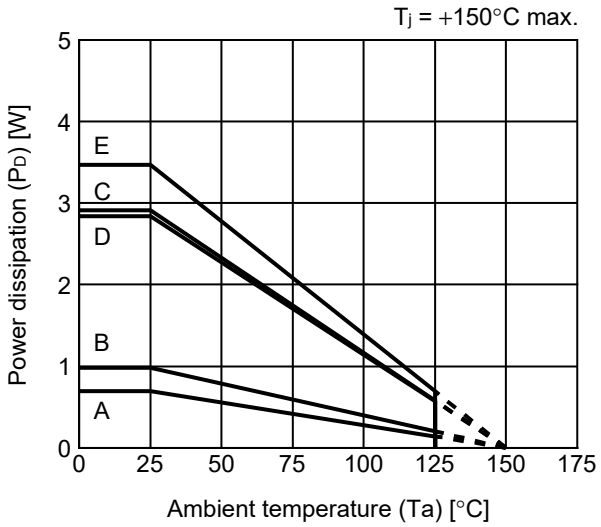
■ Power Dissipation

SOT-23-5



Board	Power Dissipation (P_D)
A	0.65 W
B	0.78 W
C	-
D	-
E	-

HSNT-6(2025)

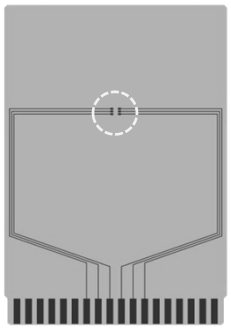


Board	Power Dissipation (P_D)
A	0.69 W
B	0.98 W
C	2.91 W
D	2.84 W
E	3.47 W

SOT-23-3/3S/5/6 Test Board

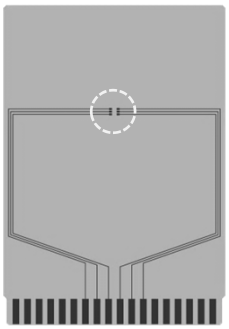
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



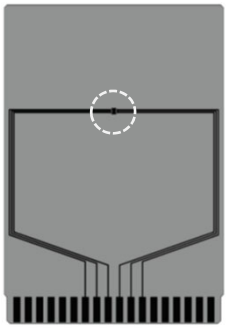
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SOT23x-A-Board-SD-2.0

HSNT-6(2025) Test Board

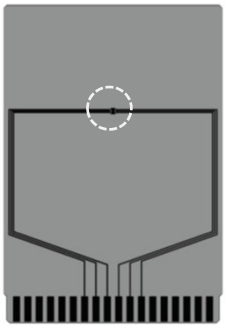
IC Mount Area

(1) Board A



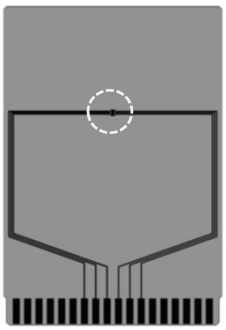
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

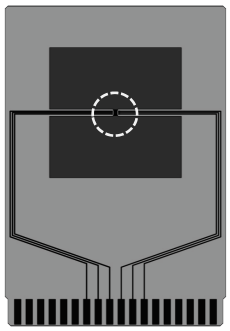
enlarged view

No. HSNT6-B-Board-SD-1.0

HSNT-6(2025) Test Board

IC Mount Area

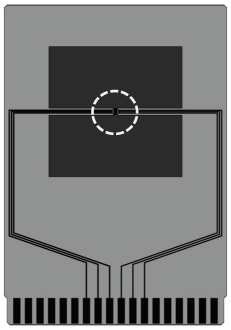
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

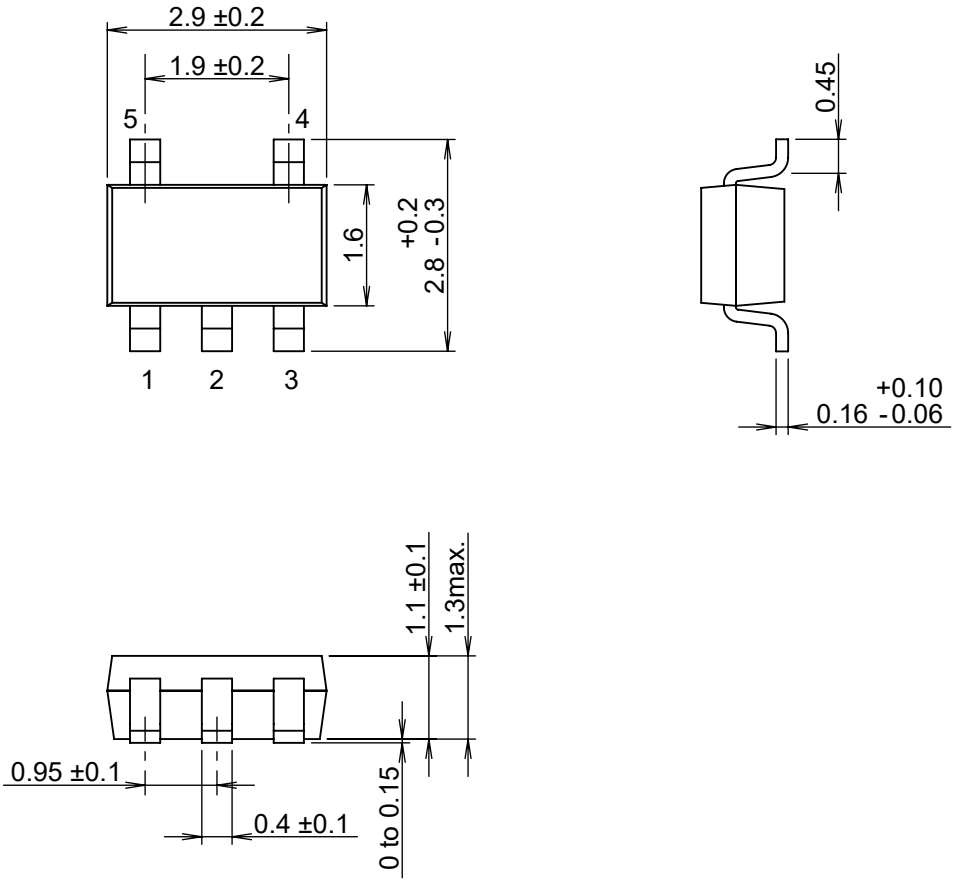
(5) Board E



enlarged view

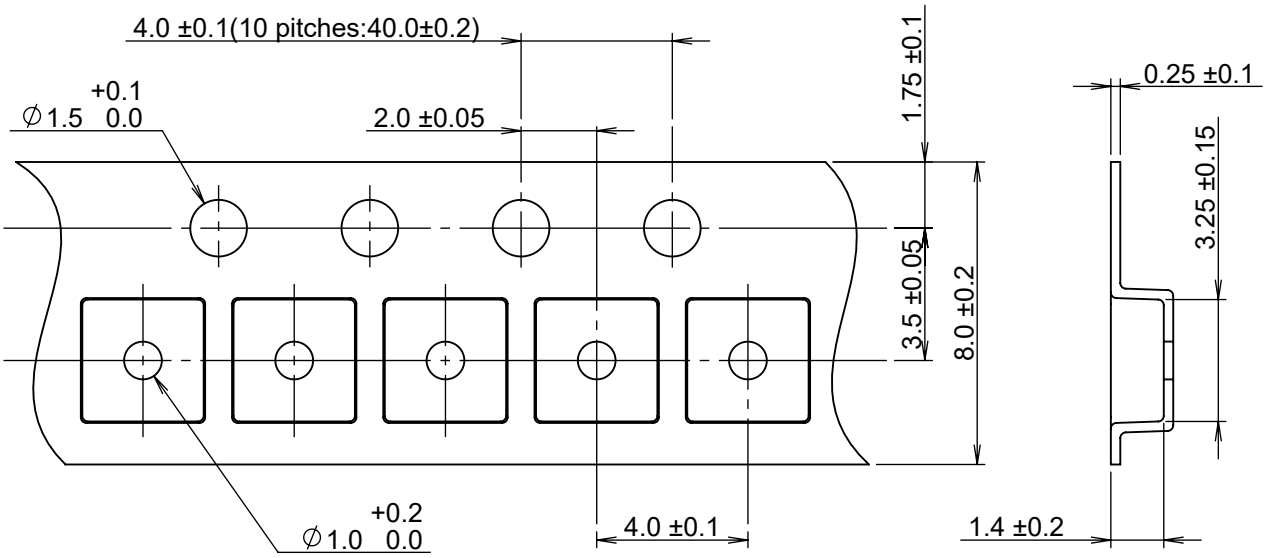
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

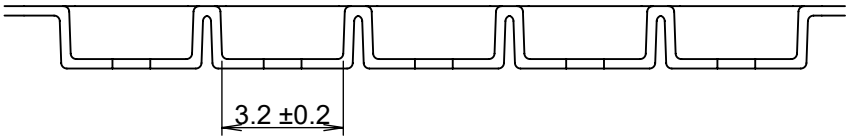
No. HSNT6-B-Board-SD-1.0

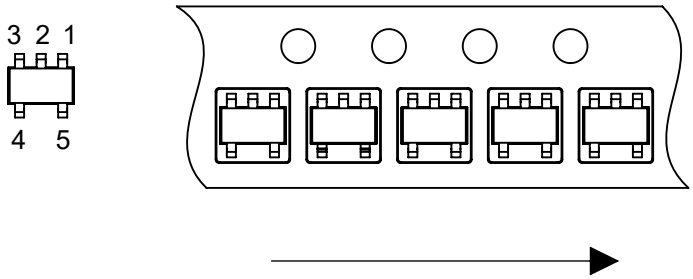


No. MP005-A-P-SD-1.3

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm
ABLIC Inc.	

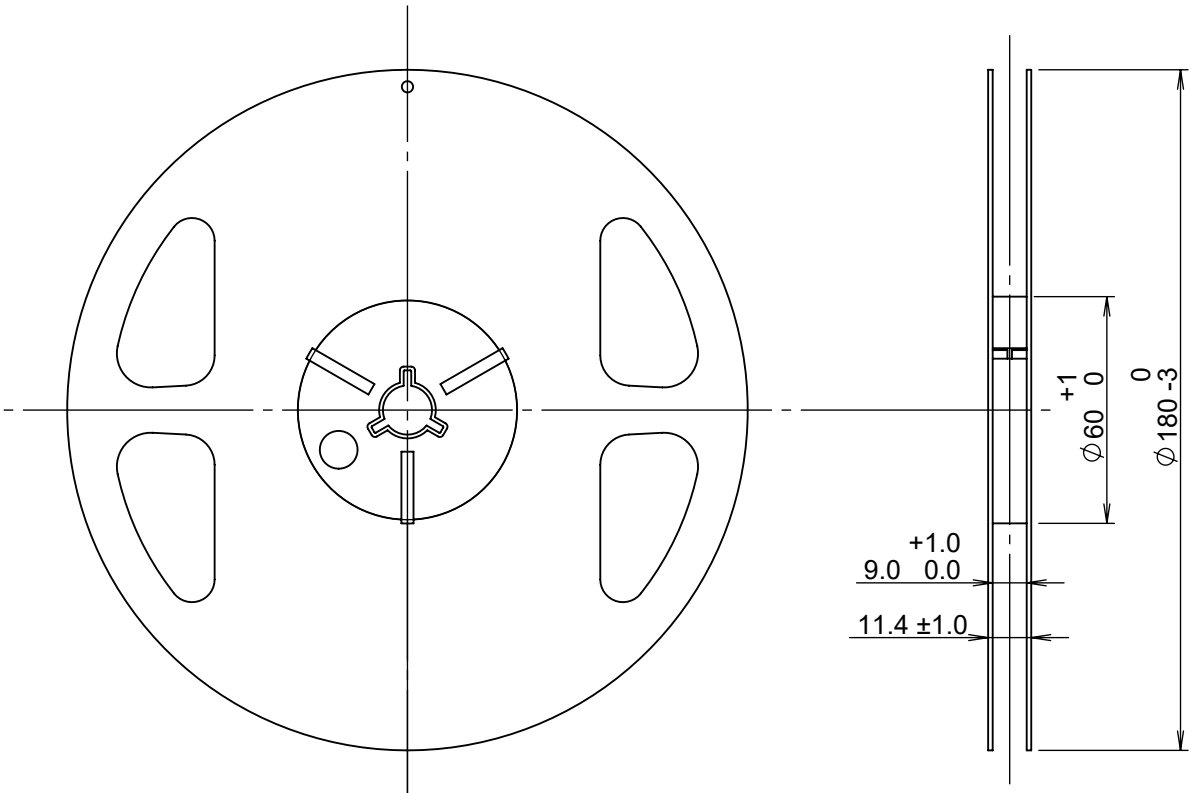




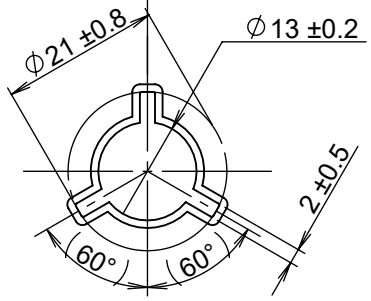


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

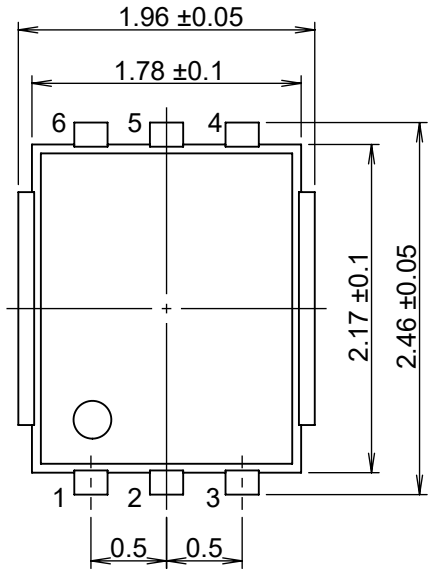


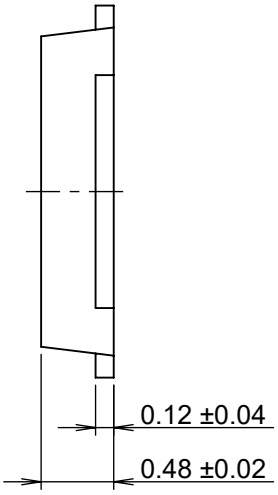
Enlarged drawing in the central part

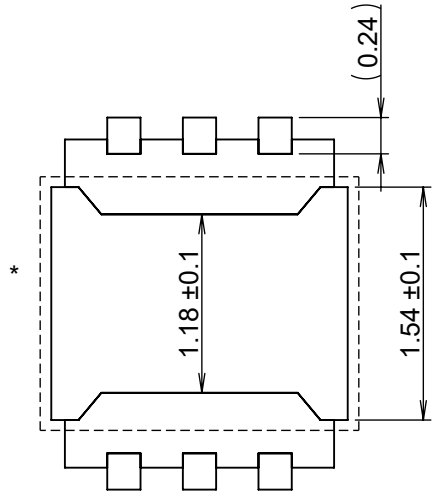


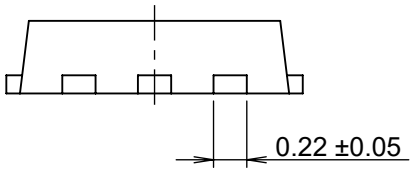
No. MP005-A-R-SD-2.0

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-2.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			





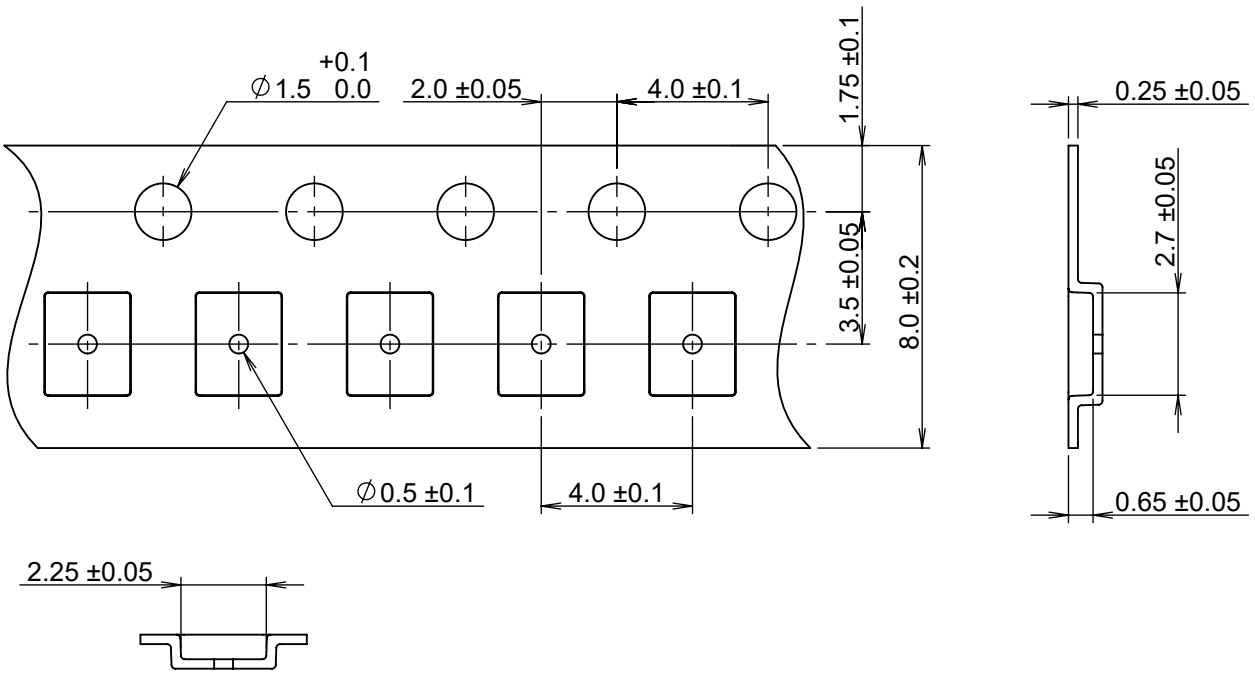


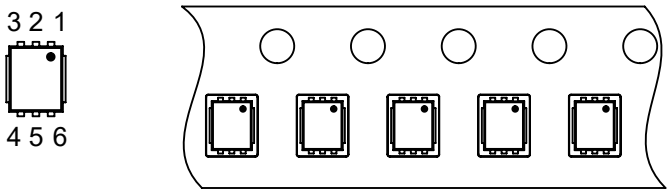


* The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PJ006-B-P-SD-1.0

TITLE	HSNT-6-C-PKG Dimensions
No.	PJ006-B-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

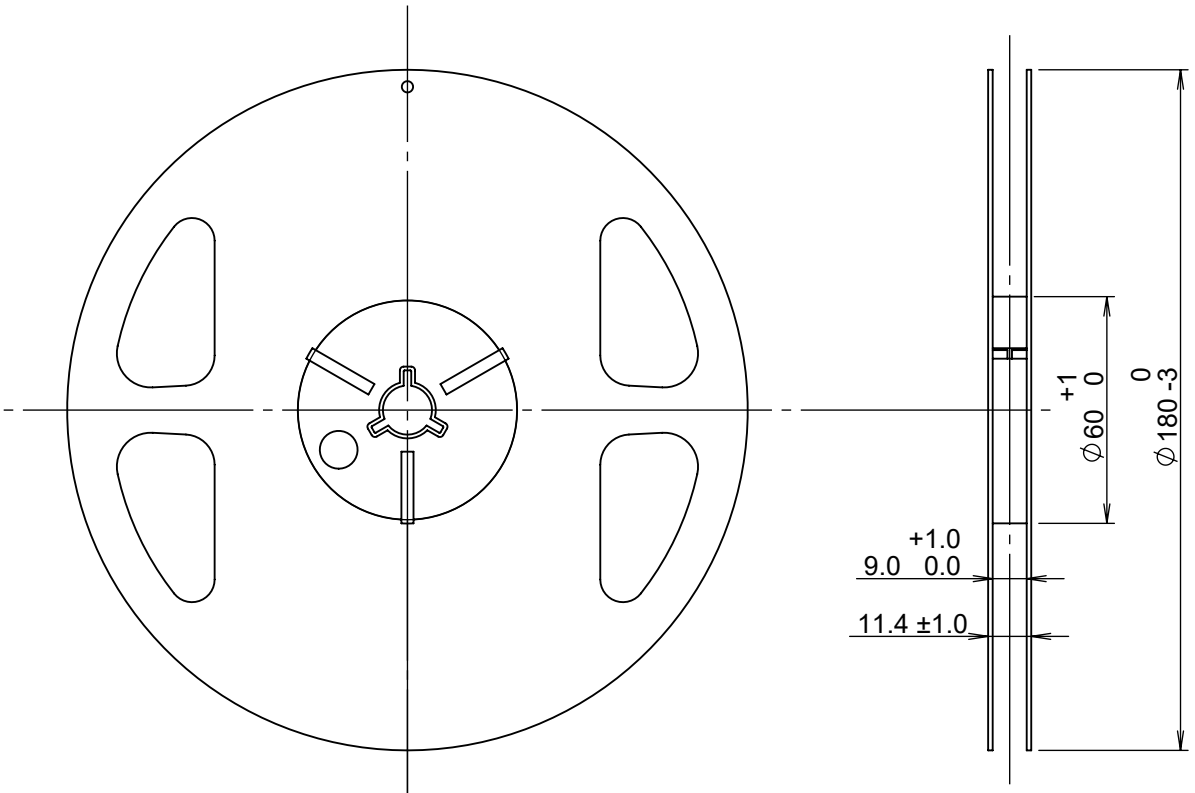




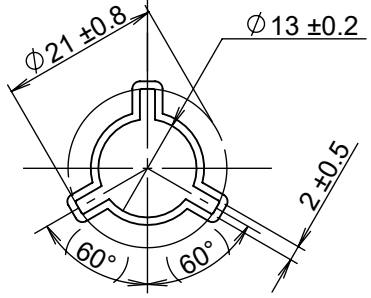
Feed direction

No. PJ006-B-C-SD-1.0

TITLE	HSNT-6-C-Carrier Tape
No.	PJ006-B-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



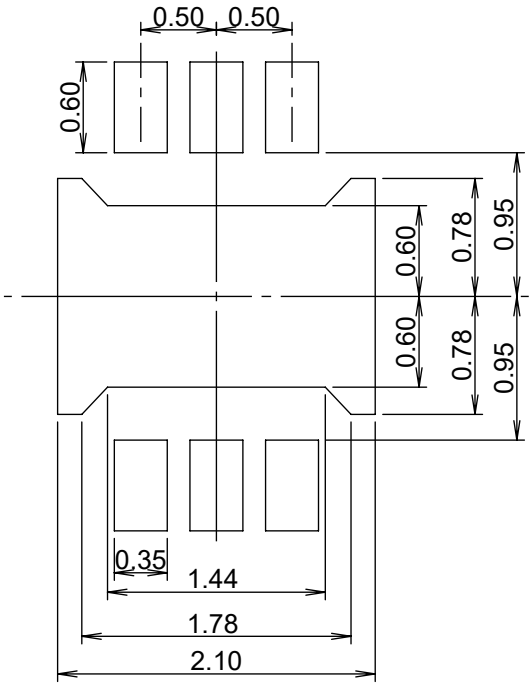
Enlarged drawing in the central part



No. PJ006-B-R-SD-1.0

TITLE	HSNT-6-C-Reel		
No.	PJ006-B-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

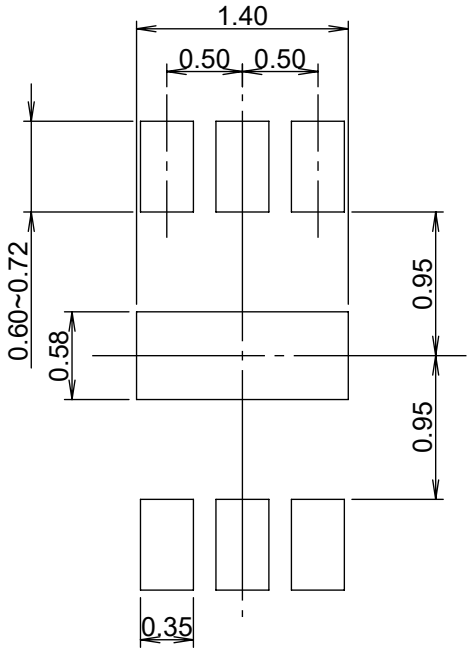
Land Recommendation



Caution　It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意　放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けすることを推奨いたします。

Stencil Opening



No. PJ006-B-LM-SD-1.0

Caution
① Mask aperture ratio of the lead mounting part is 100%~120%.
② Mask aperture ratio of the heat sink mounting part is 30%.
③ Mask thickness: t0.12mm
④ Reflow atmosphere:Nitrogen atmosphere is recommended.
(Oxygen concentration: 1000ppm or less)

注意
① リード実装部のマスク開口率は100%~120%です。
② 放熱板実装のマスク開口率は30%です。
③ マスク厚み: t0.12mm
④ リフロー雰囲気・窒素雰囲気
（酸素濃度1000ppm以下）推奨

TITLE	HSNT-6-C -Land &Stencil Opening
No.	PJ006-B-LM-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07