This IC is a protection IC for lithium-ion / lithium polymer rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. It is suitable for protecting 2-serial-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, and overcurrent. Use of an external overcurrent detection resistor enables this IC to provide high-accuracy overcurrent protection with less impact from temperature changes.

The S-82B2A Series has an input pin for charge-discharge control signal (CTL pin), allowing for charge-discharge control with an external signal. The S-82B2B Series has an input pin for power-saving signal (PS pin), allowing for reduction of current consumption by using an external signal to start the power-saving function.

**Features**

- High-accuracy voltage detection circuit
  - Overcharge detection voltage \( n \): 3.500 V to 4.800 V (5 mV step)  
    Accuracy \( \pm 20 \text{ mV} \)
  - Overcharge release voltage \( n \): 3.100 V to 4.800 V\(^*1\)  
    Accuracy \( \pm 50 \text{ mV} \)
  - Overdischarge detection voltage \( n \): 2.000 V to 3.000 V (10 mV step)  
    Accuracy \( \pm 50 \text{ mV} \)
  - Overdischarge release voltage \( n \): 2.000 V to 3.400 V\(^*2\)  
    Accuracy \( \pm 75 \text{ mV} \)
  - Discharge overcurrent 1 detection voltage: 3 mV to 100 mV (0.5 mV step)  
    Accuracy \( \pm 3.0 \text{ mV} \)
  - Discharge overcurrent 2 detection voltage: 10 mV to 100 mV (1 mV step)  
    Accuracy \( \pm 5 \text{ mV} \)
  - Load short-circuiting detection voltage: 20 mV to 100 mV (1 mV step)  
    Accuracy \( \pm 10 \text{ mV} \)
  - Charge overcurrent detection voltage: −100 mV to −3 mV (0.5 mV step)  
    Accuracy \( \pm 3.0 \text{ mV} \)

- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary).

- Charge-discharge control function (S-82B2A Series)
  - CTL pin control logic: Active "H", active "L"
  - CTL pin internal resistance connection: Pull-up, pull-down
  - CTL pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)

- Power-saving function (S-82B2B Series)
  - PS pin control logic: Active "H", active "L"
  - PS pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)

- 0 V battery charge: Enabled, inhibited

- Power-down function:
  - S-82B2A Series: Available, unavailable
  - S-82B2B Series: Available

- High-withstand voltage:
  - VM pin and CO pin: Absolute maximum rating 28 V

- Wide operation temperature range:
  - \( Ta = -40°C \) to \( +85°C \)

- Low current consumption
  - During operation: 3.0 μA typ., 6.0 μA max. (\( Ta = +25°C \))
  - During power-down: 50 nA max. (\( Ta = +25°C \))
  - During overdischarge: 1.0 μA max. (\( Ta = +25°C \))
  - During power-saving (S-82B2B Series): 50 nA max. (\( Ta = +25°C \))

- Lead-free (Sn 100%), halogen-free

\*1. Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage  
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)

\*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage  
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)
- Block Diagram

1. S-82B2A Series

![Block Diagram]

Figure 1
2. S-82B2B Series

- Overcharge detection comparator 1
- Overdischarge detection comparator 1
- Overcharge detection comparator 2
- Overdischarge detection comparator 2
- Discharge overcurrent 1 detection comparator
- Discharge overcurrent 2 detection comparator
- Load short-circuiting detection comparator
- Charge overcurrent detection comparator
- Charger detection comparator
- Pull-up / pull-down selection circuit
- Control logic
- Delay circuit
- Oscillator

Figure 2
## Product Name Structure

1. **Product name**

   
   ![Diagram of product name structure]

   - **Environmental code**
     - U: Lead-free (Sn 100%), halogen-free
   - **Package abbreviation and IC packing specifications**
     - I8T1: SNT-8A, Tape
     - A8T2: HSNT-8(1616), Tape
   - **Serial code**
     - Sequentially set from AA to ZZ
   - **Product type**
     - A: Charge-discharge control function
     - B: Power-saving function

   *1. Refer to the tape drawing.*
   *2. Refer to "3. Product name list".*

2. **Package**

   **Table 1 Package Drawing Codes**

<table>
<thead>
<tr>
<th>Package Name</th>
<th>Dimension</th>
<th>Tape</th>
<th>Reel</th>
<th>Land</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNT-8A</td>
<td>PH008-A-P-SD</td>
<td>PH008-A-C-SD</td>
<td>PH008-A-R-SD</td>
<td>PH008-A-L-SD</td>
</tr>
<tr>
<td>HSNT-8(1616)</td>
<td>PY008-A-P-SD</td>
<td>PY008-A-C-SD</td>
<td>PY008-A-R-SD</td>
<td>PY008-A-L-SD</td>
</tr>
</tbody>
</table>
3. Product name list

3.1 S-82B2A Series

3.1.1 SNT-8A

Table 2 (1 / 3)

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Overcharge Detection Voltage ([V_{CU}])</th>
<th>Overcharge Release Voltage ([V_{CL}])</th>
<th>Overdischarge Detection Voltage ([V_{DL}])</th>
<th>Overdischarge Release Voltage ([V_{DL}])</th>
<th>Discharge Overcurrent 1 Detection Voltage ([V_{DIOV1}])</th>
<th>Discharge Overcurrent 2 Detection Voltage ([V_{DIOV2}])</th>
<th>Load Short-circuiting Detection Voltage ([V_{SHORT}])</th>
<th>Charge Overcurrent Detection Voltage ([V_{CIOV}])</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2AAA-I8T1U7</td>
<td>4.230 V</td>
<td>4.080 V</td>
<td>2.700 V</td>
<td>2.900 V</td>
<td>25.0 mV</td>
<td>50 mV</td>
<td>100 mV</td>
<td>−15.0 mV</td>
</tr>
</tbody>
</table>

Table 2 (2 / 3)

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Overcharge Detection Delay Time ([t_{CU}])</th>
<th>Overdischarge Detection Delay Time ([t_{CL}])</th>
<th>Discharge Overcurrent 1 Detection Delay Time ([t_{DIOV1}])</th>
<th>Discharge Overcurrent 2 Detection Delay Time ([t_{DIOV2}])</th>
<th>Load Short-circuiting Detection Delay Time ([t_{SHORT}])</th>
<th>Charge Overcurrent Detection Delay Time ([t_{CIOV}])</th>
<th>Charge-discharge Inhibition Delay Time ([t_{CTL}])</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2AAA-I8T1U7</td>
<td>1.0 s</td>
<td>128 ms</td>
<td>512 ms</td>
<td>16 ms</td>
<td>280 μs</td>
<td>8 ms</td>
<td>48 ms</td>
</tr>
</tbody>
</table>

Table 2 (3 / 3)

<table>
<thead>
<tr>
<th>Product Name</th>
<th>CTL Pin Control Logic(^1)</th>
<th>CTL Pin Internal Resistance Connection(^2)</th>
<th>CTL Pin Internal Resistance Value(^3)</th>
<th>CTL Pin Voltage &quot;H&quot; ([V_{CTLH}])</th>
<th>CTL Pin Voltage &quot;L&quot; ([V_{CTLL}])</th>
<th>0 V Battery Charge(^6)</th>
<th>Power-down Function(^7)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2AAA-I8T1U7</td>
<td>Active &quot;H&quot;</td>
<td>Pull-down</td>
<td>3 MΩ</td>
<td>VDD − 0.90 V</td>
<td>VSS + 0.70 V</td>
<td>Inhibited</td>
<td>Available</td>
</tr>
</tbody>
</table>

\(^1\) CTL pin control logic: Active "H", active "L"
\(^2\) CTL pin internal resistance connection: Pull-up, pull-down
\(^3\) CTL pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)
\(^4\) CTL pin voltage "H": VSS + 0.75 V, VDD − 0.90 V
\(^5\) CTL pin voltage "L": VSS + 0.70 V, VDD − 0.95 V
\(^6\) 0 V battery charge: Enabled, inhibited
\(^7\) Power-down function: Available, unavailable

Remark 1. Please contact our sales representatives for products other than the above.
Remark 2. The delay times can be changed within the range listed in Table 6.
For details, please contact our sales representatives.
### Table 3 (1 / 3)

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Overcharge Detection Voltage ([V_{CU}])</th>
<th>Overcharge Release Voltage ([V_{CL}])</th>
<th>Overdischarge Detection Voltage ([V_{DL}])</th>
<th>Overdischarge Release Voltage ([V_{DU}])</th>
<th>Discharge Overcurrent 1 Detection Voltage ([V_{DIOV1}])</th>
<th>Discharge Overcurrent 2 Detection Voltage ([V_{DIOV2}])</th>
<th>Load Short-circuiting Detection Voltage ([V_{SHORT}])</th>
<th>Charge Overcurrent Detection Voltage ([V_{CIOV}])</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2AAA-A8T2U7</td>
<td>4.230 V</td>
<td>4.080 V</td>
<td>2.700 V</td>
<td>2.900 V</td>
<td>25.0 mV</td>
<td>50 mV</td>
<td>100 mV</td>
<td>−15.0 mV</td>
</tr>
</tbody>
</table>

### Table 3 (2 / 3)

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Overcharge Detection Delay Time ([t_{CU}])</th>
<th>Overdischarge Detection Delay Time ([t_{DL}])</th>
<th>Discharge Overcurrent 1 Detection Delay Time ([t_{DIOV1}])</th>
<th>Discharge Overcurrent 2 Detection Delay Time ([t_{DIOV2}])</th>
<th>Load Short-circuiting Detection Delay Time ([t_{SHORT}])</th>
<th>Charge Overcurrent Detection Delay Time ([t_{CIOV}])</th>
<th>Charge-discharge Inhibition Delay Time ([t_{CTL}])</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2AAA-A8T2U7</td>
<td>1.0 s</td>
<td>128 ms</td>
<td>512 ms</td>
<td>16 ms</td>
<td>280 μs</td>
<td>8 ms</td>
<td>48 ms</td>
</tr>
</tbody>
</table>

### Table 3 (3 / 3)

<table>
<thead>
<tr>
<th>Product Name</th>
<th>CTL Pin Control Logic(^1)</th>
<th>CTL Pin Internal Resistance Connection(^2)</th>
<th>CTL Pin Internal Resistance Value(^3)</th>
<th>CTL Pin Voltage &quot;H&quot;(^*4) (\left[V_{CTU}\right])</th>
<th>CTL Pin Voltage &quot;L&quot;(^*5) (\left[V_{CTL}\right])</th>
<th>0 V Battery Charge(^*6)</th>
<th>Power-down Function(^7)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2AAA-A8T2U7</td>
<td>Active &quot;H&quot;</td>
<td>Pull-down</td>
<td>3 MΩ</td>
<td>Vdd − 0.90 V</td>
<td>Vss + 0.70 V</td>
<td>Inhibited</td>
<td>Available</td>
</tr>
</tbody>
</table>

\(^{1}\) CTL pin control logic: Active "H", active "L"

\(^{2}\) CTL pin internal resistance connection: Pull-up, pull-down

\(^{3}\) CTL pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)

\(^{4}\) CTL pin voltage "H": Vss + 0.75 V, Vdd − 0.90 V

\(^{5}\) CTL pin voltage "L": Vss + 0.70 V, Vdd − 0.95 V

\(^{6}\) 0 V battery charge: Enabled, inhibited

\(^{7}\) Power-down function: Available, unavailable

**Remark 1.** Please contact our sales representatives for products other than the above.

2. The delay times can be changed within the range listed in Table 6.

For details, please contact our sales representatives.
### 3. 2 S-82B2B Series

#### 3. 2. 1 SNT-8A

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Overcharge Detection Voltage $[V_{CU}]$</th>
<th>Overcharge Release Voltage $[V_{CL}]$</th>
<th>Overdischarge Detection Voltage $[V_{DL}]$</th>
<th>Overdischarge Release Voltage $[V_{DU}]$</th>
<th>Discharge Overcurrent 1 Detection Voltage $[V_{DOV1}]$</th>
<th>Discharge Overcurrent 2 Detection Voltage $[V_{DOV2}]$</th>
<th>Load Short-circuiting Detection Voltage $[V_{SHORT}]$</th>
<th>Charge Overcurrent Detection Voltage $[V_{CIOV}]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2BAA-I8T1U7</td>
<td>4.475 V</td>
<td>4.325 V</td>
<td>2.100 V</td>
<td>2.300 V</td>
<td>7.0 mV</td>
<td>15 mV</td>
<td>30 mV</td>
<td>−7.0 mV</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Overcharge Detection Delay Time $[t_{CU}]$</th>
<th>Overdischarge Detection Delay Time $[t_{DL}]$</th>
<th>Discharge Overcurrent 1 Detection Delay Time $[t_{DOV1}]$</th>
<th>Discharge Overcurrent 2 Detection Delay Time $[t_{DOV2}]$</th>
<th>Load Short-circuiting Detection Delay Time $[t_{SHORT}]$</th>
<th>Charge Overcurrent Detection Delay Time $[t_{CIOV}]$</th>
<th>Power-saving Delay Time $[t_{PS}]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2BAA-I8T1U7</td>
<td>1.0 s</td>
<td>64 ms</td>
<td>3.75 s</td>
<td>16 ms</td>
<td>280 μs</td>
<td>16 ms</td>
<td>2 ms</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Product Name</th>
<th>PS Pin Control Logic</th>
<th>PS Pin Internal Resistance Value $[R_{PS}]$</th>
<th>PS Pin Voltage &quot;H&quot; $[V_{PSH}]$</th>
<th>PS Pin Voltage &quot;L&quot; $[V_{PSL}]$</th>
<th>0 V Battery Charge</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2BAA-I8T1U7</td>
<td>Active &quot;H&quot;</td>
<td>5 MΩ</td>
<td>VDD − 0.90 V</td>
<td>VSS + 0.70 V</td>
<td>Inhibited</td>
</tr>
</tbody>
</table>

*1. PS pin control logic: Active "H", active "L"

*2. PS pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)

*3. PS pin voltage "H": VSS + 0.75 V, VDD − 0.90 V

*4. PS pin voltage "L": VSS + 0.70 V, VDD − 0.95 V

*5. 0 V battery charge: Enabled, inhibited

**Remark**

1. Please contact our sales representatives for products other than the above.

2. The delay times can be changed within the range listed in Table 6.

For details, please contact our sales representatives.
3. 2. 2 HSNT-8(1616)

Table 5 (1 / 3)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2BAA-A8T2U7</td>
<td>4.475 V</td>
<td>4.325 V</td>
<td>2.100 V</td>
<td>2.300 V</td>
<td>7.0 mV</td>
<td>15 mV</td>
<td>30 mV</td>
<td>−7.0 mV</td>
</tr>
</tbody>
</table>

Table 5 (2 / 3)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2BAA-A8T2U7</td>
<td>1.0 s</td>
<td>64 ms</td>
<td>3.75 s</td>
<td>16 ms</td>
<td>280 µs</td>
<td>16 ms</td>
<td>2 ms</td>
</tr>
</tbody>
</table>

Table 5 (3 / 3)

<table>
<thead>
<tr>
<th>Product Name</th>
<th>PS Pin Control Logic¹</th>
<th>PS Pin Internal Resistance Value² [R PS]</th>
<th>PS Pin Voltage &quot;H&quot;³ [V PS]</th>
<th>PS Pin Voltage &quot;L&quot;⁴ [V PS]</th>
<th>0 V Battery Charge⁵</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2BAA-A8T2U7</td>
<td>Active &quot;H&quot;</td>
<td>5 MΩ</td>
<td>V DD − 0.90 V</td>
<td>V SS + 0.70 V</td>
<td>Inhibited</td>
</tr>
</tbody>
</table>

¹. PS pin control logic: Active "H", active "L"
². PS pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)
³. PS pin voltage "H": V SS + 0.75 V, V DD − 0.90 V
⁴. PS pin voltage "L": V SS + 0.70 V, V DD − 0.95 V
⁵. 0 V battery charge: Enabled, inhibited

Remark 1. Please contact our sales representatives for products other than the above.
Remark 2. The delay times can be changed within the range listed in Table 6.
Remark 3. For details, please contact our sales representatives.

Table 6

<table>
<thead>
<tr>
<th>Delay Time</th>
<th>Symbol</th>
<th>Selection Range</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overcharge detection delay time</td>
<td>t CU</td>
<td>256 ms, 512 ms</td>
<td>Select a value from the left.</td>
</tr>
<tr>
<td>Overdischarge detection delay time</td>
<td>t CL</td>
<td>32 ms, 64 ms, 128 ms</td>
<td>Select a value from the left.</td>
</tr>
<tr>
<td>Discharge overcurrent 1 detection delay time</td>
<td>t DOV1</td>
<td>8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms</td>
<td>Select a value from the left.</td>
</tr>
<tr>
<td>Discharge overcurrent 2 detection delay time</td>
<td>t DOV2</td>
<td>4 ms, 8 ms, 16 ms, 32 ms, 64 ms, 128 ms</td>
<td>Select a value from the left.</td>
</tr>
<tr>
<td>Load short-circuiting detection delay time</td>
<td>t SHORT</td>
<td>280 µs, 530 µs</td>
<td>Select a value from the left.</td>
</tr>
<tr>
<td>Charge overcurrent detection delay time</td>
<td>t COV</td>
<td>4 ms, 8 ms, 16 ms, 32 ms, 64 ms, 128 ms</td>
<td>Select a value from the left.</td>
</tr>
<tr>
<td>Charge-discharge inhibition delay time</td>
<td>t CTL</td>
<td>2 ms, 4 ms, 48 ms, 64 ms, 128 ms, 256 ms</td>
<td>Select a value from the left.</td>
</tr>
<tr>
<td>Power-saving delay time</td>
<td>t PS</td>
<td>2 ms, 4 ms, 48 ms, 64 ms, 128 ms, 256 ms</td>
<td>Select a value from the left.</td>
</tr>
</tbody>
</table>

ABLIC Inc.
**Pin Configuration**

1. SNT-8A

Table 7  S-82B2A Series

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CTL</td>
<td>Input pin for charge-discharge control signal</td>
</tr>
<tr>
<td>2</td>
<td>VM</td>
<td>Input pin for external negative voltage</td>
</tr>
<tr>
<td>3</td>
<td>CO</td>
<td>Connection pin of charge control FET gate (CMOS output)</td>
</tr>
<tr>
<td>4</td>
<td>DO</td>
<td>Connection pin of discharge control FET gate (CMOS output)</td>
</tr>
<tr>
<td>5</td>
<td>VINI</td>
<td>Overcurrent detection pin</td>
</tr>
<tr>
<td>6</td>
<td>VSS</td>
<td>Input pin for negative power supply, connection pin for negative voltage of battery 2</td>
</tr>
<tr>
<td>7</td>
<td>VC</td>
<td>Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2</td>
</tr>
<tr>
<td>8</td>
<td>VDD</td>
<td>Input pin for positive power supply, connection pin for positive voltage of battery 1</td>
</tr>
</tbody>
</table>

Table 8  S-82B2B Series

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PS</td>
<td>Input pin for power-saving signal</td>
</tr>
<tr>
<td>2</td>
<td>VM</td>
<td>Input pin for external negative voltage</td>
</tr>
<tr>
<td>3</td>
<td>CO</td>
<td>Connection pin of charge control FET gate (CMOS output)</td>
</tr>
<tr>
<td>4</td>
<td>DO</td>
<td>Connection pin of discharge control FET gate (CMOS output)</td>
</tr>
<tr>
<td>5</td>
<td>VINI</td>
<td>Overcurrent detection pin</td>
</tr>
<tr>
<td>6</td>
<td>VSS</td>
<td>Input pin for negative power supply, connection pin for negative voltage of battery 2</td>
</tr>
<tr>
<td>7</td>
<td>VC</td>
<td>Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2</td>
</tr>
<tr>
<td>8</td>
<td>VDD</td>
<td>Input pin for positive power supply, connection pin for positive voltage of battery 1</td>
</tr>
</tbody>
</table>
2. HSNT-8(1616)

Figure 4

Table 9  S-82B2A Series

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CTL</td>
<td>Input pin for charge-discharge control signal</td>
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<td>CO</td>
<td>Connection pin of charge control FET gate (CMOS output)</td>
</tr>
<tr>
<td>4</td>
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</tr>
<tr>
<td>5</td>
<td>VINI</td>
<td>Overcurrent detection pin</td>
</tr>
<tr>
<td>6</td>
<td>VSS</td>
<td>Input pin for negative power supply, connection pin for negative voltage of battery 2</td>
</tr>
<tr>
<td>7</td>
<td>VC</td>
<td>Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2</td>
</tr>
<tr>
<td>8</td>
<td>VDD</td>
<td>Input pin for positive power supply, connection pin for positive voltage of battery 1</td>
</tr>
</tbody>
</table>

Table 10  S-82B2B Series

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PS</td>
<td>Input pin for power-saving signal</td>
</tr>
<tr>
<td>2</td>
<td>VM</td>
<td>Input pin for external negative voltage</td>
</tr>
<tr>
<td>3</td>
<td>CO</td>
<td>Connection pin of charge control FET gate (CMOS output)</td>
</tr>
<tr>
<td>4</td>
<td>DO</td>
<td>Connection pin of discharge control FET gate (CMOS output)</td>
</tr>
<tr>
<td>5</td>
<td>VINI</td>
<td>Overcurrent detection pin</td>
</tr>
<tr>
<td>6</td>
<td>VSS</td>
<td>Input pin for negative power supply, connection pin for negative voltage of battery 2</td>
</tr>
<tr>
<td>7</td>
<td>VC</td>
<td>Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2</td>
</tr>
<tr>
<td>8</td>
<td>VDD</td>
<td>Input pin for positive power supply, connection pin for positive voltage of battery 1</td>
</tr>
</tbody>
</table>

*1. Connect the heat sink of backside at shadowed area to the board, and set electric potential open or VDD. However, do not use it as the function of electrode.
## Absolute Maximum Ratings

### Table 11

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Applied Pin</th>
<th>Absolute Maximum Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage between VDD pin and VSS pin</td>
<td>$V_{DS}$</td>
<td>VDD</td>
<td>$V_{SS} - 0.3$ to $V_{SS} + 12$</td>
<td>V</td>
</tr>
<tr>
<td>VC pin input voltage</td>
<td>$V_{VC}$</td>
<td>VC</td>
<td>$V_{DD} - 12$ to $V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>VINI pin input voltage</td>
<td>$V_{VINI}$</td>
<td>VINI</td>
<td>$V_{DD} - 12$ to $V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>CTL pin input voltage (S-82B2A Series)</td>
<td>$V_{CTL}$</td>
<td>CTL</td>
<td>$V_{DD} - 12$ to $V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>PS pin input voltage (S-82B2B Series)</td>
<td>$V_{PS}$</td>
<td>PS</td>
<td>$V_{DD} - 12$ to $V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>VM pin input voltage</td>
<td>$V_{VM}$</td>
<td>VM</td>
<td>$V_{DD} - 28$ to $V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>DO pin output voltage</td>
<td>$V_{DO}$</td>
<td>DO</td>
<td>$V_{SS} - 0.3$ to $V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>CO pin output voltage</td>
<td>$V_{CO}$</td>
<td>CO</td>
<td>$V_{VM} - 0.3$ to $V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>Operation ambient temperature</td>
<td>$T_{opr}$</td>
<td>–</td>
<td>–40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td>–</td>
<td>−55 to +125</td>
<td>°C</td>
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</tbody>
</table>

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## Thermal Resistance Value

### Table 12

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction-to-ambient thermal resistance*1</td>
<td>$\theta_{JA}$</td>
<td>SNT-8A</td>
<td>–</td>
<td>211</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–</td>
<td>173</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HSNT-8(1616)</td>
<td>Board A</td>
<td>–</td>
<td>214</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–</td>
<td>172</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

*1. **Test environment:** compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ Power Dissipation" and "Test Board" for details.
## Electrical Characteristics

1. Ta = +25°C

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
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</thead>
<tbody>
<tr>
<td>Detection Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overcharge detection voltage n</td>
<td>VCU{n}</td>
<td>–</td>
<td>VCU – 0.020</td>
<td>VCU</td>
<td>VCU + 0.020</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Overcharge release voltage n</td>
<td>VCL{n}</td>
<td>VCL ≠ VCU</td>
<td>VCL – 0.050</td>
<td>VCL</td>
<td>VCL + 0.050</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Overdischarge detection voltage n</td>
<td>VDL{n}</td>
<td>–</td>
<td>VDL – 0.050</td>
<td>VDL</td>
<td>VDL + 0.050</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Overdischarge release voltage n</td>
<td>VDU{n}</td>
<td>VDL ≠ VDU</td>
<td>VDU – 0.075</td>
<td>VDU</td>
<td>VDU + 0.075</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Discharge overcurrent 1 detection voltage</td>
<td>VDIOV1</td>
<td>–</td>
<td>VDIOV1 – 3</td>
<td>VDIOV1</td>
<td>VDIOV1 + 3</td>
<td>mV</td>
<td>5</td>
</tr>
<tr>
<td>Discharge overcurrent 2 detection voltage</td>
<td>VDIOV2</td>
<td>–</td>
<td>VDIOV2 – 5</td>
<td>VDIOV2</td>
<td>VDIOV2 + 5</td>
<td>mV</td>
<td>2</td>
</tr>
<tr>
<td>Load short-circuiting detection voltage</td>
<td>VSHORT</td>
<td>–</td>
<td>VSHORT – 10</td>
<td>VSHORT</td>
<td>VSHORT + 10</td>
<td>mV</td>
<td>2</td>
</tr>
<tr>
<td>Load short-circuiting 2 detection voltage</td>
<td>VSHORT2</td>
<td>–</td>
<td>VDD – 1.2</td>
<td>VDD – 0.9</td>
<td>VDD – 0.6</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Charge overcurrent detection voltage</td>
<td>VCIOV</td>
<td>–</td>
<td>VCIOV – 3</td>
<td>VCIOV</td>
<td>VCIOV + 3</td>
<td>mV</td>
<td>2</td>
</tr>
<tr>
<td>Discharge overcurrent release voltage</td>
<td>VDIROV</td>
<td>V1 = V2 = 3.4 V</td>
<td>VDD – 1.3</td>
<td>VDD – 1.2</td>
<td>VDD – 1.1</td>
<td>V</td>
<td>5</td>
</tr>
<tr>
<td>0 V Battery Charge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>0 V battery charge starting charger voltage</td>
<td>V0CHA</td>
<td>0 V battery charge enabled</td>
<td>0.7</td>
<td>1.1</td>
<td>1.5</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td>0 V battery charge inhibition battery voltage n</td>
<td>V0INH{n}</td>
<td>0 V battery charge inhibited</td>
<td>1.00</td>
<td>1.25</td>
<td>1.40</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Internal Resistance</td>
<td></td>
<td></td>
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<tr>
<td>Resistance between VDD pin and VM pin</td>
<td>RVMD</td>
<td>V1 = V2 = 1.8 V, VVM = 0 V</td>
<td>1000</td>
<td>2500</td>
<td>5000</td>
<td>kΩ</td>
<td>3</td>
</tr>
<tr>
<td>Resistance between VDD pin and VM pin 2</td>
<td>RVMD2</td>
<td>S-82B2B Series</td>
<td>12</td>
<td>18</td>
<td>24</td>
<td>kΩ</td>
<td>3</td>
</tr>
<tr>
<td>Resistance between VM pin and VSS pin</td>
<td>RVMS</td>
<td>V1 = V2 = 3.4 V, VVM = 1.0 V</td>
<td>3.5</td>
<td>7</td>
<td>14</td>
<td>kΩ</td>
<td>3</td>
</tr>
<tr>
<td>CTL pin internal resistance</td>
<td>RCTL</td>
<td>S-82B2A Series</td>
<td>RCTL × 0.5</td>
<td>RCTL</td>
<td>RCTL × 2.0</td>
<td>MΩ</td>
<td>3</td>
</tr>
<tr>
<td>PS pin internal resistance</td>
<td>RPS</td>
<td>S-82B2B Series</td>
<td>RPS × 0.5</td>
<td>RPS</td>
<td>RPS × 2.0</td>
<td>MΩ</td>
<td>3</td>
</tr>
<tr>
<td>Input Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Operation voltage between VDD pin and VSS pin</td>
<td>VDSOP1</td>
<td>–</td>
<td>1.5</td>
<td>–</td>
<td>10</td>
<td>V</td>
<td>–</td>
</tr>
<tr>
<td>Operation voltage between VDD pin and VM pin</td>
<td>VDSOP2</td>
<td>–</td>
<td>1.5</td>
<td>–</td>
<td>28</td>
<td>V</td>
<td>–</td>
</tr>
<tr>
<td>CTL pin voltage &quot;H&quot;</td>
<td>VCTLH</td>
<td>S-82B2A Series</td>
<td>VCTLH – 0.3</td>
<td>VCTLH</td>
<td>VCTLH + 0.3</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>CTL pin voltage &quot;L&quot;</td>
<td>VCTLL</td>
<td>S-82B2A Series</td>
<td>VCTLL – 0.3</td>
<td>VCTLL</td>
<td>VCTLL + 0.3</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>PS pin voltage &quot;H&quot;</td>
<td>VPSH</td>
<td>S-82B2B Series</td>
<td>VPSH – 0.3</td>
<td>VPSH</td>
<td>VPSH + 0.3</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>PS pin voltage &quot;L&quot;</td>
<td>VPSL</td>
<td>S-82B2B Series</td>
<td>VPSL – 0.3</td>
<td>VPSL</td>
<td>VPSL + 0.3</td>
<td>V</td>
<td>2</td>
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</tbody>
</table>

Remark  n = 1, 2
**Table 13 (2 / 2)**

(Ta = +25°C unless otherwise specified)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
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</thead>
<tbody>
<tr>
<td><strong>Input Current</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Current consumption during operation</td>
<td>IOPE</td>
<td>V1 = V2 = 3.4 V, VVM = 0 V</td>
<td>–</td>
<td>3.0</td>
<td>6.0</td>
<td>μA</td>
<td>3</td>
</tr>
<tr>
<td>VC pin current</td>
<td>IVC</td>
<td>V1 = V2 = 3.4 V, VVM = 0 V</td>
<td>–0.1</td>
<td>0.0</td>
<td>0.1</td>
<td>μA</td>
<td>3</td>
</tr>
<tr>
<td>Current consumption during power-down</td>
<td>IPDN</td>
<td>V1 = V2 = 1.5 V, VVM = 3.0 V</td>
<td>–</td>
<td>–</td>
<td>50</td>
<td>nA</td>
<td>3</td>
</tr>
<tr>
<td>Current consumption during overdischarge</td>
<td>IOPED</td>
<td>V1 = V2 = 1.5 V, VVM = 3.0 V</td>
<td>–</td>
<td>–</td>
<td>1.0</td>
<td>μA</td>
<td>3</td>
</tr>
<tr>
<td>Current consumption during power-saving</td>
<td>IPS</td>
<td>S-82B2B Series</td>
<td>–</td>
<td>–</td>
<td>50</td>
<td>nA</td>
<td>3</td>
</tr>
<tr>
<td><strong>Output Resistance</strong></td>
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<tr>
<td>CO pin resistance &quot;H&quot;</td>
<td>RCOH</td>
<td>–</td>
<td>3</td>
<td>6</td>
<td>12</td>
<td>kΩ</td>
<td>4</td>
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<tr>
<td>CO pin resistance &quot;L&quot;</td>
<td>RCOL</td>
<td>–</td>
<td>1.5</td>
<td>3</td>
<td>6</td>
<td>kΩ</td>
<td>4</td>
</tr>
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<td>DO pin resistance &quot;H&quot;</td>
<td>RDOH</td>
<td>–</td>
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<td>7</td>
<td>14</td>
<td>kΩ</td>
<td>4</td>
</tr>
<tr>
<td>DO pin resistance &quot;L&quot;</td>
<td>RDOL</td>
<td>–</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>kΩ</td>
<td>4</td>
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<tr>
<td><strong>Delay Time</strong></td>
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</tr>
<tr>
<td>Overcharge detection delay time</td>
<td>tCU</td>
<td>–</td>
<td>tCU × 0.7</td>
<td>tCU</td>
<td>tCU × 1.3</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>Overdischarge detection delay time</td>
<td>tDL</td>
<td>–</td>
<td>tDL × 0.7</td>
<td>tDL</td>
<td>tDL × 1.3</td>
<td>–</td>
<td>5</td>
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<tr>
<td>Discharge overcurrent 1 detection delay time</td>
<td>tDIOV1</td>
<td>–</td>
<td>tDIOV1 × 0.75</td>
<td>tDIOV1</td>
<td>tDIOV1 × 1.25</td>
<td>–</td>
<td>5</td>
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<tr>
<td>Discharge overcurrent 2 detection delay time</td>
<td>tDIOV2</td>
<td>–</td>
<td>tDIOV2 × 0.7</td>
<td>tDIOV2</td>
<td>tDIOV2 × 1.3</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>Load short-circuiting detection delay time</td>
<td>tSHORT</td>
<td>–</td>
<td>tSHORT × 0.7</td>
<td>tSHORT</td>
<td>tSHORT × 1.3</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>Charge overcurrent detection delay time</td>
<td>tCIOV</td>
<td>–</td>
<td>tCIOV × 0.7</td>
<td>tCIOV</td>
<td>tCIOV × 1.3</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>Charge-discharge inhibition delay time</td>
<td>tCTL</td>
<td>S-82B2A Series</td>
<td>tCTL × 0.7</td>
<td>tCTL</td>
<td>tCTL × 1.3</td>
<td>–</td>
<td>5</td>
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<tr>
<td>Power-saving delay time</td>
<td>tPS</td>
<td>S-82B2B Series</td>
<td>tPS × 0.7</td>
<td>tPS</td>
<td>tPS × 1.3</td>
<td>–</td>
<td>5</td>
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</table>
## 2. $T_a = -20^\circ C$ to $+60^\circ C$¹

### Table 14 (1 / 2)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
</tr>
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<tbody>
<tr>
<td><strong>Detection Voltage</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overcharge detection voltage n</td>
<td>$V_{CU,n}$</td>
<td>–</td>
<td>$V_{CU} - 0.025$</td>
<td>$V_{CU}$</td>
<td>$V_{CU} + 0.025$</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Overcharge release voltage n</td>
<td>$V_{CL,n}$</td>
<td>$V_{CL} \neq V_{CU}$</td>
<td>$V_{CL} - 0.065$</td>
<td>$V_{CL}$</td>
<td>$V_{CL} + 0.057$</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Overdischarge detection voltage n</td>
<td>$V_{DL,n}$</td>
<td>–</td>
<td>$V_{DL} - 0.060$</td>
<td>$V_{DL}$</td>
<td>$V_{DL} + 0.055$</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Overdischarge release voltage n</td>
<td>$V_{DU,n}$</td>
<td>$V_{DU} \neq V_{DU}$</td>
<td>$V_{DU} - 0.085$</td>
<td>$V_{DU}$</td>
<td>$V_{DU} + 0.080$</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{DU} = V_{DU}$</td>
<td>$V_{DU} - 0.060$</td>
<td>$V_{DU}$</td>
<td>$V_{DU} + 0.055$</td>
<td>V</td>
</tr>
<tr>
<td>Discharge overcurrent 1 detection voltage</td>
<td>$V_{DIOV1}$</td>
<td>–</td>
<td>$V_{DIOV1} - 5$</td>
<td>$V_{DIOV1}$</td>
<td>$V_{DIOV1} + 5$</td>
<td>mV</td>
<td>5</td>
</tr>
<tr>
<td>Discharge overcurrent 2 detection voltage</td>
<td>$V_{DIOV2}$</td>
<td>–</td>
<td>$V_{DIOV2} - 8$</td>
<td>$V_{DIOV2}$</td>
<td>$V_{DIOV2} + 8$</td>
<td>mV</td>
<td>2</td>
</tr>
<tr>
<td>Load short-circuiting detection voltage</td>
<td>$V_{SHORT}$</td>
<td>–</td>
<td>$V_{DD} - 1.3$</td>
<td>$V_{DD} - 0.9$</td>
<td>$V_{DD} - 0.5$</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Load short-circuiting 2 detection voltage</td>
<td>$V_{SHORT2}$</td>
<td>–</td>
<td>$V_{DD} - 1.3$</td>
<td>$V_{DD} - 0.9$</td>
<td>$V_{DD} - 0.5$</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Charge overcurrent detection voltage</td>
<td>$V_{CIOV}$</td>
<td>–</td>
<td>$V_{CIOV} - 5$</td>
<td>$V_{CIOV}$</td>
<td>$V_{CIOV} + 5$</td>
<td>mV</td>
<td>2</td>
</tr>
<tr>
<td>Discharge overcurrent release voltage</td>
<td>$V_{RIOV}$</td>
<td>$V_1 = V_2 = 3.4$ V</td>
<td>$V_{DD} - 1.3$</td>
<td>$V_{DD} - 1.2$</td>
<td>$V_{DD} - 1.1$</td>
<td>V</td>
<td>5</td>
</tr>
<tr>
<td><strong>0 V Battery Charge</strong></td>
<td></td>
<td></td>
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<tr>
<td>0 V battery charge starting charger voltage</td>
<td>$V_{0CHA}$</td>
<td>0 V battery charge enabled</td>
<td>0.5</td>
<td>1.1</td>
<td>1.7</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td>0 V battery charge inhibition battery voltage n</td>
<td>$V_{0INHn}$</td>
<td>0 V battery charge inhibited</td>
<td>1.00</td>
<td>1.25</td>
<td>1.40</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td><strong>Internal Resistance</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Resistance between VDD pin and VM pin</td>
<td>$R_{VM}$</td>
<td>$V_1 = V_2 = 1.8$ V, $V_{VM} = 0$ V</td>
<td>500</td>
<td>2500</td>
<td>7000</td>
<td>kΩ</td>
<td>3</td>
</tr>
<tr>
<td>Resistance between VDD pin and VM pin 2</td>
<td>$R_{VM2}$</td>
<td>S-82B2B Series</td>
<td>8</td>
<td>18</td>
<td>30</td>
<td>kΩ</td>
<td>3</td>
</tr>
<tr>
<td>Resistance between VM pin and VSS pin</td>
<td>$R_{VMS}$</td>
<td>$V_1 = V_2 = 1.5$ V, $V_{VM} = 3.0$ V</td>
<td>3.5</td>
<td>7</td>
<td>14</td>
<td>kΩ</td>
<td>3</td>
</tr>
<tr>
<td>CTL pin internal resistance</td>
<td>$R_{CTL}$</td>
<td>S-82B2A Series</td>
<td>$R_{CTL} \times 0.25$</td>
<td>$R_{CTL}$</td>
<td>$R_{CTL} \times 3.0$</td>
<td>MΩ</td>
<td>3</td>
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<tr>
<td>PS pin internal resistance</td>
<td>$R_{PS}$</td>
<td>S-82B2B Series</td>
<td>$R_{PS} \times 0.25$</td>
<td>$R_{PS}$</td>
<td>$R_{PS} \times 3.0$</td>
<td>MΩ</td>
<td>3</td>
</tr>
<tr>
<td><strong>Input Voltage</strong></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Operation voltage between VDD pin and VSS pin</td>
<td>$V_{DSOP1}$</td>
<td>–</td>
<td>1.5</td>
<td>–</td>
<td>10</td>
<td>V</td>
<td>–</td>
</tr>
<tr>
<td>Operation voltage between VDD pin and VM pin</td>
<td>$V_{DSOP2}$</td>
<td>–</td>
<td>1.5</td>
<td>–</td>
<td>28</td>
<td>V</td>
<td>–</td>
</tr>
<tr>
<td>CTL pin voltage &quot;H&quot;</td>
<td>$V_{CTLH}$</td>
<td>S-82B2A Series</td>
<td>$V_{CTLH} - 0.4$</td>
<td>$V_{CTLH}$</td>
<td>$V_{CTLH} + 0.4$</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>CTL pin voltage &quot;L&quot;</td>
<td>$V_{CTLL}$</td>
<td>S-82B2A Series</td>
<td>$V_{CTLL} - 0.4$</td>
<td>$V_{CTLL}$</td>
<td>$V_{CTLL} + 0.4$</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>PS pin voltage &quot;H&quot;</td>
<td>$V_{PSH}$</td>
<td>S-82B2B Series</td>
<td>$V_{PSH} - 0.4$</td>
<td>$V_{PSH}$</td>
<td>$V_{PSH} + 0.4$</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>PS pin voltage &quot;L&quot;</td>
<td>$V_{PSL}$</td>
<td>S-82B2B Series</td>
<td>$V_{PSL} - 0.4$</td>
<td>$V_{PSL}$</td>
<td>$V_{PSL} + 0.4$</td>
<td>V</td>
<td>2</td>
</tr>
</tbody>
</table>

**Remark** $n = 1, 2$
### Table 14 (2 / 2)

(\(\text{Ta} = -20^\circ\text{C to } +60^\circ\text{C}\) unless otherwise specified)

<table>
<thead>
<tr>
<th>Input Current</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption during operation</td>
<td>IOPE</td>
<td>(V1 = V2 = 3.4 , \text{V}, \ V_{\text{VM}} = 0 , \text{V})</td>
<td>–</td>
<td>3.0</td>
<td>7.0</td>
<td>μA</td>
<td>3</td>
</tr>
<tr>
<td>VC pin current</td>
<td>IVC</td>
<td>(V1 = V2 = 3.4 , \text{V}, \ V_{\text{VM}} = 0 , \text{V})</td>
<td>–0.1</td>
<td>0.0</td>
<td>0.1</td>
<td>μA</td>
<td>3</td>
</tr>
<tr>
<td>Current consumption during power-down</td>
<td>IPON</td>
<td>(V1 = V2 = 1.5 , \text{V}, \ V_{\text{VM}} = 3.0 , \text{V})</td>
<td>–</td>
<td>–</td>
<td>100</td>
<td>nA</td>
<td>3</td>
</tr>
<tr>
<td>Current consumption during overdischarge</td>
<td>IPOED</td>
<td>(V1 = V2 = 1.5 , \text{V}, \ V_{\text{VM}} = 3.0 , \text{V})</td>
<td>–</td>
<td>–</td>
<td>1.2</td>
<td>μA</td>
<td>3</td>
</tr>
<tr>
<td>Current consumption during power-saving</td>
<td>IPS</td>
<td>S-82B2B Series</td>
<td>–</td>
<td>–</td>
<td>100</td>
<td>nA</td>
<td>3</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Output Resistance</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO pin resistance &quot;H&quot;</td>
<td>RHCOH</td>
<td>–</td>
<td>1.5</td>
<td>6</td>
<td>18</td>
<td>kΩ</td>
</tr>
<tr>
<td>DO pin resistance &quot;H&quot;</td>
<td>RHDOH</td>
<td>–</td>
<td>0.75</td>
<td>3</td>
<td>9</td>
<td>kΩ</td>
</tr>
<tr>
<td>CO pin resistance &quot;L&quot;</td>
<td>RCHOL</td>
<td>–</td>
<td>1.8</td>
<td>7</td>
<td>21</td>
<td>kΩ</td>
</tr>
<tr>
<td>DO pin resistance &quot;L&quot;</td>
<td>RDOCOL</td>
<td>–</td>
<td>0.5</td>
<td>2</td>
<td>6</td>
<td>kΩ</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Delay Time</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Overcharge detection delay time</td>
<td>tCU</td>
<td>–</td>
<td>(t_{\text{CU}} \times 0.6)</td>
<td>(t_{\text{CU}})</td>
<td>(t_{\text{CU}} \times 1.4)</td>
<td>– 5</td>
</tr>
<tr>
<td>Overdischarge detection delay time</td>
<td>tDL</td>
<td>–</td>
<td>(t_{\text{DL}} \times 0.6)</td>
<td>(t_{\text{DL}})</td>
<td>(t_{\text{DL}} \times 1.4)</td>
<td>– 5</td>
</tr>
<tr>
<td>Discharge overcurrent 1 detection delay time</td>
<td>tDIOV1</td>
<td>–</td>
<td>(t_{\text{DIOV1}} \times 0.65)</td>
<td>(t_{\text{DIOV1}})</td>
<td>(t_{\text{DIOV1}} \times 1.35)</td>
<td>– 5</td>
</tr>
<tr>
<td>Discharge overcurrent 2 detection delay time</td>
<td>tDIOV2</td>
<td>–</td>
<td>(t_{\text{DIOV2}} \times 0.6)</td>
<td>(t_{\text{DIOV2}})</td>
<td>(t_{\text{DIOV2}} \times 1.4)</td>
<td>– 5</td>
</tr>
<tr>
<td>Load short-circuiting detection delay time</td>
<td>tSHORT</td>
<td>–</td>
<td>(t_{\text{SHORT}} \times 0.6)</td>
<td>(t_{\text{SHORT}})</td>
<td>(t_{\text{SHORT}} \times 1.4)</td>
<td>– 5</td>
</tr>
<tr>
<td>Charge overcurrent detection delay time</td>
<td>tCIOV</td>
<td>–</td>
<td>(t_{\text{CIOV}} \times 0.6)</td>
<td>(t_{\text{CIOV}})</td>
<td>(t_{\text{CIOV}} \times 1.4)</td>
<td>– 5</td>
</tr>
<tr>
<td>Charge-discharge inhibition delay time</td>
<td>tCTL</td>
<td>S-82B2A Series</td>
<td>(t_{\text{CTL}} \times 0.6)</td>
<td>(t_{\text{CTL}})</td>
<td>(t_{\text{CTL}} \times 1.4)</td>
<td>– 5</td>
</tr>
<tr>
<td>Power-saving delay time</td>
<td>IPS</td>
<td>S-82B2B Series</td>
<td>(t_{\text{IPS}} \times 0.6)</td>
<td>(t_{\text{IPS}})</td>
<td>(t_{\text{IPS}} \times 1.4)</td>
<td>– 5</td>
</tr>
</tbody>
</table>

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.
3. \( T_a = -40°C \) to +85°C

Table 15 (1 / 2)

<table>
<thead>
<tr>
<th>(Item)</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overcharge detection voltage ( n )</td>
<td>( V_{CU} )</td>
<td>–</td>
<td>( V_{CU} - 0.050 )</td>
<td>( V_{CU} )</td>
<td>( V_{CU} + 0.035 )</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Overcharge release voltage ( n )</td>
<td>( V_{CL} )</td>
<td>( V_{CL} )</td>
<td>( V_{CL} - 0.080 )</td>
<td>( V_{CL} )</td>
<td>( V_{CL} + 0.060 )</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Overdischarge detection voltage ( n )</td>
<td>( V_{DL} )</td>
<td>–</td>
<td>( V_{DL} - 0.060 )</td>
<td>( V_{DL} )</td>
<td>( V_{DL} + 0.060 )</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Overdischarge release voltage ( n )</td>
<td>( V_{DU} )</td>
<td>( V_{DU} )</td>
<td>( V_{DU} - 0.105 )</td>
<td>( V_{DU} )</td>
<td>( V_{DU} + 0.085 )</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Discharge overcurrent 1 detection voltage</td>
<td>( V_{DI1} )</td>
<td>–</td>
<td>( V_{DI1} - 5 )</td>
<td>( V_{DI1} )</td>
<td>( V_{DI1} + 5 )</td>
<td>mV</td>
<td>5</td>
</tr>
<tr>
<td>Discharge overcurrent 2 detection voltage</td>
<td>( V_{DI2} )</td>
<td>–</td>
<td>( V_{DI2} - 8 )</td>
<td>( V_{DI2} )</td>
<td>( V_{DI2} + 8 )</td>
<td>mV</td>
<td>2</td>
</tr>
<tr>
<td>Load short-circuiting detection voltage</td>
<td>( V_{SHORT} )</td>
<td>–</td>
<td>( V_{SHORT} - 20 )</td>
<td>( V_{SHORT} )</td>
<td>( V_{SHORT} + 20 )</td>
<td>mV</td>
<td>2</td>
</tr>
<tr>
<td>Load short-circuiting 2 detection voltage</td>
<td>( V_{SHORT2} )</td>
<td>–</td>
<td>( V_{DD} - 1.4 )</td>
<td>( V_{DD} - 0.9 )</td>
<td>( V_{DD} - 0.3 )</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>Charge overcurrent detection voltage</td>
<td>( V_{CI} )</td>
<td>–</td>
<td>( V_{CI} - 5 )</td>
<td>( V_{CI} )</td>
<td>( V_{CI} + 5 )</td>
<td>mV</td>
<td>2</td>
</tr>
<tr>
<td>Discharge overcurrent release voltage</td>
<td>( V_{RO} )</td>
<td>( V_{1} = V_{2} = 3.4 ) V</td>
<td>( V_{DD} - 1.3 )</td>
<td>( V_{DD} - 1.2 )</td>
<td>( V_{DD} - 1.1 )</td>
<td>V</td>
<td>5</td>
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<tr>
<td>0 V Battery Charge</td>
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<tr>
<td>0 V battery charge starting charger voltage</td>
<td>( V_{OCHA} )</td>
<td>( 0 ) V battery charge enabled</td>
<td>0.5</td>
<td>1.1</td>
<td>1.7</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td>0 V battery charge inhibition battery voltage ( n )</td>
<td>( V_{OINH} )</td>
<td>( 0 ) V battery charge inhibited</td>
<td>1.00</td>
<td>1.25</td>
<td>1.40</td>
<td>V</td>
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<tr>
<td>Internal Resistance</td>
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<td></td>
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<tr>
<td>Resistance between VDD pin and VM pin</td>
<td>( R_{VMD} )</td>
<td>( V_{1} = V_{2} = 1.8 ) V, ( V_{VM} = 0 ) V</td>
<td>500</td>
<td>2500</td>
<td>7000</td>
<td>kΩ</td>
<td>3</td>
</tr>
<tr>
<td>Resistance between VDD pin and VM pin 2</td>
<td>( R_{VMD2} )</td>
<td>S-82B2B Series</td>
<td>8</td>
<td>18</td>
<td>30</td>
<td>kΩ</td>
<td>3</td>
</tr>
<tr>
<td>Resistance between VM pin and VSS pin</td>
<td>( R_{VMS} )</td>
<td>( V_{1} = V_{2} = 1.5 ) V, ( V_{VM} = 3.0 ) V</td>
<td>3.5</td>
<td>7</td>
<td>14</td>
<td>kΩ</td>
<td>3</td>
</tr>
<tr>
<td>CTL pin internal resistance</td>
<td>( R_{CTL} )</td>
<td>S-82B2A Series</td>
<td>( R_{CTL} \times 0.25 )</td>
<td>( R_{CTL} )</td>
<td>( R_{CTL} \times 3.0 )</td>
<td>MΩ</td>
<td>3</td>
</tr>
<tr>
<td>PS pin internal resistance</td>
<td>( R_{PS} )</td>
<td>S-82B2B Series</td>
<td>( R_{PS} \times 0.25 )</td>
<td>( R_{PS} )</td>
<td>( R_{PS} \times 3.0 )</td>
<td>MΩ</td>
<td>3</td>
</tr>
<tr>
<td>Input Voltage</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operation voltage between VDD pin and VSS pin</td>
<td>( V_{DSOP1} )</td>
<td>–</td>
<td>1.5</td>
<td>–</td>
<td>10</td>
<td>V</td>
<td>–</td>
</tr>
<tr>
<td>Operation voltage between VDD pin and VM pin</td>
<td>( V_{DSOP2} )</td>
<td>–</td>
<td>1.5</td>
<td>–</td>
<td>28</td>
<td>V</td>
<td>–</td>
</tr>
<tr>
<td>CTL pin voltage &quot;H&quot;</td>
<td>( V_{CTLH} )</td>
<td>S-82B2A Series</td>
<td>( V_{CTLH} - 0.4 )</td>
<td>( V_{CTLH} )</td>
<td>( V_{CTLH} + 0.4 )</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>CTL pin voltage &quot;L&quot;</td>
<td>( V_{CTLL} )</td>
<td>S-82B2A Series</td>
<td>( V_{CTLL} - 0.4 )</td>
<td>( V_{CTLL} )</td>
<td>( V_{CTLL} + 0.4 )</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>PS pin voltage &quot;H&quot;</td>
<td>( V_{PSH} )</td>
<td>S-82B2B Series</td>
<td>( V_{PSH} - 0.4 )</td>
<td>( V_{PSH} )</td>
<td>( V_{PSH} + 0.4 )</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>PS pin voltage &quot;L&quot;</td>
<td>( V_{PSL} )</td>
<td>S-82B2B Series</td>
<td>( V_{PSL} - 0.4 )</td>
<td>( V_{PSL} )</td>
<td>( V_{PSL} + 0.4 )</td>
<td>V</td>
<td>2</td>
</tr>
</tbody>
</table>

Remark \( n = 1, 2 \)
### Table 15 (2 / 2)

(\(Ta = -40^\circ C \text{ to } +85^\circ C\)^1 unless otherwise specified)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
</tr>
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<tbody>
<tr>
<td><strong>Input Current</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current consumption during operation</td>
<td>(I_{OPE})</td>
<td>(V1 = V2 = 3.4 \text{ V}, V_{VM} = 0 \text{ V})</td>
<td>–</td>
<td>3.0</td>
<td>7.0</td>
<td>(\mu A)</td>
<td>3</td>
</tr>
<tr>
<td>VC pin current</td>
<td>(I_{VC})</td>
<td>(V1 = V2 = 3.4 \text{ V}, V_{VM} = 0 \text{ V})</td>
<td>–0.15</td>
<td>0.0</td>
<td>0.15</td>
<td>(\mu A)</td>
<td>3</td>
</tr>
<tr>
<td>Current consumption during power-down</td>
<td>(I_{PON})</td>
<td>(V1 = V2 = 1.5 \text{ V}, V_{VM} = 3.0 \text{ V})</td>
<td>–</td>
<td>–</td>
<td>150</td>
<td>nA</td>
<td>3</td>
</tr>
<tr>
<td>Current consumption during overdischarge</td>
<td>(I_{OPED})</td>
<td>(V1 = V2 = 1.5 \text{ V}, V_{VM} = 3.0 \text{ V})</td>
<td>–</td>
<td>–</td>
<td>1.2</td>
<td>(\mu A)</td>
<td>3</td>
</tr>
<tr>
<td>Current consumption during power-saving</td>
<td>(I_{PS})</td>
<td>S-82B2B Series</td>
<td>–</td>
<td>–</td>
<td>150</td>
<td>nA</td>
<td>3</td>
</tr>
<tr>
<td><strong>Output Resistance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>CO pin resistance &quot;H&quot;</td>
<td>(R_{COH})</td>
<td>–</td>
<td>1.5</td>
<td>6</td>
<td>18</td>
<td>k(\Omega)</td>
<td>4</td>
</tr>
<tr>
<td>CO pin resistance &quot;L&quot;</td>
<td>(R_{COL})</td>
<td>–</td>
<td>0.75</td>
<td>3</td>
<td>9</td>
<td>k(\Omega)</td>
<td>4</td>
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<tr>
<td>DO pin resistance &quot;H&quot;</td>
<td>(R_{DOH})</td>
<td>–</td>
<td>1.8</td>
<td>7</td>
<td>21</td>
<td>k(\Omega)</td>
<td>4</td>
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<tr>
<td>DO pin resistance &quot;L&quot;</td>
<td>(R_{DOL})</td>
<td>–</td>
<td>0.5</td>
<td>2</td>
<td>6</td>
<td>k(\Omega)</td>
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<tr>
<td><strong>Delay Time</strong></td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>Overcharge detection delay time</td>
<td>(t_{CU})</td>
<td>–</td>
<td>(t_{CU} \times 0.4)</td>
<td>(t_{CU})</td>
<td>(t_{CU} \times 1.6)</td>
<td>–</td>
<td>5</td>
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<tr>
<td>Overdischarge detection delay time</td>
<td>(t_{DL})</td>
<td>–</td>
<td>(t_{DL} \times 0.4)</td>
<td>(t_{DL})</td>
<td>(t_{DL} \times 1.6)</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>Discharge overcurrent 1 detection delay time</td>
<td>(t_{DIOV1})</td>
<td>–</td>
<td>(t_{DIOV1} \times 0.4)</td>
<td>(t_{DIOV1})</td>
<td>(t_{DIOV1} \times 1.6)</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>Discharge overcurrent 2 detection delay time</td>
<td>(t_{DIOV2})</td>
<td>–</td>
<td>(t_{DIOV2} \times 0.4)</td>
<td>(t_{DIOV2})</td>
<td>(t_{DIOV2} \times 1.6)</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>Load short-circuiting detection delay time</td>
<td>(t_{SHORT})</td>
<td>–</td>
<td>(t_{SHORT} \times 0.4)</td>
<td>(t_{SHORT})</td>
<td>(t_{SHORT} \times 1.6)</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>Charge overcurrent detection delay time</td>
<td>(t_{CIOV})</td>
<td>–</td>
<td>(t_{CIOV} \times 0.4)</td>
<td>(t_{CIOV})</td>
<td>(t_{CIOV} \times 1.6)</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>Charge-discharge inhibition delay time</td>
<td>(t_{CTL})</td>
<td>S-82B2A Series</td>
<td>(t_{CTL} \times 0.4)</td>
<td>(t_{CTL})</td>
<td>(t_{CTL} \times 1.6)</td>
<td>–</td>
<td>5</td>
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<tr>
<td>Power-saving delay time</td>
<td>(t_{PS})</td>
<td>S-82B2B Series</td>
<td>(t_{PS} \times 0.4)</td>
<td>(t_{PS})</td>
<td>(t_{PS} \times 1.6)</td>
<td>–</td>
<td>5</td>
</tr>
</tbody>
</table>

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.
Test Circuits

When CTL pin or PS pin control logic is active "H", SW1 and SW3 are turned off, SW2 and SW4 are turned on. When CTL pin or PS pin control logic is active "L", SW1 and SW3 are turned on, SW2 and SW4 are turned off.

Caution  Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V CO) and DO pin (V DO) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V VM and the DO pin level with respect to V SS.

1. Overcharge detection voltage, overcharge release voltage
   (Test circuit 1)
   Overcharge detection voltage 1 (V CUI1) is defined as the voltage V1 at which V CO goes from "H" to "L" when the voltage V1 is gradually increased after setting V1 = V2 = V CUI − 0.05 V. Overcharge release voltage 1 (V CUL1) is defined as the voltage V1 at which V CO goes from "L" to "H" when setting V2 = 3.4 V and when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage 1 (V HC1) is defined as the difference between V CUI1 and V CUL1.
   Overcharge detection voltage 2 (V CUI2), overcharge release voltage 2 (V CUL2) and overcharge hysteresis voltage 2 (V HC2) can be determined in the same way.

2. Overdischarge detection voltage, overdischarge release voltage
   (Test circuit 2)
   Overdischarge detection voltage 1 (V DLI1) is defined as the voltage V1 at which V DO goes from "H" to "L" when the voltage V1 is gradually decreased after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V. Overdischarge release voltage 1 (V DLI1) is defined as the voltage V1 at which V DO goes from "L" to "H" when setting V3 = 0.01 V, V6 = V7 = 0 V and when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage 1 (V HD1) is defined as the difference between V DLI1 and V DLI1.
   Overdischarge detection voltage 2 (V DLI2), overdischarge release voltage 2 (V DLI2) and overdischarge hysteresis voltage 2 (V HD2) can be determined in the same way.

3. Discharge overcurrent 1 detection voltage, discharge overcurrent release voltage
   (Test circuit 5)
   Discharge overcurrent 1 detection voltage (V DOI1) is defined as the voltage V6 at which delay time from when V6 is increased after setting V1 = V2 = 3.4 V, V3 = 1.0 V, V6 = V7 = 0 V to when V DO goes from "H" to "L" is discharge overcurrent 1 detection delay time (t DOI1). Discharge overcurrent release voltage (V DOI1) is defined as the voltage V6 at which V DO goes from "L" to "H" when setting V3 = 6.8 V, V6 = 0 V and when the voltage V3 is then gradually decreased. When the voltage V3 falls below V DOI, V DO will go to "H" after 1.0 ms typ. and maintain "H" during load short-circuiting detection delay time (t SHORT).

4. Discharge overcurrent 2 detection voltage
   (Test circuit 2)
   Discharge overcurrent 2 detection voltage (V DOI2) is defined as the voltage V6 at which delay time from when V6 is increased after setting V1 = V2 = 3.4 V, V3 = 1.0 V, V6 = V7 = 0 V to when V DO goes from "H" to "L" is discharge overcurrent 2 detection delay time (t DOI2).

5. Load short-circuiting detection voltage
   (Test circuit 2)
   Load short-circuiting detection voltage (V SHORT) is defined as the voltage V6 at which delay time from when V6 is increased after setting V1 = V2 = 3.4 V, V3 = 1.0 V, V6 = V7 = 0 V to when V DO goes from "H" to "L" is t SHORT.

6. Load short-circuiting 2 detection voltage
   (Test circuit 2)
   Load short-circuiting 2 detection voltage (V SHORT2) is defined as the voltage V3 at which delay time from when V3 is increased after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V to when V DO goes from "H" to "L" is t SHORT.
7. Charge overcurrent detection voltage (Test circuit 2)

Charge overcurrent detection voltage \( V_{\text{CIDV}} \) is defined as the voltage \( V_6 \) at which delay time from when \( V_6 \) is decreased after setting \( V_1 = V_2 = 3.4 \, V \), \( V_3 = V_6 = V_7 = 0 \, V \) to when \( V_{\text{CO}} \) goes from "H" to "L" is charge overcurrent detection delay time \( t_{\text{CIDV}} \).

8. CTL pin voltage "H", CTL pin voltage "L" (S-82B2A Series) (Test circuit 2)

8.1 CTL pin control logic active "H"

The CTL pin voltage "H" \( (V_{\text{CTLH}}) \) is defined as the voltage \( V_7 \) at which \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go from "H" to "L" when the voltage \( V_7 \) is gradually increased after setting \( V_1 = V_2 = 3.4 \, V \), \( V_3 = V_6 = V_7 = 0 \, V \). After that, the CTL pin voltage "L" \( (V_{\text{CTLL}}) \) is defined as the voltage \( V_7 \) at which \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go from "L" to "H" after \( V_7 \) is gradually decreased.

8.2 CTL pin control logic active "L"

\( V_{\text{CTLL}} \) is defined as the voltage difference between the voltage \( V_7 \) and the voltage \( V_1 + V_2 - V_7 \) at which \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go from "H" to "L" when the voltage \( V_7 \) is gradually increased after setting \( V_1 = V_2 = 3.4 \, V \), \( V_3 = V_6 = V_7 = 0 \, V \). After that, \( V_{\text{CTLL}} \) is defined as \( V_1 + V_2 - V_7 \) at which \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go from "L" to "H" after \( V_7 \) is gradually decreased.

9. PS pin voltage "H", PS pin voltage "L" (S-82B2B Series) (Test circuit 2)

9.1 PS pin control logic active "H"

The PS pin voltage "H" \( (V_{\text{PSH}}) \) is defined as the voltage \( V_7 \) at which \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go from "H" to "L" when the voltage \( V_7 \) is gradually increased after setting \( V_1 = V_2 = 3.4 \, V \), \( V_3 = V_6 = V_7 = 0 \, V \). After that, the PS pin voltage "L" \( (V_{\text{PSL}}) \) is defined as the voltage \( V_7 \) at which \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go from "L" to "H" after \( V_7 \) is gradually decreased.

9.2 PS pin control logic active "L"

\( V_{\text{PSL}} \) is defined as the voltage difference between the voltage \( V_7 \) and the voltage \( V_1 + V_2 - V_7 \) at which \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go from "H" to "L" when the voltage \( V_7 \) is gradually increased after setting \( V_1 = V_2 = 3.4 \, V \), \( V_3 = V_6 = V_7 = 0 \, V \). After that, \( V_{\text{PSH}} \) is defined as \( V_1 + V_2 - V_7 \) at which \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go from "L" to "H" after \( V_7 \) is gradually decreased.

10. Current consumption during operation (Test circuit 3)

The current consumption during operation \( (I_{\text{OPE}}) \) is the current that flows through the VDD pin \( (I_{\text{DD}}) \) under the set conditions of \( V_1 = V_2 = 3.4 \, V \), \( V_3 = V_6 = V_7 = 0 \, V \). However, the current flowing through the CTL pin or the PS pin internal resistance is excluded.

11. VC pin current (Test circuit 3)

The VC pin current \( (I_{\text{VC}}) \) is the current that flows through the VC pin under the set conditions of \( V_1 = V_2 = 3.4 \, V \), \( V_3 = V_6 = V_7 = 0 \, V \).
12. Current consumption during power-down, current consumption during overdischarge (Test circuit 3)

12.1 With power-down function
The current consumption during power-down (I_{PDN}) is I_{DD} under the set conditions of V1 = V2 = 1.5 V, V3 = 3.0 V, V6 = V7 = 0 V.

12.2 Without power-down function
The current consumption during overdischarge (I_{OPED}) is I_{DD} under the set conditions of V1 = V2 = 1.5 V, V3 = 3.0 V, V6 = V7 = 0 V.

13. Current consumption during power-saving (S-82B2B Series) (Test circuit 3)
The current consumption during power-saving (I_{PS}) is I_{DD} under the set conditions of V1 = V2 = 3.4 V, V3 = 6.8 V, V6 = 0 V, V7 = 6.8 V.

14. Resistance between VDD pin and VM pin (Test circuit 3)
R_{VMD} is the resistance between VDD pin and VM pin under the set conditions of V1 = V2 = 1.8 V, V3 = V6 = V7 = 0 V.

15. Resistance between VDD pin and VM pin 2 (S-82B2B Series) (Test circuit 3)
R_{VMD2} is the resistance between VDD pin and VM pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = 0 V, V7 = 6.8 V.

16. Resistance between VM pin and VSS pin (Test circuit 3)
R_{VMS} is the resistance between VM pin and VSS pin when the voltage V6 is decreased to 0 V after setting V1 = V2 = 3.4 V, V3 = V6 = 1.0 V, V7 = 0 V.

17. CTL pin internal resistance (S-82B2A Series) (Test circuit 3)

17.1 CTL pin internal resistance connection "pull-up"
The CTL pin internal resistance (R_{CTL}) is the resistance between CTL pin and VDD pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V.

17.2 CTL pin internal resistance connection "pull-down"
R_{CTL} is the resistance between CTL pin and VSS pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = 0 V, V7 = 6.8 V.

18. PS pin internal resistance (S-82B2B Series) (Test circuit 3)

18.1 PS pin control logic active "H"
The PS pin internal resistance (R_{PS}) is the resistance between PS pin and VDD pin when the voltage V7 is decreased to 3.4 V after setting V1 = V2 = 3.4 V, V3 = V6 = 0 V, V7 = 6.8 V.

18.2 PS pin control logic active "L"
R_{PS} is the resistance between PS pin and VSS pin when the voltage V7 is increased to 3.4 V after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V.
19. **CO pin resistance "H"**  
   (Test circuit 4)  
   The CO pin resistance "H" (R_{COH}) is the resistance between VDD pin and CO pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = 0 V, V4 = 6.4 V.

20. **CO pin resistance "L"**  
   (Test circuit 4)  
   The CO pin resistance "L" (R_{COL}) is the resistance between VM pin and CO pin under the set conditions of V1 = V2 = 4.9 V, V3 = V6 = 0 V, V4 = 0.4 V.

21. **DO pin resistance "H"**  
   (Test circuit 4)  
   The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = 0 V, V5 = 6.4 V.

22. **DO pin resistance "L"**  
   (Test circuit 4)  
   The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = V2 = 1.8 V, V3 = V6 = 0 V, V5 = 0.4 V.

23. **Overcharge detection delay time**  
   (Test circuit 5)  
   After setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V, the voltage V1 is increased. The time interval from when the voltage V1 exceeds V_{CU} until V_{CO} goes to "L" is the overcharge detection delay time (t_{CU}).

24. **Overdischarge detection delay time**  
   (Test circuit 5)  
   After setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V, the voltage V1 is decreased. The time interval from when the voltage V1 falls below V_{DL} until V_{DO} goes to "L" is the overdischarge detection delay time (t_{DL}).

25. **Discharge overcurrent n detection delay time**  
   (Test circuit 5)  
   After setting V1 = V2 = 3.4 V, V3 = 1.0 V, V6 = V7 = 0 V, the voltage V6 is increased. The time interval from when the voltage V6 exceeds V_{DIOVn} until V_{DO} goes to "L" is the discharge overcurrent n detection delay time (t_{DIOVn}).

26. **Load short-circuiting detection delay time**  
   (Test circuit 5)  
   After setting V1 = V2 = 3.4 V, V3 = 1.0 V, V6 = V7 = 0 V, the voltage V6 is increased. The time interval from when the voltage V6 exceeds V_{SHORT} until V_{DO} goes to "L" is the load short-circuiting detection delay time (t_{SHORT}).

27. **Charge overcurrent detection delay time**  
   (Test circuit 5)  
   After setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V, the voltage V6 is decreased. The time interval from when the voltage V6 falls below V_{CIOV} until V_{CO} goes to "L" is the charge overcurrent detection delay time (t_{CIOV}).

Remark  \( n = 1, 2 \)
28. Charge-discharge inhibition delay time (S-82B2A Series)
   (Test circuit 5)

   28.1 CTL pin control logic active "H"
   After setting \( V_1 = V_2 = 3.4 \text{ V}, V_3 = V_6 = V_7 = 0 \text{ V} \), the voltage \( V_7 \) is increased. The time interval from when the voltage \( V_7 \) exceeds \( V_{\text{CTLH}} \) until \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go to "L" is the charge-discharge inhibition delay time \( (t_{\text{CTL}}) \).

   28.2 CTL pin control logic active "L"
   After setting \( V_1 = V_2 = 3.4 \text{ V}, V_3 = V_6 = V_7 = 0 \text{ V} \), the voltage \( V_7 \) is increased. The time interval from when the voltage \( V_1 + V_2 - V_7 \) falls below \( V_{\text{CTLH}} \) until \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go to "L" is \( t_{\text{CTL}} \).

29. Power-saving delay time (S-82B2B Series)
   (Test circuit 5)

   29.1 PS pin control logic active "H"
   After setting \( V_1 = V_2 = 3.4 \text{ V}, V_3 = V_6 = V_7 = 0 \text{ V} \), the voltage \( V_7 \) is increased. The time interval from when the voltage \( V_7 \) exceeds \( V_{\text{PSH}} \) until \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go to "L" is the power-saving delay time \( (t_{\text{PS}}) \).

   29.2 PS pin control logic active "L"
   After setting \( V_1 = V_2 = 3.4 \text{ V}, V_3 = V_6 = V_7 = 0 \text{ V} \), the voltage \( V_7 \) is increased. The time interval from when the voltage \( V_1 + V_2 - V_7 \) falls below \( V_{\text{PSL}} \) until \( V_{\text{CO}} \) and \( V_{\text{DO}} \) go to "L" is \( t_{\text{PSL}} \).

30. 0 V battery charge starting charger voltage (0 V battery charge enabled)
   (Test circuit 4)
   The 0 V battery charge starting charger voltage \( (V_{\text{CHA}}) \) is defined as the absolute value of voltage \( V_3 \) at which the current flowing through the CO pin \( (I_{\text{CO}}) \) exceeds 1.0 \( \mu \text{A} \) when the voltage \( V_3 \) is gradually decreased after setting \( V_1 = V_2 = V_6 = 0 \text{ V}, V_3 = V_4 = -0.5 \text{ V} \).

31. 0 V battery charge inhibition battery voltage n (0 V battery charge inhibited)
   (Test circuit 2)
   The 0 V battery charge inhibition battery voltage \( n \) \( (V_{\text{INH}}) \) is defined as the voltage \( V_n \) at which \( V_{\text{CO}} \) goes to "L" \( (V_{\text{CO}} = V_{\text{VM}}) \) when the voltage \( V_n \) is gradually decreased after setting \( V_1 = V_2 = 1.5 \text{ V}, V_3 = -1.0 \text{ V}, V_6 = V_7 = 0 \text{ V} \).

Remark \( n = 1, 2 \)
Figure 5  Test Circuit 1

Figure 6  Test Circuit 2

Figure 7  Test Circuit 3

Figure 8  Test Circuit 4

Figure 9  Test Circuit 5
### Operation

**Remark** Refer to "Battery Protection IC Connection Example".

1. **Normal status**

   This IC monitors the voltage of the battery connected between VDD pin and VC pin, VC pin and VSS pin, and the voltage between VIN1 pin and VSS pin to control charging and discharging.

   When the battery voltage is in the range from overdischarge detection voltage (V_DL) to overcharge detection voltage (V_CU), the VIN1 pin voltage is in the range from charge overcurrent detection voltage (V_CIOV) to discharge overcurrent 1 detection voltage (V_DIOV), both charge and discharge control FETs are turned on. This status is called the normal status, and in this condition charging and discharging can be carried out freely.

   Also, for the S-82B2A Series, input the voltage that releases the charge-discharge inhibition status to the CTL pin, and for the S-82B2B Series, input the voltage that releases the power-saving status to the PS pin.

   The resistance between VDD pin and VM pin (R_{VMD}), and the resistance between VM pin and VSS pin (R_{VMS}) are not connected in the normal status.

   *1. Refer to "6. Charge-discharge inhibition status (S-82B2A Series)".
   *2. Refer to "7. Power-saving status (S-82B2B Series)".

   **Caution** After the battery is connected, discharging may not be carried out. In this case, this IC returns to the normal status by connecting a charger.

2. **Overcharge status**

   2.1 \( V_{CL} \neq V_{CU} \) (Product in which overcharge release voltage differs from overcharge detection voltage)

       When the battery voltage becomes higher than \( V_{CU} \) during charging in the normal status and the status continues for the overcharge detection delay time \( t_{CU} \) or longer, the charge control FET is turned off and charging is stopped. This status is called the overcharge status.

       The overcharge status is released in the following two cases.

       (1) In the case that the VM pin voltage is lower than 0.35 V typ., this IC releases the overcharge status when the battery voltage falls below overcharge release voltage \( V_{CL} \).

       (2) In the case that the VM pin voltage is equal to or higher than 0.35 V typ., this IC releases the overcharge status when the battery voltage falls below \( V_{CU} \).

       When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the \( V_f \) voltage of the internal parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., this IC releases the overcharge status when the battery voltage is equal to or lower than \( V_{CU} \).

       **Caution** If the battery is charged to a voltage higher than \( V_{CU} \) and the battery voltage does not fall below \( V_{CU} \) even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below \( V_{CU} \). Since an actual battery has an internal impedance of tens of m\( \Omega \), the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.
2.2  $V_{CL} = V_{CU}$ (Product in which overcharge release voltage is the same as overcharge detection voltage)

When the battery voltage becomes higher than $V_{CU}$ during charging in the normal status and the status continues for $t_{CU}$ or longer, the charge control FET is turned off and charging is stopped. This status is called the overcharge status. In the case that the VM pin voltage is equal to or higher than 0.35 V typ. and the battery voltage falls below $V_{CU}$, this IC releases the overcharge status.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the $V_i$ voltage of the internal parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., this IC releases the overcharge status when the battery voltage is equal to or lower than $V_{CU}$.

Caution 1. If the battery is charged to a voltage higher than $V_{CU}$ and the battery voltage does not fall below $V_{CU}$ even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below $V_{CU}$. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below $V_{CL}$. The overcharge status is released when the discharge current flows and the VM pin voltage goes over 0.35 V typ. by removing the charger.

3. Overdischarge status

When the battery voltage falls below $V_{DL}$ during discharging in the normal status and the status continues for the overdischarge detection delay time ($t_{DL}$) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the overdischarge status. Under the overdischarge status, VDD pin and VM pin are shorted by $R_{VMD}$ in this IC. The VM pin voltage is pulled up by $R_{VMD}$.

When connecting a charger in the overdischarge status, the battery voltage reaches $V_{DL}$ or higher and this IC releases the overdischarge status if the VM pin voltage is below 0 V typ. The battery voltage reaches the overdischarge release voltage ($V_{DU}$) or higher and this IC releases the overdischarge status if the VM pin voltage is not below 0 V typ. $R_{VMS}$ is not connected in the overdischarge status.

3.1 With power-down function

Under the overdischarge status, when the VM pin voltage is 0.7 V typ. or higher, the power-down function works and the current consumption is reduced to the current consumption during power-down ($I_{PDN}$). By connecting a battery charger, the power-down function is released when the VM pin voltage is 0.7 V typ. or lower.

- When a battery is not connected to a charger and the VM pin voltage $\geq$ 0.7 V typ., this IC maintains the overdischarge status even when the battery voltage reaches $V_{DU}$ or higher.
- When a battery is connected to a charger and 0.7 V typ. $> V_{DU}$ or higher and this IC releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ. $\geq$ the VM pin voltage, the battery voltage reaches $V_{DL}$ or higher and this IC releases the overdischarge status.

3.2 Without power-down function

Under the overdischarge status, the power-down function does not work even when the VM pin voltage is 0.7 V typ. or higher.

- When a battery is not connected to a charger and the VM pin voltage $\geq$ 0.7 V typ., the battery voltage reaches $V_{DU}$ or higher and this IC releases the overdischarge status.
- When a battery is connected to a charger and 0.7 V typ. $> V_{DU}$ or higher and this IC releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ. $\geq$ the VM pin voltage, the battery voltage reaches $V_{DL}$ or higher and this IC releases the overdischarge status.
4. Discharge overcurrent status
   (discharge overcurrent 1, discharge overcurrent 2, load short-circuiting, load short-circuiting 2)

4.1 Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting
   When a battery in the normal status is in the status where the VINI pin voltage is equal to or higher than V\textsubscript{DISC1} because the discharge current is equal to or higher than the specified value and the status continues for the discharge overcurrent 1 detection delay time (t\textsubscript{DISC1}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.
   Under the discharge overcurrent status, VM pin and VSS pin are shorted by R\textsubscript{VM} in this IC. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, VM pin returns to the VSS pin voltage.
   When the VM pin voltage returns to V\textsubscript{DISC} or lower, this IC releases the discharge overcurrent status.
   R\textsubscript{VM} is not connected in the discharge overcurrent status.

4.2 Load short-circuiting 2
   When a battery in the normal status is in the status where a load causing discharge overcurrent is connected, and the VM pin voltage is equal to or higher than V\textsubscript{SHORT2} and the status continues for the load short-circuiting detection delay time (t\textsubscript{SHORT}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.
   This IC releases the discharge overcurrent status in the same way as in “4.1 Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting”.

5. Charge overcurrent status
   When a battery in the normal status is in the status where the VINI pin voltage is equal to or lower than V\textsubscript{CHG} because the charge current is equal to or higher than the specified value and the status continues for the charge overcurrent detection delay time (t\textsubscript{CHG}) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.
   This IC releases the charge overcurrent status when the discharge current flows and the VM pin voltage is 0.35 V typ. or higher by removing the charger.
   The charge overcurrent detection does not function in the overdischarge status.
6. Charge-discharge inhibition status (S-82B2A Series)

6.1 CTL pin control logic active "H"
When the CTL pin voltage is equal to or higher than CTL pin voltage "H" (VCTLH) and the status continues for the charge-discharge inhibition delay time (tCTL) or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the charge-discharge inhibition status. This IC releases charge-discharge inhibition status when the CTL pin voltage is equal to or lower than CTL pin voltage "L" (VCTLL).

6.2 CTL pin control logic active "L"
When the CTL pin voltage is equal to or lower than VCTLL and the status continues for tCTL or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the charge-discharge inhibition status. This IC releases charge-discharge inhibition status when the CTL pin voltage is equal to or higher than VCTLH.

6.3 CTL pin internal resistance connection

6.3.1 CTL pin internal resistance connection "pull-up"
The CTL pin is shorted to the VDD pin by the CTL pin internal resistance (RCTL).

6.3.2 CTL pin internal resistance connection "pull-down"
The CTL pin is shorted to the VSS pin by RCTL.

When the power-down function works, RCTL is disconnected, and the input current and the output current to the CTL pin are cut off. The charge-discharge control by the CTL pin does not function in the overdischarge status.

7. Power-saving status (S-82B2B Series)

7.1 PS pin control logic active "H"
When the PS pin voltage is equal to or higher than PS pin voltage "H" (VPsiL) and the status continues for the power-saving delay time (tPS) or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the power-saving status. In the power-saving status, PS pin internal resistance (RPS) is shorted to the VDD pin, and the VM pin is pulled-up by resistance between VDD pin and VM pin 2 (RVMZ2) and is shorted to the VDD pin, reducing current consumption down to current consumption during power-saving (IPS). When PS pin voltage falls below PS pin voltage "L" (VPsiL), power-saving status is released and RPS is shorted to the VSS pin. At this time, RVMZ2 is not connected.

7.2 PS pin control logic active "L"
When the PS pin voltage is equal to or lower than VPsiL and the status continues for tPS or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the power-saving status. In the power-saving status, RPS is shorted to the VSS pin, and the VM pin is pulled-up by RVMZ2 and is shorted to the VDD pin, reducing current consumption down to tPS. When PS pin voltage falls below VPsiL, power-saving status is released and RPS is shorted to the VDD pin. At this time, RVMZ2 is not connected.

When the power-down function works, RPS is disconnected, and the input current and the output current to the PS pin are cut off. The charge-discharge control by the PS pin does not function in the overcharge status and the overdischarge status.
8. **0 V battery charge enabled**

   This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage \( V_{CHA} \) or a higher voltage is applied between the \( EB^+ \) and \( EB^- \) pins by connecting a charger, the charge control FET gate is fixed to the VDD pin voltage. When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charging current flows through the internal parasitic diode in the discharge control FET. When the battery voltage becomes equal to or higher than \( V_{DL} \), this IC returns to the normal status.

   **Caution**
   1. Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. It depends on the characteristics of the lithium-ion rechargeable battery to be used; therefore, please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.
   2. The 0 V battery charge has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than \( V_{DL} \).

9. **0 V battery charge inhibited**

   This function inhibits charging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage \( V_{INH} \) or lower, the charge control FET gate is fixed to the \( EB^- \) pin voltage to inhibit charging. When the battery voltage is \( V_{INH} \) or higher, charging can be performed.

   **Caution**
   Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. It depends on the characteristics of the lithium-ion rechargeable battery to be used; therefore, please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.

10. **Delay circuit**

   The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

   **Remark** \( t_{DIOV1}, t_{DIOV2} \) and \( t_{SHORT} \) start when \( V_{DIOV1} \) is detected. When \( V_{DIOV2} \) or \( V_{SHORT} \) is detected over \( t_{DIOV2} \) or \( t_{SHORT} \) after the detection of \( V_{DIOV1} \), this IC turns the discharge control FET off within \( t_{DIOV2} \) or \( t_{SHORT} \) of each detection.

---

**Figure 10**

- DO pin voltage
- VINI pin voltage
- VDD
- VSS
- \( V_{DIOV1} \)
- \( V_{DIOV2} \)
- \( V_{SHORT} \)
- Time
- \( t_{D} \)
- \( 0 \leq t_{D} \leq t_{SHORT} \)

---

ABLIC Inc.
**Timing Charts**

1. **Overcharge detection, overdischarge detection**

![Timing Chart Diagram]

- **Battery voltage**
  - $V_{CLn}$ ($V_{CLn} - V_{HCn}$)
  - $V_{DL}$

- **DO pin voltage**
  - $V_{DO}$
  - $V_{SS}$

- **CO pin voltage**
  - $V_{DD}$
  - $V_{SS}$
  - $V_{EB}$

- **VM pin voltage**
  - 0.35 V typ.
    - $V_{SS}$
    - $V_{EB}$

- **VINI pin voltage**
  - $V_{DD}$
  - $V_{DOV1}$
  - $V_{SS}$
  - $V_{COV}$

- **Charger connection**
- **Load connection**

Overcharge detection delay time ($t_{CU}$) | Overdischarge detection delay time ($t_{DL}$)
---|---
(1) | (2) | (1) | (3) | (1)

**Status**

1. Normal status
2. Overcharge status
3. Overdischarge status

**Remark 1.** The charger is assumed to charge with a constant current.

2. $n = 1, 2$

---

ABLIC Inc. 29
2. Discharge overcurrent detection

\[ V_{CLn} \ (V_{CUn} - V_{HCn}) \]

Battery voltage

\[ V_{DUn} \ (V_{DLn} + V_{HDn}) \]

\[ V_{DLn} \]

\[ V_{DO} \]

DO pin voltage

\[ V_{SO} \]

CO pin voltage

\[ V_{DD} \]

\[ V_{DD} \]

VM pin voltage

\[ V_{DD} \]

VINI pin voltage

Load connection

\[ V_{SHORT} \]

\[ V_{DOV2} \]

\[ V_{DOV1} \]

\[ V_{SS} \]

\[ V_{RDV} \]

\[ V_{SS} \]

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3. Charge overcurrent detection

*1. (1): Normal status  
(2): Charge overcurrent status  
(3): Overdischarge status

Remark 1. The charger is assumed to charge with a constant current.
2. \( n = 1, 2 \)

Figure 13
4. Charge-discharge inhibition operation (S-82B2A Series)

![Diagram showing VDD, VSS, DO pin voltage, CO pin voltage, VM pin voltage, CTL pin voltage, Charger connection, Load connection, Charge-discharge inhibition delay time (tCTL), Overdischarge detection delay time (tDL), Charge-discharge inhibition delay time (tCTL)]

*1. (1): Normal status
 (2): Charge-discharge inhibition status
 (3): Overdischarge status

Remark 1. The charger is assumed to charge with a constant current.
2. $n = 1, 2$
5. Power-saving operation (S-82B2B Series)

- **Battery voltage**
  - \( V_{\text{CLn}} \) (\( V_{\text{CLn}} - V_{\text{HCn}} \))
  - \( V_{\text{DLn}} \) (\( V_{\text{DLn}} + V_{\text{HDn}} \))

- **DO pin voltage**
  - \( V_{\text{DD}} \)
  - \( V_{\text{SS}} \)

- **CO pin voltage**
  - \( V_{\text{DD}} \)
  - \( V_{\text{SS}} \)
  - \( V_{\text{EB}} \)

- **VM pin voltage**
  - \( V_{\text{DD}} \)
  - \( V_{\text{SS}} \)
  - \( V_{\text{EB}} \)
  - \( V_{\text{IOV1}} \)

- **PS pin voltage (Active "H")**
  - \( V_{\text{DD}} \)
  - \( V_{\text{PSH}} \)
  - \( V_{\text{PSL}} \)
  - \( V_{\text{SS}} \)

- **PS pin voltage (Active "L")**
  - \( V_{\text{DD}} \)
  - \( V_{\text{PSH}} \)
  - \( V_{\text{PSL}} \)
  - \( V_{\text{SS}} \)

**Charger connection**
- Power-saving delay time \( (t_{\text{PS}}) \)
- Overdischarge detection delay time \( (t_{\text{DL}}) \)
- Power-saving delay time \( (t_{\text{PS}}) \)

**Status**
- (1): Normal status
- (2): Power-saving status
- (3): Overdischarge status

**Remark 1.**
- The charger is assumed to charge with a constant current.
- \( n = 1, 2 \)

---

Figure 15

ABLIC Inc.
### Battery Protection IC Connection Example

![Diagram of Battery Protection IC Connection Example]

#### Table 16  Constants for External Components

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Part</th>
<th>Purpose</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>FET1</td>
<td>N-channel MOS FET</td>
<td>Discharge control</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>Threshold voltage ≤ Overdischarge detection voltage ³¹</td>
</tr>
<tr>
<td>FET2</td>
<td>N-channel MOS FET</td>
<td>Charge control</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>Threshold voltage ≤ Overdischarge detection voltage ³¹</td>
</tr>
<tr>
<td>R1, R2</td>
<td>Resistor</td>
<td>ESD protection, For power fluctuation</td>
<td>100 Ω</td>
<td>100 Ω</td>
<td>150 Ω²</td>
<td>–</td>
</tr>
<tr>
<td>C1, C2</td>
<td>Capacitor</td>
<td>For power fluctuation</td>
<td>0.068 μF</td>
<td>0.1 μF</td>
<td>1.0 μF</td>
<td>–</td>
</tr>
<tr>
<td>R3</td>
<td>Resistor</td>
<td>ESD protection, Protection for reverse connection of a charger</td>
<td>300 Ω</td>
<td>1.0 kΩ</td>
<td>1.5 kΩ</td>
<td>–</td>
</tr>
<tr>
<td>R4</td>
<td>Resistor</td>
<td>Overcurrent detection</td>
<td>–</td>
<td>1 mΩ</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>R5</td>
<td>Resistor</td>
<td>CTL / PS pin input protection</td>
<td>–</td>
<td>1 kΩ</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

¹. If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.
². Accuracy of overcharge detection voltage is guaranteed by R1 = 100 Ω. Connecting resistors with other values will worsen the accuracy.

**Caution**

1. The constants may be changed without notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.
Precautions

- The application status for the input voltage, output voltage, and load current should not exceed the power dissipation.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.
Characteristics (Typical Data)

1. Current consumption

1.1 $I_{OPE}$ vs. $T_a$

![Graph 1.1: $I_{OPE}$ vs. $T_a$]

1.2 $I_{VC}$ vs. $T_a$

![Graph 1.2: $I_{VC}$ vs. $T_a$]

1.3 $I_{PDN}$ vs. $T_a$

![Graph 1.3: $I_{PDN}$ vs. $T_a$]

1.4 $I_{OPED}$ vs. $T_a$

![Graph 1.4: $I_{OPED}$ vs. $T_a$]

1.5 $I_{OPE}$ vs. $V_{DD}$

1.5.1 With power-down function

![Graph 1.5.1: $I_{OPE}$ vs. $V_{DD}$ (S-82B2A Series) with power-down function]

1.5.2 Without power-down function

![Graph 1.5.2: $I_{OPE}$ vs. $V_{DD}$ (S-82B2A Series) without power-down function]

1.6 $I_{PS}$ vs. $T_a$ (S-82B2B Series)

![Graph 1.6: $I_{PS}$ vs. $T_a$ (S-82B2B Series)]

1.7 $I_{PS}$ vs. $V_{DD}$ (S-82B2B Series)

![Graph 1.7: $I_{PS}$ vs. $V_{DD}$ (S-82B2B Series)]
2. Detection voltage, release voltage

2.1 $V_{\text{CUn vs. } T_a}$

2.2 $V_{\text{CLn vs. } T_a}$

2.3 $V_{\text{DLn vs. } T_a}$

2.4 $V_{\text{DUl vs. } T_a}$

2.5 $V_{\text{DIOV1 vs. } V_{\text{DD}}}$

2.6 $V_{\text{DIOV1 vs. } T_a}$

2.7 $V_{\text{DIOV2 vs. } V_{\text{DD}}}$

2.8 $V_{\text{DIOV2 vs. } T_a}$

Remark $n = 1, 2$
2.9 $V_{\text{SHORT}}$ vs. $V_{\text{DD}}$

- $V_{\text{SHORT}}$ [mV]:
  - 94
  - 97
  - 100
  - 103
  - 106

- $V_{\text{DD}}$ [V]:
  - 4.8
  - 5.8
  - 6.8
  - 7.8
  - 8.8

2.10 $V_{\text{SHORT}}$ vs. $T_a$

- $V_{\text{SHORT}}$ [mV]:
  - 94
  - 97
  - 100
  - 103
  - 106

- $T_a$ [°C]:
  - -40
  - -25
  - 0
  - 25
  - 50
  - 75
  - 85

2.11 $V_{\text{CIOV}}$ vs. $V_{\text{DD}}$

- $V_{\text{CIOV}}$ [mV]:
  - -13
  - -14
  - -15
  - -16
  - -17

- $V_{\text{DD}}$ [V]:
  - 4.8
  - 5.8
  - 6.8
  - 7.8
  - 8.8

2.12 $V_{\text{CIOV}}$ vs. $T_a$

- $V_{\text{CIOV}}$ [mV]:
  - -13
  - -14
  - -15
  - -16
  - -17

- $T_a$ [°C]:
  - -40
  - -25
  - 0
  - 25
  - 50
  - 75
  - 85
3. Delay time

3.1 $t_{CU}$ vs. $T_a$

3.2 $t_{DL}$ vs. $T_a$

3.3 $t_{DIOV1}$ vs. $V_{DD}$

3.4 $t_{DIOV1}$ vs. $T_a$

3.5 $t_{DIOV2}$ vs. $V_{DD}$

3.6 $t_{DIOV2}$ vs. $T_a$

3.7 $t_{SHORT}$ vs. $V_{DD}$

3.8 $t_{SHORT}$ vs. $T_a$
3. 9 \( t_{CIOV} \) vs. \( V_{DD} \)

3. 10 \( t_{CIOV} \) vs. \( T_a \)

3. 11 \( t_{CTL} \) vs. \( V_{DD} \) (S-82B2A Series)

3. 12 \( t_{CTL} \) vs. \( T_a \) (S-82B2A Series)

3. 13 \( t_{PS} \) vs. \( V_{DD} \) (S-82B2B Series)

3. 14 \( t_{PS} \) vs. \( T_a \) (S-82B2B Series)
4. Output resistance

4.1 $R_{COH}$ vs. $V_{CO}$

4.2 $R_{COL}$ vs. $V_{CO}$

4.3 $R_{DOH}$ vs. $V_{DO}$

4.4 $R_{DOL}$ vs. $V_{DO}$
Marking Specifications

1. **SNT-8A**

   ![Top View Diagram]

   - (1): Blank
   - (2) to (4): Product code (Refer to Product name vs. Product code)
   - (5), (6): Blank
   - (7) to (11): Lot number

   **Product name vs. Product code**

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Product Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2AAA-I8T1U7</td>
<td>9 D E</td>
</tr>
<tr>
<td>S-82B2AAA-A8T2U7</td>
<td>9 D E</td>
</tr>
</tbody>
</table>

2. **HSNT-8(1616)**

   ![Top View Diagram]

   - (1): Blank
   - (2) to (4): Product code (Refer to Product name vs. Product code)
   - (5) to (7): Lot number

   **Product name vs. Product code**

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Product Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-82B2AAA-I8T1U7</td>
<td>9 D E</td>
</tr>
<tr>
<td>S-82B2AAA-A8T2U7</td>
<td>9 D E</td>
</tr>
</tbody>
</table>
**Power Dissipation**

**SNT-8A**

<table>
<thead>
<tr>
<th>Board</th>
<th>Power Dissipation (Pd) [W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.47 W</td>
</tr>
<tr>
<td>B</td>
<td>0.58 W</td>
</tr>
<tr>
<td>C</td>
<td>–</td>
</tr>
<tr>
<td>D</td>
<td>–</td>
</tr>
<tr>
<td>E</td>
<td>–</td>
</tr>
</tbody>
</table>

**HSNT-8(1616)**

<table>
<thead>
<tr>
<th>Board</th>
<th>Power Dissipation (Pd) [W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.47 W</td>
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<tr>
<td>C</td>
<td>–</td>
</tr>
<tr>
<td>D</td>
<td>–</td>
</tr>
<tr>
<td>E</td>
<td>–</td>
</tr>
</tbody>
</table>
### Board A

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size [mm]</td>
<td>114.3 x 76.2 x t1.6</td>
</tr>
<tr>
<td>Material</td>
<td>FR-4</td>
</tr>
<tr>
<td>Number of copper foil layer</td>
<td>2</td>
</tr>
<tr>
<td>Copper foil layer [mm]</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Land pattern and wiring for testing: t0.070</td>
</tr>
<tr>
<td>2</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>74.2 x 74.2 x t0.070</td>
</tr>
<tr>
<td>Thermal via</td>
<td>-</td>
</tr>
</tbody>
</table>

### Board B

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size [mm]</td>
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<td>Copper foil layer [mm]</td>
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<tr>
<td>1</td>
<td>Land pattern and wiring for testing: t0.070</td>
</tr>
<tr>
<td>2</td>
<td>74.2 x 74.2 x t0.035</td>
</tr>
<tr>
<td>3</td>
<td>74.2 x 74.2 x t0.035</td>
</tr>
<tr>
<td>4</td>
<td>74.2 x 74.2 x t0.070</td>
</tr>
<tr>
<td>Thermal via</td>
<td>-</td>
</tr>
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</table>
## HSNT-8(1616) Test Board

### (1) Board A

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Size [mm]</td>
<td>114.3 x 76.2 x t1.6</td>
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<tr>
<td>Material</td>
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<tr>
<td>Number of copper foil layer</td>
<td>2</td>
</tr>
<tr>
<td>Copper foil layer [mm]</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Land pattern and wiring for testing: t0.070</td>
</tr>
<tr>
<td>2</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>74.2 x 74.2 x t0.070</td>
</tr>
<tr>
<td>Thermal via</td>
<td>-</td>
</tr>
</tbody>
</table>

### (2) Board B

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Size [mm]</td>
<td>114.3 x 76.2 x t1.6</td>
</tr>
<tr>
<td>Material</td>
<td>FR-4</td>
</tr>
<tr>
<td>Number of copper foil layer</td>
<td>4</td>
</tr>
<tr>
<td>Copper foil layer [mm]</td>
<td></td>
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<tr>
<td>1</td>
<td>Land pattern and wiring for testing: t0.070</td>
</tr>
<tr>
<td>2</td>
<td>74.2 x 74.2 x t0.035</td>
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<td>4</td>
<td>74.2 x 74.2 x t0.070</td>
</tr>
<tr>
<td>Thermal via</td>
<td>-</td>
</tr>
</tbody>
</table>

No. HSNT8-B-Board-SD-1.0
No. PH008-A-P-SD-2.1

<table>
<thead>
<tr>
<th>TITLE</th>
<th>SNT-8A-A-PKG Dimensions</th>
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<tbody>
<tr>
<td>No.</td>
<td>PH008-A-P-SD-2.1</td>
</tr>
<tr>
<td>ANGLE</td>
<td></td>
</tr>
<tr>
<td>UNIT</td>
<td>mm</td>
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</tbody>
</table>

ABLIC Inc.
Enlarged drawing in the central part

No. PH008-A-R-SD-2.0

<table>
<thead>
<tr>
<th>TITLE</th>
<th>SNT-8A-A-Reel</th>
</tr>
</thead>
<tbody>
<tr>
<td>No.</td>
<td>PH008-A-R-SD-2.0</td>
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<tr>
<td>ANGLE</td>
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<tr>
<td>UNIT</td>
<td>mm</td>
</tr>
<tr>
<td>QTY.</td>
<td>5,000</td>
</tr>
</tbody>
</table>

ABLIC Inc.
※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げてください (1.96 mm ～ 2.06 mm)。

注意 1. パッケージのモールド樹脂にシルク印刷やハング印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm
   以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は“SNTパッケージ活用の手引き”を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm
   or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ～ 2.06 mm)。

注意 1. 请勿在焊盘型封装的下面印制丝网、锡丝。
2. 在封装下，布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅"SNT 封装的应用指南"。

<table>
<thead>
<tr>
<th>TITLE</th>
<th>SNT-8A-A -Land Recommendation</th>
</tr>
</thead>
<tbody>
<tr>
<td>No.</td>
<td>PH008-A-L-SD-4.1</td>
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</table>

<table>
<thead>
<tr>
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<th>PH008-A-L-SD-4.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>UNIT</td>
<td>mm</td>
</tr>
</tbody>
</table>

ABLIC Inc.
※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PY008-A-P-SD-1.0

<table>
<thead>
<tr>
<th>TITLE</th>
<th>HSNT-8-B-PKG Dimensions</th>
</tr>
</thead>
<tbody>
<tr>
<td>No.</td>
<td>PY008-A-P-SD-1.0</td>
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<tr>
<td>ANGLE</td>
<td>℃</td>
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<tr>
<td>UNIT</td>
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</table>

ABLIC Inc.
No. PY008-A-C-SD-1.0

<table>
<thead>
<tr>
<th>TITLE</th>
<th>HSNT-8-B-Carrier Tape</th>
</tr>
</thead>
<tbody>
<tr>
<td>No.</td>
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</tr>
<tr>
<td>ANGLE</td>
<td></td>
</tr>
<tr>
<td>UNIT</td>
<td>mm</td>
</tr>
</tbody>
</table>

ABLIC Inc.
Enlarged drawing in the central part

No. PY008-A-R-SD-1.0

<table>
<thead>
<tr>
<th>TITLE</th>
<th>HSNT-8-B-Reel</th>
</tr>
</thead>
<tbody>
<tr>
<td>No.</td>
<td>PY008-A-R-SD-1.0</td>
</tr>
<tr>
<td>ANGLE</td>
<td>QTY. 5,000</td>
</tr>
<tr>
<td>UNIT</td>
<td>mm</td>
</tr>
</tbody>
</table>

ABLIC Inc.
Caution: It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意: 放熱性を確保する為に、PKGの裏面放熱板(ヒートシンク)を基板に半田付けする事を推奨いたします。

### Metal Mask Pattern

<table>
<thead>
<tr>
<th>TITLE</th>
<th>HSNT-8-B -Land Recommendation</th>
</tr>
</thead>
<tbody>
<tr>
<td>No.</td>
<td>PY008-A-L-SD-1.0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ANGLE</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>UNIT</td>
<td>mm</td>
</tr>
</tbody>
</table>

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