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BATTERY PROTECTION IC FOR 2-SERIAL-CELL PACK

Rev.2.2_00

This IC is a protection IC for lithium-ion / lithium polymer rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. It is suitable for protecting 2-serial-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, and overcurrent.
Use of an external overcurrent detection resistor enables this IC to provide high-accuracy overcurrent protection with less impact from temperature changes.
The S-82B2A Series has an input pin for charge-discharge control signal (CTL pin), allowing for charge-discharge control with an external signal. The S-82B2B Series has an input pin for power-saving signal (PS pin), allowing for reduction of current consumption by using an external signal to start the power-saving function.

■ Features

- High-accuracy voltage detection circuit

Overcharge detection voltage n	3.500 V to 4.800 V (5 mV step)	Accuracy ±20 mV
Overcharge release voltage n	3.100 V to 4.800 V*1	Accuracy ±50 mV
Overdischarge detection voltage n	2.000 V to 3.000 V (10 mV step)	Accuracy ±50 mV
Overdischarge release voltage n	2.000 V to 3.400 V*2	Accuracy ±75 mV
Discharge overcurrent 1 detection voltage	3 mV to 100 mV (0.5 mV step)	Accuracy ±3.0 mV
Discharge overcurrent 2 detection voltage	10 mV to 100 mV (1 mV step)	Accuracy ±5 mV
Load short-circuiting detection voltage	20 mV to 100 mV (1 mV step)	Accuracy ±10 mV
Charge overcurrent detection voltage	–100 mV to –3 mV (0.5 mV step)	Accuracy ±3.0 mV

- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary).
- Charge-discharge control function (S-82B2A Series)
  - CTL pin control logic: Active "H", active "L"
  - CTL pin internal resistance connection: Pull-up, pull-down
  - CTL pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)
- Power-saving function (S-82B2B Series)
  - PS pin control logic: Active "H", active "L"
  - PS pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)
- 0 V battery charge: Enabled, inhibited
- Power-down function: S-82B2A Series: Available, unavailable
  S-82B2B Series: Available
- High-withstand voltage: VM pin and CO pin: Absolute maximum rating 28 V
- Wide operation temperature range: Ta = –40°C to +85°C
- Low current consumption
  - During operation: 3.0 μA typ., 6.0 μA max. (Ta = +25°C)
  - During power-down: 50 nA max. (Ta = +25°C)
  - During overdischarge: 1.0 μA max. (Ta = +25°C)
  - During power-saving (S-82B2B Series): 50 nA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)
***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)

Remark n = 1, 2

■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Packages

- SNT-8A
- HSNT-8(1616)

■ Block Diagram

1. S-82B2A Series

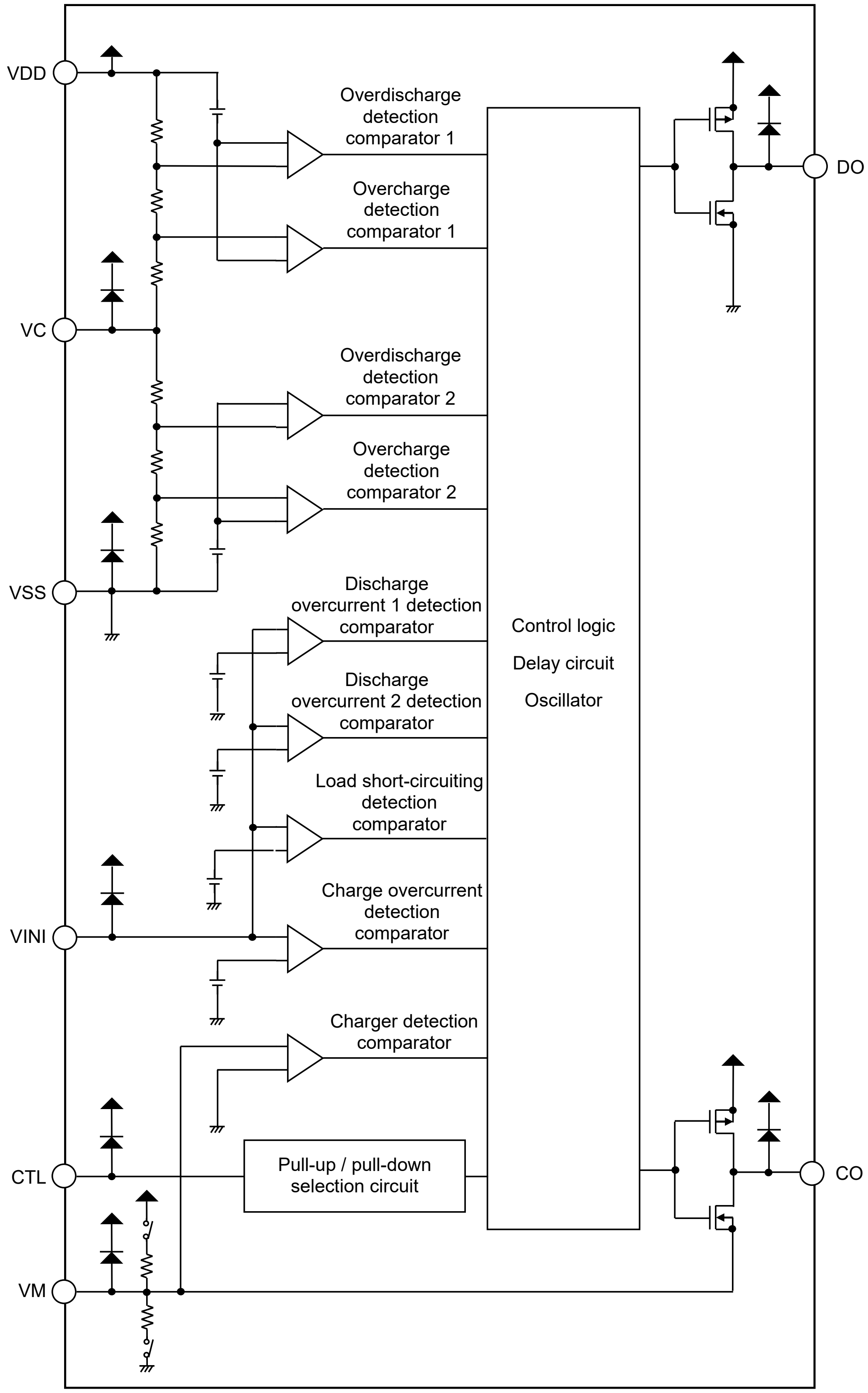


Figure 1

2. S-82B2B Series

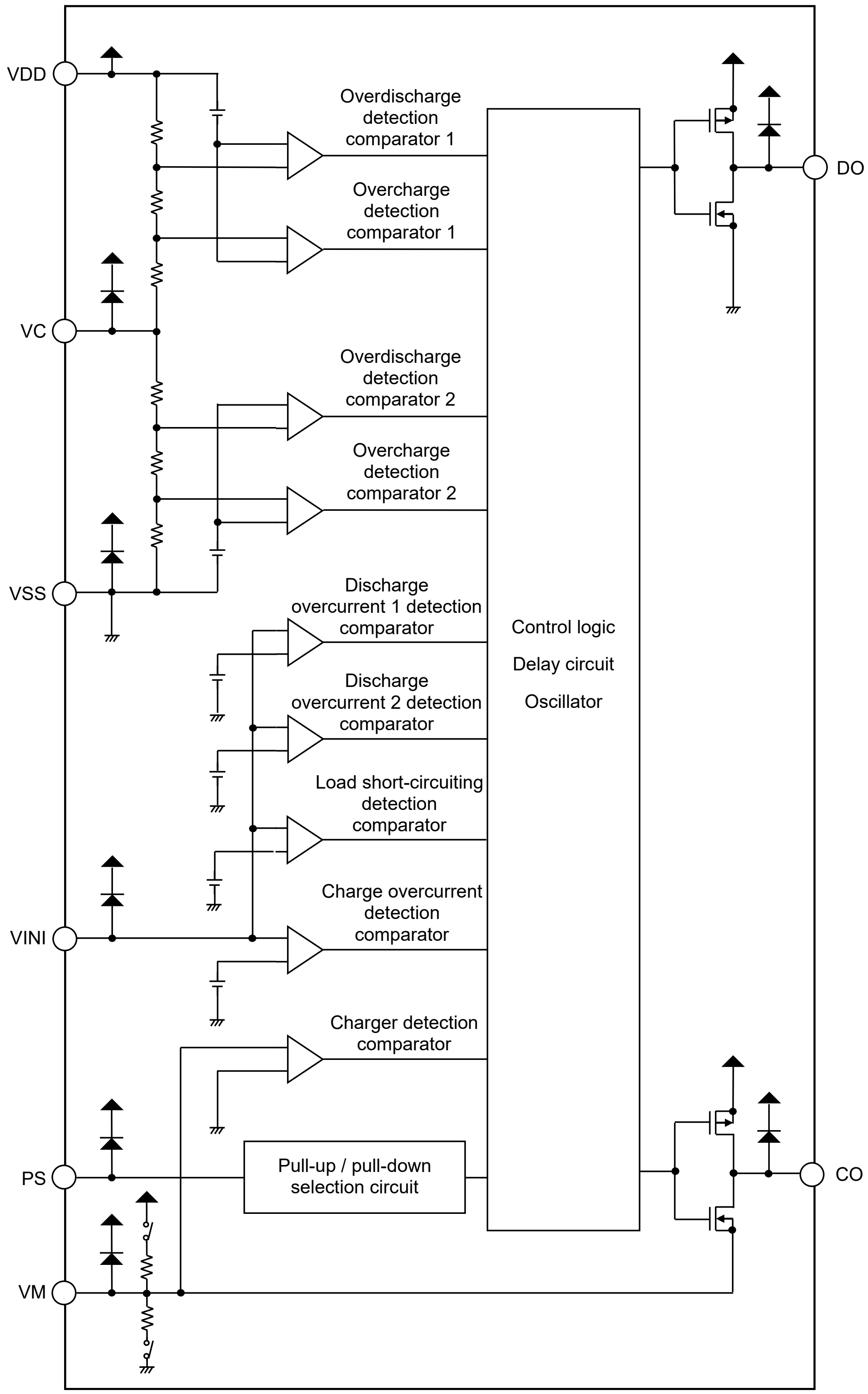


Figure 2

■ Product Name Structure

1. Product name

S-82B2 x xx - xxxx U 7

- U: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- xxxx: Package abbreviation and IC packing specifications*1
  - I8T1: SNT-8A, Tape
  - A8T2: HSNT-8(1616), Tape
- xx: Serial code*2
  - Sequentially set from AA to ZZ
- x: Product type
  - A: Charge-discharge control function
  - B: Power-saving function

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD
HSNT-8(1616)	PY008-A-P-SD	PY008-A-C-SD	PY008-A-R-SD	PY008-A-L-SD

3. Product name list

3. 1 S-82B2A Series

3. 1. 1 SNT-8A

Table 2 (1 / 3)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent 1 Detection Voltage [V_{DIOV1}]	Discharge Overcurrent 2 Detection Voltage [V_{DIOV2}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]
S-82B2AAA-I8T1U7	4.230 V	4.080 V	2.700 V	2.900 V	25.0 mV	50 mV	100 mV	−15.0 mV

Table 2 (2 / 3)

Product Name	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]	Discharge Overcurrent 1 Detection Delay Time [t_{DIOV1}]	Discharge Overcurrent 2 Detection Delay Time [t_{DIOV2}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]	Charge-discharge Inhibition Delay Time [t_{CTL}]
S-82B2AAA-I8T1U7	1.0 s	128 ms	512 ms	16 ms	280 μs	8 ms	48 ms

Table 2 (3 / 3)

Product Name	CTL Pin Control Logic*1	CTL Pin Internal Resistance Connection*2	CTL Pin Internal Resistance Value*3 [R_{CTL}]	CTL Pin Voltage "H"*4 [V_{CTLH}]	CTL Pin Voltage "L"*5 [V_{CTLL}]	0 V Battery Charge*6	Power-down Function*7
S-82B2AAA-I8T1U7	Active "H"	Pull-down	3 MΩ	V_{DD} − 0.90 V	V_{SS} + 0.70 V	Inhibited	Available

***1.** CTL pin control logic: Active "H", active "L"
***2.** CTL pin internal resistance connection: Pull-up, pull-down
***3.** CTL pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)
***4.** CTL pin voltage "H": V_{SS} + 0.75 V, V_{DD} − 0.90 V
***5.** CTL pin voltage "L": V_{SS} + 0.70 V, V_{DD} − 0.95 V
***6.** 0 V battery charge: Enabled, inhibited
***7.** Power-down function: Available, unavailable

Remark 1. Please contact our sales representatives for products other than the above.
2. The delay times can be changed within the range listed in **Table 6**.
For details, please contact our sales representatives.

3. 1. 2 HSNT-8(1616)

Table 3 (1 / 3)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent 1 Detection Voltage [V_{DIOV1}]	Discharge Overcurrent 2 Detection Voltage [V_{DIOV2}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]
S-82B2AAA-A8T2U7	4.230 V	4.080 V	2.700 V	2.900 V	25.0 mV	50 mV	100 mV	−15.0 mV

Table 3 (2 / 3)

Product Name	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]	Discharge Overcurrent 1 Detection Delay Time [t_{DIOV1}]	Discharge Overcurrent 2 Detection Delay Time [t_{DIOV2}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]	Charge-discharge Inhibition Delay Time [t_{CTL}]
S-82B2AAA-A8T2U7	1.0 s	128 ms	512 ms	16 ms	280 μs	8 ms	48 ms

Table 3 (3 / 3)

Product Name	CTL Pin Control Logic*1	CTL Pin Internal Resistance Connection*2	CTL Pin Internal Resistance Value*3 [R_{CTL}]	CTL Pin Voltage "H"*4 [V_{CTLH}]	CTL Pin Voltage "L"*5 [V_{CTLL}]	0 V Battery Charge*6	Power-down Function*7
S-82B2AAA-A8T2U7	Active "H"	Pull-down	3 MΩ	V_{DD} − 0.90 V	V_{SS} + 0.70 V	Inhibited	Available

***1.** CTL pin control logic: Active "H", active "L"
***2.** CTL pin internal resistance connection: Pull-up, pull-down
***3.** CTL pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)
***4.** CTL pin voltage "H": V_{SS} + 0.75 V, V_{DD} − 0.90 V
***5.** CTL pin voltage "L": V_{SS} + 0.70 V, V_{DD} − 0.95 V
***6.** 0 V battery charge: Enabled, inhibited
***7.** Power-down function: Available, unavailable

Remark 1. Please contact our sales representatives for products other than the above.
2. The delay times can be changed within the range listed in **Table 6**.
For details, please contact our sales representatives.

3. 2 S-82B2B Series

3. 2. 1 SNT-8A

Table 4 (1 / 3)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent 1 Detection Voltage [V_{DIOV1}]	Discharge Overcurrent 2 Detection Voltage [V_{DIOV2}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]
S-82B2BAA-I8T1U7	4.475 V	4.325 V	2.100 V	2.300 V	7.0 mV	15 mV	30 mV	−7.0 mV

Table 4 (2 / 3)

Product Name	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]	Discharge Overcurrent 1 Detection Delay Time [t_{DIOV1}]	Discharge Overcurrent 2 Detection Delay Time [t_{DIOV2}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]	Power-saving Delay Time [t_{PS}]
S-82B2BAA-I8T1U7	1.0 s	64 ms	3.75 s	16 ms	280 μs	16 ms	2 ms

Table 4 (3 / 3)

Product Name	PS Pin Control Logic*1	PS Pin Internal Resistance Value*2 [R_{PS}]	PS Pin Voltage "H"*3 [V_{PSH}]	PS Pin Voltage "L"*4 [V_{PSL}]	0 V Battery Charge*5
S-82B2BAA-I8T1U7	Active "H"	5 MΩ	V_{DD} − 0.90 V	V_{SS} + 0.70 V	Inhibited

***1.** PS pin control logic: Active "H", active "L"
***2.** PS pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)
***3.** PS pin voltage "H": V_{SS} + 0.75 V, V_{DD} − 0.90 V
***4.** PS pin voltage "L": V_{SS} + 0.70 V, V_{DD} − 0.95 V
***5.** 0 V battery charge: Enabled, inhibited

Remark 1. Please contact our sales representatives for products other than the above.
2. The delay times can be changed within the range listed in **Table 6**.
For details, please contact our sales representatives.

3. 2. 2 HSNT-8(1616)

Table 5 (1 / 3)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent 1 Detection Voltage [V_{DIOV1}]	Discharge Overcurrent 2 Detection Voltage [V_{DIOV2}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]
S-82B2BAA-A8T2U7	4.475 V	4.325 V	2.100 V	2.300 V	7.0 mV	15 mV	30 mV	−7.0 mV

Table 5 (2 / 3)

Product Name	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]	Discharge Overcurrent 1 Detection Delay Time [t_{DIOV1}]	Discharge Overcurrent 2 Detection Delay Time [t_{DIOV2}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]	Power-saving Delay Time [t_{PS}]
S-82B2BAA-A8T2U7	1.0 s	64 ms	3.75 s	16 ms	280 μs	16 ms	2 ms

Table 5 (3 / 3)

Product Name	PS Pin Control Logic*1	PS Pin Internal Resistance Value*2 [R_{PS}]	PS Pin Voltage "H"*3 [V_{PSH}]	PS Pin Voltage "L"*4 [V_{PSL}]	0 V Battery Charge*5
S-82B2BAA-A8T2U7	Active "H"	5 MΩ	V_{DD} − 0.90 V	V_{SS} + 0.70 V	Inhibited

***1.** PS pin control logic: Active "H", active "L"
***2.** PS pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)
***3.** PS pin voltage "H": V_{SS} + 0.75 V, V_{DD} − 0.90 V
***4.** PS pin voltage "L": V_{SS} + 0.70 V, V_{DD} − 0.95 V
***5.** 0 V battery charge: Enabled, inhibited

Remark 1. Please contact our sales representatives for products other than the above.
2. The delay times can be changed within the range listed in **Table 6**.
For details, please contact our sales representatives.

Table 6

Delay Time	Symbol	Selection Range						Remark
Overcharge detection delay time	t_{CU}	256 ms	512 ms	1.0 s	–	–	–	Select a value from the left.
Overdischarge detection delay time	t_{DL}	32 ms	64 ms	128 ms	–	–	–	Select a value from the left.
Discharge overcurrent 1 detection delay time	t_{DIOV1}	8 ms	16 ms	32 ms	64 ms	128 ms	256 ms	Select a value from the left.
		512 ms	1.0 s	1.28 s	2.0 s	3.0 s	3.75 s	
		4.0 s	–	–	–	–	–	
Discharge overcurrent 2 detection delay time	t_{DIOV2}	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.
Load short-circuiting detection delay time	t_{SHORT}	280 μs	530 μs	–	–	–	–	Select a value from the left.
Charge overcurrent detection delay time	t_{CIOV}	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.
Charge-discharge inhibition delay time	t_{CTL}	2 ms	4 ms	48 ms	64 ms	128 ms	256 ms	Select a value from the left.
Power-saving delay time	t_{PS}	2 ms	4 ms	48 ms	64 ms	128 ms	256 ms	Select a value from the left.

■ Pin Configuration

1. SNT-8A

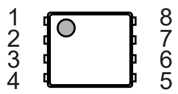


Figure 3

Table 7 S-82B2A Series

Pin No.	Symbol	Description
1	CTL	Input pin for charge-discharge control signal
2	VM	Input pin for external negative voltage
3	CO	Connection pin of charge control FET gate (CMOS output)
4	DO	Connection pin of discharge control FET gate (CMOS output)
5	VINI	Overcurrent detection pin
6	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 2
7	VC	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
8	VDD	Input pin for positive power supply, connection pin for positive voltage of battery 1

Table 8 S-82B2B Series

Pin No.	Symbol	Description
1	PS	Input pin for power-saving signal
2	VM	Input pin for external negative voltage
3	CO	Connection pin of charge control FET gate (CMOS output)
4	DO	Connection pin of discharge control FET gate (CMOS output)
5	VINI	Overcurrent detection pin
6	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 2
7	VC	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
8	VDD	Input pin for positive power supply, connection pin for positive voltage of battery 1

2. HSNT-8(1616)

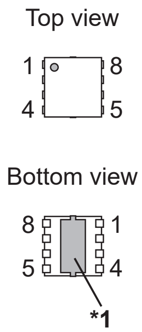


Figure 4

Table 9 S-82B2A Series

Pin No.	Symbol	Description
1	CTL	Input pin for charge-discharge control signal
2	VM	Input pin for external negative voltage
3	CO	Connection pin of charge control FET gate (CMOS output)
4	DO	Connection pin of discharge control FET gate (CMOS output)
5	VINI	Overcurrent detection pin
6	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 2
7	VC	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
8	VDD	Input pin for positive power supply, connection pin for positive voltage of battery 1

Table 10 S-82B2B Series

Pin No.	Symbol	Description
1	PS	Input pin for power-saving signal
2	VM	Input pin for external negative voltage
3	CO	Connection pin of charge control FET gate (CMOS output)
4	DO	Connection pin of discharge control FET gate (CMOS output)
5	VINI	Overcurrent detection pin
6	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 2
7	VC	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
8	VDD	Input pin for positive power supply, connection pin for positive voltage of battery 1

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential open or V_{DD}.
However, do not use it as the function of electrode.

■ Absolute Maximum Ratings

Table 11

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 12	V
VC pin input voltage	V_{VC}	VC	V_{DD} – 12 to V_{DD} + 0.3	V
VINI pin input voltage	V_{VINI}	VINI	V_{DD} – 12 to V_{DD} + 0.3	V
CTL pin input voltage (S-82B2A Series)	V_{CTL}	CTL	V_{DD} – 12 to V_{DD} + 0.3	V
PS pin input voltage (S-82B2B Series)	V_{PS}	PS	V_{DD} – 12 to V_{DD} + 0.3	V
VM pin input voltage	V_{VM}	VM	V_{DD} – 28 to V_{DD} + 0.3	V
DO pin output voltage	V_{DO}	DO	V_{SS} – 0.3 to V_{DD} + 0.3	V
CO pin output voltage	V_{CO}	CO	V_{VM} – 0.3 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 12

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SNT-8A	Board A	–	211	–	°C/W
			Board B	–	173	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		HSNT-8(1616)	Board A	–	214	–	°C/W
			Board B	–	172	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Ta = +25°C

Table 13 (1 / 2)

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n	V_{CUn}	–	V_{CU} – 0.020	V_{CU}	V_{CU} + 0.020	V	1
Overcharge release voltage n	V_{CLn}	$V_{CL} \neq V_{CU}$	V_{CL} – 0.050	V_{CL}	V_{CL} + 0.050	V	1
		$V_{CL} = V_{CU}$	V_{CL} – 0.025	V_{CL}	V_{CL} + 0.020	V	1
Overdischarge detection voltage n	V_{DLn}	–	V_{DL} – 0.050	V_{DL}	V_{DL} + 0.050	V	2
Overdischarge release voltage n	V_{DUn}	$V_{DL} \neq V_{DU}$	V_{DU} – 0.075	V_{DU}	V_{DU} + 0.075	V	2
		$V_{DL} = V_{DU}$	V_{DU} – 0.050	V_{DU}	V_{DU} + 0.050	V	2
Discharge overcurrent 1 detection voltage	V_{DIOV1}	–	V_{DIOV1} – 3	V_{DIOV1}	V_{DIOV1} + 3	mV	5
Discharge overcurrent 2 detection voltage	V_{DIOV2}	–	V_{DIOV2} – 5	V_{DIOV2}	V_{DIOV2} + 5	mV	2
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} – 10	V_{SHORT}	V_{SHORT} + 10	mV	2
Load short-circuiting 2 detection voltage	V_{SHORT2}	–	V_{DD} – 1.2	V_{DD} – 0.9	V_{DD} – 0.6	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 3	V_{CIOV}	V_{CIOV} + 3	mV	2
Discharge overcurrent release voltage	V_{RIOV}	V1 = V2 = 3.4 V	V_{DD} – 1.3	V_{DD} – 1.2	V_{DD} – 1.1	V	5
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled	0.7	1.1	1.5	V	4
0 V battery charge inhibition battery voltage n	V_{0INHn}	0 V battery charge inhibited	1.00	1.25	1.40	V	2
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	V1 = V2 = 1.8 V, V_{VM} = 0 V	1000	2500	5000	kΩ	3
Resistance between VDD pin and VM pin 2	R_{VMD2}	S-82B2B Series	12	18	24	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	V1 = V2 = 3.4 V, V_{VM} = 1.0 V	3.5	7	14	kΩ	3
CTL pin internal resistance	R_{CTL}	S-82B2A Series	R_{CTL} × 0.5	R_{CTL}	R_{CTL} × 2.0	MΩ	3
PS pin internal resistance	R_{PS}	S-82B2B Series	R_{PS} × 0.5	R_{PS}	R_{PS} × 2.0	MΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	10	V	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–	1.5	–	28	V	–
CTL pin voltage "H"	V_{CTLH}	S-82B2A Series	V_{CTLH} – 0.3	V_{CTLH}	V_{CTLH} + 0.3	V	2
CTL pin voltage "L"	V_{CTLL}	S-82B2A Series	V_{CTLL} – 0.3	V_{CTLL}	V_{CTLL} + 0.3	V	2
PS pin voltage "H"	V_{PSH}	S-82B2B Series	V_{PSH} – 0.3	V_{PSH}	V_{PSH} + 0.3	V	2
PS pin voltage "L"	V_{PSL}	S-82B2B Series	V_{PSL} – 0.3	V_{PSL}	V_{PSL} + 0.3	V	2

Remark n = 1, 2

Table 13 (2 / 2)

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Input Current							
Current consumption during operation	I_{OPE}	V1 = V2 = 3.4 V, V_{VM} = 0 V	–	3.0	6.0	μA	3
VC pin current	I_{VC}	V1 = V2 = 3.4 V, V_{VM} = 0 V	–0.1	0.0	0.1	μA	3
Current consumption during power-down	I_{PDN}	V1 = V2 = 1.5 V, V_{VM} = 3.0 V	–	–	50	nA	3
Current consumption during overdischarge	I_{OPED}	V1 = V2 = 1.5 V, V_{VM} = 3.0 V	–	–	1.0	μA	3
Current consumption during power-saving	I_{PS}	S-82B2B Series	–	–	50	nA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	3	6	12	kΩ	4
CO pin resistance "L"	R_{COL}	–	1.5	3	6	kΩ	4
DO pin resistance "H"	R_{DOH}	–	3.5	7	14	kΩ	4
DO pin resistance "L"	R_{DOL}	–	1	2	4	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.7$	t_{CU}	$t_{CU} \times 1.3$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.7$	t_{DL}	$t_{DL} \times 1.3$	–	5
Discharge overcurrent 1 detection delay time	t_{DIOV1}	–	$t_{DIOV1} \times 0.75$	t_{DIOV1}	$t_{DIOV1} \times 1.25$	–	5
Discharge overcurrent 2 detection delay time	t_{DIOV2}	–	$t_{DIOV2} \times 0.7$	t_{DIOV2}	$t_{DIOV2} \times 1.3$	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	$t_{SHORT} \times 0.7$	t_{SHORT}	$t_{SHORT} \times 1.3$	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.7$	t_{CIOV}	$t_{CIOV} \times 1.3$	–	5
Charge-discharge inhibition delay time	t_{CTL}	S-82B2A Series	$t_{CTL} \times 0.7$	t_{CTL}	$t_{CTL} \times 1.3$	–	5
Power-saving delay time	t_{PS}	S-82B2B Series	$t_{PS} \times 0.7$	t_{PS}	$t_{PS} \times 1.3$	–	5

2. Ta = −20°C to +60°C*1

Table 14 (1 / 2)

(Ta = −20°C to +60°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n	V_{CUn}	–	V_{CU} − 0.025	V_{CU}	V_{CU} + 0.025	V	1
Overcharge release voltage n	V_{CLn}	$V_{CL} \neq V_{CU}$	V_{CL} − 0.065	V_{CL}	V_{CL} + 0.057	V	1
		$V_{CL} = V_{CU}$	V_{CL} − 0.030	V_{CL}	V_{CL} + 0.025	V	1
Overdischarge detection voltage n	V_{DLn}	–	V_{DL} − 0.060	V_{DL}	V_{DL} + 0.055	V	2
Overdischarge release voltage n	V_{DUn}	$V_{DL} \neq V_{DU}$	V_{DU} − 0.085	V_{DU}	V_{DU} + 0.080	V	2
		$V_{DL} = V_{DU}$	V_{DU} − 0.060	V_{DU}	V_{DU} + 0.055	V	2
Discharge overcurrent 1 detection voltage	V_{DIOV1}	–	V_{DIOV1} − 5	V_{DIOV1}	V_{DIOV1} + 5	mV	5
Discharge overcurrent 2 detection voltage	V_{DIOV2}	–	V_{DIOV2} − 8	V_{DIOV2}	V_{DIOV2} + 8	mV	2
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} − 20	V_{SHORT}	V_{SHORT} + 20	mV	2
Load short-circuiting 2 detection voltage	V_{SHORT2}	–	V_{DD} − 1.3	V_{DD} − 0.9	V_{DD} − 0.5	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} − 5	V_{CIOV}	V_{CIOV} + 5	mV	2
Discharge overcurrent release voltage	V_{RIOV}	V1 = V2 = 3.4 V	V_{DD} − 1.3	V_{DD} − 1.2	V_{DD} − 1.1	V	5
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled	0.5	1.1	1.7	V	4
0 V battery charge inhibition battery voltage n	V_{0INHn}	0 V battery charge inhibited	1.00	1.25	1.40	V	2
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	V1 = V2 = 1.8 V, V_{VM} = 0 V	500	2500	7000	kΩ	3
Resistance between VDD pin and VM pin 2	R_{VMD2}	S-82B2B Series	8	18	30	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	V1 = V2 = 1.5 V, V_{VM} = 3.0 V	3.5	7	14	kΩ	3
CTL pin internal resistance	R_{CTL}	S-82B2A Series	R_{CTL} × 0.25	R_{CTL}	R_{CTL} × 3.0	MΩ	3
PS pin internal resistance	R_{PS}	S-82B2B Series	R_{PS} × 0.25	R_{PS}	R_{PS} × 3.0	MΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	10	V	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–	1.5	–	28	V	–
CTL pin voltage "H"	V_{CTLH}	S-82B2A Series	V_{CTLH} − 0.4	V_{CTLH}	V_{CTLH} + 0.4	V	2
CTL pin voltage "L"	V_{CTLL}	S-82B2A Series	V_{CTLL} − 0.4	V_{CTLL}	V_{CTLL} + 0.4	V	2
PS pin voltage "H"	V_{PSH}	S-82B2B Series	V_{PSH} − 0.4	V_{PSH}	V_{PSH} + 0.4	V	2
PS pin voltage "L"	V_{PSL}	S-82B2B Series	V_{PSL} − 0.4	V_{PSL}	V_{PSL} + 0.4	V	2

Remark n = 1, 2

Table 14 (2 / 2)

(Ta = −20°C to +60°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Input Current							
Current consumption during operation	I_{OPE}	V1 = V2 = 3.4 V, V_{VM} = 0 V	–	3.0	7.0	μA	3
VC pin current	I_{VC}	V1 = V2 = 3.4 V, V_{VM} = 0 V	−0.1	0.0	0.1	μA	3
Current consumption during power-down	I_{PDN}	V1 = V2 = 1.5 V, V_{VM} = 3.0 V	–	–	100	nA	3
Current consumption during overdischarge	I_{OPED}	V1 = V2 = 1.5 V, V_{VM} = 3.0 V	–	–	1.2	μA	3
Current consumption during power-saving	I_{PS}	S-82B2B Series	–	–	100	nA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	1.5	6	18	kΩ	4
CO pin resistance "L"	R_{COL}	–	0.75	3	9	kΩ	4
DO pin resistance "H"	R_{DOH}	–	1.8	7	21	kΩ	4
DO pin resistance "L"	R_{DOL}	–	0.5	2	6	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.6$	t_{CU}	$t_{CU} \times 1.4$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.6$	t_{DL}	$t_{DL} \times 1.4$	–	5
Discharge overcurrent 1 detection delay time	t_{DIOV1}	–	$t_{DIOV1} \times 0.65$	t_{DIOV1}	$t_{DIOV1} \times 1.35$	–	5
Discharge overcurrent 2 detection delay time	t_{DIOV2}	–	$t_{DIOV2} \times 0.6$	t_{DIOV2}	$t_{DIOV2} \times 1.4$	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	$t_{SHORT} \times 0.6$	t_{SHORT}	$t_{SHORT} \times 1.4$	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.6$	t_{CIOV}	$t_{CIOV} \times 1.4$	–	5
Charge-discharge inhibition delay time	t_{CTL}	S-82B2A Series	$t_{CTL} \times 0.6$	t_{CTL}	$t_{CTL} \times 1.4$	–	5
Power-saving delay time	t_{PS}	S-82B2B Series	$t_{PS} \times 0.6$	t_{PS}	$t_{PS} \times 1.4$	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

3. Ta = −40°C to +85°C*1

Table 15 (1 / 2)

(Ta = −40°C to +85°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n	V_{CUn}	−	V_{CU} − 0.050	V_{CU}	V_{CU} + 0.035	V	1
Overcharge release voltage n	V_{CLn}	$V_{CL} \neq V_{CU}$	V_{CL} − 0.080	V_{CL}	V_{CL} + 0.060	V	1
		$V_{CL} = V_{CU}$	V_{CL} − 0.055	V_{CL}	V_{CL} + 0.035	V	1
Overdischarge detection voltage n	V_{DLn}	−	V_{DL} − 0.060	V_{DL}	V_{DL} + 0.060	V	2
Overdischarge release voltage n	V_{DUn}	$V_{DL} \neq V_{DU}$	V_{DU} − 0.105	V_{DU}	V_{DU} + 0.085	V	2
		$V_{DL} = V_{DU}$	V_{DU} − 0.080	V_{DU}	V_{DU} + 0.060	V	2
Discharge overcurrent 1 detection voltage	V_{DIOV1}	−	V_{DIOV1} − 5	V_{DIOV1}	V_{DIOV1} + 5	mV	5
Discharge overcurrent 2 detection voltage	V_{DIOV2}	−	V_{DIOV2} − 8	V_{DIOV2}	V_{DIOV2} + 8	mV	2
Load short-circuiting detection voltage	V_{SHORT}	−	V_{SHORT} − 20	V_{SHORT}	V_{SHORT} + 20	mV	2
Load short-circuiting 2 detection voltage	V_{SHORT2}	−	V_{DD} − 1.4	V_{DD} − 0.9	V_{DD} − 0.3	V	2
Charge overcurrent detection voltage	V_{CIOV}	−	V_{CIOV} − 5	V_{CIOV}	V_{CIOV} + 5	mV	2
Discharge overcurrent release voltage	V_{RIOV}	V1 = V2 = 3.4 V	V_{DD} − 1.3	V_{DD} − 1.2	V_{DD} − 1.1	V	5
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled	0.5	1.1	1.7	V	4
0 V battery charge inhibition battery voltage n	V_{0INHn}	0 V battery charge inhibited	1.00	1.25	1.40	V	2
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	V1 = V2 = 1.8 V, V_{VM} = 0 V	500	2500	7000	kΩ	3
Resistance between VDD pin and VM pin 2	R_{VMD2}	S-82B2B Series	8	18	30	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	V1 = V2 = 1.5 V, V_{VM} = 3.0 V	3.5	7	14	kΩ	3
CTL pin internal resistance	R_{CTL}	S-82B2A Series	R_{CTL} × 0.25	R_{CTL}	R_{CTL} × 3.0	MΩ	3
PS pin internal resistance	R_{PS}	S-82B2B Series	R_{PS} × 0.25	R_{PS}	R_{PS} × 3.0	MΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	−	1.5	−	10	V	−
Operation voltage between VDD pin and VM pin	V_{DSOP2}	−	1.5	−	28	V	−
CTL pin voltage "H"	V_{CTLH}	S-82B2A Series	V_{CTLH} − 0.4	V_{CTLH}	V_{CTLH} + 0.4	V	2
CTL pin voltage "L"	V_{CTLL}	S-82B2A Series	V_{CTLL} − 0.4	V_{CTLL}	V_{CTLL} + 0.4	V	2
PS pin voltage "H"	V_{PSH}	S-82B2B Series	V_{PSH} − 0.4	V_{PSH}	V_{PSH} + 0.4	V	2
PS pin voltage "L"	V_{PSL}	S-82B2B Series	V_{PSL} − 0.4	V_{PSL}	V_{PSL} + 0.4	V	2

Remark n = 1, 2

Table 15 (2 / 2)

(Ta = −40°C to +85°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Input Current							
Current consumption during operation	I_{OPE}	V1 = V2 = 3.4 V, V_{VM} = 0 V	−	3.0	7.0	μA	3
VC pin current	I_{VC}	V1 = V2 = 3.4 V, V_{VM} = 0 V	−0.15	0.0	0.15	μA	3
Current consumption during power-down	I_{PDN}	V1 = V2 = 1.5 V, V_{VM} = 3.0 V	−	−	150	nA	3
Current consumption during overdischarge	I_{OPED}	V1 = V2 = 1.5 V, V_{VM} = 3.0 V	−	−	1.2	μA	3
Current consumption during power-saving	I_{PS}	S-82B2B Series	−	−	150	nA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	−	1.5	6	18	kΩ	4
CO pin resistance "L"	R_{COL}	−	0.75	3	9	kΩ	4
DO pin resistance "H"	R_{DOH}	−	1.8	7	21	kΩ	4
DO pin resistance "L"	R_{DOL}	−	0.5	2	6	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	−	$t_{CU} \times 0.4$	t_{CU}	$t_{CU} \times 1.6$	−	5
Overdischarge detection delay time	t_{DL}	−	$t_{DL} \times 0.4$	t_{DL}	$t_{DL} \times 1.6$	−	5
Discharge overcurrent 1 detection delay time	t_{DIOV1}	−	$t_{DIOV1} \times 0.4$	t_{DIOV1}	$t_{DIOV1} \times 1.6$	−	5
Discharge overcurrent 2 detection delay time	t_{DIOV2}	−	$t_{DIOV2} \times 0.4$	t_{DIOV2}	$t_{DIOV2} \times 1.6$	−	5
Load short-circuiting detection delay time	t_{SHORT}	−	$t_{SHORT} \times 0.4$	t_{SHORT}	$t_{SHORT} \times 1.6$	−	5
Charge overcurrent detection delay time	t_{CIOV}	−	$t_{CIOV} \times 0.4$	t_{CIOV}	$t_{CIOV} \times 1.6$	−	5
Charge-discharge inhibition delay time	t_{CTL}	S-82B2A Series	$t_{CTL} \times 0.4$	t_{CTL}	$t_{CTL} \times 1.6$	−	5
Power-saving delay time	t_{PS}	S-82B2B Series	$t_{PS} \times 0.4$	t_{PS}	$t_{PS} \times 1.6$	−	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

When CTL pin or PS pin control logic is active "H", SW1 and SW3 are turned off, SW2 and SW4 are turned on. When CTL pin or PS pin control logic is active "L", SW1 and SW3 are turned on, SW2 and SW4 are turned off.

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

Overcharge detection voltage 1 (V_{CU1}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased after setting V1 = V2 = V_{CU} − 0.05 V. Overcharge release voltage 1 (V_{CL1}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when setting V2 = 3.4 V and when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage 1 (V_{HC1}) is defined as the difference between V_{CU1} and V_{CL1}.
Overcharge detection voltage 2 (V_{CU2}), overcharge release voltage 2 (V_{CL2}) and overcharge hysteresis voltage 2 (V_{HC2}) can be determined in the same way.

2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage 1 (V_{DL1}) is defined as the voltage V1 at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V. Overdischarge release voltage 1 (V_{DU1}) is defined as the voltage V1 at which V_{DO} goes from "L" to "H" when setting V3 = 0.01 V, V6 = V7 = 0 V and when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage 1 (V_{HD1}) is defined as the difference between V_{DU1} and V_{DL1}.
Overdischarge detection voltage 2 (V_{DL2}), overdischarge release voltage 2 (V_{DU2}) and overdischarge hysteresis voltage 2 (V_{HD2}) can be determined in the same way.

3. Discharge overcurrent 1 detection voltage, discharge overcurrent release voltage (Test circuit 5)

Discharge overcurrent 1 detection voltage (V_{DIOV1}) is defined as the voltage V6 at which delay time from when V6 is increased after setting V1 = V2 = 3.4 V, V3 = 1.0 V, V6 = V7 = 0 V to when V_{DO} goes from "H" to "L" is discharge overcurrent 1 detection delay time (t_{DIOV1}). Discharge overcurrent release voltage (V_{RIOV}) is defined as the voltage V3 at which V_{DO} goes from "L" to "H" when setting V3 = 6.8 V, V6 = 0 V and when the voltage V3 is then gradually decreased. When the voltage V3 falls below V_{RIOV}, V_{DO} will go to "H" after 1.0 ms typ. and maintain "H" during load short-circuiting detection delay time (t_{SHORT}).

4. Discharge overcurrent 2 detection voltage (Test circuit 2)

Discharge overcurrent 2 detection voltage (V_{DIOV2}) is defined as the voltage V6 at which delay time from when V6 is increased after setting V1 = V2 = 3.4 V, V3 = 1.0 V, V6 = V7 = 0 V to when V_{DO} goes from "H" to "L" is discharge overcurrent 2 detection delay time (t_{DIOV2}).

5. Load short-circuiting detection voltage (Test circuit 2)

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage V6 at which delay time from when V6 is increased after setting V1 = V2 = 3.4 V, V3 = 1.0 V, V6 = V7 = 0 V to when V_{DO} goes from "H" to "L" is t_{SHORT}.

6. Load short-circuiting 2 detection voltage (Test circuit 2)

Load short-circuiting 2 detection voltage (V_{SHORT2}) is defined as the voltage V3 at which delay time from when V3 is increased after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V to when V_{DO} goes from "H" to "L" is t_{SHORT}.

7. Charge overcurrent detection voltage (Test circuit 2)

Charge overcurrent detection voltage (V_{CIOV}) is defined as the voltage V6 at which delay time from when V6 is decreased after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V to when V_{CO} goes from "H" to "L" is charge overcurrent detection delay time (t_{CIOV}).

8. CTL pin voltage "H", CTL pin voltage "L" (S-82B2A Series) (Test circuit 2)

8. 1 CTL pin control logic active "H"

The CTL pin voltage "H" (V_{CTLH}) is defined as the voltage V7 at which V_{CO} and V_{DO} go from "H" to "L" when the voltage V7 is gradually increased after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V.
After that, the CTL pin voltage "L" (V_{CTLL}) is defined as the voltage V7 at which V_{CO} and V_{DO} go from "L" to "H" after V7 is gradually decreased.

8. 2 CTL pin control logic active "L"

V_{CTLL} is defined as the voltage difference between the voltage V7 and the voltage V1 + V2 (V1 + V2 − V7) at which V_{CO} and V_{DO} go from "H" to "L" when the voltage V7 is gradually increased after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V.
After that, V_{CTLH} is defined as V1 + V2 − V7 at which V_{CO} and V_{DO} go from "L" to "H" after V7 is gradually decreased.

9. PS pin voltage "H", PS pin voltage "L" (S-82B2B Series) (Test circuit 2)

9. 1 PS pin control logic active "H"

The PS pin voltage "H" (V_{PSH}) is defined as the voltage V7 at which V_{CO} and V_{DO} go from "H" to "L" when the voltage V7 is gradually increased after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V.
After that, the PS pin voltage "L" (V_{PSL}) is defined as the voltage V7 at which V_{CO} and V_{DO} go from "L" to "H" after V7 is gradually decreased.

9. 2 PS pin control logic active "L"

V_{PSL} is defined as the voltage difference between the voltage V7 and the voltage V1 + V2 (V1 + V2 − V7) at which V_{CO} and V_{DO} go from "H" to "L" when the voltage V7 is gradually increased after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V.
After that, V_{PSH} is defined as V1 + V2 − V7 at which V_{CO} and V_{DO} go from "L" to "H" after V7 is gradually decreased.

10. Current consumption during operation (Test circuit 3)

The current consumption during operation (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V. However, the current flowing through the CTL pin or the PS pin internal resistance is excluded.

11. VC pin current (Test circuit 3)

The VC pin current (I_{VC}) is the current that flows through the VC pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V.

12. Current consumption during power-down, current consumption during overdischarge (Test circuit 3)

12. 1 With power-down function

The current consumption during power-down (I_{PDN}) is I_{DD} under the set conditions of V1 = V2 = 1.5 V, V3 = 3.0 V, V6 = V7 = 0 V.

12. 2 Without power-down function

The current consumption during overdischarge (I_{OPED}) is I_{DD} under the set conditions of V1 = V2 = 1.5 V, V3 = 3.0 V, V6 = V7 = 0 V.

13. Current consumption during power-saving (S-82B2B Series) (Test circuit 3)

The current consumption during power-saving (I_{PS}) is I_{DD} under the set conditions of V1 = V2 = 3.4 V, V3 = 6.8 V, V6 = 0 V, V7 = 6.8 V.

14. Resistance between VDD pin and VM pin (Test circuit 3)

R_{VMD} is the resistance between VDD pin and VM pin under the set conditions of V1 = V2 = 1.8 V, V3 = V6 = V7 = 0 V.

15. Resistance between VDD pin and VM pin 2 (S-82B2B Series) (Test circuit 3)

R_{VMD2} is the resistance between VDD pin and VM pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = 0 V, V7 = 6.8 V.

16. Resistance between VM pin and VSS pin (Test circuit 3)

R_{VMS} is the resistance between VM pin and VSS pin when the voltage V6 is decreased to 0 V after setting V1 = V2 = 3.4 V, V3 = V6 = 1.0 V, V7 = 0 V.

17. CTL pin internal resistance (S-82B2A Series) (Test circuit 3)

17. 1 CTL pin internal resistance connection "pull-up"

The CTL pin internal resistance (R_{CTL}) is the resistance between CTL pin and VDD pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V.

17. 2 CTL pin internal resistance connection "pull-down"

R_{CTL} is the resistance between CTL pin and VSS pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = 0 V, V7 = 6.8 V.

18. PS pin internal resistance (S-82B2B Series) (Test circuit 3)

18. 1 PS pin control logic active "H"

The PS pin internal resistance (R_{PS}) is the resistance between PS pin and VDD pin when the voltage V7 is decreased to 3.4 V after setting V1 = V2 = 3.4 V, V3 = V6 = 0 V, V7 = 6.8 V.

18. 2 PS pin control logic active "L"

R_{PS} is the resistance between PS pin and VSS pin when the voltage V7 is increased to 3.4 V after setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V.

19. CO pin resistance "H" (Test circuit 4)

The CO pin resistance "H" (R_{COH}) is the resistance between VDD pin and CO pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = 0 V, V4 = 6.4 V.

20. CO pin resistance "L" (Test circuit 4)

The CO pin resistance "L" (R_{COL}) is the resistance between VM pin and CO pin under the set conditions of V1 = V2 = 4.9 V, V3 = V6 = 0 V, V4 = 0.4 V.

21. DO pin resistance "H" (Test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = V2 = 3.4 V, V3 = V6 = 0 V, V5 = 6.4 V.

22. DO pin resistance "L" (Test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = V2 = 1.8 V, V3 = V6 = 0 V, V5 = 0.4 V.

23. Overcharge detection delay time (Test circuit 5)

After setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V, the voltage V1 is increased. The time interval from when the voltage V1 exceeds V_{CU} until V_{CO} goes to "L" is the overcharge detection delay time (t_{CU}).

24. Overdischarge detection delay time (Test circuit 5)

After setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V, the voltage V1 is decreased. The time interval from when the voltage V1 falls below V_{DL} until V_{DO} goes to "L" is the overdischarge detection delay time (t_{DL}).

25. Discharge overcurrent n detection delay time (Test circuit 5)

After setting V1 = V2 = 3.4 V, V3 = 1.0 V, V6 = V7 = 0 V, the voltage V6 is increased. The time interval from when the voltage V6 exceeds V_{DIOVn} until V_{DO} goes to "L" is the discharge overcurrent n detection delay time (t_{DIOVn}).

26. Load short-circuiting detection delay time (Test circuit 5)

After setting V1 = V2 = 3.4 V, V3 = 1.0 V, V6 = V7 = 0 V, the voltage V6 is increased. The time interval from when the voltage V6 exceeds V_{SHORT} until V_{DO} goes to "L" is the load short-circuiting detection delay time (t_{SHORT}).

27. Charge overcurrent detection delay time (Test circuit 5)

After setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V, the voltage V6 is decreased. The time interval from when the voltage V6 falls below V_{CIOV} until V_{CO} goes to "L" is the charge overcurrent detection delay time (t_{CIOV}).

Remark n = 1, 2

28. Charge-discharge inhibition delay time (S-82B2A Series) (Test circuit 5)

28. 1 CTL pin control logic active "H"

After setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V, the voltage V7 is increased. The time interval from when the voltage V7 exceeds V_{CTLH} until V_{CO} and V_{DO} go to "L" is the charge-discharge inhibition delay time (t_{CTL}).

28. 2 CTL pin control logic active "L"

After setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V, the voltage V7 is increased. The time interval from when the voltage V1 + V2 − V7 falls below V_{CTLL} until V_{CO} and V_{DO} go to "L" is t_{CTL}.

29. Power-saving delay time (S-82B2B Series) (Test circuit 5)

29. 1 PS pin control logic active "H"

After setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V, the voltage V7 is increased. The time interval from when the voltage V7 exceeds V_{PSH} until V_{CO} and V_{DO} go to "L" is the power-saving delay time (t_{PS}).

29. 2 PS pin control logic active "L"

After setting V1 = V2 = 3.4 V, V3 = V6 = V7 = 0 V, the voltage V7 is increased. The time interval from when the voltage V1 + V2 − V7 falls below V_{PSL} until V_{CO} and V_{DO} go to "L" is t_{PSL}.

30. 0 V battery charge starting charger voltage (0 V battery charge enabled) (Test circuit 4)

The 0 V battery charge starting charger voltage (V_{0CHA}) is defined as the absolute value of voltage V3 at which the current flowing through the CO pin (I_{CO}) exceeds 1.0 μA when the voltage V3 is gradually decreased after setting V1 = V2 = V6 = 0 V, V3 = V4 = −0.5 V.

31. 0 V battery charge inhibition battery voltage n (0 V battery charge inhibited) (Test circuit 2)

The 0 V battery charge inhibition battery voltage n (V_{0INHn}) is defined as the voltage Vn at which V_{CO} goes to "L" (V_{CO} = V_{VM}) when the voltage Vn is gradually decreased after setting V1 = V2 = 1.5 V, V3 = −1.0 V, V6 = V7 = 0 V.

Remark n = 1, 2

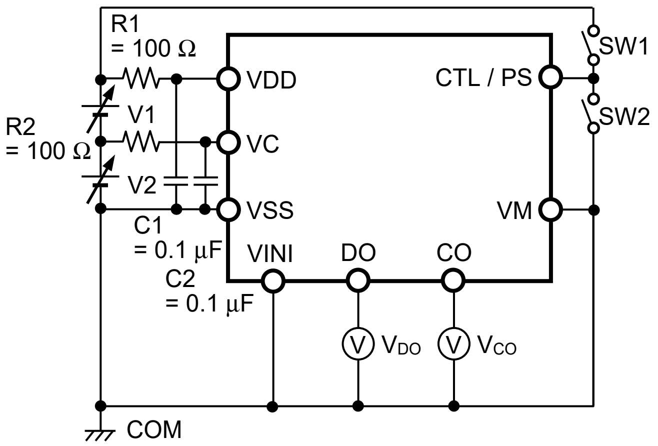


Figure 5 Test Circuit 1

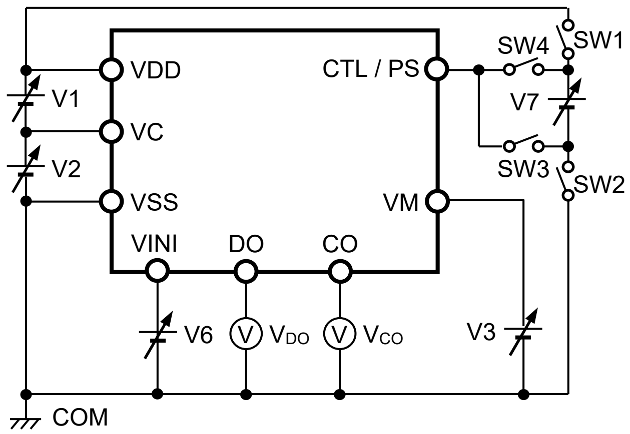


Figure 6 Test Circuit 2

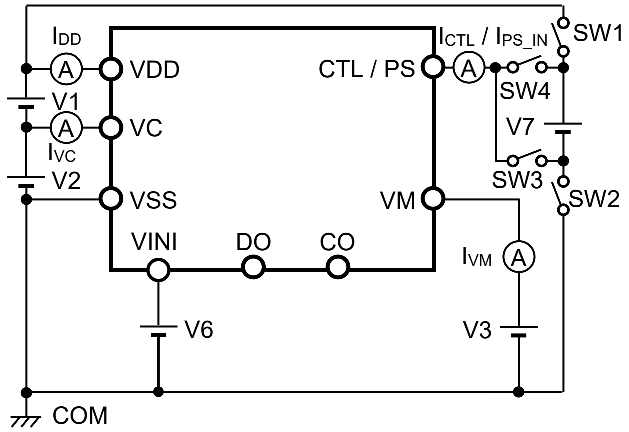


Figure 7 Test Circuit 3

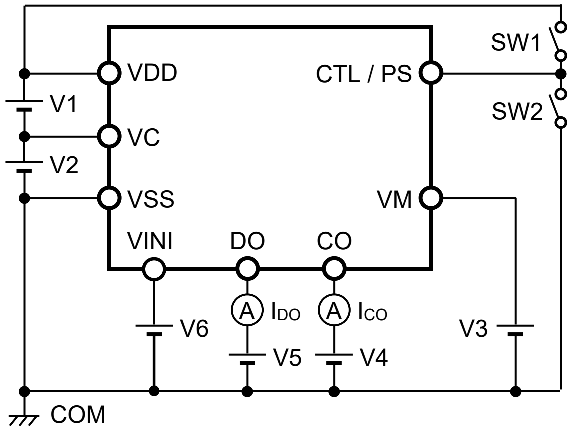


Figure 8 Test Circuit 4

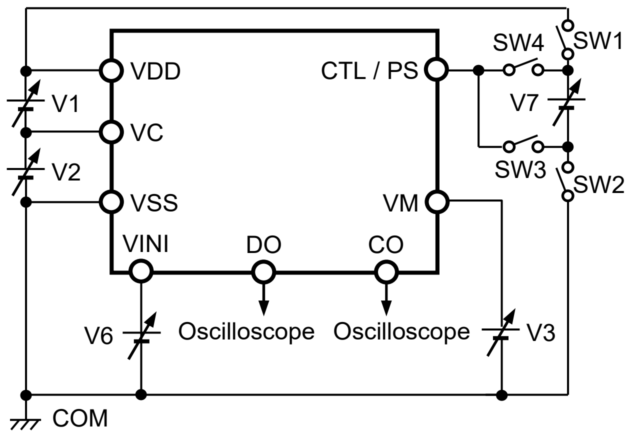


Figure 9 Test Circuit 5

■ Operation

Remark Refer to "**■ Battery Protection IC Connection Example**".

1. Normal status

This IC monitors the voltage of the battery connected between VDD pin and VC pin, VC pin and VSS pin, and the voltage between VINI pin and VSS pin to control charging and discharging.

When the battery voltage is in the range from overdischarge detection voltage (V_{DL}) to overcharge detection voltage (V_{CU}), the VINI pin voltage is in the range from charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent 1 detection voltage (V_{DIOV1}), both charge and discharge control FETs are turned on. This status is called the normal status, and in this condition charging and discharging can be carried out freely.
Also, for the S-82B2A Series, input the voltage that releases the charge-discharge inhibition status to the CTL pin*1, and for the S-82B2B Series, input the voltage that releases the power-saving status to the PS pin*2.
The resistance between VDD pin and VM pin (R_{VMD}), and the resistance between VM pin and VSS pin (R_{VMS}) are not connected in the normal status.

***1.** Refer to "**6. Charge-discharge inhibition status (S-82B2A Series)**".
***2.** Refer to "**7. Power-saving status (S-82B2B Series)**".

Caution After the battery is connected, discharging may not be carried out. In this case, this IC returns to the normal status by connecting a charger.

2. Overcharge status

2. 1 $V_{CL} \neq V_{CU}$ (Product in which overcharge release voltage differs from overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the status continues for the overcharge detection delay time (t_{CU}) or longer, the charge control FET is turned off and charging is stopped. This status is called the overcharge status.
The overcharge status is released in the following two cases.

(1) In the case that the VM pin voltage is lower than 0.35 V typ., this IC releases the overcharge status when the battery voltage falls below overcharge release voltage (V_{CL}).
(2) In the case that the VM pin voltage is equal to or higher than 0.35 V typ., this IC releases the overcharge status when the battery voltage falls below V_{CU}.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the V_f voltage of the internal parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., this IC releases the overcharge status when the battery voltage is equal to or lower than V_{CU}.

Caution If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

2. 2 $V_{CL} = V_{CU}$ (Product in which overcharge release voltage is the same as overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the status continues for t_{CU} or longer, the charge control FET is turned off and charging is stopped. This status is called the overcharge status. In the case that the VM pin voltage is equal to or higher than 0.35 V typ. and the battery voltage falls below V_{CU}, this IC releases the overcharge status.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the V_f voltage of the internal parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., this IC releases the overcharge status when the battery voltage is equal to or lower than V_{CU}.

Caution 1. If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below V_{CL}. The overcharge status is released when the discharge current flows and the VM pin voltage goes over 0.35 V typ. by removing the charger.

3. Overdischarge status

When the battery voltage falls below V_{DL} during discharging in the normal status and the status continues for the overdischarge detection delay time (t_{DL}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the overdischarge status.
Under the overdischarge status, VDD pin and VM pin are shorted by R_{VMD} in this IC. The VM pin voltage is pulled up by R_{VMD}.
When connecting a charger in the overdischarge status, the battery voltage reaches V_{DL} or higher and this IC releases the overdischarge status if the VM pin voltage is below 0 V typ.
The battery voltage reaches the overdischarge release voltage (V_{DU}) or higher and this IC releases the overdischarge status if the VM pin voltage is not below 0 V typ.
R_{VMS} is not connected in the overdischarge status.

3. 1 With power-down function

Under the overdischarge status, when the VM pin voltage is 0.7 V typ. or higher, the power-down function works and the current consumption is reduced to the current consumption during power-down (I_{PDN}). By connecting a battery charger, the power-down function is released when the VM pin voltage is 0.7 V typ. or lower.

- When a battery is not connected to a charger and the VM pin voltage ≥ 0.7 V typ., this IC maintains the overdischarge status even when the battery voltage reaches V_{DU} or higher.
- When a battery is connected to a charger and 0.7 V typ. > the VM pin voltage > 0 V typ., the battery voltage reaches V_{DU} or higher and this IC releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ. ≥ the VM pin voltage, the battery voltage reaches V_{DL} or higher and this IC releases the overdischarge status.

3. 2 Without power-down function

Under the overdischarge status, the power-down function does not work even when the VM pin voltage is 0.7 V typ. or higher.

- When a battery is not connected to a charger and the VM pin voltage ≥ 0.7 V typ., the battery voltage reaches V_{DU} or higher and this IC releases the overdischarge status.
- When a battery is connected to a charger and 0.7 V typ. > the VM pin voltage > 0 V typ., the battery voltage reaches V_{DU} or higher and this IC releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ. ≥ the VM pin voltage, the battery voltage reaches V_{DL} or higher and this IC releases the overdischarge status.

4. Discharge overcurrent status (discharge overcurrent 1, discharge overcurrent 2, load short- circuiting, load short-circuiting 2)

4. 1 Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting

When a battery in the normal status is in the status where the VINI pin voltage is equal to or higher than V_{DIOV1} because the discharge current is equal to or higher than the specified value and the status continues for the discharge overcurrent 1 detection delay time (t_{DIOV1}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.
Under the discharge overcurrent status, VM pin and VSS pin are shorted by R_{VMS} in this IC. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, VM pin returns to the VSS pin voltage.
When the VM pin voltage returns to V_{RIOV} or lower, this IC releases the discharge overcurrent status.
R_{VMD} is not connected in the discharge overcurrent status.

4. 2 Load short-circuiting 2

When a battery in the normal status is in the status where a load causing discharge overcurrent is connected, and the VM pin voltage is equal to or higher than V_{SHORT2} and the status continues for the load short-circuiting detection delay time (t_{SHORT}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.
This IC releases the discharge overcurrent status in the same way as in "**4. 1 Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting**".

5. Charge overcurrent status

When a battery in the normal status is in the status where the VINI pin voltage is equal to or lower than V_{CIOV} because the charge current is equal to or higher than the specified value and the status continues for the charge overcurrent detection delay time (t_{CIOV}) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.
This IC releases the charge overcurrent status when the discharge current flows and the VM pin voltage is 0.35 V typ. or higher by removing the charger.
The charge overcurrent detection does not function in the overdischarge status.

6. Charge-discharge inhibition status (S-82B2A Series)

6. 1 CTL pin control logic active "H"

When the CTL pin voltage is equal to or higher than CTL pin voltage "H" (V_{CTLH}) and the status continues for the charge-discharge inhibition delay time (t_{CTL}) or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the charge-discharge inhibition status.
This IC releases charge-discharge inhibition status when the CTL pin voltage is equal to or lower than CTL pin voltage "L" (V_{CTLL}).

6. 2 CTL pin control logic active "L"

When the CTL pin voltage is equal to or lower than V_{CTLL} and the status continues for t_{CTL} or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the charge-discharge inhibition status.
This IC releases charge-discharge inhibition status when the CTL pin voltage is equal to or higher than V_{CTLH}.

6. 3 CTL pin internal resistance connection

6. 3. 1 CTL pin internal resistance connection "pull-up"

The CTL pin is shorted to the VDD pin by the CTL pin internal resistance (R_{CTL}).

6. 3. 2 CTL pin internal resistance connection "pull-down"

The CTL pin is shorted to the VSS pin by R_{CTL}.

When the power-down function works, R_{CTL} is disconnected, and the input current and the output current to the CTL pin are cut off.
The charge-discharge control by the CTL pin does not function in the overdischarge status.

7. Power-saving status (S-82B2B Series)

7. 1 PS pin control logic active "H"

When the PS pin voltage is equal to or higher than PS pin voltage "H" (V_{PSH}) and the status continues for the power-saving delay time (t_{PS}) or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the power-saving status.
In the power-saving status, PS pin internal resistance (R_{PS}) is shorted to the VDD pin, and the VM pin is pulled-up by resistance between VDD pin and VM pin 2 (R_{VMD2}) and is shorted to the VDD pin, reducing current consumption down to current consumption during power-saving (I_{PS}).
When PS pin voltage falls below PS pin voltage "L" (V_{PSL}), power-saving status is released and R_{PS} is shorted to the VSS pin. At this time, R_{VMD2} is not connected.

7. 2 PS pin control logic active "L"

When the PS pin voltage is equal to or lower than V_{PSL} and the status continues for t_{PS} or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the power-saving status.
In the power-saving status, R_{PS} is shorted to the VSS pin, and the VM pin is pulled-up by R_{VMD2} and is shorted to the VDD pin, reducing current consumption down to I_{PS}.
When PS pin voltage falls below V_{PSL}, power-saving status is released and R_{PS} is shorted to the VDD pin. At this time, R_{VMD2} is not connected.

When the power-down function works, R_{PS} is disconnected, and the input current and the output current to the PS pin are cut off.
The charge-discharge control by the PS pin does not function in the overcharge status and the overdischarge status.

8. 0 V battery charge enabled

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or a higher voltage is applied between the EB+ and EB− pins by connecting a charger, the charge control FET gate is fixed to the VDD pin voltage.
When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charging current flows through the internal parasitic diode in the discharge control FET. When the battery voltage becomes equal to or higher than V_{DL}, this IC returns to the normal status.

Caution 1. Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. It depends on the characteristics of the lithium-ion rechargeable battery to be used; therefore, please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.
2. The 0 V battery charge has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than V_{DL}.

9. 0 V battery charge inhibited

This function inhibits charging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charge control FET gate is fixed to the EB− pin voltage to inhibit charging. When the battery voltage is V_{0INH} or higher, charging can be performed.

Caution Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. It depends on the characteristics of the lithium-ion rechargeable battery to be used; therefore, please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.

10. Delay circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

Remark t_{DIOV1}, t_{DIOV2} and t_{SHORT} start when V_{DIOV1} is detected. When V_{DIOV2} or V_{SHORT} is detected over t_{DIOV2} or t_{SHORT} after the detection of V_{DIOV1}, this IC turns the discharge control FET off within t_{DIOV2} or t_{SHORT} of each detection.

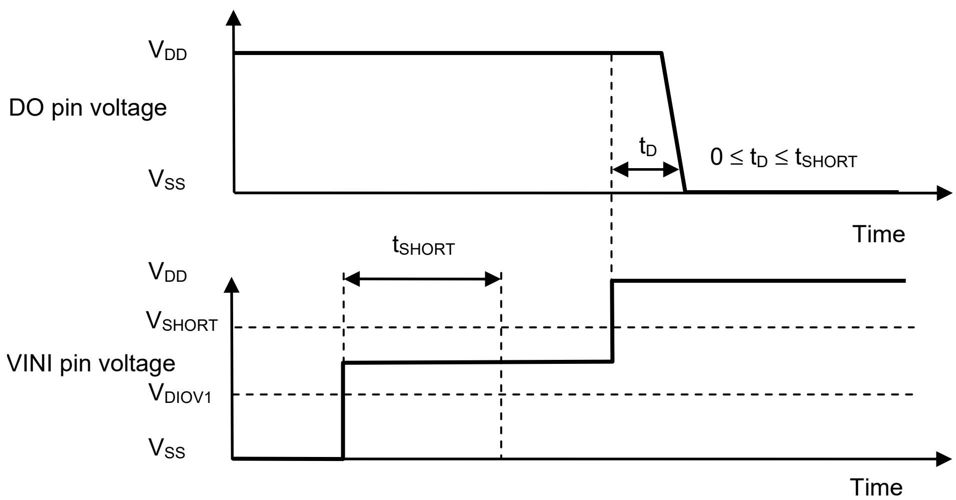
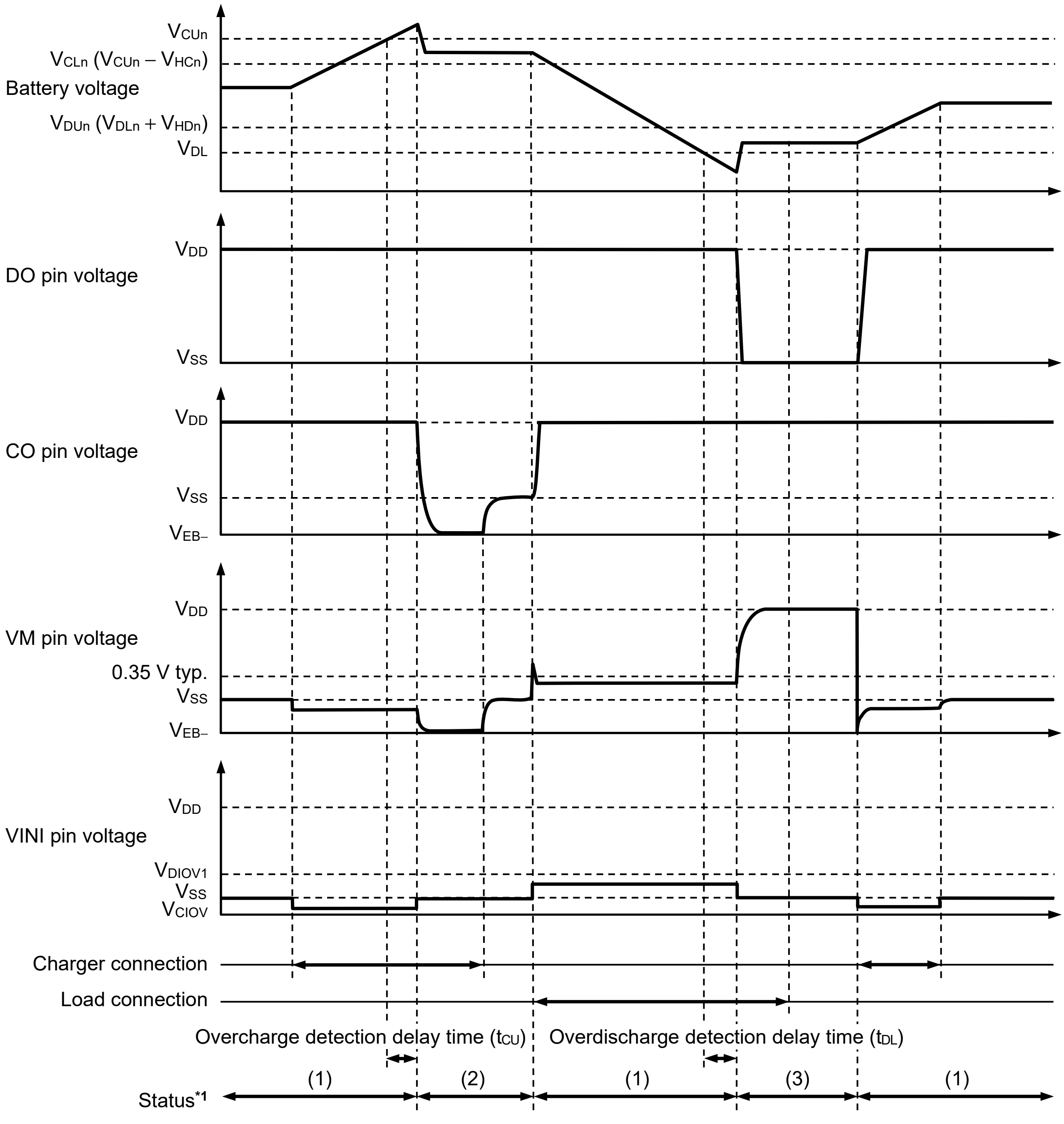


Figure 10

■ Timing Charts

1. Overcharge detection, overdischarge detection

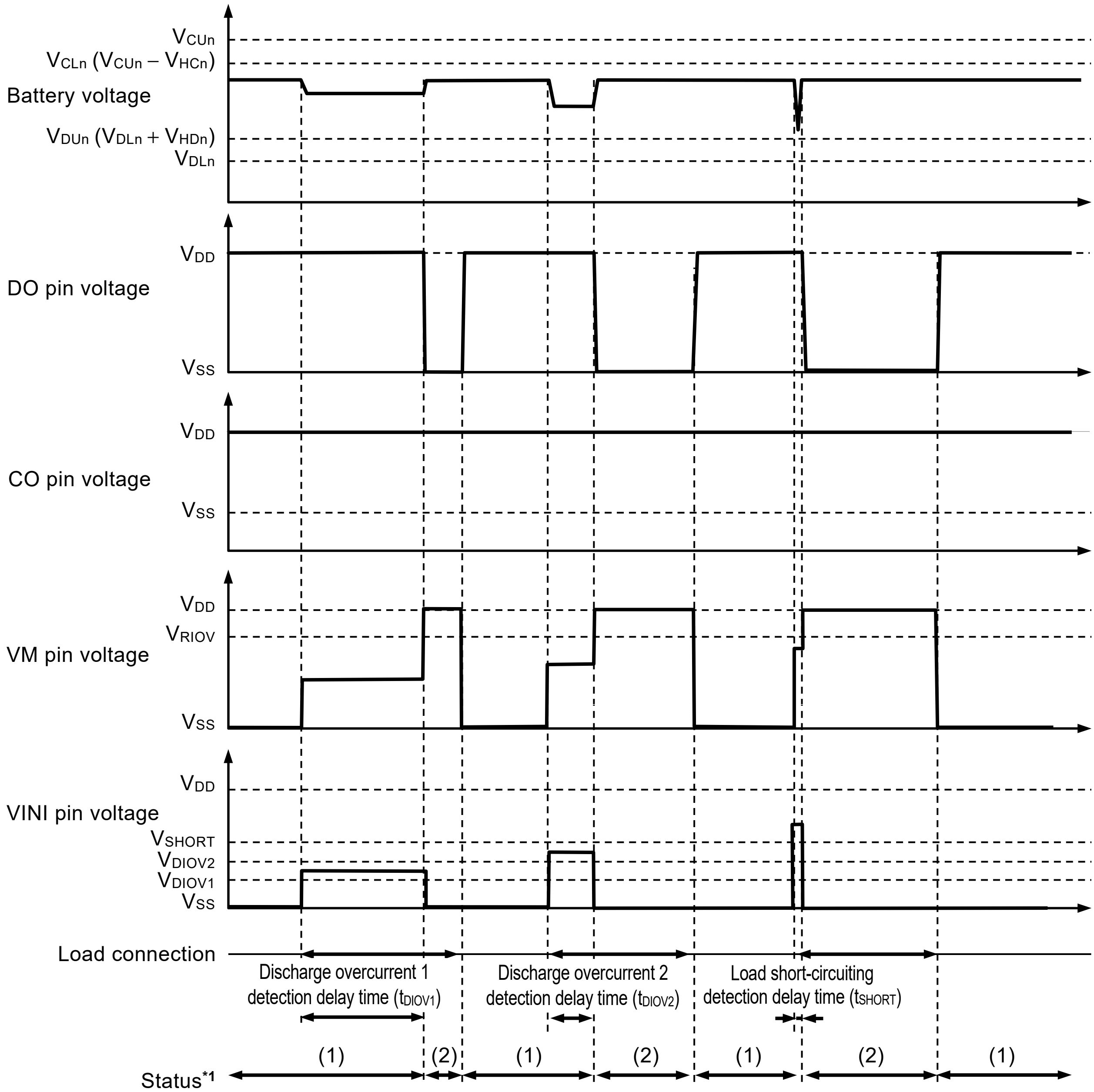


***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status

Remark 1. The charger is assumed to charge with a constant current.
2. n = 1, 2

Figure 11

2. Discharge overcurrent detection

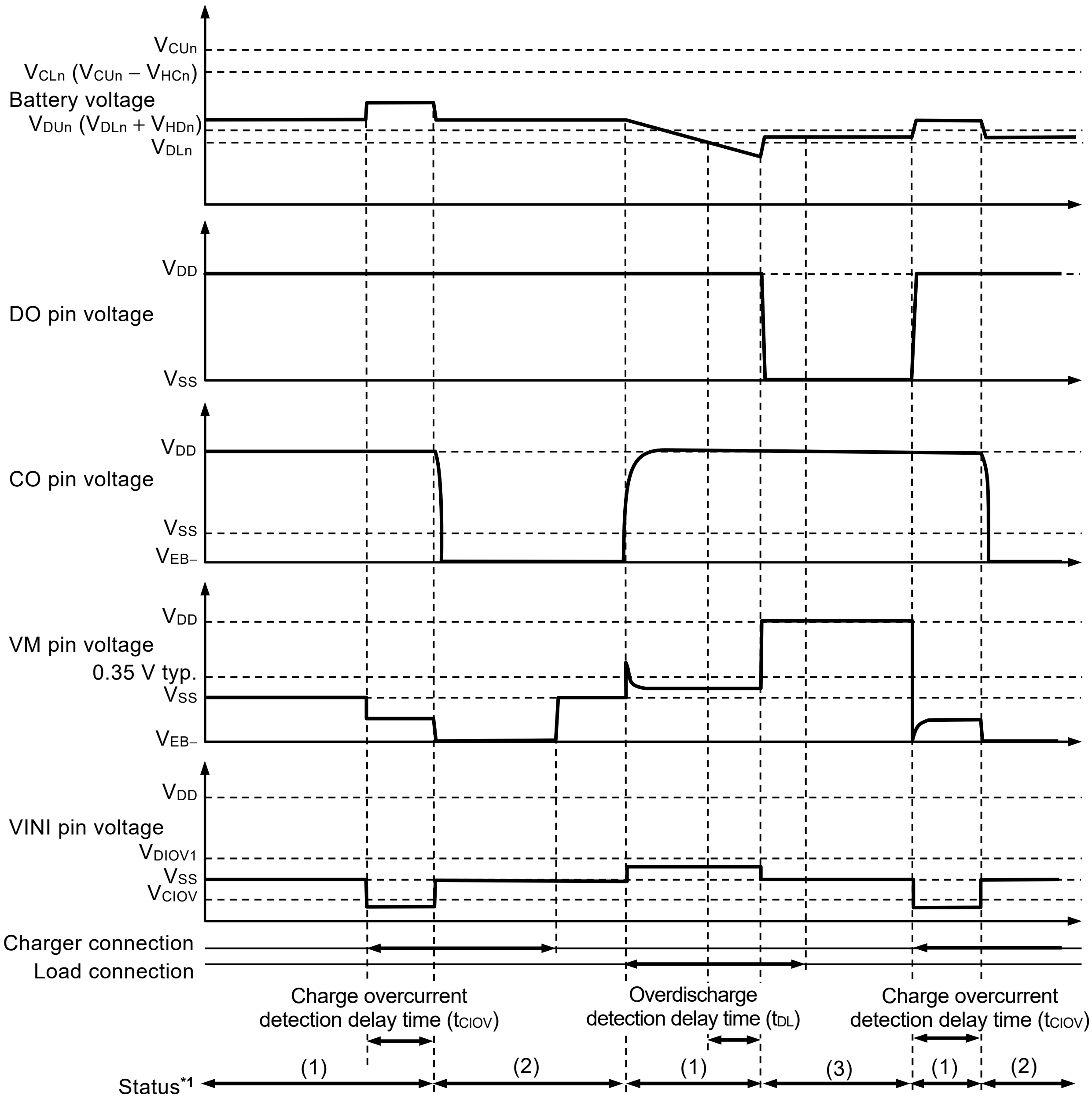


***1.** (1): Normal status
(2): Discharge overcurrent status

Remark n = 1, 2

Figure 12

3. Charge overcurrent detection

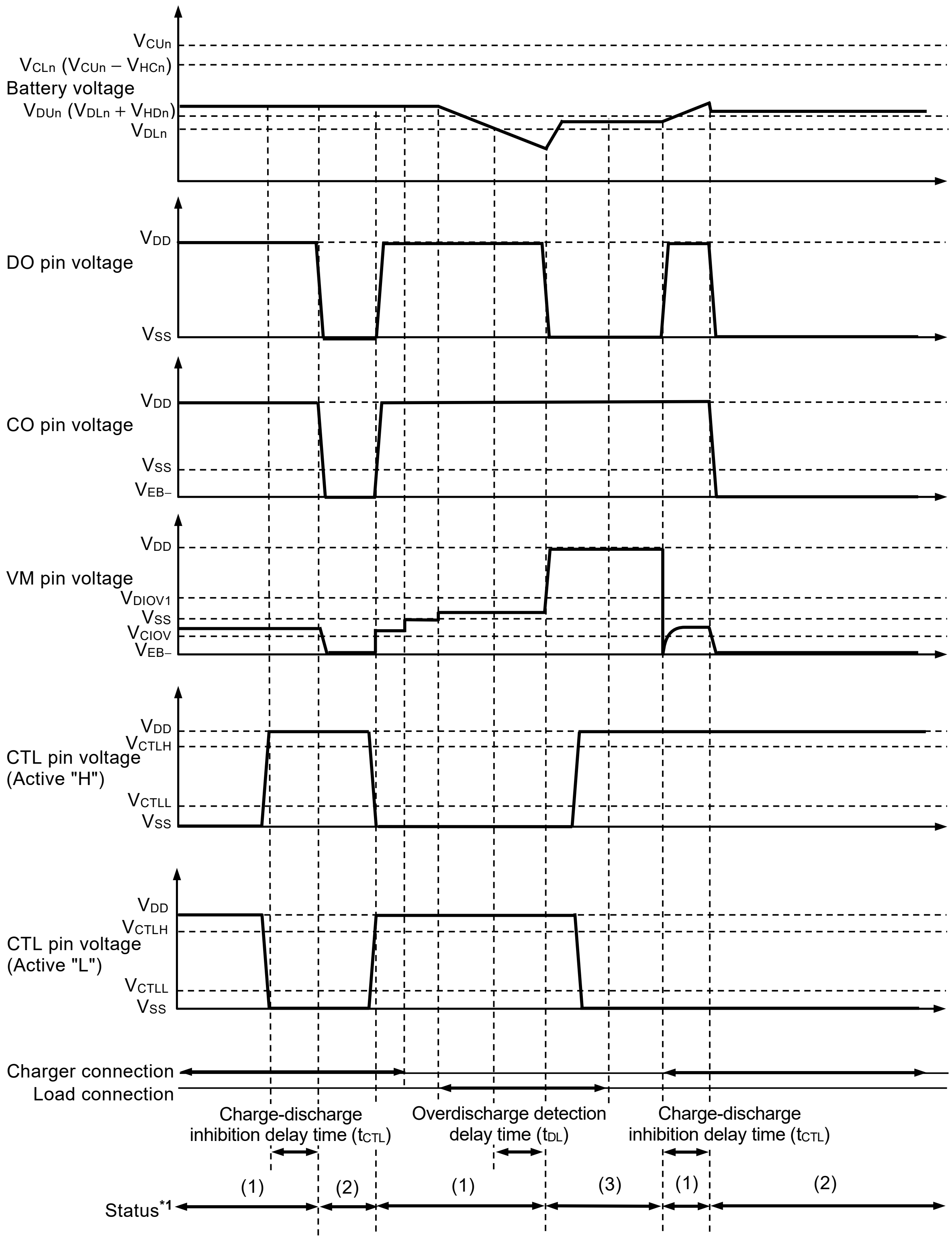


***1.** (1): Normal status
(2): Charge overcurrent status
(3): Overdischarge status

Remark 1. The charger is assumed to charge with a constant current.
2. n = 1, 2

Figure 13

4. Charge-discharge inhibition operation (S-82B2A Series)

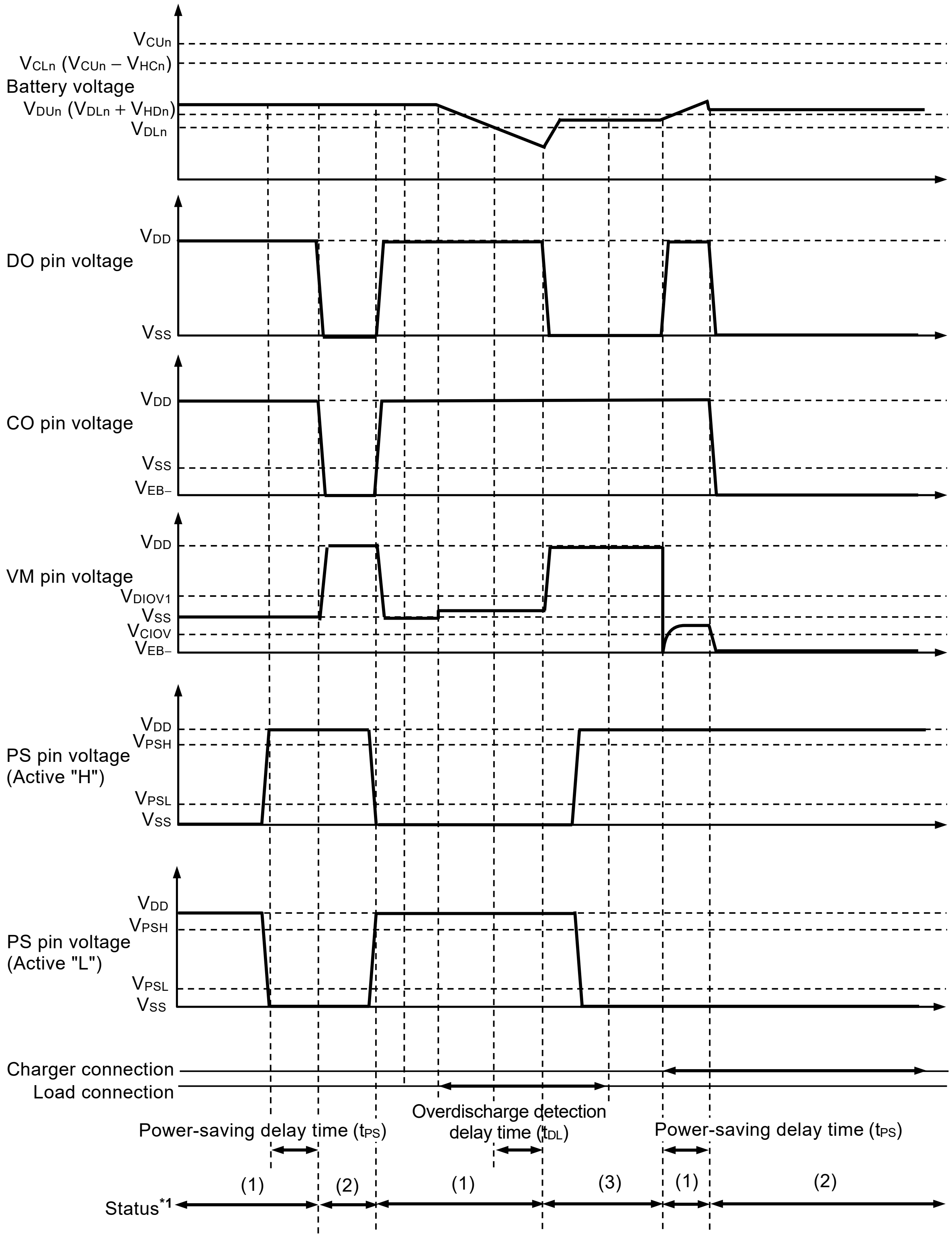


***1.** (1): Normal status
(2): Charge-discharge inhibition status
(3): Overdischarge status

Remark 1. The charger is assumed to charge with a constant current.
2. n = 1, 2

Figure 14

5. Power-saving operation (S-82B2B Series)



***1.** (1): Normal status
(2): Power-saving status
(3): Overdischarge status

Remark 1. The charger is assumed to charge with a constant current.
2. n = 1, 2

Figure 15

■ Battery Protection IC Connection Example

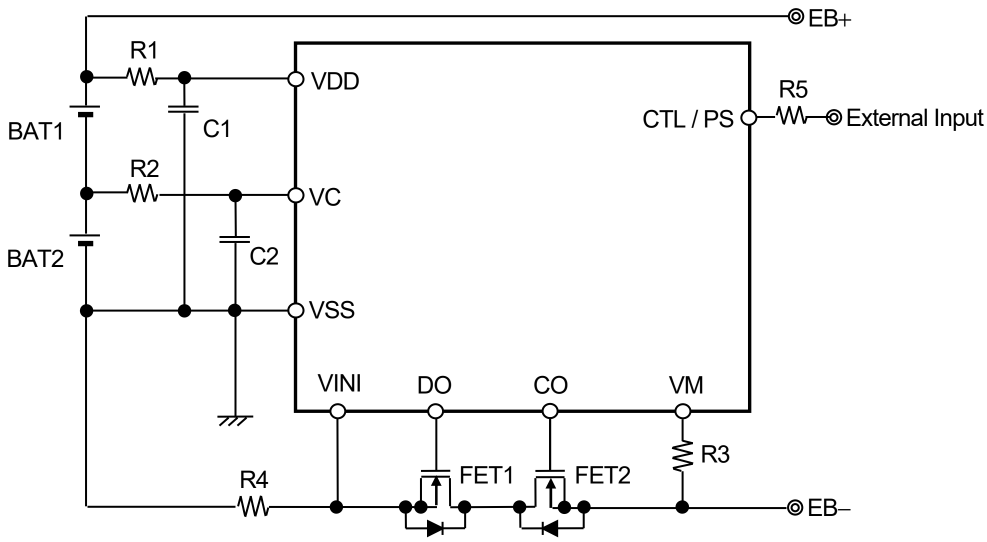


Figure 16

Table 16 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
FET1	N-channel MOS FET	Discharge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*1
FET2	N-channel MOS FET	Charge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*1
R1, R2	Resistor	ESD protection, For power fluctuation	100 Ω	100 Ω	150 Ω*2	–
C1, C2	Capacitor	For power fluctuation	0.068 μF	0.1 μF	1.0 μF	–
R3	Resistor	ESD protection, Protection for reverse connection of a charger	300 Ω	1.0 kΩ	1.5 kΩ	–
R4	Resistor	Overcurrent detection	–	1 mΩ	–	–
R5	Resistor	CTL / PS pin input protection	–	1 kΩ	–	–

***1.** If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

***2.** Accuracy of overcharge detection voltage is guaranteed by R1 = 100 Ω. Connecting resistors with other values will worsen the accuracy.

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

■ Precautions

- The application status s for the input voltage, output voltage, and load current should not exceed the power dissipation.

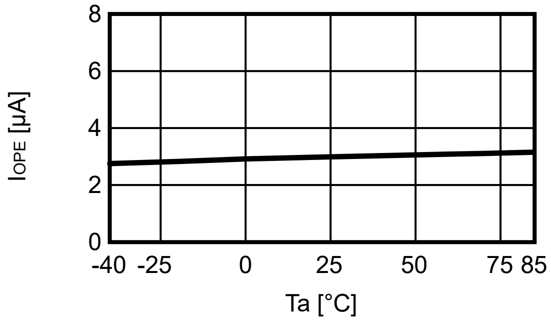
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

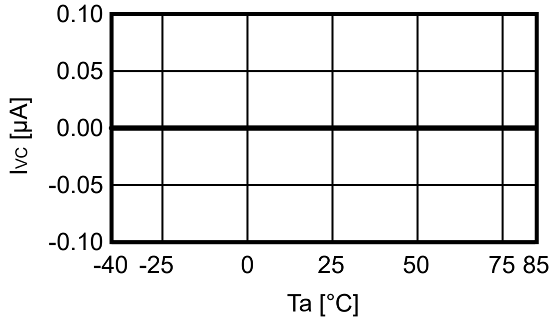
■ Characteristics (Typical Data)

1. Current consumption

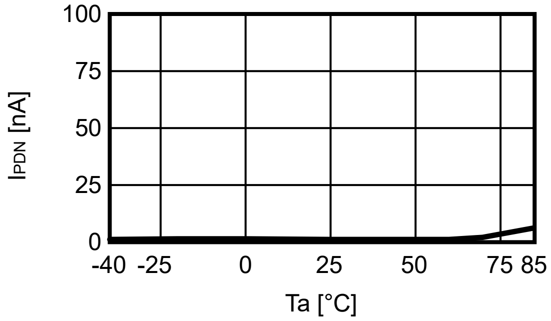
1. 1 I_{OPE} vs. Ta



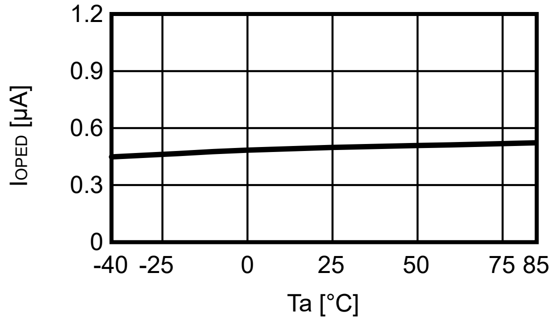
1. 2 I_{VC} vs. Ta



1. 3 I_{PDN} vs. Ta

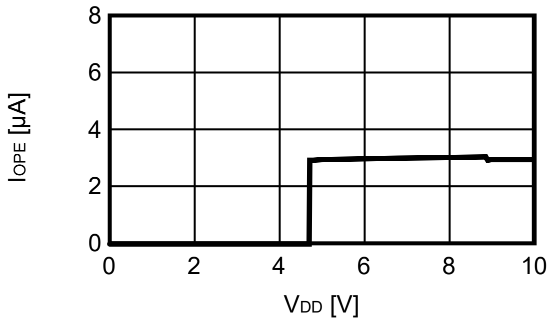


1. 4 I_{OPED} vs. Ta

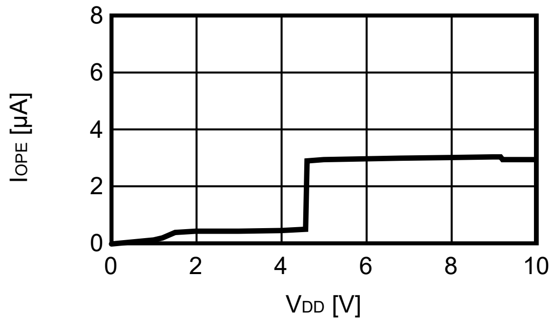


1. 5 I_{OPE} vs. V_{DD}

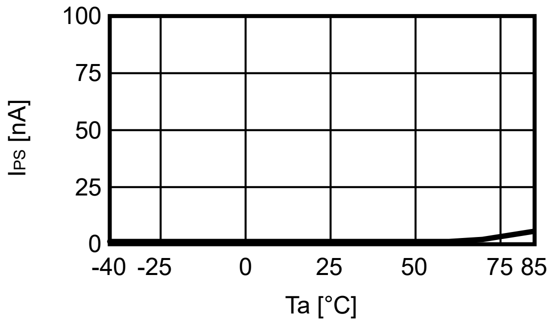
1. 5. 1 With power-down function



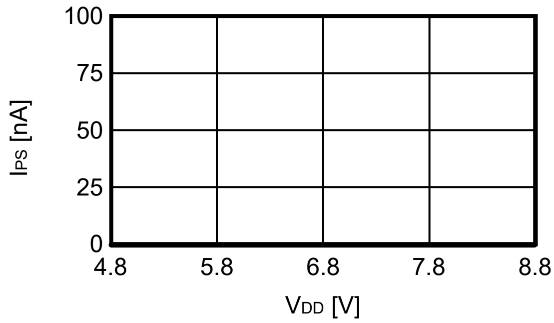
1. 5. 2 Without power-down function



1. 6 I_{PS} vs. Ta (S-82B2B Series)

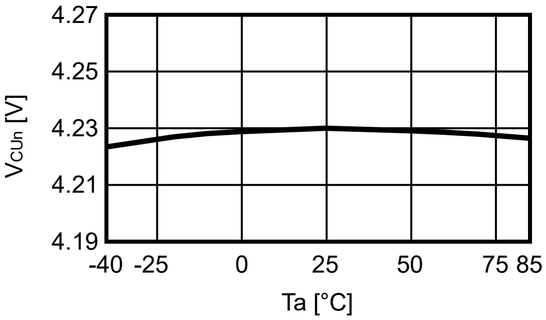


1. 7 I_{PS} vs. V_{DD} (S-82B2B Series)

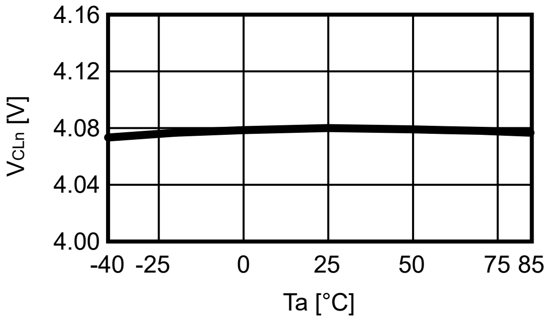


2. Detection voltage, release voltage

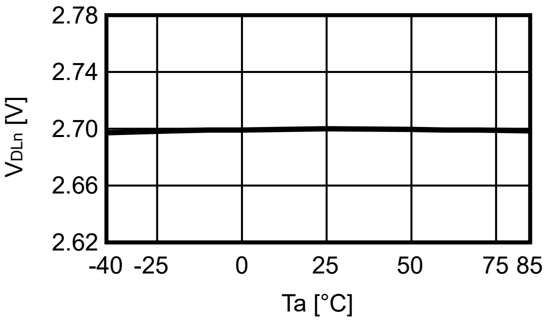
2. 1 V_{CUn} vs. Ta



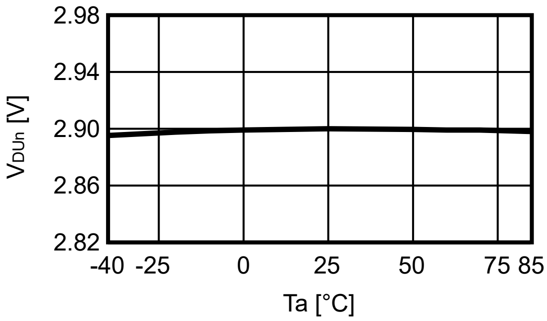
2. 2 V_{CLn} vs. Ta



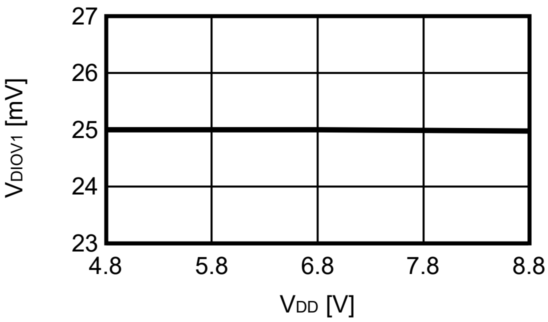
2. 3 V_{DLn} vs. Ta



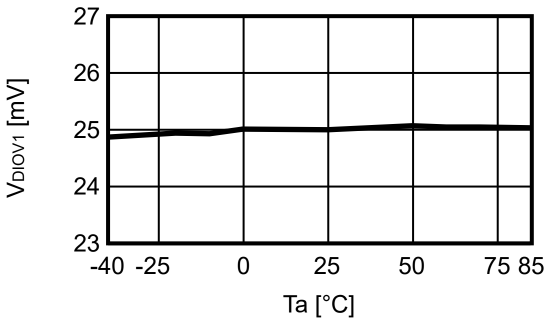
2. 4 V_{DUn} vs. Ta



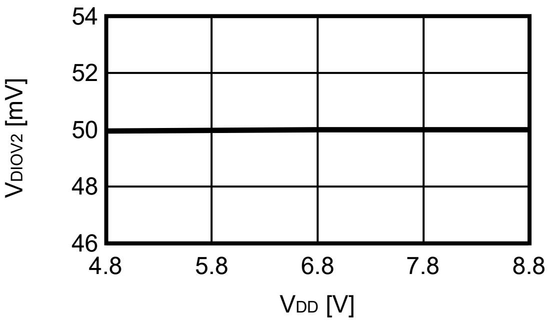
2. 5 V_{DIOV1} vs. V_{DD}



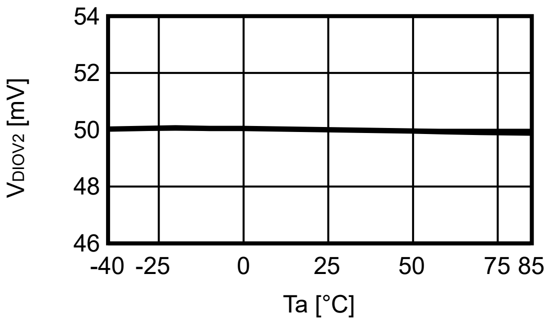
2. 6 V_{DIOV1} vs. Ta



2. 7 V_{DIOV2} vs. V_{DD}

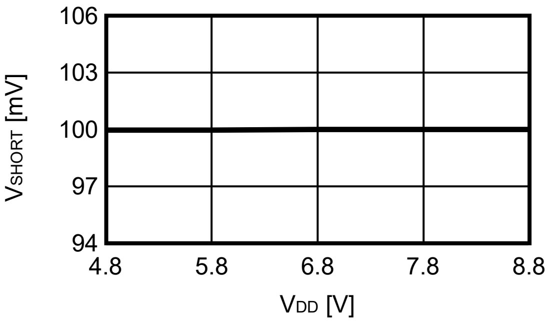


2. 8 V_{DIOV2} vs. Ta

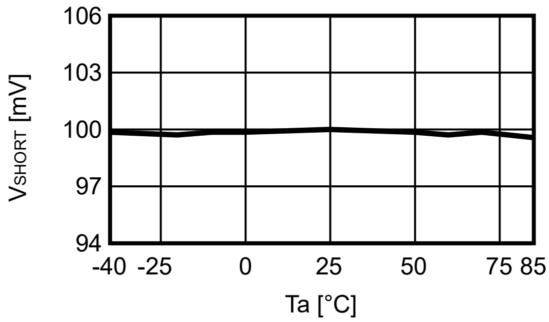


Remark n = 1, 2

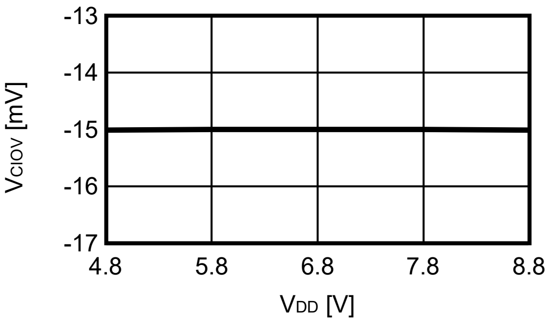
2. 9 V_{SHORT} vs. V_{DD}



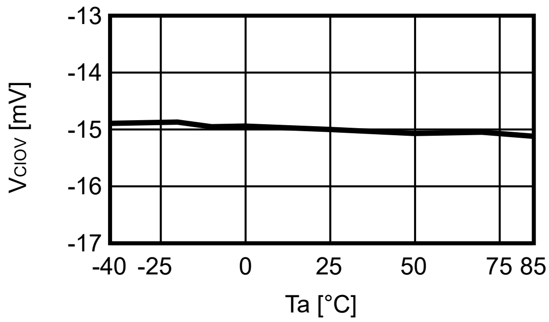
2. 10 V_{SHORT} vs. Ta



2. 11 V_{CIOV} vs. V_{DD}

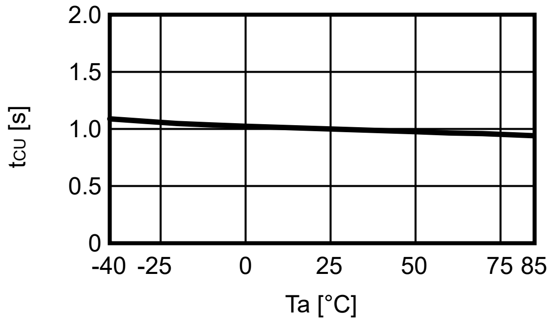


2. 12 V_{CIOV} vs. Ta

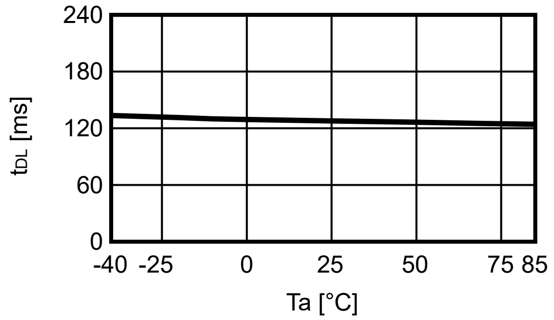


3. Delay time

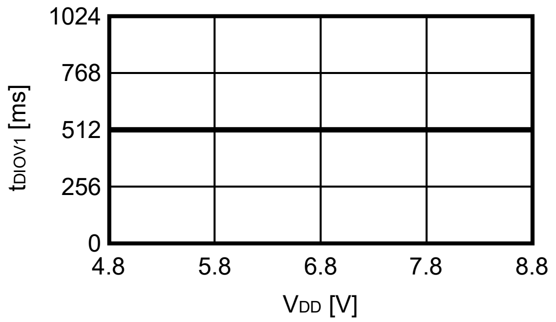
3. 1 t_{CU} vs. Ta



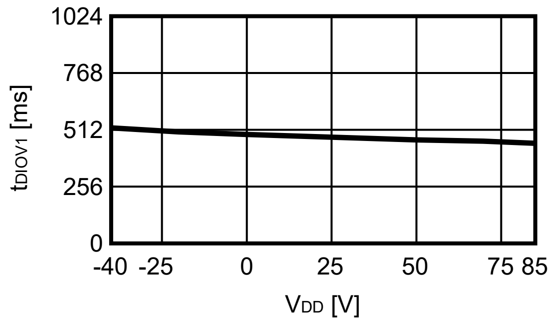
3. 2 t_{DL} vs. Ta



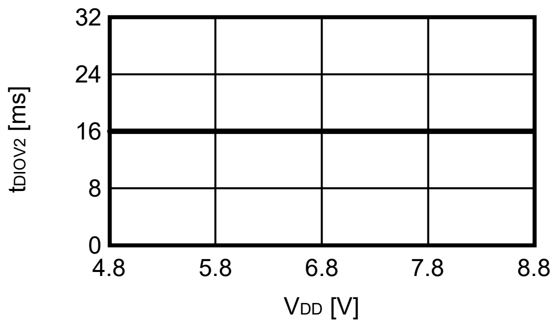
3. 3 t_{DIOV1} vs. V_{DD}



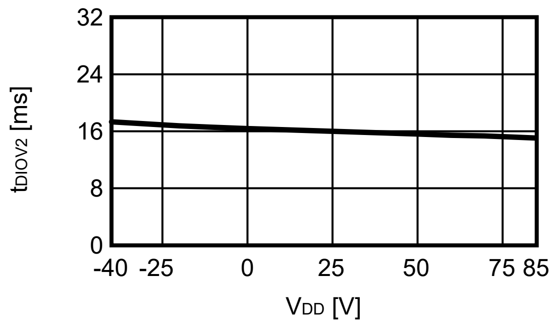
3. 4 t_{DIOV1} vs. Ta



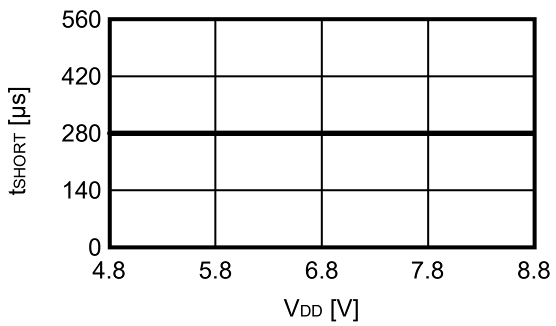
3. 5 t_{DIOV2} vs. V_{DD}



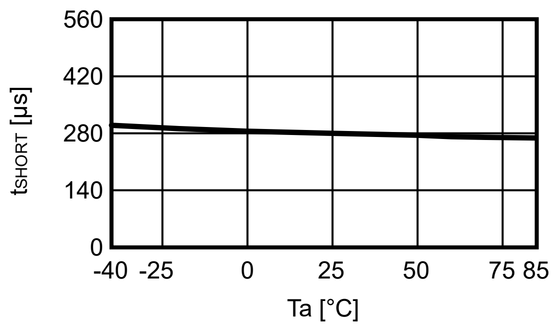
3. 6 t_{DIOV2} vs. Ta



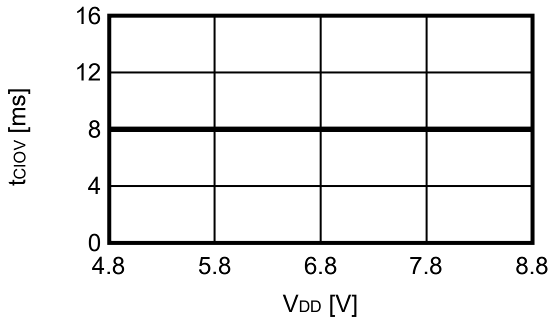
3. 7 t_{SHORT} vs. V_{DD}



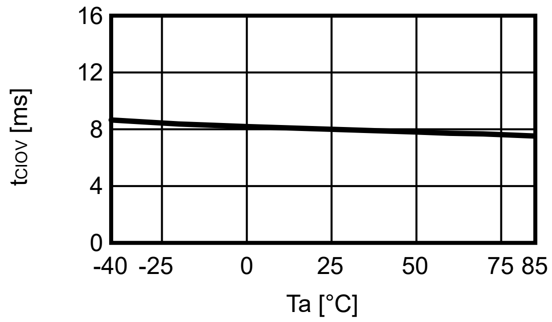
3. 8 t_{SHORT} vs. Ta



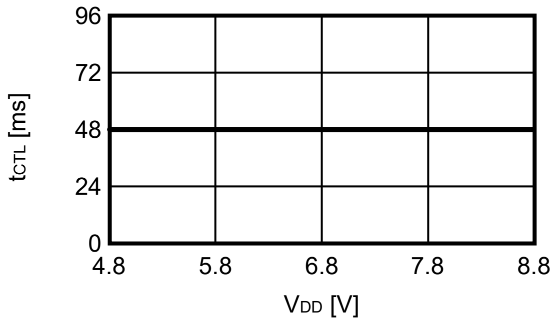
3. 9 t_{CIOV} vs. V_{DD}



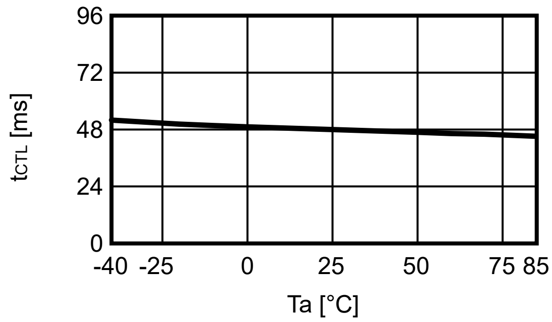
3. 10 t_{CIOV} vs. Ta



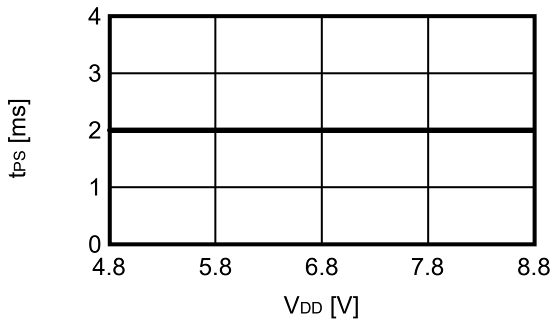
3. 11 t_{CTL} vs. V_{DD} (S-82B2A Series)



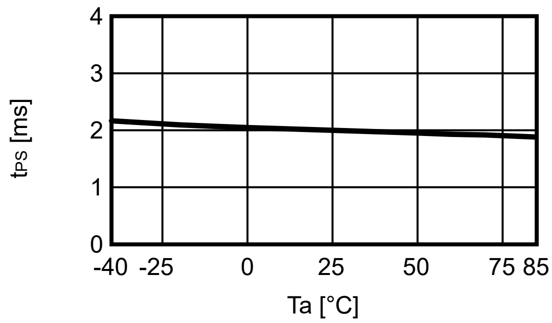
3. 12 t_{CTL} vs. Ta (S-82B2A Series)



3. 13 t_{PS} vs. V_{DD} (S-82B2B Series)

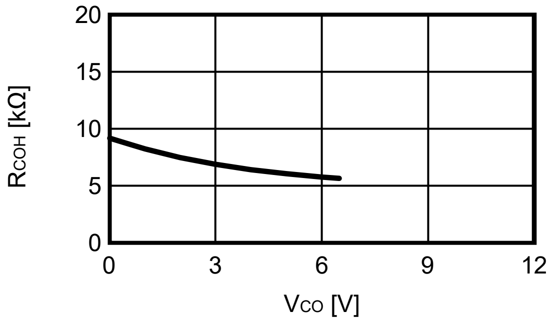


3. 14 t_{PS} vs. Ta (S-82B2B Series)

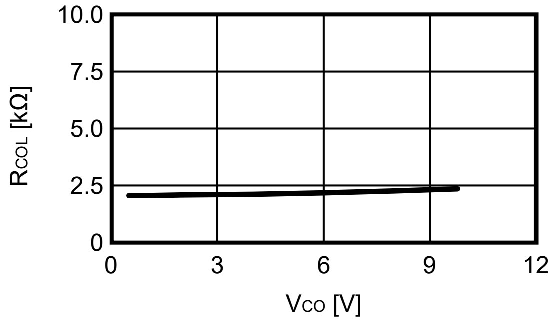


4. Output resistance

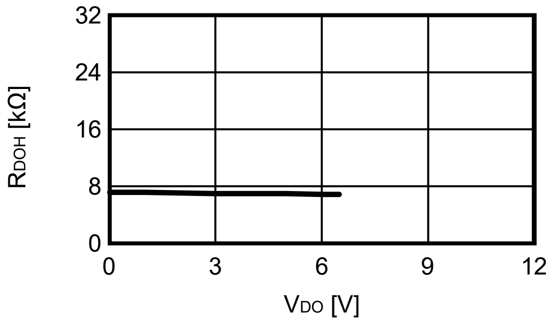
4. 1 R_{COH} vs. V_{CO}



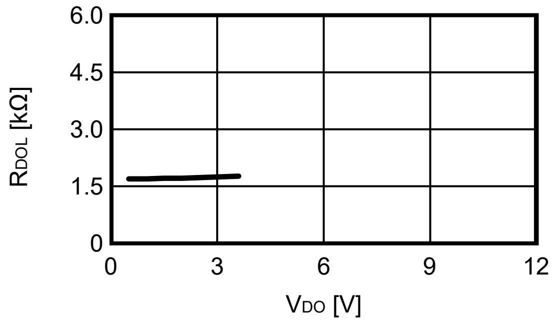
4. 2 R_{COL} vs. V_{CO}



4. 3 R_{DOH} vs. V_{DO}

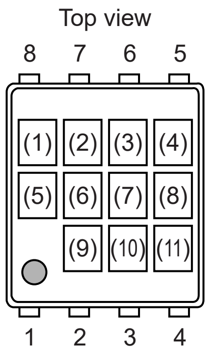


4. 4 R_{DOL} vs. V_{DO}



■ Marking Specifications

1. SNT-8A



(1): Blank
(2) to (4): Product code (Refer to **Product name vs. Product code**)
(5), (6): Blank
(7) to (11): Lot number

Product name vs. Product code

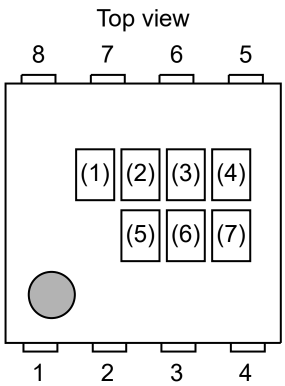
1. 1 S-82B2A Series

Product Name	Product Code		
	(2)	(3)	(4)
S-82B2AAA-I8T1U7	9	D	E

1. 2 S-82B2B Series

Product Name	Product Code		
	(2)	(3)	(4)
S-82B2BAA-I8T1U7	9	D	I

2. HSNT-8(1616)



(1): Blank
(2) to (4): Product code (Refer to **Product name vs. Product code**)
(5) to (7): Lot number

Product name vs. Product code

2. 1 S-82B2A Series

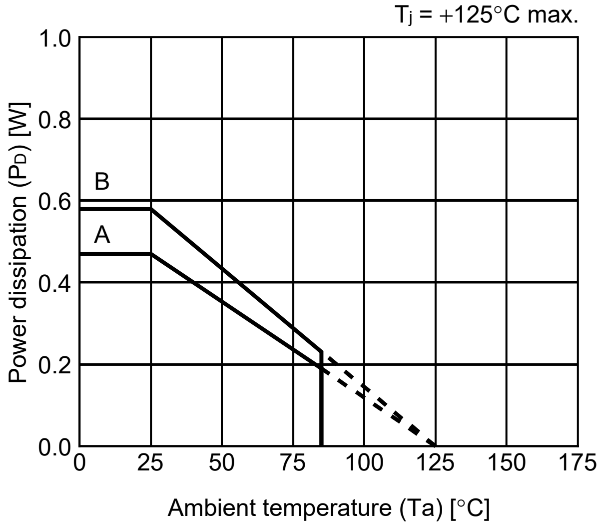
Product Name	Product Code		
	(2)	(3)	(4)
S-82B2AAA-A8T2U7	9	D	E

2. 2 S-82B2B Series

Product Name	Product Code		
	(2)	(3)	(4)
S-82B2BAA-A8T2U7	9	D	I

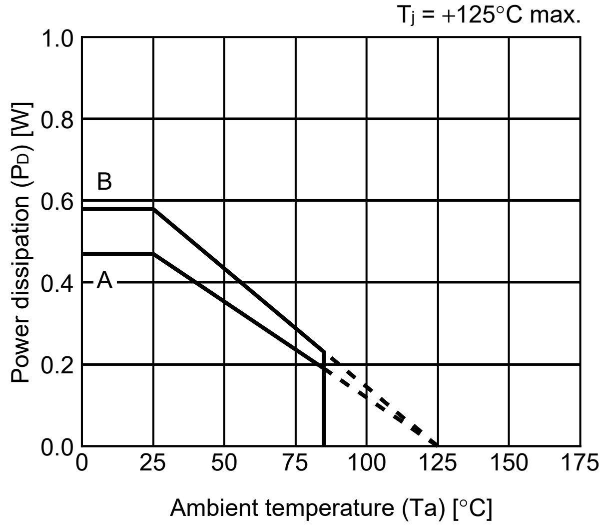
■ Power Dissipation

SNT-8A



Board	Power Dissipation (P_D)
A	0.47 W
B	0.58 W
C	–
D	–
E	–

HSNT-8(1616)

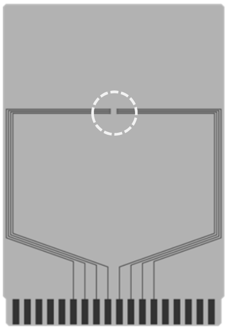


Board	Power Dissipation (P_D)
A	0.47 W
B	0.58 W
C	–
D	–
E	–

SNT-8A Test Board

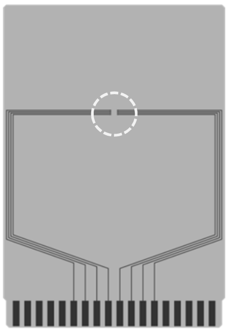
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



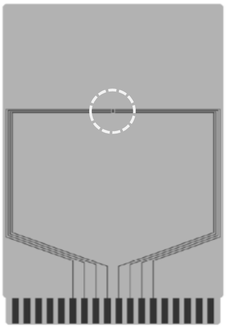
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SNT8A-A-Board-SD-1.0

HSNT-8(1616) Test Board

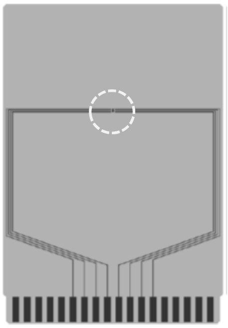
IC Mount Area

(1) Board A



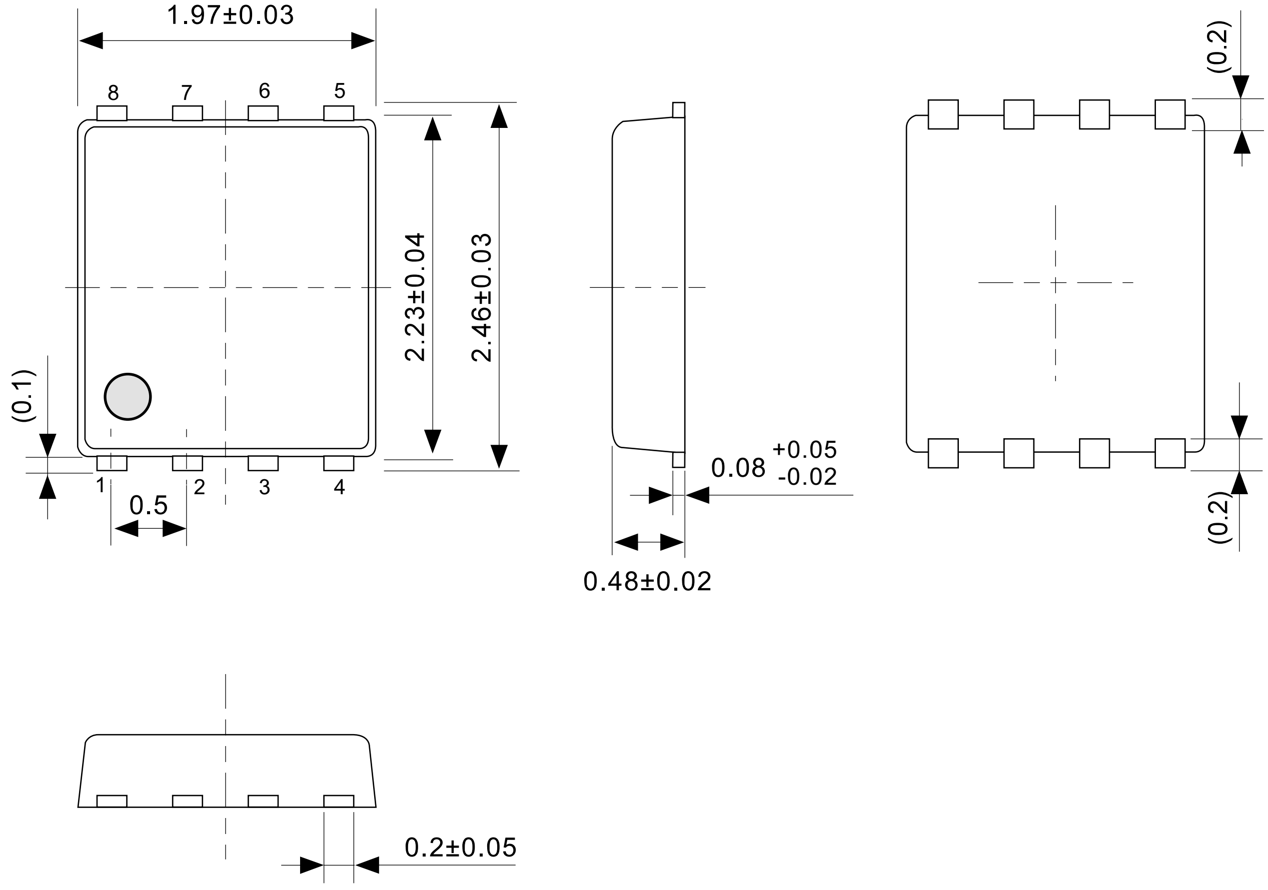
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

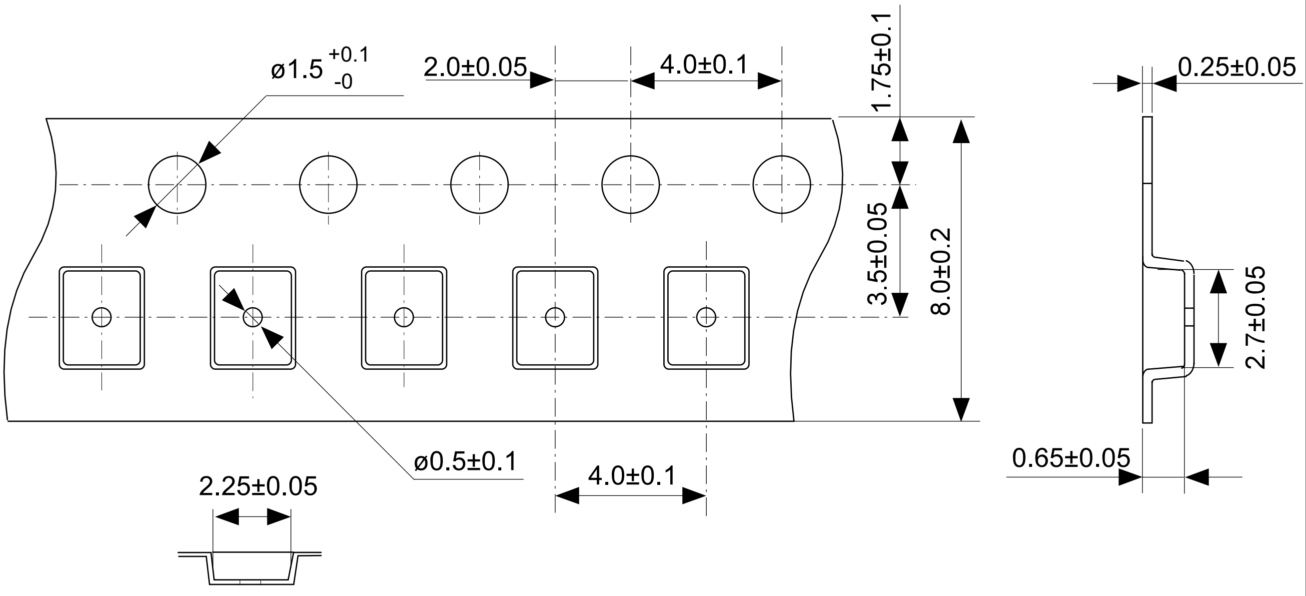
No. HSNT8-B-Board-SD-1.0

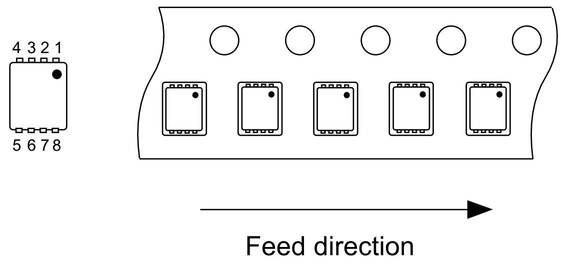


No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm

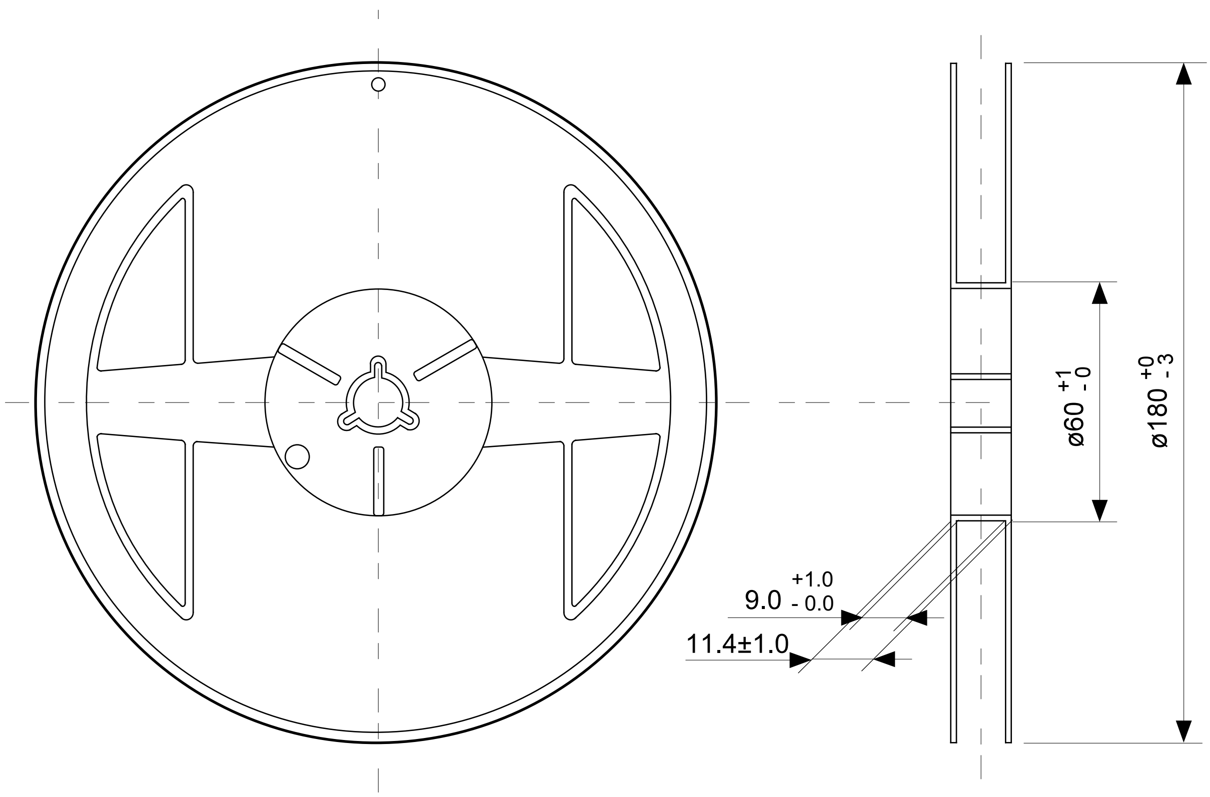
ABLIC Inc.



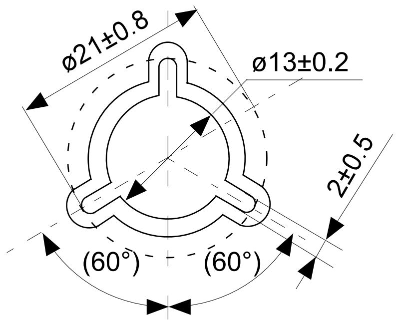


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

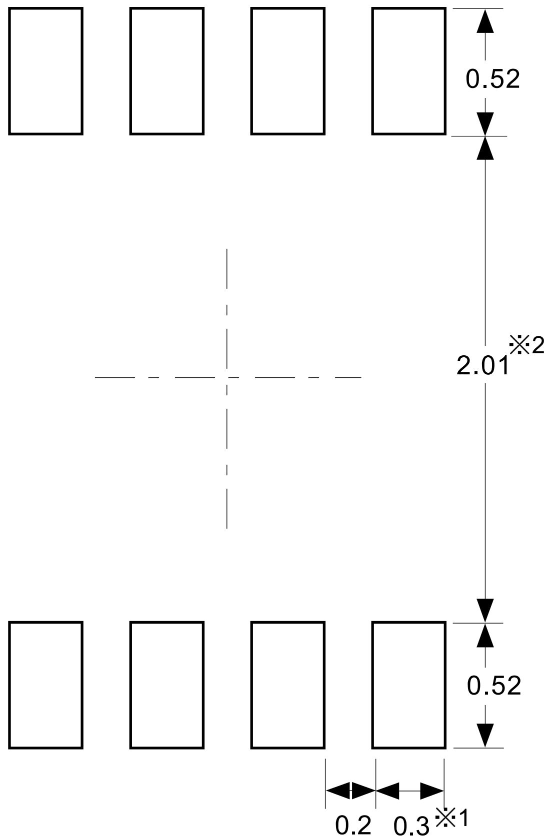


Enlarged drawing in the central part



No. PH008-A-R-SD-2.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

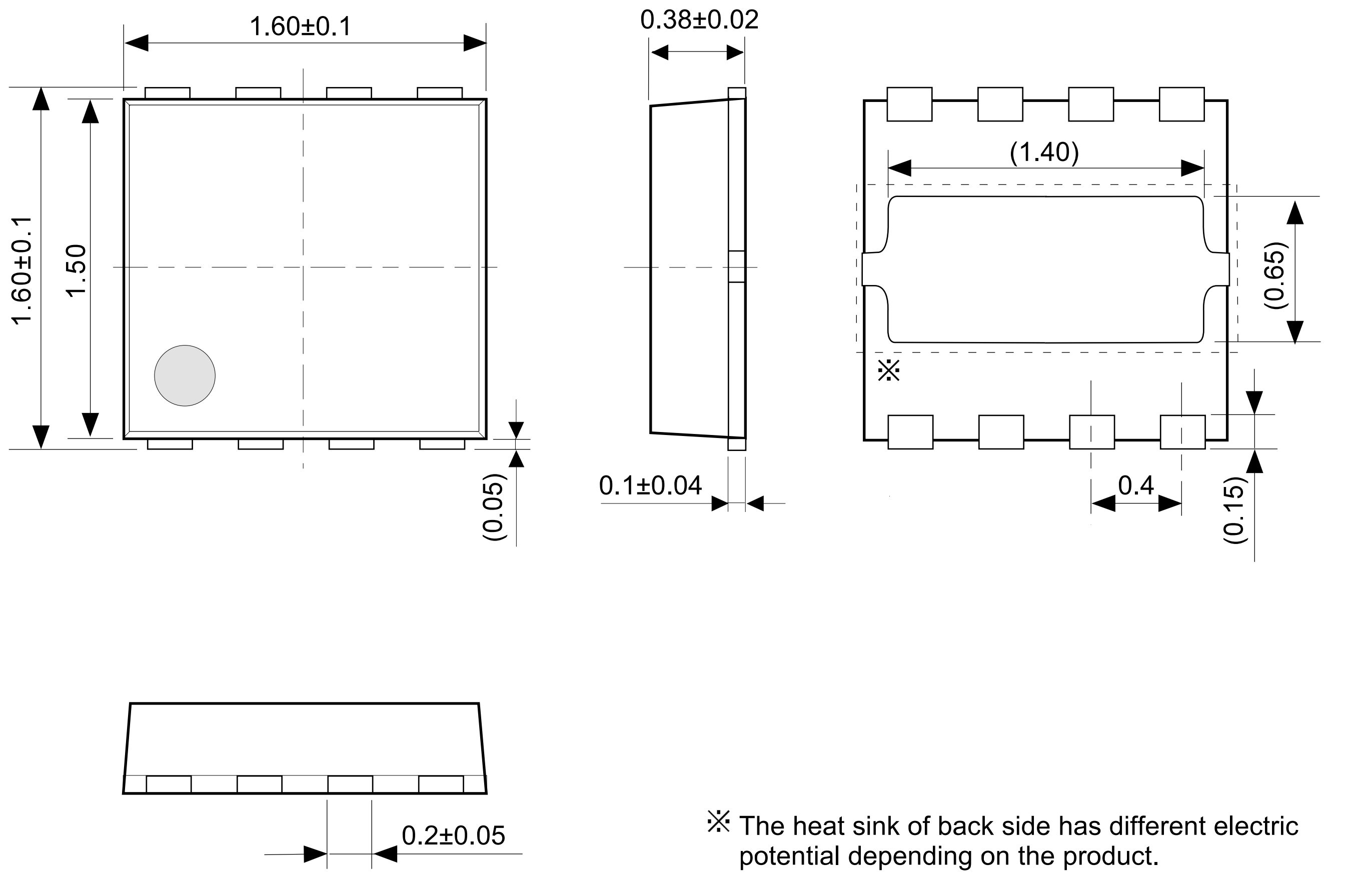
Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

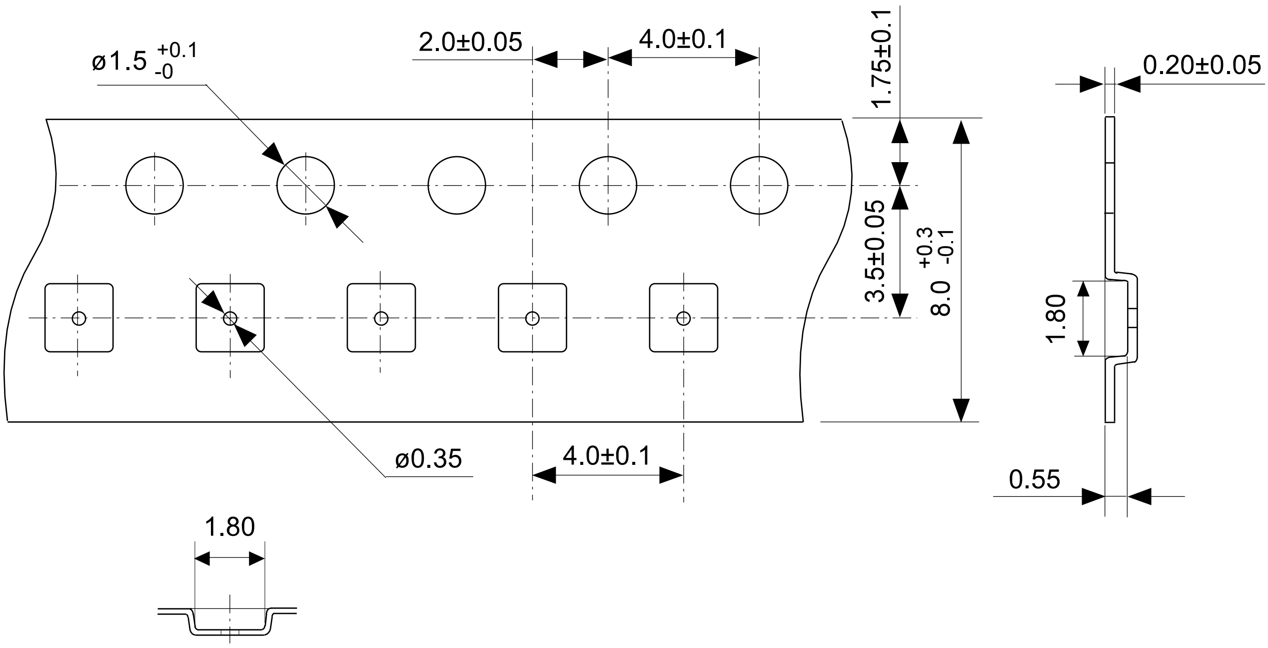


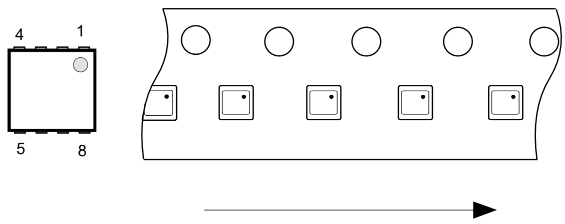
※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PY008-A-P-SD-1.0

TITLE	HSNT-8-B-PKG Dimensions
No.	PY008-A-P-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.

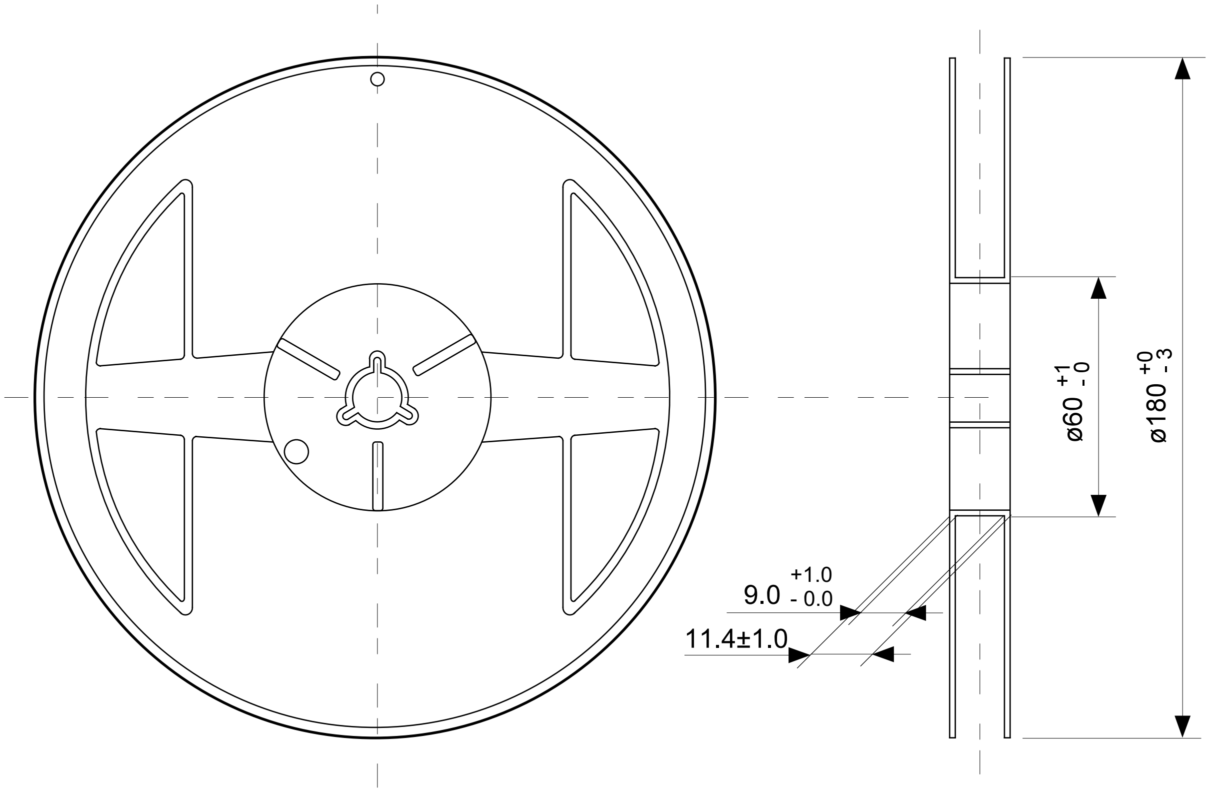




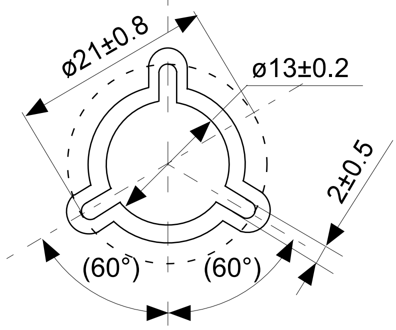
No. PY008-A-C-SD-1.0

TITLE	HSNT-8-B-Carrier Tape
No.	PY008-A-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



Enlarged drawing in the central part

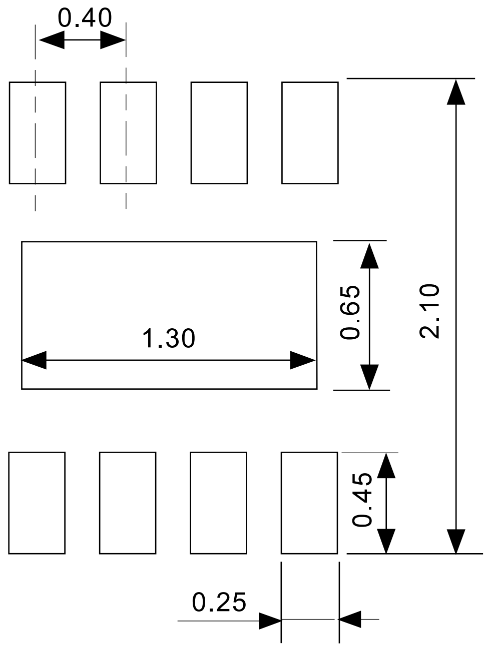


No. PY008-A-R-SD-1.0

TITLE	HSNT-8-B-Reel		
No.	PY008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		

ABLIC Inc.

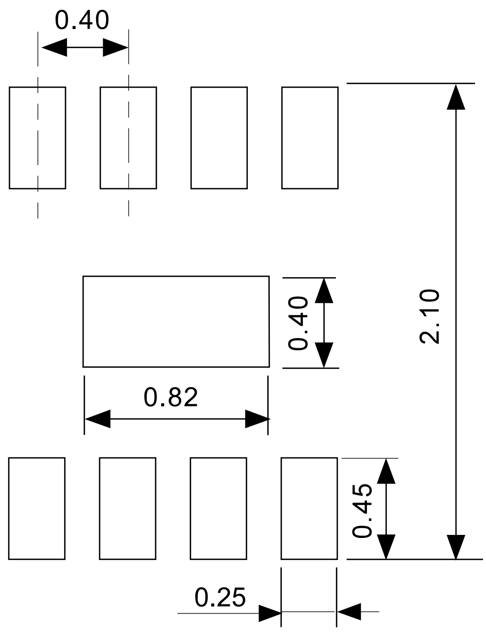
Land Pattern



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意　放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Metal Mask Pattern



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is 40%.
③ Mask thickness: t0.12 mm

注意 ①リード実装部のマスク開口率は100%です。
②放熱板実装のマスク開口率は40%です。
③マスク厚み：t0.12 mm

No. PY008-A-L-SD-1.0

TITLE	HSNT-8-B -Land Recommendation
No.	PY008-A-L-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.

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   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
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