BATTERY PROTECTION IC WITH POWER-SAVING FUNCTION FOR 1-CELL PACK

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The S-82B1B Series is a protection IC for lithium-ion / lithium polymer rechargeable batteries and includes high-accuracy voltage detection circuits and delay circuits. It is suitable for protecting 1-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, and overcurrent.
The S-82B1B Series has an input pin for power-saving signal (PS pin), allowing for reduction of current consumption by using an external signal to start the power-saving function.

■ Features

- High-accuracy voltage detection circuit

Overcharge detection voltage	3.500 V to 4.600 V (5 mV step)	Accuracy ±20 mV
Overcharge release voltage	3.100 V to 4.600 V*1	Accuracy ±50 mV
Overdischarge detection voltage	2.000 V to 3.000 V (10 mV step)	Accuracy ±50 mV
Overdischarge release voltage	2.000 V to 3.400 V*2	Accuracy ±100 mV
Discharge overcurrent detection voltage 1	0.010 V to 0.100 V (1 mV step)	Accuracy ±3 mV
Discharge overcurrent detection voltage 2	0.030 V to 0.200 V (1 mV step)	Accuracy ±5 mV
Load short-circuiting detection voltage	0.050 V to 0.500 V (5 mV step)	Accuracy ±20 mV
Charge overcurrent detection voltage	−0.100 V to −0.010 V (1 mV step)	Accuracy ±3 mV

- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary).
- Power-saving function
  - PS pin control logic is selectable: Active "H", active "L"
  - PS pin internal resistance connection is selectable: Pull-up, pull-down
  - PS pin internal resistance value is selectable: 1.0 MΩ, 2.0 MΩ, 3.0 MΩ, 4.0 MΩ, 5.0 MΩ
- 0 V battery charge function is selectable: Available, unavailable
- Power-down function
- Release condition of discharge overcurrent status is selectable: Load disconnection, charger connection
- Release voltage of discharge overcurrent status is selectable:
  Discharge overcurrent detection voltage 1 (V_{DIOV1}),
  Discharge overcurrent release voltage (V_{RIOV}) = $V_{DD} \times 0.8$ (typ.)
- High-withstand voltage: VM pin and CO pin: Absolute maximum rating 28 V
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  - During operation: 2.0 μA typ., 4.0 μA max. (Ta = +25°C)
  - During power-down: 50 nA max. (Ta = +25°C)
  - During power-saving: 50 nA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)
***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)

■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Package

- SNT-6A

■ Block Diagram

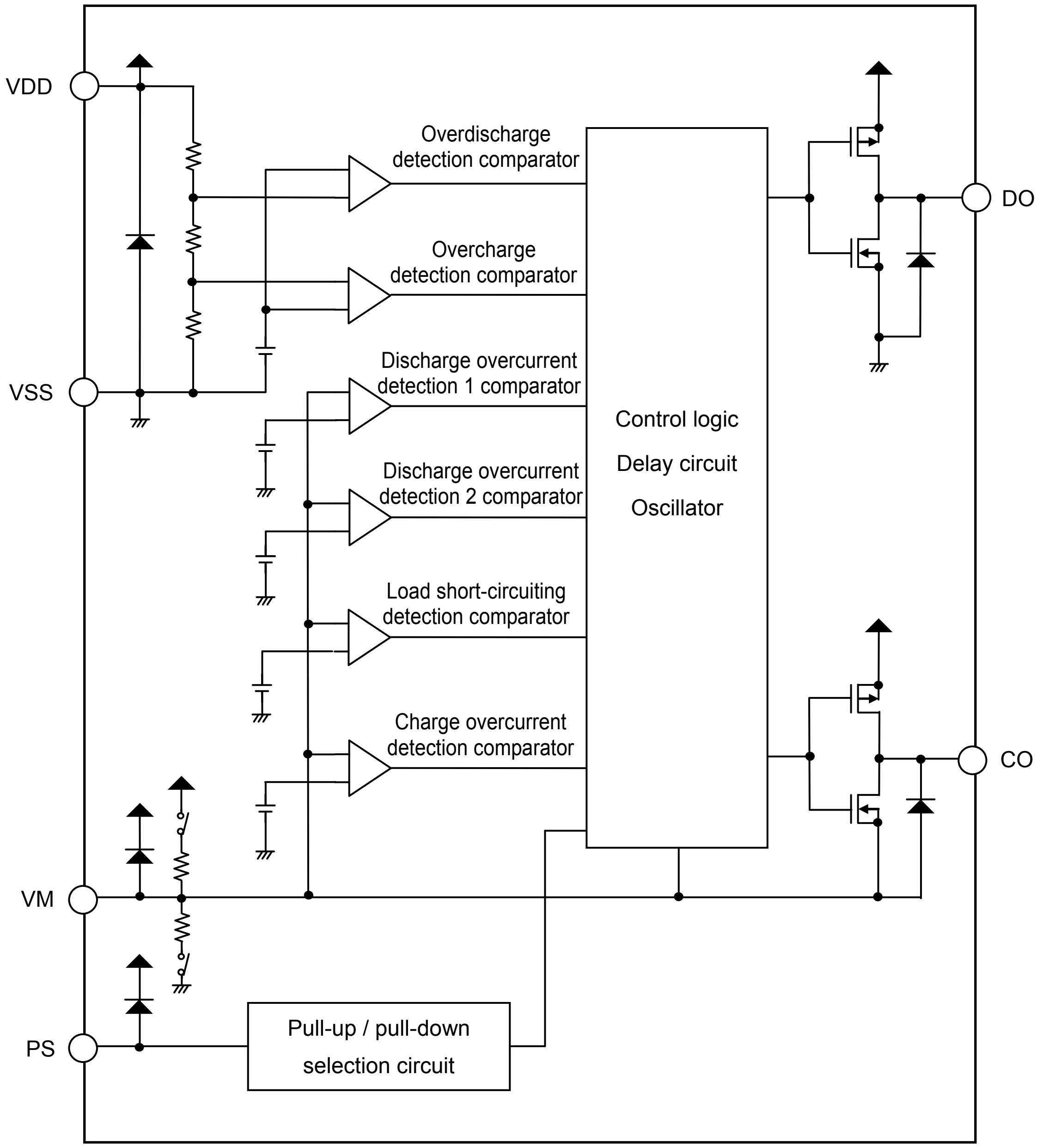


Figure 1

■ Product Name Structure

1. Product name

S-82B1B xx - I6T1 U

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications*1
I6T1: SNT-6A, Tape

Serial code*2
Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. Product name list

3. 1 SNT-6A

Table 2 (1 / 2)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Delay Time Combination*1	Function Combination*2
S-82B1BAA-I6T1U	4.275 V	4.075 V	3.100 V	3.200 V	(1)	(1)

Table 2 (2 / 2)

Product Name	Discharge Overcurrent Detection Voltage 1 [V_{DIOV1}]	Discharge Overcurrent Detection Voltage 2 [V_{DIOV2}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]
S-82B1BAA-I6T1U	0.030 V	0.045 V	0.205 V	−0.030 V

***1.** Refer to **Table 3** about the details of the delay time combinations.
***2.** Refer to **Table 5** about the details of the function combinations.

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

Table 3

Delay Time Combination	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]	Discharge Overcurrent Detection Delay Time 1 [t_{DIOV1}]	Discharge Overcurrent Detection Delay Time 2 [t_{DIOV2}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]	Power-saving Delay Time [t_{PS}]
(1)	256 ms	32 ms	256 ms	16 ms	280 μs	8 ms	256 ms

Remark The delay times can be changed within the range listed in **Table 4**. For details, please contact our sales office.

Table 4

Delay Time	Symbol	Selection Range						Remark
Overcharge detection delay time	t_{CU}	256 ms	512 ms	1.0 s	–	–	–	Select a value from the left.
Overdischarge detection delay time	t_{DL}	32 ms	64 ms	128 ms	256 ms	–	–	Select a value from the left.
Discharge overcurrent detection delay time 1	t_{DIOV1}	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.
		256 ms	512 ms	1.0 s	2.0 s	4.0 s	–	
Discharge overcurrent detection delay time 2	t_{DIOV2}	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.
Load short-circuiting detection delay time	t_{SHORT}	280 μs	530 μs	–	–	–	–	Select a value from the left.
Charge overcurrent detection delay time	t_{CIOV}	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.
Power-saving delay time	t_{PS}	32 ms	64 ms	128 ms	256 ms	–	–	Select a value from the left.

Table 5

Function Combination	PS pin			0 V Battery Charge Function*4	Release Condition of Discharge Overcurrent Status*5	Release Voltage of Discharge Overcurrent Status*6
	Control Logic*1	Internal Resistance Connection*2	Internal Resistance Value*3 [R_{PS}]			
(1)	Active "H"	Pull-down	5.0 MΩ	Unavailable	Charger connection	V_{DIOV1}

***1.** PS pin control logic active "H" / active "L" is selectable.
***2.** PS pin internal resistance connection "pull-up" / "pull-down" is selectable.
***3.** PS pin internal resistance value 1.0 MΩ / 2.0 MΩ / 3.0 MΩ / 4.0 MΩ / 5.0 MΩ is selectable.
***4.** 0 V battery charge function "available" / "unavailable" is selectable.
***5.** Release condition of discharge overcurrent status "load disconnection" / "charger connection" is selectable.
***6.** Release voltage of discharge overcurrent status "V_{DIOV1}" / "$V_{RIOV} = V_{DD} \times 0.8$ (typ.)" is selectable.

Remark Please contact our sales office for the products with function combinations other than those specified above.

■ Pin Configuration

1. SNT-6A

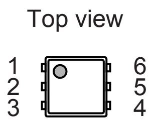


Figure 2

Table 6

Pin No.	Symbol	Description
1	VM	Overcurrent detection pin
2	CO	Connection pin of charge control FET gate (CMOS output)
3	DO	Connection pin of discharge control FET gate (CMOS output)
4	VSS	Input pin for negative power supply
5	VDD	Input pin for positive power supply
6	PS	Input pin for power-saving signal

■ Absolute Maximum Ratings

Table 7

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 6	V
PS pin input voltage	V_{PS}	PS	V_{DD} − 6 to V_{DD} + 0.3	V
VM pin input voltage	V_{VM}	VM	V_{DD} − 28 to V_{DD} + 0.3	V
DO pin output voltage	V_{DO}	DO	V_{SS} − 0.3 to V_{DD} + 0.3	V
CO pin output voltage	V_{CO}	CO	V_{VM} − 0.3 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	−	−40 to +85	°C
Storage temperature	T_{stg}	−	−55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 8

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SNT-6A	Board A	−	224	−	°C/W
			Board B	−	176	−	°C/W
			Board C	−	−	−	°C/W
			Board D	−	−	−	°C/W
			Board E	−	−	−	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Ta = +25°C

Table 9

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	V_{CU} − 0.020	V_{CU}	V_{CU} + 0.020	V	1
		Ta = −10°C to +60°C*1	V_{CU} − 0.025	V_{CU}	V_{CU} + 0.025	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	V_{CL} − 0.050	V_{CL}	V_{CL} + 0.050	V	1
		$V_{CL} = V_{CU}$	V_{CL} − 0.025	V_{CL}	V_{CL} + 0.020	V	1
Overdischarge detection voltage	V_{DL}	–	V_{DL} − 0.050	V_{DL}	V_{DL} + 0.050	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	V_{DU} − 0.100	V_{DU}	V_{DU} + 0.100	V	2
		$V_{DL} = V_{DU}$	V_{DU} − 0.050	V_{DU}	V_{DU} + 0.050	V	2
Discharge overcurrent detection voltage 1	V_{DIOV1}	–	V_{DIOV1} − 0.003	V_{DIOV1}	V_{DIOV1} + 0.003	V	2
Discharge overcurrent detection voltage 2	V_{DIOV2}	–	V_{DIOV2} − 0.005	V_{DIOV2}	V_{DIOV2} + 0.005	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} − 0.020	V_{SHORT}	V_{SHORT} + 0.020	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} − 0.003	V_{CIOV}	V_{CIOV} + 0.003	V	2
Discharge overcurrent release voltage	V_{RIOV}	V_{DD} = 3.4 V	V_{DD} × 0.77	V_{DD} × 0.8	V_{DD} × 0.83	V	2
0 V Battery Charge Function							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge function "available"	0.0	0.7	1.0	V	2
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge function "unavailable"	0.9	1.2	1.5	V	2
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V	500	1000	2000	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	V_{DD} = 3.4 V, V_{VM} = 1.0 V	5	10	15	kΩ	3
PS pin internal resistance	R_{PS}	–	R_{PS} × 0.5	R_{PS}	R_{PS} × 2.0	MΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.0	V	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–	1.5	–	28	V	–
PS pin voltage "H"	V_{PSH}	–	–	–	V_{DD} × 0.9	V	2
PS pin voltage "L"	V_{PSL}	–	V_{DD} × 0.1	–	–	V	2
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	2.0	4.0	μA	3
Current consumption during power-down	I_{PDN}	V_{DD} = V_{VM} = 1.5 V	–	–	0.05	μA	3
Current consumption during power-saving	I_{PS}	V_{DD} = V_{VM} = 3.4 V	–	–	0.05	μA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	5	10	20	kΩ	4
CO pin resistance "L"	R_{COL}	–	5	10	20	kΩ	4
DO pin resistance "H"	R_{DOH}	–	5	10	20	kΩ	4
DO pin resistance "L"	R_{DOL}	–	5	10	20	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	t_{CU} × 0.7	t_{CU}	t_{CU} × 1.3	–	5
Overdischarge detection delay time	t_{DL}	–	t_{DL} × 0.7	t_{DL}	t_{DL} × 1.3	–	5
Discharge overcurrent detection delay time 1	t_{DIOV1}	–	t_{DIOV1} × 0.7	t_{DIOV1}	t_{DIOV1} × 1.3	–	5
Discharge overcurrent detection delay time 2	t_{DIOV2}	–	t_{DIOV2} × 0.7	t_{DIOV2}	t_{DIOV2} × 1.3	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	t_{SHORT} × 0.7	t_{SHORT}	t_{SHORT} × 1.3	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	t_{CIOV} × 0.7	t_{CIOV}	t_{CIOV} × 1.3	–	5
Power-saving delay time	t_{PS}	–	t_{PS} × 0.7	t_{PS}	t_{PS} × 1.3	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

2. Ta = −40°C to +85°C*1

Table 10

(Ta = −40°C to +85°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	−	V_{CU} − 0.045	V_{CU}	V_{CU} + 0.030	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	V_{CL} − 0.080	V_{CL}	V_{CL} + 0.060	V	1
		$V_{CL} = V_{CU}$	V_{CL} − 0.050	V_{CL}	V_{CL} + 0.030	V	1
Overdischarge detection voltage	V_{DL}	−	V_{DL} − 0.080	V_{DL}	V_{DL} + 0.060	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	V_{DU} − 0.130	V_{DU}	V_{DU} + 0.110	V	2
		$V_{DL} = V_{DU}$	V_{DU} − 0.080	V_{DU}	V_{DU} + 0.060	V	2
Discharge overcurrent detection voltage 1	V_{DIOV1}	−	V_{DIOV1} − 0.003	V_{DIOV1}	V_{DIOV1} + 0.003	V	2
Discharge overcurrent detection voltage 2	V_{DIOV2}	−	V_{DIOV2} − 0.005	V_{DIOV2}	V_{DIOV2} + 0.005	V	2
Load short-circuiting detection voltage	V_{SHORT}	−	V_{SHORT} − 0.020	V_{SHORT}	V_{SHORT} + 0.020	V	2
Charge overcurrent detection voltage	V_{CIOV}	−	V_{CIOV} − 0.003	V_{CIOV}	V_{CIOV} + 0.003	V	2
Discharge overcurrent release voltage	V_{RIOV}	V_{DD} = 3.4 V	V_{DD} × 0.77	V_{DD} × 0.8	V_{DD} × 0.83	V	2
0 V Battery Charge Function							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge function "available"	0.0	0.7	1.5	V	2
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge function "unavailable"	0.7	1.2	1.7	V	2
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V	250	1000	3000	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	V_{DD} = 3.4 V, V_{VM} = 1.0 V	3.5	10	20	kΩ	3
PS pin internal resistance	R_{PS}	−	R_{PS} × 0.25	R_{PS}	R_{PS} × 3.0	MΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	−	1.5	−	6.0	V	−
Operation voltage between VDD pin and VM pin	V_{DSOP2}	−	1.5	−	28	V	−
PS pin voltage "H"	V_{PSH}	−	−	−	V_{DD} × 0.95	V	2
PS pin voltage "L"	V_{PSL}	−	V_{DD} × 0.05	−	−	V	2
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	−	2.0	5.0	μA	3
Current consumption during power-down	I_{PDN}	$V_{DD} = V_{VM}$ = 1.5 V	−	−	0.1	μA	3
Current consumption during power-saving	I_{PS}	$V_{DD} = V_{VM}$ = 3.4 V	−	−	0.1	μA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	−	2.5	10	30	kΩ	4
CO pin resistance "L"	R_{COL}	−	2.5	10	30	kΩ	4
DO pin resistance "H"	R_{DOH}	−	2.5	10	30	kΩ	4
DO pin resistance "L"	R_{DOL}	−	2.5	10	30	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	−	t_{CU} × 0.4	t_{CU}	t_{CU} × 2.5	−	5
Overdischarge detection delay time	t_{DL}	−	t_{DL} × 0.4	t_{DL}	t_{DL} × 2.5	−	5
Discharge overcurrent detection delay time 1	t_{DIOV1}	−	t_{DIOV1} × 0.4	t_{DIOV1}	t_{DIOV1} × 2.5	−	5
Discharge overcurrent detection delay time 2	t_{DIOV2}	−	t_{DIOV2} × 0.4	t_{DIOV2}	t_{DIOV2} × 2.5	−	5
Load short-circuiting detection delay time	t_{SHORT}	−	t_{SHORT} × 0.4	t_{SHORT}	t_{SHORT} × 2.5	−	5
Charge overcurrent detection delay time	t_{CIOV}	−	t_{CIOV} × 0.4	t_{CIOV}	t_{CIOV} × 2.5	−	5
Power-saving delay time	t_{PS}	−	t_{PS} × 0.4	t_{PS}	t_{PS} × 2.5	−	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

When PS pin control logic is active "H", SW1 and SW3 are turned off, SW2 and SW4 are turned on. When PS pin control logic is active "L", SW1 and SW3 are turned on, SW2 and SW4 are turned off.

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = 3.4 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL}.

2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage (V_{DL}) is defined as the voltage V1 at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased from the starting conditions of V1 = 3.4 V, V2 = V5 = 0 V. Overdischarge release voltage (V_{DU}) is defined as the voltage V1 at which V_{DO} goes from "L" to "H" when setting V2 = 0.01 V, V5 = 0 V and when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage (V_{HD}) is defined as the difference between V_{DU} and V_{DL}.

3. Discharge overcurrent detection voltage 1, discharge overcurrent release voltage (Test circuit 2)

3. 1 Release voltage of discharge overcurrent status "V_{DIOV1}"

Discharge overcurrent detection voltage 1 (V_{DIOV1}) is defined as the voltage V2 whose delay time for changing V_{DO} from "H" to "L" is discharge overcurrent detection delay time (t_{DIOV1}) when the voltage V2 is increased from the starting conditions of V1 = 3.4 V, V2 = V5 = 0 V. V_{DO} goes from "L" to "H" when setting V2 = 3.4 V and when the voltage V2 is then gradually decreased to V_{DIOV1} typ. or lower.

3. 2 Release voltage of discharge overcurrent status "V_{RIOV}"

V_{DIOV1} is defined as the voltage V2 whose delay time for changing V_{DO} from "H" to "L" is t_{DIOV1} when the voltage V2 is increased from the starting conditions of V1 = 3.4 V, V2 = V5 = 0 V. Discharge overcurrent release voltage (V_{RIOV}) is defined as the voltage V2 at which V_{DO} goes from "L" to "H" when setting V2 = 3.4 V and when the voltage V2 is then gradually decreased.

4. Discharge overcurrent detection voltage 2 (Test circuit 2)

Discharge overcurrent detection voltage 2 (V_{DIOV2}) is defined as the voltage V2 whose delay time for changing V_{DO} from "H" to "L" is discharge overcurrent detection delay time 2 (t_{DIOV2}) when the voltage V2 is increased from the starting conditions of V1 = 3.4 V, V2 = V5 = 0 V.

5. Load short-circuiting detection voltage (Test circuit 2)

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage V2 whose delay time for changing V_{DO} from "H" to "L" is load short-circuiting detection delay time (t_{SHORT}) when the voltage V2 is increased from the starting conditions of V1 = 3.4 V, V2 = V5 = 0 V.

6. Charge overcurrent detection voltage (Test circuit 2)

Charge overcurrent detection voltage (V_{CIOV}) is defined as the voltage V2 whose delay time for changing V_{CO} from "H" to "L" is charge overcurrent detection delay time (t_{CIOV}) when the voltage V2 is decreased from the starting conditions of V1 = 3.4 V, V2 = V5 = 0 V.

7. Current consumption during operation
(Test circuit 3)

The current consumption during operation (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = 3.4 V and V2 = V5 = 0 V. However, the current flowing through the internal resistor of the PS pin is excluded.

8. Current consumption during power-down
(Test circuit 3)

The current consumption during power-down (I_{PDN}) is I_{DD} under the set conditions of V1 = V2 = 1.5 V, V5 = 0 V.

9. Current consumption during power-saving
(Test circuit 3)

The current consumption during power-saving (I_{PS}) is I_{DD} under the set conditions of V1 = V2 = V5 = 3.4 V.

10. Resistance between VDD pin and VM pin
(Test circuit 3)

R_{VMD} is the resistance between VDD pin and VM pin under the set conditions of V1 = 1.8 V, V2 = V5 = 0 V.

11. Resistance between VM pin and VSS pin (Release condition of discharge overcurrent status "load disconnection")
(Test circuit 3)

R_{VMS} is the resistance between VM pin and VSS pin under the set conditions of V1 = 3.4 V, V2 = 1.0 V, V5 = 0 V.

12. PS pin internal resistance
(Test circuit 3)

12. 1 PS pin control logic active "H" and PS pin internal resistance connection "pull-up"

Resistance between PS pin and VDD pin is R_{PS} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

12. 2 PS pin control logic active "H" and PS pin internal resistance connection "pull-down"

Resistance between PS pin and VSS pin is R_{PS} under the set conditions of V1 = V5 = 3.4 V, V2 = 0 V.

12. 3 PS pin control logic active "L" and PS pin internal resistance connection "pull-up"

Resistance between PS pin and VDD pin is R_{PS} under the set conditions of V1 = V5 = 3.4 V, V2 = 0 V.

12. 4 PS pin control logic active "L" and PS pin internal resistance connection "pull-down"

Resistance between PS pin and VSS pin is R_{PS} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

13. CO pin resistance "H"
(Test circuit 4)

The CO pin resistance "H" (R_{COH}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V3 = 3.0 V.

14. CO pin resistance "L"
(Test circuit 4)

The CO pin resistance "L" (R_{COL}) is the resistance between VM pin and CO pin under the set conditions of V1 = 4.7 V, V2 = 0 V, V3 = 0.4 V.

15. DO pin resistance "H" (Test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V4 = 3.0 V.

16. DO pin resistance "L" (Test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = 1.8 V, V2 = 0 V, V4 = 0.4 V.

17. PS pin voltage "H", PS pin voltage "L" (Test circuit 2)

17. 1 PS pin control logic active "H"

The PS pin voltage "H" (V_{PSH}) is defined as the voltage V5 at which V_{DO} goes from "H" to "L" and when the voltage V5 is gradually increased under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

17. 2 PS pin control logic active "L"

The PS pin voltage "L" (V_{PSL}) is defined as the voltage difference between the voltage V5 and the voltage V1 (V1 − V5) at which V_{DO} goes from "H" to "L" when the voltage V5 is gradually increased under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

18. Overcharge detection delay time (Test circuit 5)

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "L" just after the voltage V1 increases and exceeds V_{CU} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

19. Overdischarge detection delay time (Test circuit 5)

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to go to "L" after the voltage V1 decreases and falls below V_{DL} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

20. Discharge overcurrent detection delay time 1 (Test circuit 5)

The discharge overcurrent detection delay time 1 (t_{DIOV1}) is the time needed for V_{DO} to go to "L" after the voltage V2 increases and exceeds V_{DIOV1} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

21. Discharge overcurrent detection delay time 2 (Test circuit 5)

The discharge overcurrent detection delay time 2 (t_{DIOV2}) is the time needed for V_{DO} to go to "L" after the voltage V2 increases and exceeds V_{DIOV2} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

22. Load short-circuiting detection delay time (Test circuit 5)

The load short-circuiting detection delay time (t_{SHORT}) is the time needed for V_{DO} to go to "L" after the voltage V2 increases and exceeds V_{SHORT} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

23. Charge overcurrent detection delay time (Test circuit 5)

The charge overcurrent detection delay time (t_{CIOV}) is the time needed for V_{CO} to go to "L" after the voltage V2 decreases and falls below V_{CIOV} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

24. Power-saving delay time (Test circuit 5)

24. 1 PS pin control logic active "H"

Power-saving delay time (t_{PS}) is the time needed for V_{DO} to go to "L" after the voltage V5 increases and exceeds V_{PSH} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

24. 2 PS pin control logic active "L"

Power-saving delay time (t_{PS}) is the time needed for V_{DO} to go to "L" after the voltage V5 increases and V1 − V5 falls below V_{PSL} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

25. 0 V battery charge starting charger voltage (0 V battery charge function "available") (Test circuit 2)

The 0 V battery charge starting charger voltage (V_{0CHA}) is defined as the absolute value of voltage V2 at which V_{CO} goes to "H" (V_{CO} = V_{DD}) when the voltage V2 is gradually decreased from the starting condition of V1 = V2 = V5 = 0 V.

26. 0 V battery charge inhibition battery voltage (0 V battery charge function "unavailable") (Test circuit 2)

The 0 V battery charge inhibition battery voltage (V_{0INH}) is defined as the voltage V1 at which V_{CO} goes to "L" (V_{CO} = V_{VM}) when the voltage V1 is gradually decreased, after setting V1 = 1.9 V, V2 = −2.0 V, V5 = 0 V.

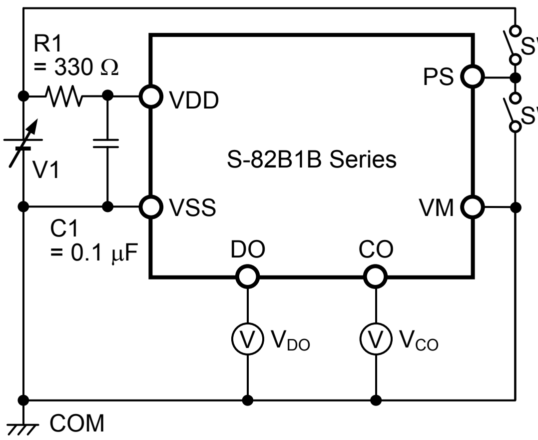


Figure 4 Test Circuit 1

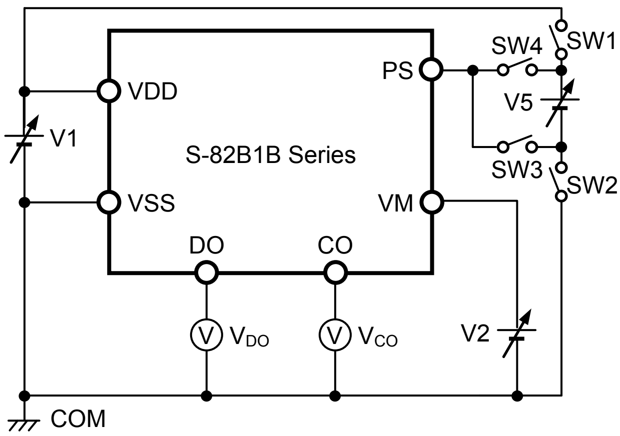


Figure 5 Test Circuit 2

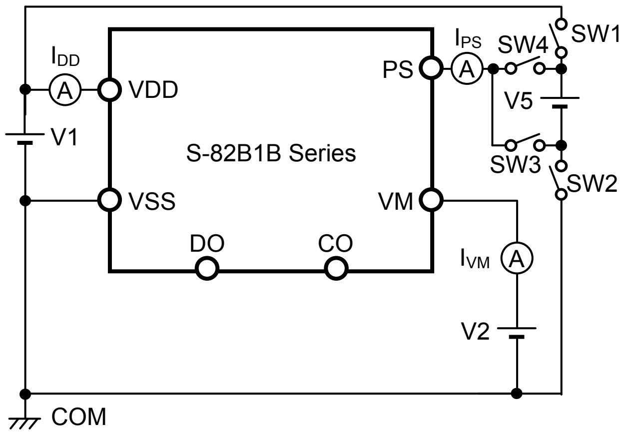


Figure 6 Test Circuit 3

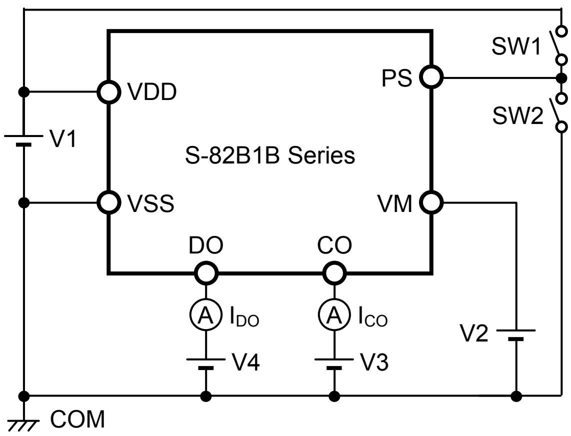


Figure 7 Test Circuit 4

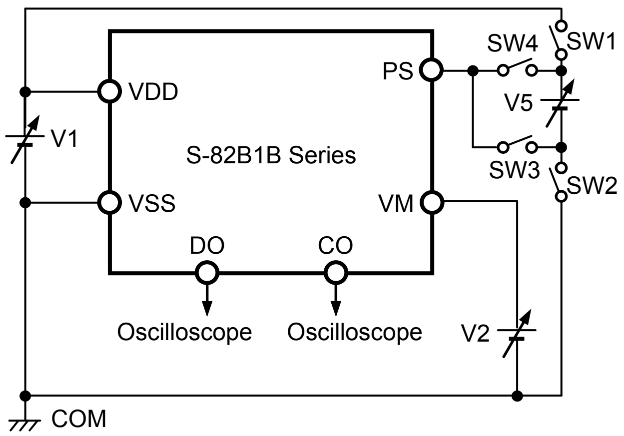


Figure 8 Test Circuit 5

■ Operation

Remark Refer to "**■ Battery Protection IC Connection Example**".

1. Normal status

The S-82B1B Series monitors the voltage of the battery connected between VDD pin and VSS pin, the voltage between VM pin and VSS pin and the voltage between PS pin and VSS pin to control charging and discharging.
When the battery voltage is in the range from overdischarge detection voltage (V_{DL}) to overcharge detection voltage (V_{CU}), the VM pin voltage is in the range from charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent detection voltage 1 (V_{DIOV1}), the S-82B1B Series turns both the charge-discharge control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.
The resistance between VDD pin and VM pin (R_{VMD}), and the resistance between VM pin and VSS pin (R_{VMS}) are not connected in the normal status.

Caution After the battery is connected, discharging may not be carried. In this case, the S-82B1B Series becomes the normal status by connecting a charger.

2. Overcharge status

2. 1 $V_{CL} \neq V_{CU}$ (Product in which overcharge release voltage differs from overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, the S-82B1B Series turns the charge control FET off to stop charging. This condition is called the overcharge status.
The overcharge status is released in the following two cases.

(1) In the case that the VM pin voltage is lower than 0.35 V typ., the S-82B1B Series releases the overcharge status when the battery voltage falls below overcharge release voltage (V_{CL}).
(2) In the case that the VM pin voltage is equal to or higher than 0.35 V typ., the S-82B1B Series releases the overcharge status when the battery voltage falls below V_{CU}.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the V_f voltage of the parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., the S-82B1B Series releases the overcharge status when the battery voltage is equal to or lower than V_{CU}.

Caution If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

2. 2 $V_{CL} = V_{CU}$ (Product in which overcharge release voltage is the same as overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, the S-82B1B Series turns the charge control FET off to stop charging. This condition is called the overcharge status.
In the case that the VM pin voltage is equal to or higher than 0.35 V typ. and the battery voltage falls below V_{CU}, the S-82B1B Series releases the overcharge status.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the V_f voltage of the parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., the S-82B1B Series releases the overcharge status when the battery voltage is equal to or lower than V_{CU}.

Caution 1. If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.
2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below V_{CL}. The overcharge status is released when the discharge current flows and the VM pin voltage goes over 0.35 V typ. by removing the charger.

3. Overdischarge status

When the battery voltage falls below V_{DL} during discharging in the normal status and the condition continues for the overdischarge detection delay time (t_{DL}) or longer, the S-82B1B Series turns the discharge control FET off to stop discharging. This condition is called the overdischarge status.
Under the overdischarge status, VDD pin and VM pin are shorted by R_{VMD} in the S-82B1B Series. The VM pin voltage is pulled up by R_{VMD}.
When connecting a charger in the overdischarge status, the battery voltage reaches V_{DL} or higher and the S-82B1B Series releases the overdischarge status if the VM pin voltage falls below 0 V typ.
The battery voltage reaches the overdischarge release voltage (V_{DU}) or higher and the S-82B1B Series releases the overdischarge status if the VM pin voltage does not fall below 0 V typ.
R_{VMS} is not connected in the overdischarge status.
Under the overdischarge status, when voltage difference between VDD pin and VM pin is 0.8 V typ. or lower, the power-down function works and the current consumption is reduced to the current consumption during power-down (I_{PDN}). By connecting a battery charger, the power-down function is released when the VM pin voltage is 0.7 V typ. or lower.

- When a battery is not connected to a charger and the VM pin voltage $\geq$ 0.7 V typ., the S-82B1B Series maintains the overdischarge status even when the battery voltage reaches V_{DU} or higher.
- When a battery is connected to a charger and 0.7 V typ. $>$ the VM pin voltage $>$ 0 V typ., the battery voltage reaches V_{DU} or higher and the S-82B1B Series releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ. $\geq$ the VM pin voltage, the battery voltage reaches V_{DL} or higher and the S-82B1B Series releases the overdischarge status.

4. Discharge overcurrent status (discharge overcurrent 1, discharge overcurrent 2, load short-circuiting)

When a battery in the normal status is in the status where the VM pin voltage is equal to or higher than V_{DIOV1} because the discharge current is equal to or higher than the specified value and the status lasts for the discharge overcurrent detection delay time (t_{DIOV1}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

4. 1 Release condition of discharge overcurrent status "load disconnection" and release voltage of discharge overcurrent status "V_{DIOV1}"

Under the discharge overcurrent status, VM pin and VSS pin are shorted by R_{VMS} in the S-82B1B Series. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, VM pin returns to the VSS pin voltage.
When the VM pin voltage returns to V_{DIOV1} or lower, the S-82B1B Series releases the discharge overcurrent status.
R_{VMD} is not connected in the discharge overcurrent status.

4. 2 Release condition of discharge overcurrent status "load disconnection" and release voltage of discharge overcurrent status "V_{RIOV}"

Under the discharge overcurrent status, VM pin and VSS pin are shorted by R_{VMS} in the S-82B1B Series. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, VM pin returns to the VSS pin voltage.
When the VM pin voltage returns to V_{RIOV} or lower, the S-82B1B Series releases the discharge overcurrent status.
R_{VMD} is not connected in the discharge overcurrent status.

4. 3 Release condition of discharge overcurrent status "charger connection"

Under the discharge overcurrent status, VDD pin and VM pin are shorted by R_{VMD} in the S-82B1B Series.
When a battery is connected to a charger and the VM pin voltage returns to V_{DIOV1} or lower, the S-82B1B Series releases the discharge overcurrent status.
R_{VMS} is not connected in the discharge overcurrent status.

5. Charge overcurrent status

When a battery in the normal status is in the status where the VM pin voltage is equal to or lower than V_{CIOV} because the charge current is equal to or higher than the specified value and the status lasts for the charge overcurrent detection delay time (t_{CIOV}) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.
The S-82B1B Series releases the charge overcurrent status when the discharge current flows and the VM pin voltage is 0.35 V typ. or higher by removing the charger.
The charge overcurrent detection does not function in the overdischarge status.

6. Power-saving function

6. 1 PS pin control logic active "H"

When a battery in the normal status is in the status where the PS pin voltage is equal to higher than PS pin voltage "H" (V_{PSH}) and the status lasts for the power-saving delay time (t_{PS}) or longer, the discharge control FET is turned off, and discharging is stopped. This status is called the discharge inhibition status.
Under the discharge inhibition status, VDD pin and VM pin are shorted by R_{VMD} in the S-82B1B Series, and VM pin is pulled up by R_{VMD}.
When the discharge inhibition status lasts for the overdischarge detection delay time (t_{DL}) or longer, the power-saving function works and the current consumption is reduced to the current consumption during power-saving (I_{PS}) if voltage difference between VDD pin and VM pin is 0.8 V typ. or lower.

6. 2 PS pin control logic active "L"

When a battery in the normal status is in the status where the PS pin voltage is equal to lower than PS pin voltage "L" (V_{PSL}) and the status lasts for the power-saving delay time (t_{PS}) or longer, the discharge control FET is turned off, and discharging is stopped. This status is called the discharge inhibition status.
Under the discharge inhibition status, VDD pin and VM pin are shorted by R_{VMD} in the S-82B1B Series, and VM pin is pulled up by R_{VMD}.
When the discharge inhibition status lasts for the overdischarge detection delay time (t_{DL}) or longer, the power-saving function works and the current consumption is reduced to the current consumption during power-saving (I_{PS}) if voltage difference between VDD pin and VM pin is 0.8 V typ. or lower.

When the PS pin is active and the condition lasts for t_{PS} + t_{DL} or longer, the power-saving function works and it continues working even if the PS pin is made inactive.
By connecting a battery charger, the power-saving function is released when the VM pin voltage is 0.7 V typ. or lower.

7. 0 V battery charge function "available"

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or a higher voltage is applied between the EB+ and EB− pins by connecting a charger, the charge control FET gate is fixed to the VDD pin voltage.
When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than V_{DL}, the S-82B1B Series enters the normal status.

Caution 1. Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.

2. The 0 V battery charge function has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge function is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than V_{DL}.

8. 0 V battery charge function "unavailable"

This function inhibits charging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charge control FET gate is fixed to the EB− pin voltage to inhibit charging. When the battery voltage is V_{0INH} or higher, charging can be performed.

Caution Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.

9. Delay circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

Remark t_{DIOV1}, t_{DIOV2} and t_{SHORT} start when V_{DIOV1} is detected. When V_{DIOV2} or V_{SHORT} is detected over t_{DIOV2} or t_{SHORT} after the detection of V_{DIOV1}, the S-82B1B Series turns the discharge control FET off within t_{DIOV2} or t_{SHORT} of each detection.

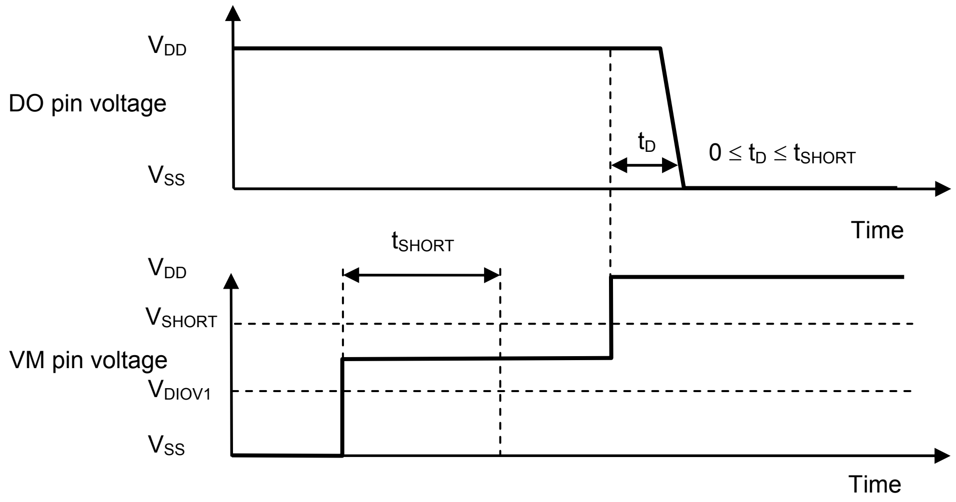
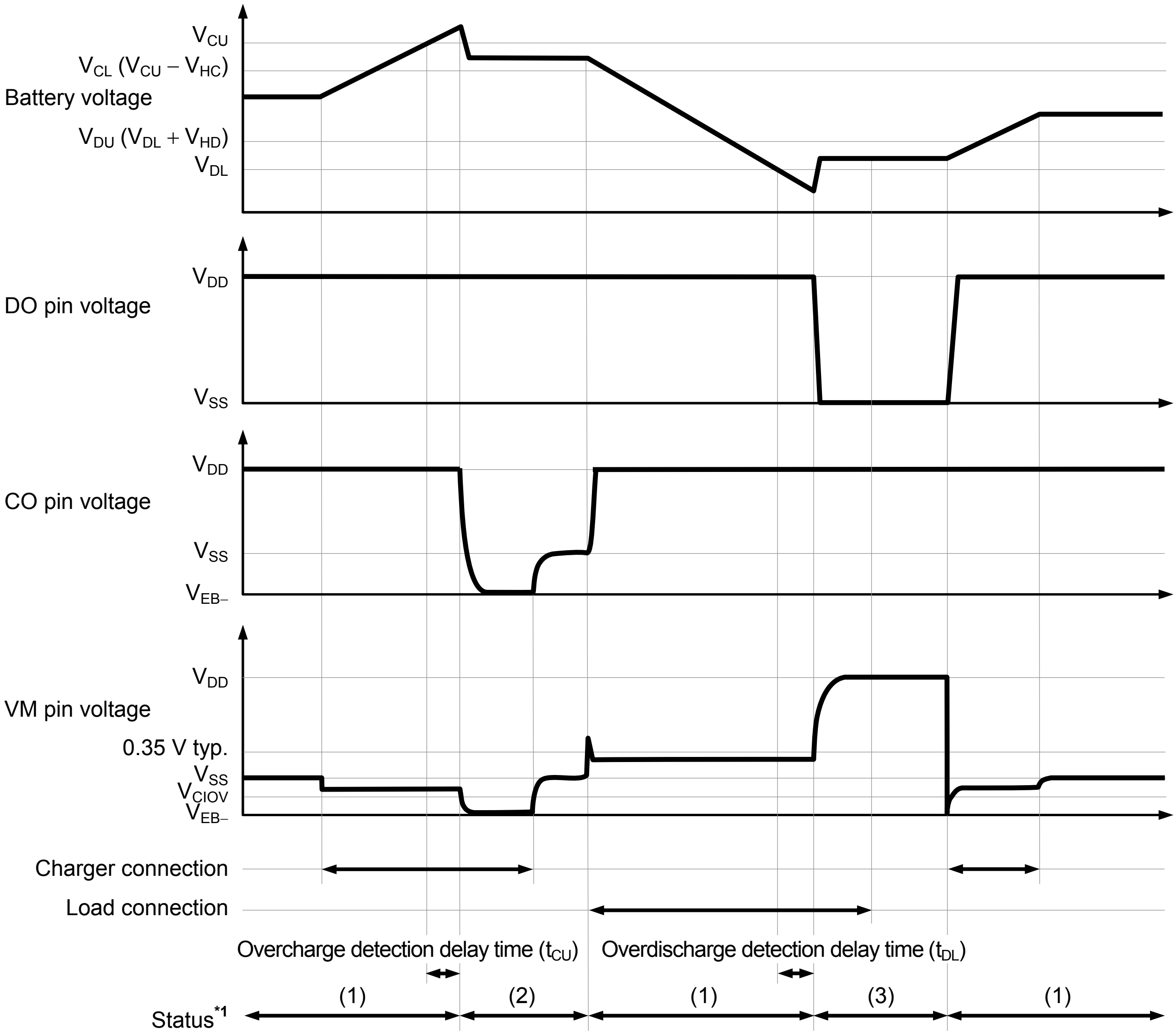


Figure 9

■ Timing Charts

1. Overcharge detection, overdischarge detection



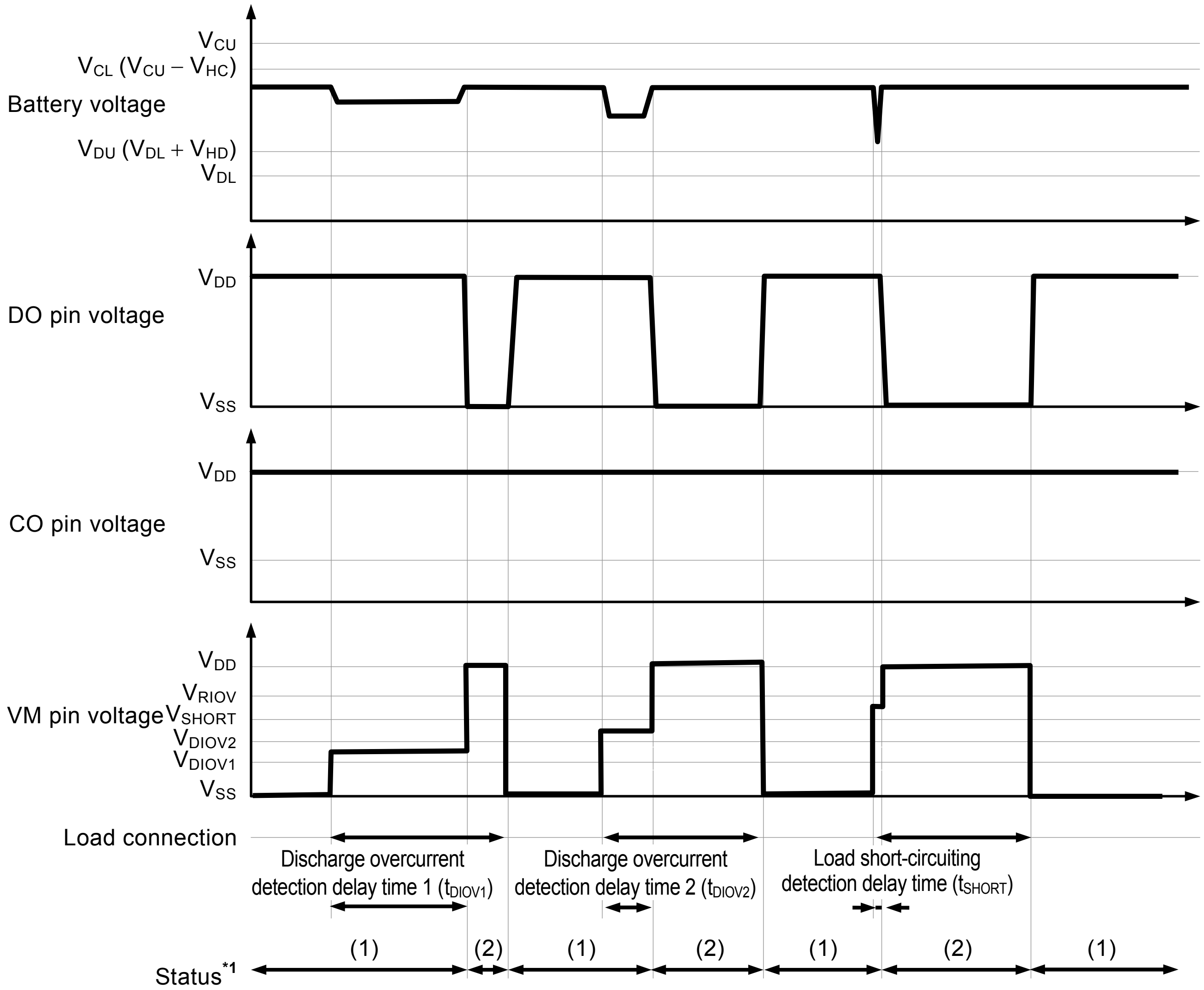
***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 10

2. Discharge overcurrent detection

2. 1 Release condition of discharge overcurrent status "load disconnection"

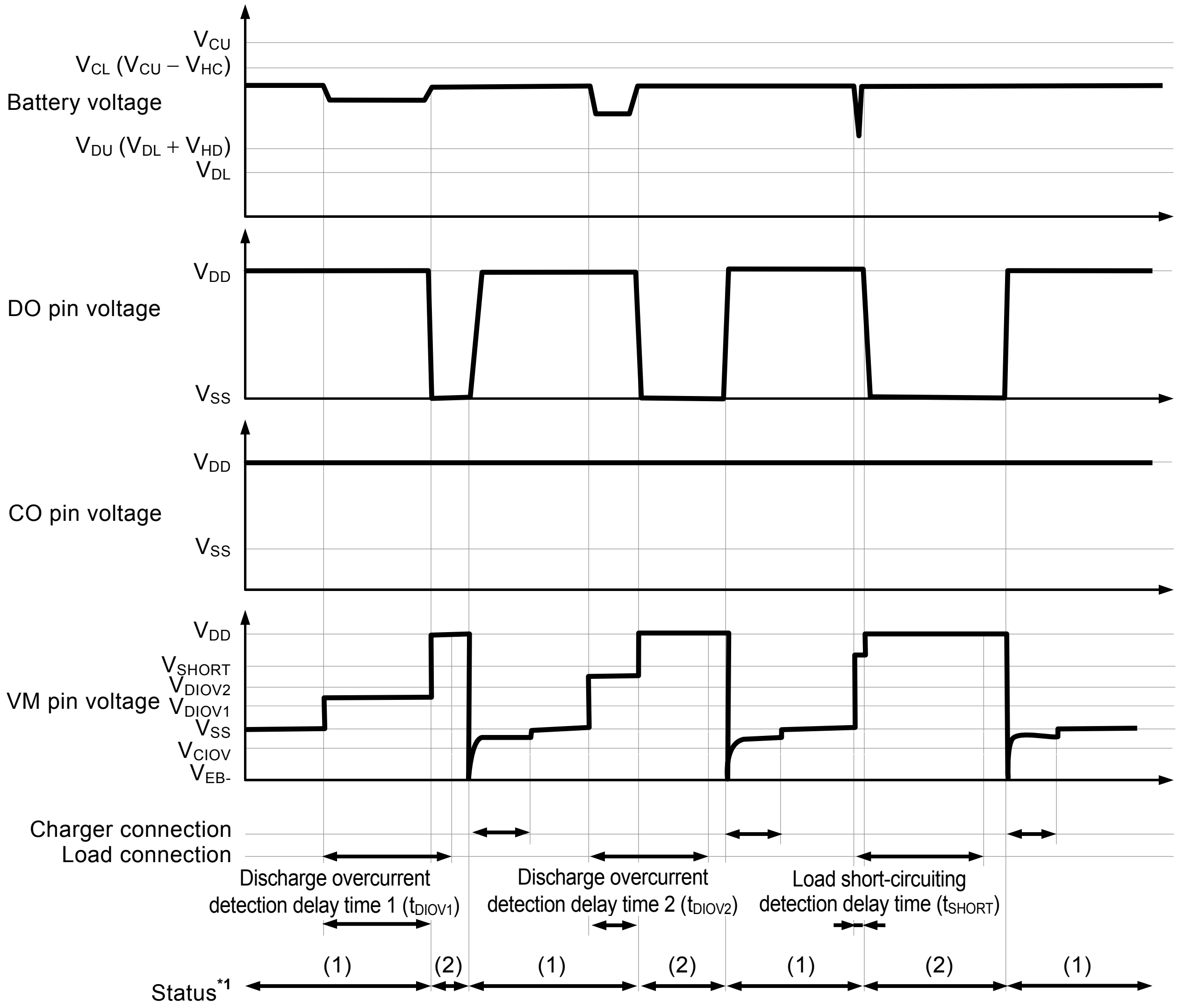


***1.** (1): Normal status
(2): Discharge overcurrent status

Remark The charger is assumed to charge with a constant current.

Figure 11

2. 2 Release condition of discharge overcurrent status "charger connection"

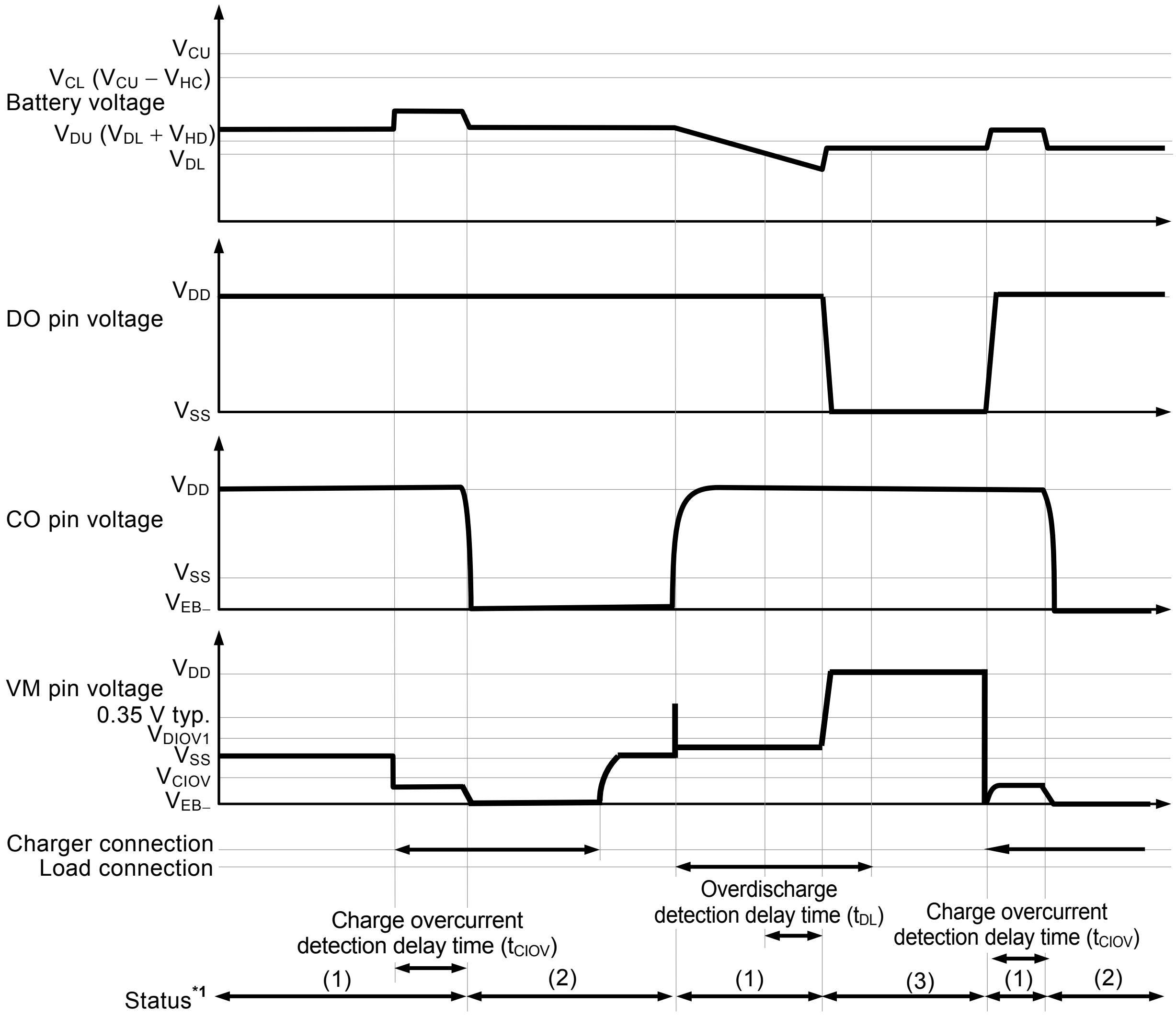


***1.** (1): Normal status
(2): Discharge overcurrent status

Remark The charger is assumed to charge with a constant current.

Figure 12

3. Charge overcurrent detection

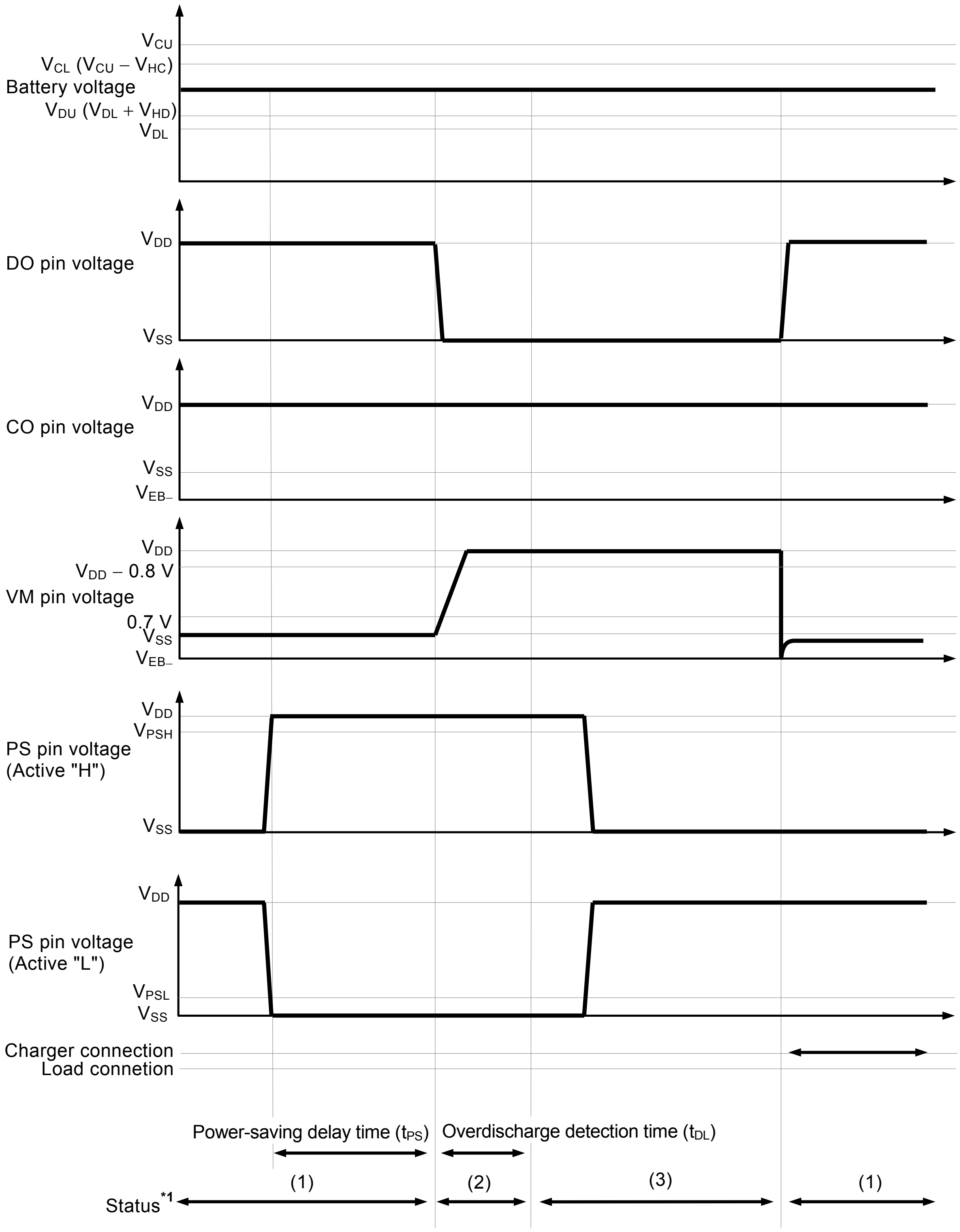


***1.** (1): Normal status
(2): Charge overcurrent status
(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 13

4. Power-saving function



***1.** (1): Normal status
(2): Discharge inhibition status
(3): Working of power-saving function

Remark The charger is assumed to charge with a constant current.

Figure 14

■ Battery Protection IC Connection Example

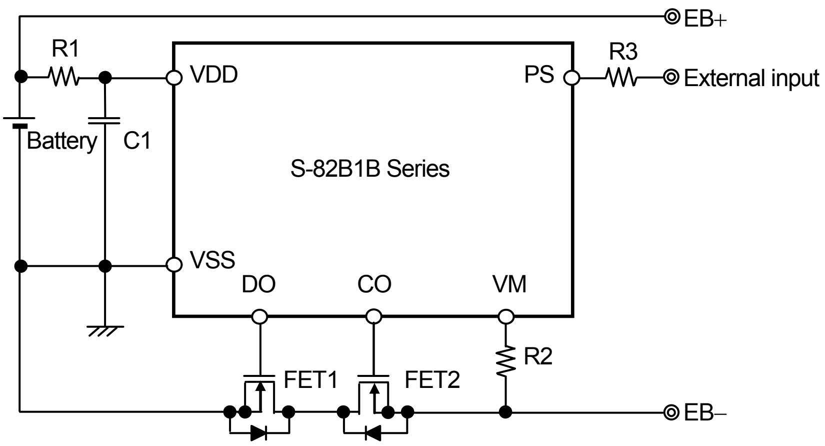


Figure 15

Table 11 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
FET1	N-channel MOS FET	Discharge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*1
FET2	N-channel MOS FET	Charge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*1
R1	Resistor	ESD protection, For power fluctuation	270 Ω	330 Ω	1 kΩ	Caution should be exercised when setting V_{DIOV1} ≤ 30 mV, V_{CIOV} ≥ −30 mV.*2
C1	Capacitor	For power fluctuation	0.068 μF	0.1 μF	1.0 μF	Caution should be exercised when setting V_{DIOV1} ≤ 30 mV, V_{CIOV} ≥ −30 mV.*2
R2	Resistor	ESD protection, Protection for reverse connection of a charger	300 Ω	470 Ω	1.5 kΩ	–
R3	Resistor	PS pin input protection	–	1 kΩ	–	–

***1.** If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

***2.** When setting V_{DIOV1} ≤ 30 mV, V_{CIOV} ≥ −30 mV for power fluctuation protection, the condition of R1 × C1 ≥ 100 μF • Ω should be met.

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

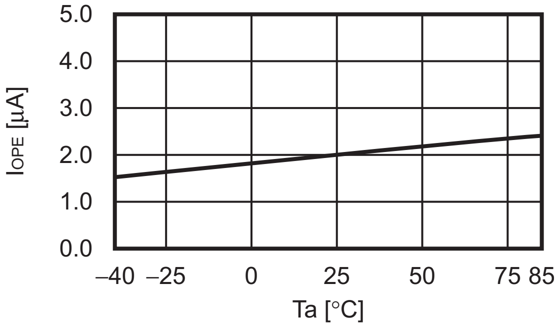
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

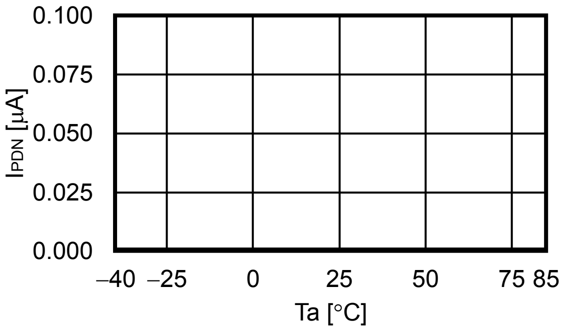
■ Characteristics (Typical Data)

1. Current consumption

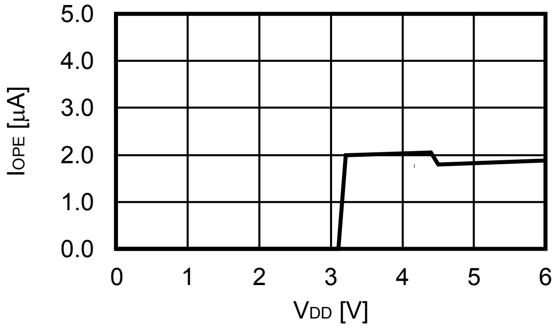
1. 1 I_{OPE} vs. Ta



1. 2 I_{PDN} vs. Ta

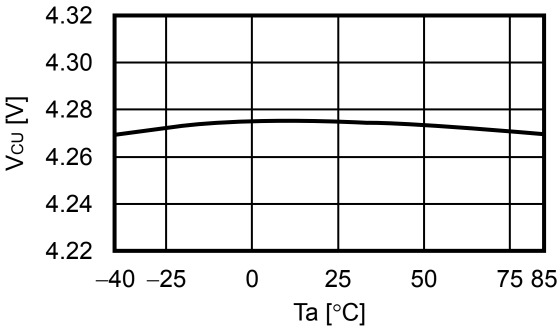


1. 3 I_{OPE} vs. V_{DD}

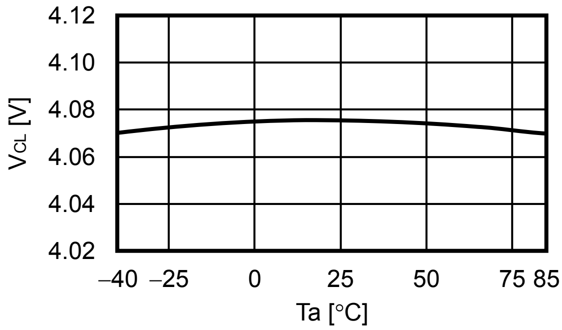


2. Detection voltage

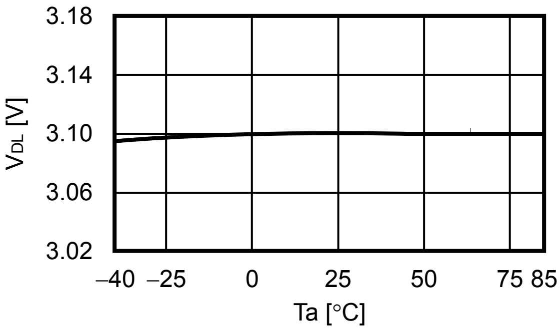
2. 1 V_{CU} vs. Ta



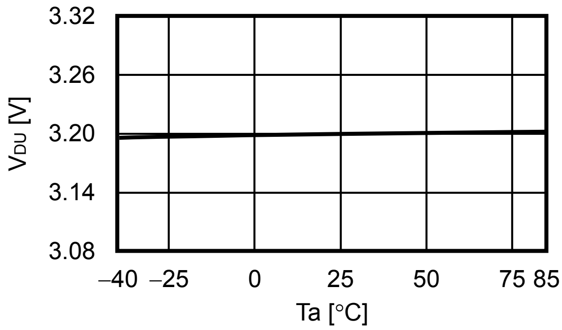
2. 2 V_{CL} vs. Ta



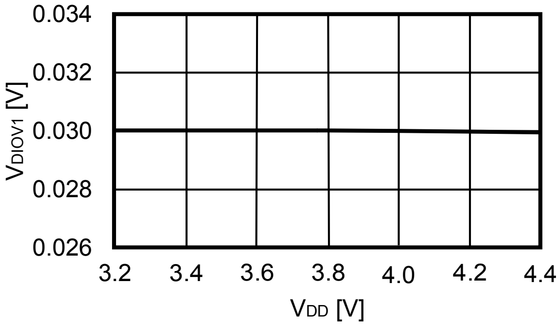
2. 3 V_{DL} vs. Ta



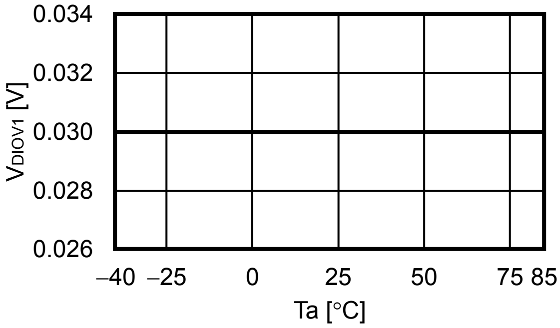
2. 4 V_{DU} vs. Ta



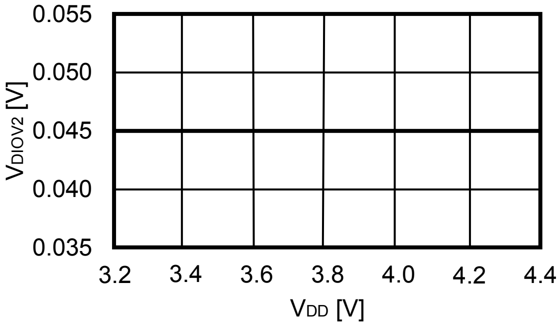
2. 5 V_{DIOV1} vs. V_{DD}



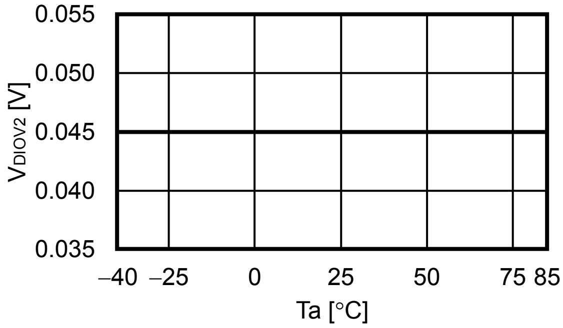
2. 6 V_{DIOV1} vs. Ta



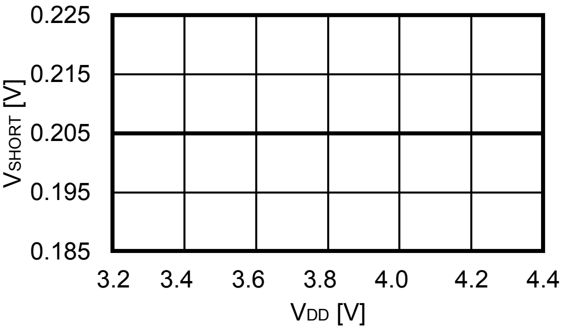
2. 7 V_{DIOV2} vs. V_{DD}



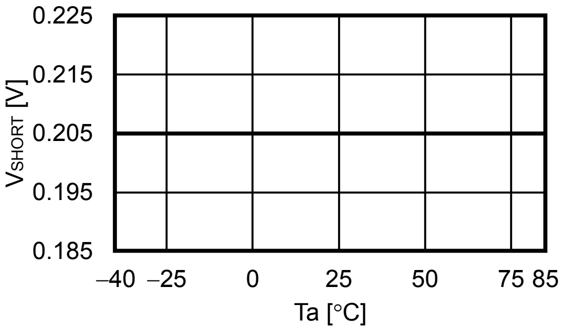
2. 8 V_{DIOV2} vs. Ta



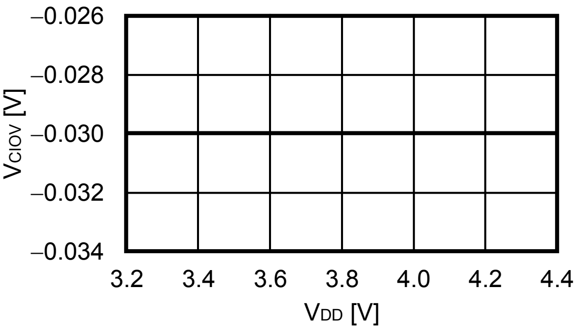
2. 9 V_{SHORT} vs. V_{DD}



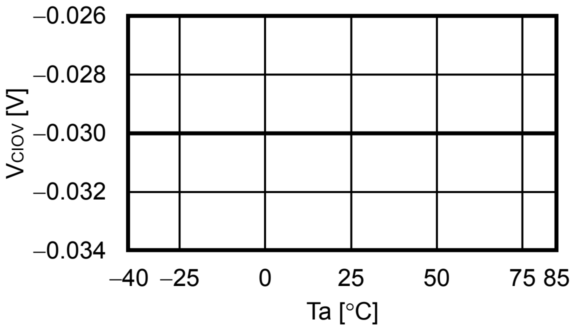
2. 10 V_{SHORT} vs. Ta



2. 11 V_{CIOV} vs. V_{DD}

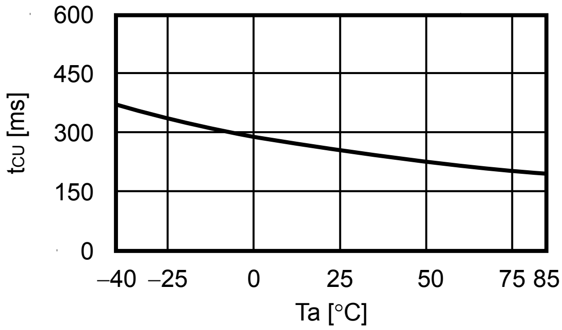


2. 12 V_{CIOV} vs. Ta

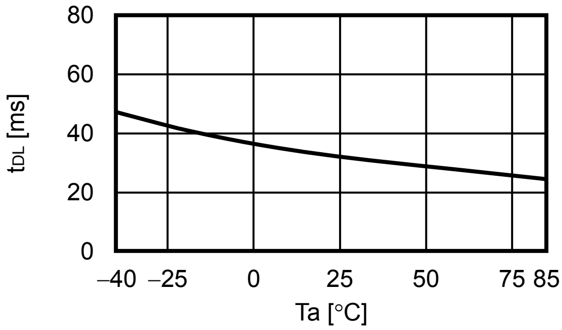


3. Delay time

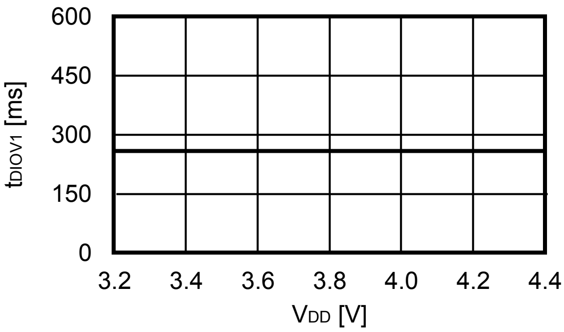
3. 1 t_{CU} vs. Ta



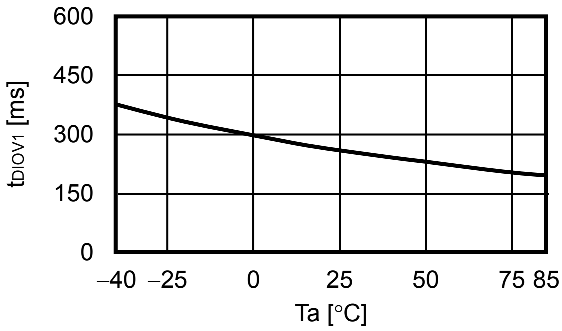
3. 2 t_{DL} vs. Ta



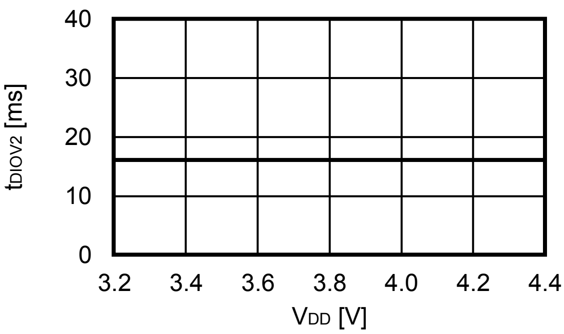
3. 3 t_{DIOV1} vs. V_{DD}



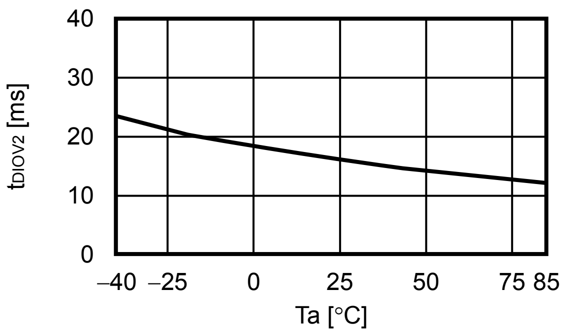
3. 4 t_{DIOV1} vs. Ta



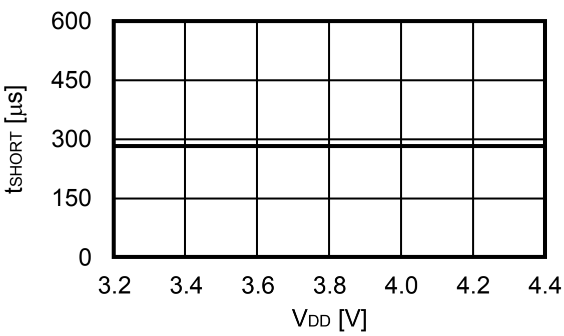
3. 5 t_{DIOV2} vs. V_{DD}



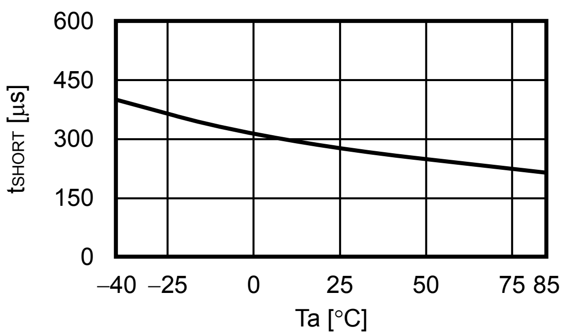
3. 6 t_{DIOV2} vs. Ta



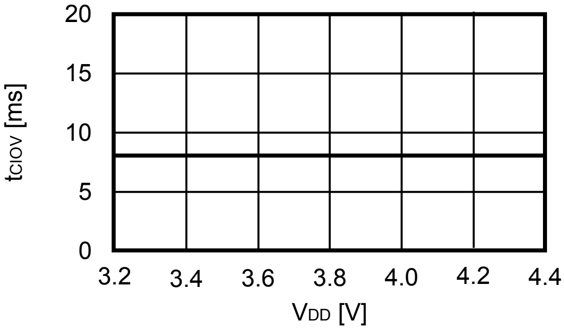
3. 7 t_{SHORT} vs. V_{DD}



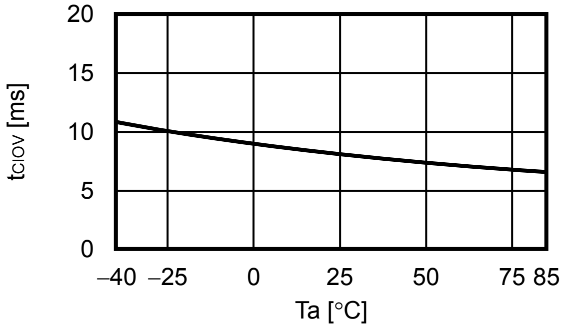
3. 8 t_{SHORT} vs. Ta



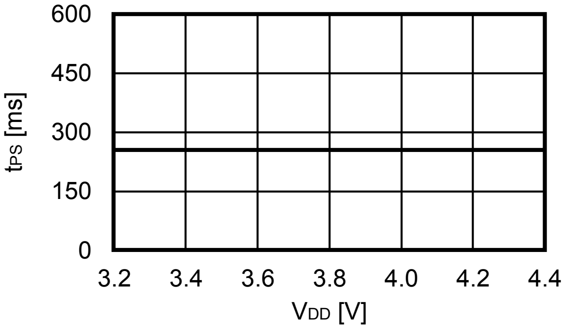
3. 9 t_{CIOV} vs. V_{DD}



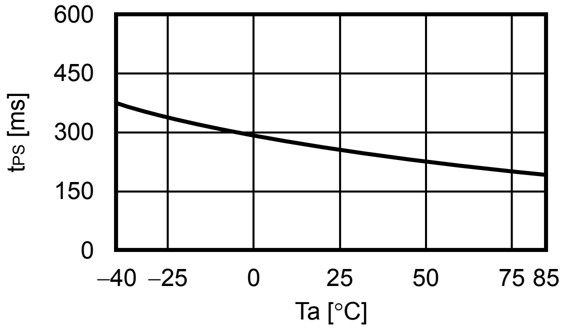
3. 10 t_{CIOV} vs. Ta



3. 11 t_{PS} vs. V_{DD}

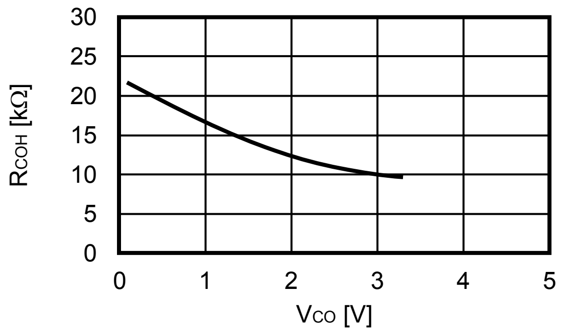


3. 12 t_{PS} vs. Ta

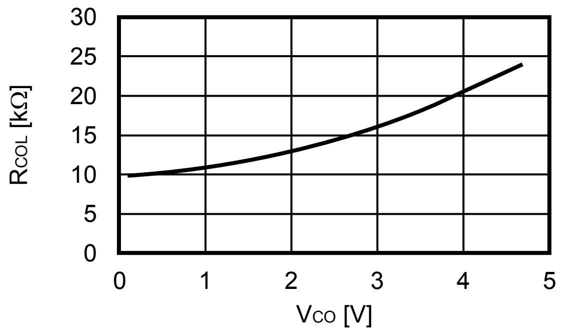


4. Output resistance

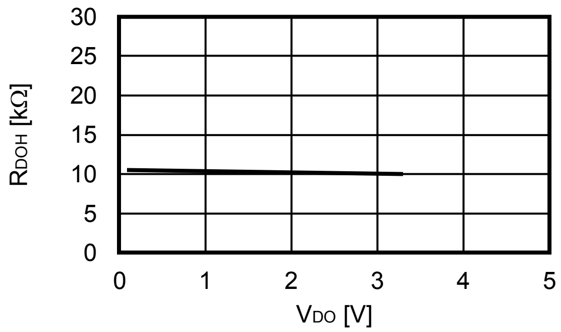
4. 1 R_{COH} vs. V_{CO}



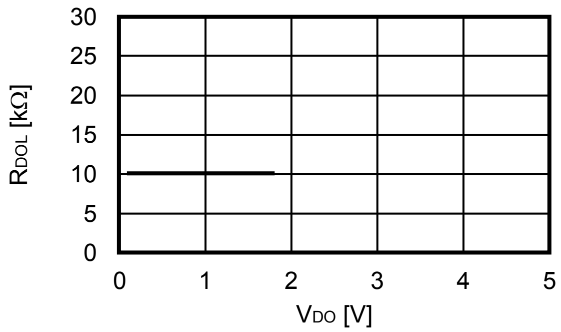
4. 2 R_{COL} vs. V_{CO}



4. 3 R_{DOH} vs. V_{DO}

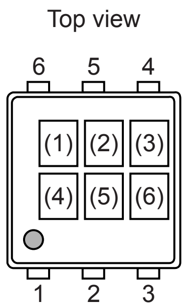


4. 4 R_{DOL} vs. V_{DO}



■ Marking Specifications

1. SNT-6A



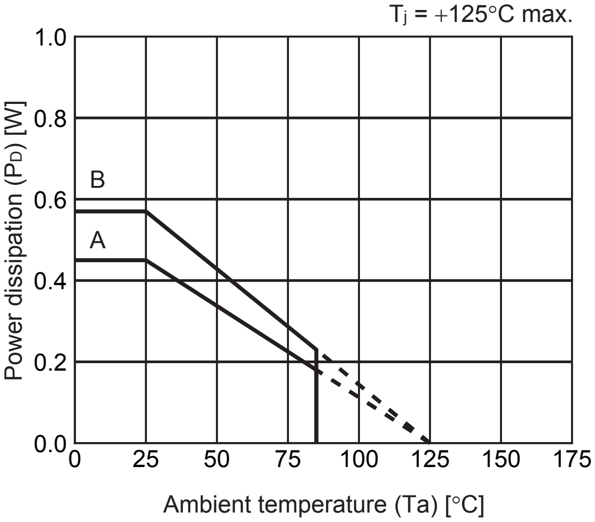
(1) to (3): Product code (refer to **Product name vs. Product code**)
(4) to (6): Lot number

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-82B1BAA-I6T1U	7	L	A

■ Power Dissipation

SNT-6A

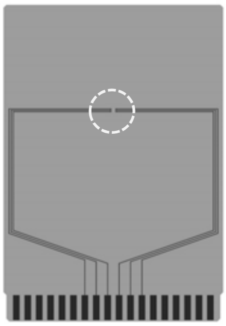


Board	Power Dissipation (P_D)
A	0.45 W
B	0.57 W
C	–
D	–
E	–

SNT-6A Test Board

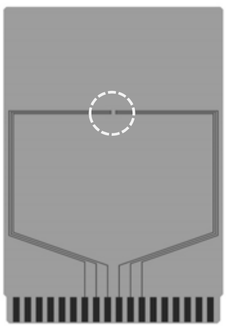
(1) Board A

IC Mount Area



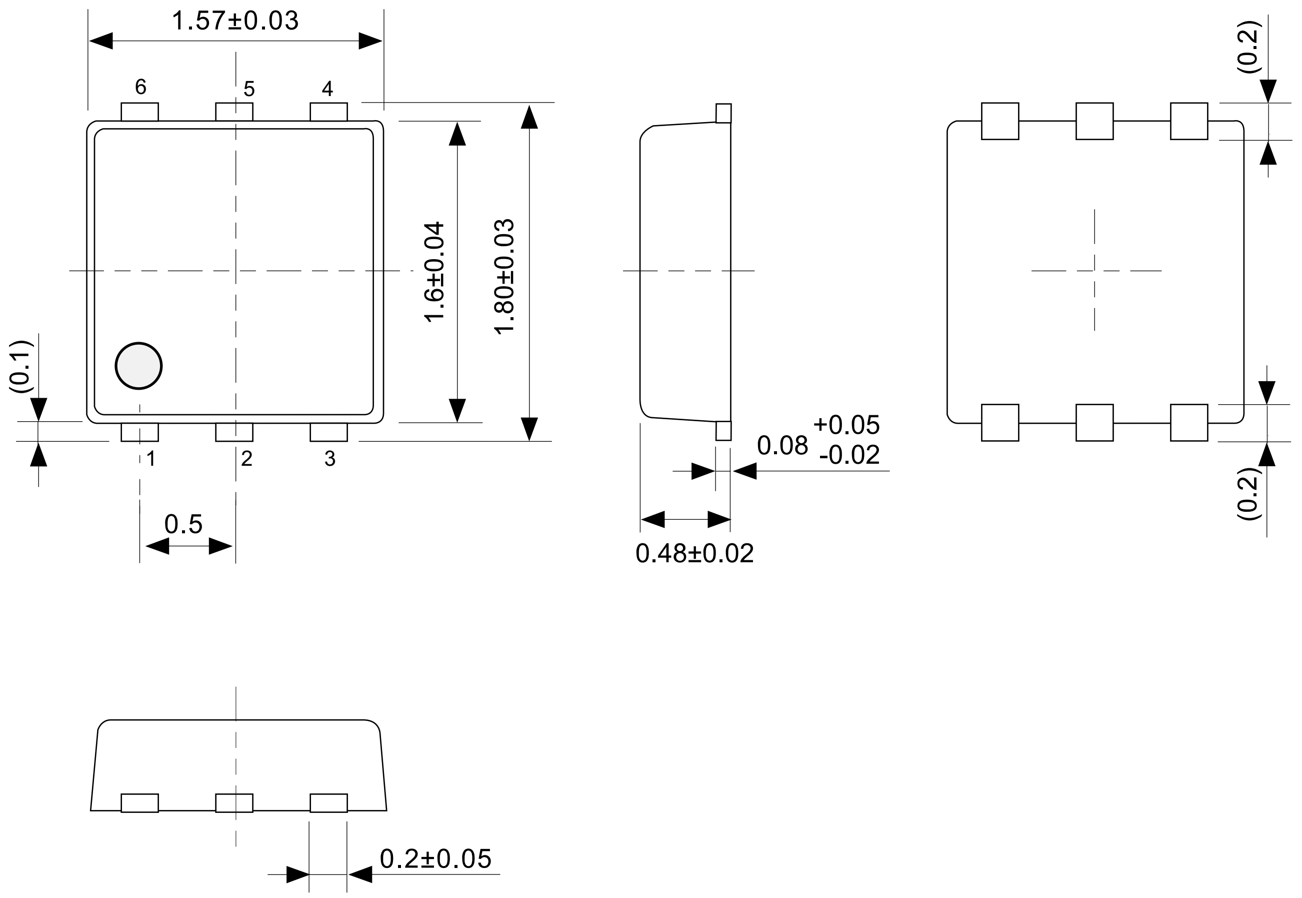
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

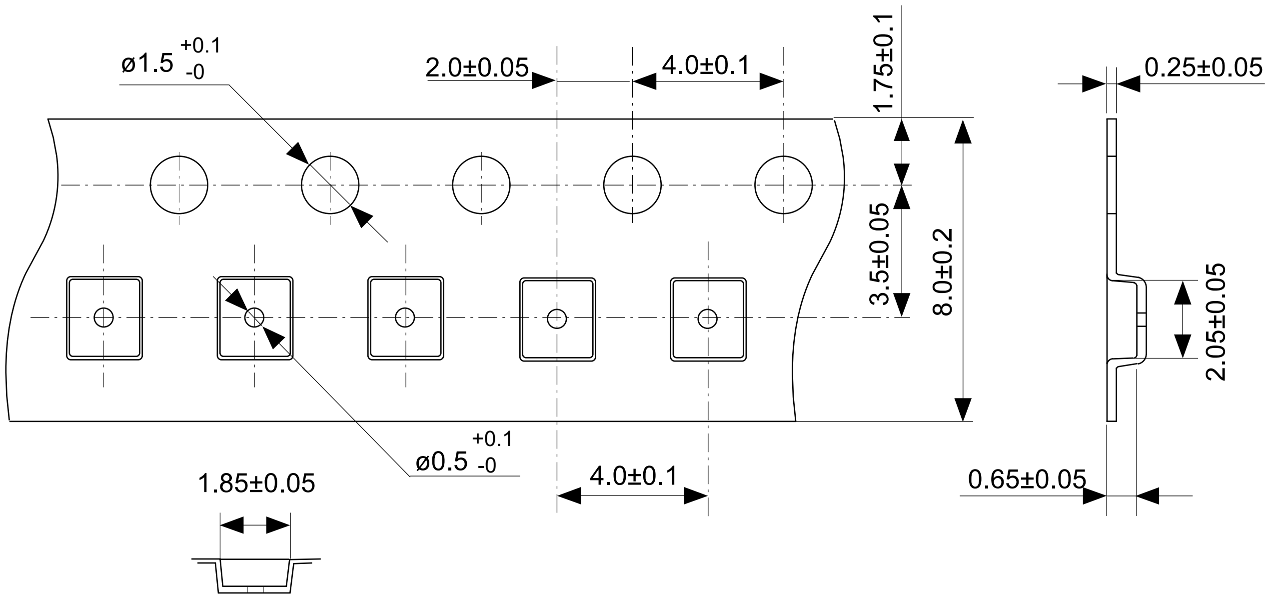
No. SNT6A-A-Board-SD-1.0

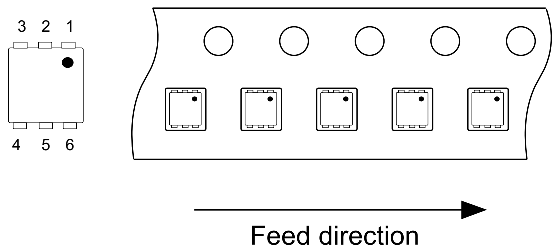


No. PG006-A-P-SD-2.1

TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm

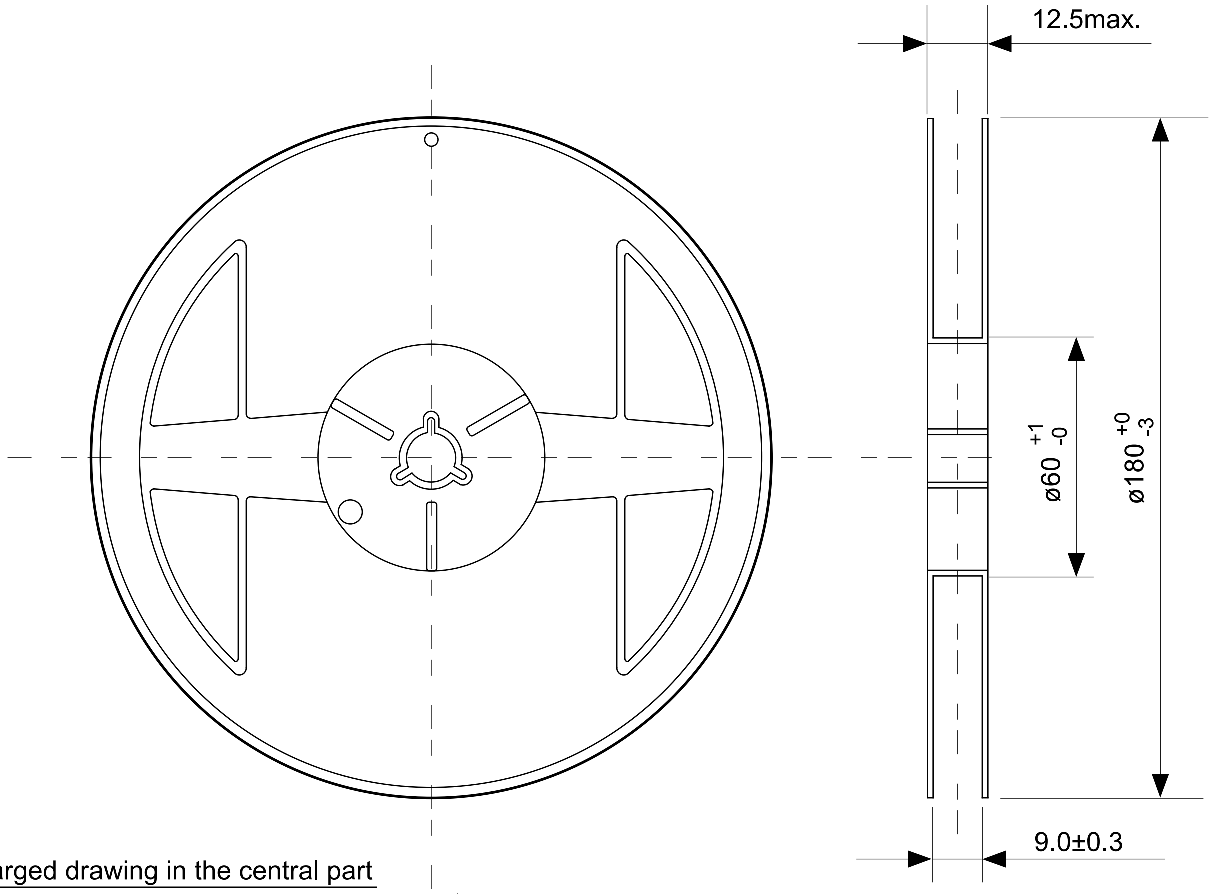
ABLIC Inc.



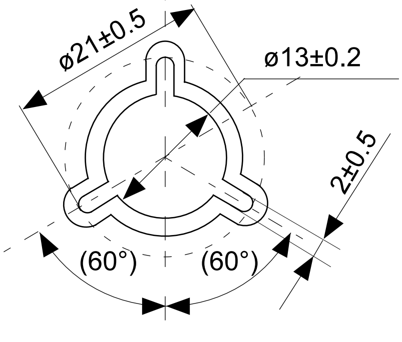


No. PG006-A-C-SD-2.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



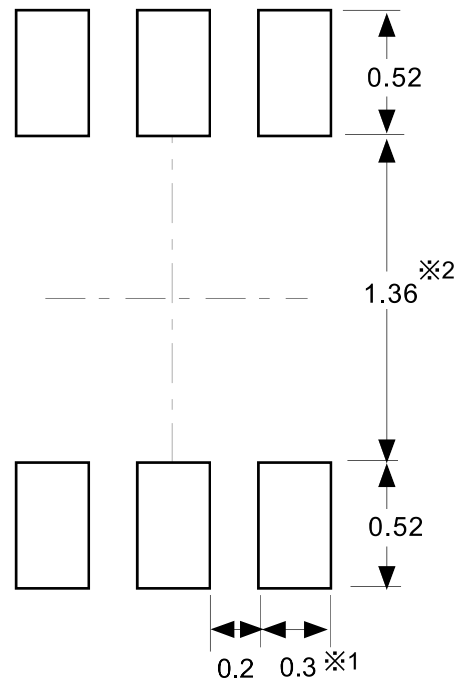
Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		

ABLIC Inc.



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

注意
1. **パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。**
2. **パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。**
3. **マスク開口サイズと開口位置はランドパターンと合わせてください。**
4. **詳細は〝SNTパッケージ活用の手引き〟を参照してください。**

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

Caution
1. **Do not do silkscreen printing and solder printing under the mold resin of the package.**
2. **The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.**
3. **Match the mask aperture size and aperture position with the land pattern.**
4. **Refer to "SNT Package User's Guide" for details.**

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

注意
1. **请勿在树脂型封装的下面印刷丝网、焊锡。**
2. **在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。**
3. **钢网的开口尺寸和开口位置请与焊盘模式对齐。**
4. **详细内容请参阅 "SNT 封装的应用指南"。**

No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm

ABLIC Inc.

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2.4-2019.07