The S-82B1B Series is a protection IC for lithium-ion / lithium polymer rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. It is suitable for protecting 1-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, and overcurrent. The S-82B1B Series has an input pin for power-saving signal (PS pin), allowing for reduction of current consumption by using an external signal to start the power-saving function.

This application note is a reference describing typical connection examples with notes on power-saving function as well as providing recommended circuit examples for using the S-82B1B Series.

Refer to the datasheet for details and specs of this IC.
Contents

1. Battery Protection IC Connection Example ................................................................. 3

2. S-82B1B Series Power-saving Function (PS pin control logic active “L”) ..................... 4
   2.1 S-82B1B Series power-saving function ................................................................. 4
   2.2 Notes and countermeasures for an actual application ............................................. 4

3. Recommended Circuit Examples for Large Load Capacitance Case .......................... 5
   3.1 Recommended circuit example 1 (PS pin control logic active “L”, internal resistor connection “pull-down”) .... 5
   3.2 Recommended circuit example 2 (PS pin control logic active “L”, internal resistor connection “pull-up”) ....... 6
   3.3 Recommended circuit example 3 (PS pin control logic active “H”, internal resistor connection “pull-down”) ..... 7
   3.4 Recommended circuit example 4 (PS pin control logic active “H”, internal resistor connection “pull-up”) .... 8

4. Notes on PS Pin Active Status .................................................................................. 9

5. Precautions ............................................................................................................. 10

6. Related Source ..................................................................................................... 10
1. Battery Protection IC Connection Example

![Battery Protection IC Connection Diagram]

Figure 1

<table>
<thead>
<tr>
<th>Table 1 Constants for External Components</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
</tr>
<tr>
<td>--------</td>
</tr>
<tr>
<td>FET1</td>
</tr>
<tr>
<td>FET2</td>
</tr>
<tr>
<td>R1</td>
</tr>
<tr>
<td>C1</td>
</tr>
<tr>
<td>R2</td>
</tr>
<tr>
<td>R3</td>
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</table>

*1. If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

*2. When setting $V_{DIOV1} \leq 30 \text{ mV}$, $V_{CIOV} \geq -30 \text{ mV}$ for power fluctuation protection, the condition of $R1 \times C1 \geq 100 \text{ μF} \times \Omega$ should be met.

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.
2. **S-82B1B Series Power-saving Function (PS pin control logic active "L")**

2.1 **S-82B1B Series power-saving function**

When the battery is in the normal status and the PS pin voltage drops below PS pin voltage "L" (V_{PSL}) and stays in that state for the power-saving delay time (t_{PS}) or longer, a discharge control FET is turned off and discharging is stopped. This status is called the discharge inhibition status. Under the discharge inhibition status, S-82B1B Series is internally shorted by the resistance between VDD pin and VM pin (R_{VMD}), and the VM pin is pulled up by R_{VMD} (1 MΩ typ.). When the VM pin voltage becomes V_{DD} − 0.8 V typ. or higher within the overdischarge detection delay time (t_{DL}) after the discharge control FET has been turned off, the IC transitions to the power-saving mode and this condition is latched. Current consumption drops to the level of current consumption during power-saving (IPS).

2.2 **Notes and countermeasures for an actual application**

In an actual application, capacitors (C_2, C_3) for ESD protection and noise countermeasures are usually added as shown in Figure 2. The capacitance components (C_2 and C_3) may delay the rise of the VM pin voltage, disable the power-saving function and may also cause oscillation as shown in Figure 3.

When the PS pin is active and this status continues for \( t_{PS} + t_{DL} \) or longer, the power-saving function is activated. However, when the VM pin voltage does not rise above \( V_{DD} - 0.8 \text{ V} \) within \( t_{DL} \), the IC starts to oscillate by repeatedly transitioning to and releasing the power-saving status.

As a countermeasure, a FET and a resistor can be connected beside the PS pin to ensure transition to the power-saving mode. When the load capacitance of peripheral circuits is large, refer to "3. Recommended Circuit Examples for Large Load Capacitance Case".

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**Figure 2**

**Figure 3**

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*1. (1): Normal status
   (2): Discharge inhibition status
3. Recommended Circuit Examples for Large Load Capacitance Case

3.1 Recommended circuit example 1 (PS pin control logic active "L", internal resistor connection "pull-down")

As shown in Figure 4, input of the "L" signal to the PS pin or setting it open will enable transitioning to the power-saving mode even with the presence of capacitance components.

Caution 1. Method for inputting the "L" signal to the PS pin is described below.
- Input negative potential for battery voltage with reference to VDD (EB+)
- Input the "L" signal directly from the VSS of the battery

2. Do not input signals to the PS pin with reference to EB−. If signals are input, FET1 is turned off during discharge inhibition, causing EB− to enter the floating status, resulting in the loss of the "L" level.
3.2 Recommended circuit example 2 (PS pin control logic active "L", internal resistor connection "pull-up")

As shown in Figure 5, input of the "L" signal to the PS pin will enable transitioning to the power-saving mode even with the presence of capacitance components. When the PS pin is open, it will stay in the normal status.

Caution 1. Method for inputting the "L" signal to the PS pin is described below.
- Input negative potential for battery voltage with reference to VDD (EB+)
- Input the "L" signal directly from the VSS of the battery

2. Do not input signals to the PS pin with reference to EB-. If signals are input, FET1 is turned off during discharge inhibition, causing EB- to enter the floating status, resulting in the loss of the "L" level.
3.3 Recommended circuit example 3 (PS pin control logic active "H", internal resistor connection "pull-down")

As shown in Figure 6, input of the "H" signal to the PS pin will enable transitioning to the power-saving mode even with the presence of capacitance components. When the PS pin is open, it will stay in the normal status.

![Circuit Diagram]

**Figure 6**

Caution 1. Input the "H" signal directly to the PS pin using VDD (EB+) as reference.

2. Do not input signals to the PS pin with reference to EB−. If signals are input, FET1 is turned off during discharge inhibition, causing EB− to enter the floating status, resulting in the loss of the "L" level.
3.4 Recommended circuit example 4 (PS pin control logic active "H", internal resistor connection "pull-up")

As shown in Figure 7, input of the "H" signal to the PS pin or setting it open will enable transitioning to the power-saving mode even with the presence of capacitance components. The PS pin must remain at "L" level to retain the normal status. Then current will flow through the pull-up resistor (R_{PS}) in the IC from V_{DD} (EB+) to the PS pin, causing a voltage drop in R1, resulting in a minor error in the battery voltage detection.

![Figure 7](image)

**Figure 7**

**Caution 1.** Method for inputting the "L" signal to the PS pin is described below.
- Input negative potential for battery voltage with reference to V_{DD} (EB+)
- Input the "L" signal directly from the V_{SS} of the battery

**2.** Do not input signals to the PS pin with reference to EB−. If signals are input, FET1 is turned off during discharge inhibition, causing EB− to enter the floating status, resulting in the loss of the "L" level.
4. Notes on PS Pin Active Status

Do not charge when the PS pin is in active status. If charging is performed in active status, the oscillations shown in Figure 8 will occur. The CO pin voltage may not reach "L", and overcharge voltage detection may not operate normally.

Take careful note of combination of the PS pin options, including the contents of "3. Recommended Circuit Example for Large Load Capacitance".

*1. (1): Normal status
   (2): Discharge inhibition status

Remark The charger is assumed to charge with a constant current.

Figure 8
5. Precautions

- The usage described in this application note is typical example with our IC. Perform evaluation fully before use.

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6. Related Source

Refer to the following datasheet for details of the S-82B1B Series.

S-82B1B Series Datasheet

The information described in this application note and the datasheet is subject to change without notice. Contact our sales representatives for details. Regarding the newest version, select product category and product name on our website, and download the PDF file.

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