

The S-8253C/D Series is a protection ICs for 2-series or 3-series cell lithium-ion rechargeable battery and includes high-accuracy voltage detector and delay circuit.

This IC is suitable for protecting lithium-ion battery packs from overcharge, overdischarge and overcurrent.

## ■ Features

- (1) High-accuracy voltage detection for each cell
  - Overcharge detection voltage n (n = 1 to 3)                      3.900 V to 4.400 V (50 mV step)                      Accuracy ±25 mV
  - Overcharge release voltage n (n = 1 to 3)                      3.800 V to 4.400 V<sup>\*1</sup>                      Accuracy ±50 mV
  - Overdischarge detection voltage n (n = 1 to 3)                      2.000 V to 3.000 V (100 mV step)                      Accuracy ±80 mV
  - Overdischarge release voltage n (n = 1 to 3)                      2.000 V to 3.400 V<sup>\*2</sup>                      Accuracy ±100 mV
- (2) Three-level overcurrent detection (Including load short circuiting detection)
  - Overcurrent detection voltage 1                      0.050 V to 0.300 V (50 mV step)                      Accuracy ±25 mV
  - Overcurrent detection voltage 2                      0.500 V (Fixed)
  - Overcurrent detection voltage 3                      1.200 V (Fixed)
- (3) Delay time (Overcharge, overdischarge, overcurrent) is available by only using an internal circuit. (External capacitors are unnecessary).
- (4) Charge / discharge operation can be inhibited by the control pin.
- (5) 0 V battery charge function available / unavailable is selectable.
- (6) High-withstand voltage                      Absolute maximum rating 26 V
- (7) Wide range of operating voltage                      2 V to 24 V
- (8) Wide range of operating temperature                      -40°C to +85°C
- (9) Low current consumption
  - During operation                      28 μA max. (+25°C)
  - During power-down                      0.1 μA max. (+25°C)
- (10) Lead-free, Sn100%, halogen-free<sup>\*3</sup>

\*1. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage  
(Overcharge hysteresis voltage n (n = 1 to 3) can be selected in 0 V, or in 0.1 V to 0.4 V in 50 mV step.)

\*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage  
(Overdischarge hysteresis voltage n (n = 1 to 3) can be selected in 0 V, or in 0.2 V to 0.7 V in 100 mV step.)

\*3. Refer to “**Product Name Structure**” for details.

## ■ Applications

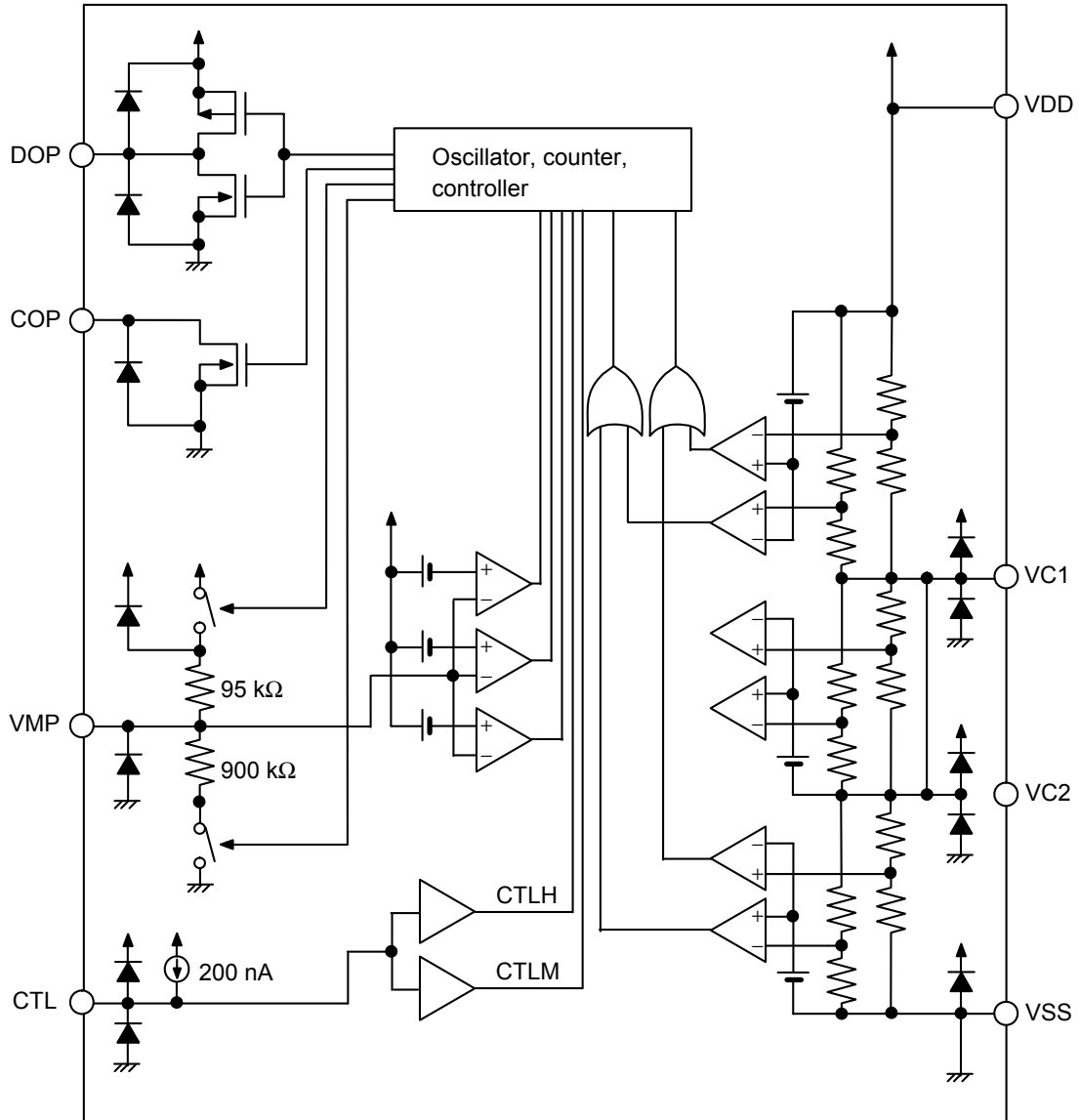
- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

## ■ Package

- 8-Pin TSSOP

■ **Block Diagrams**

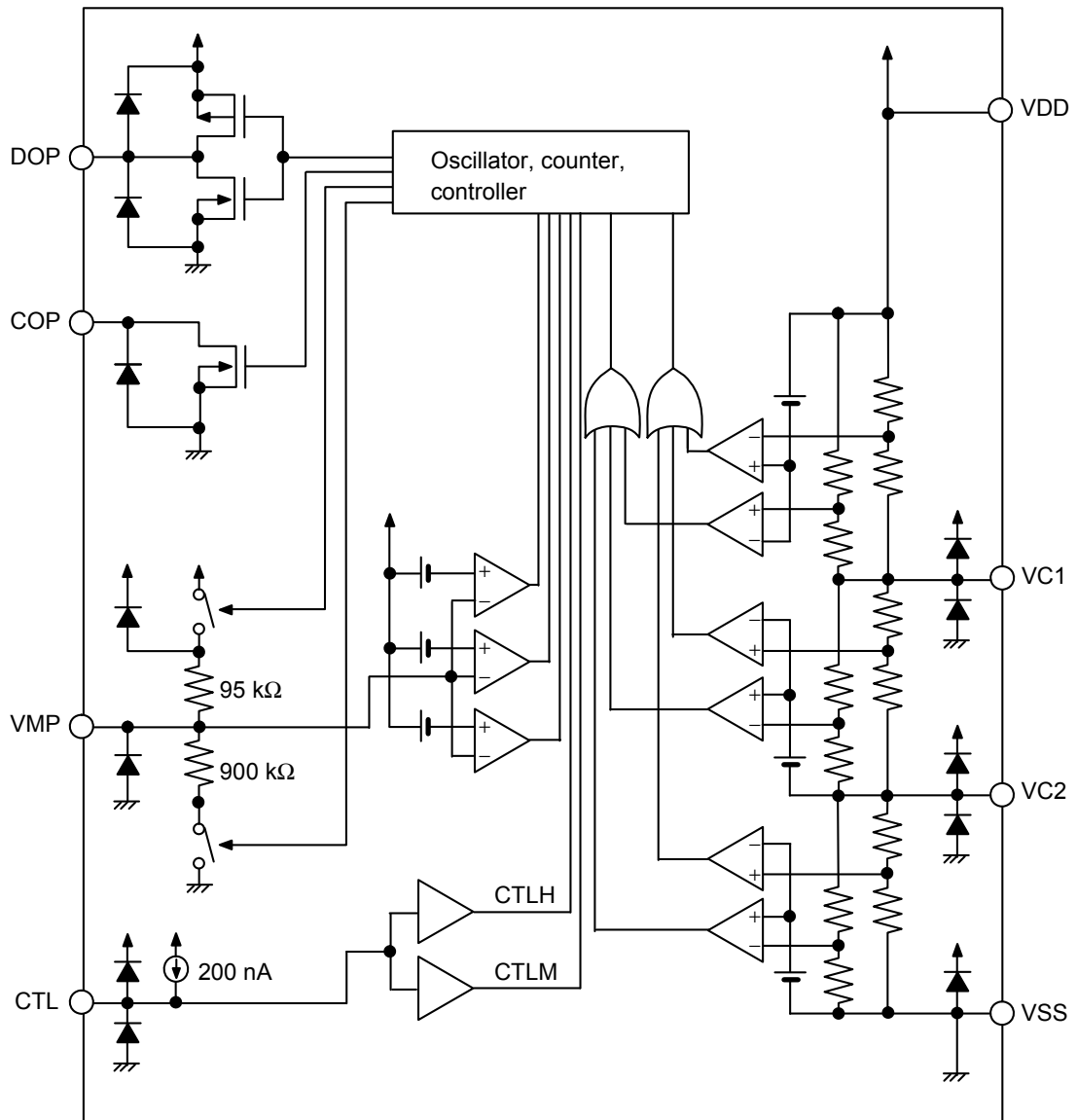
1. S-8253C Series



**Remark** All diodes shown in figure are parasitic diodes.

Figure 1

**2. S-8253D Series**



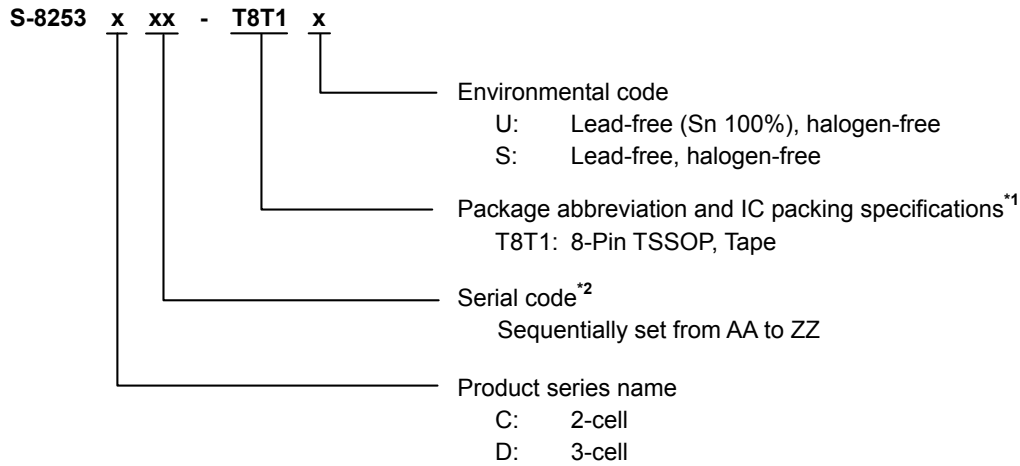
**Remark** All diodes shown in figure are parasitic diodes.

**Figure 2**

■ **Product Name Structure**

**1. Product Name**

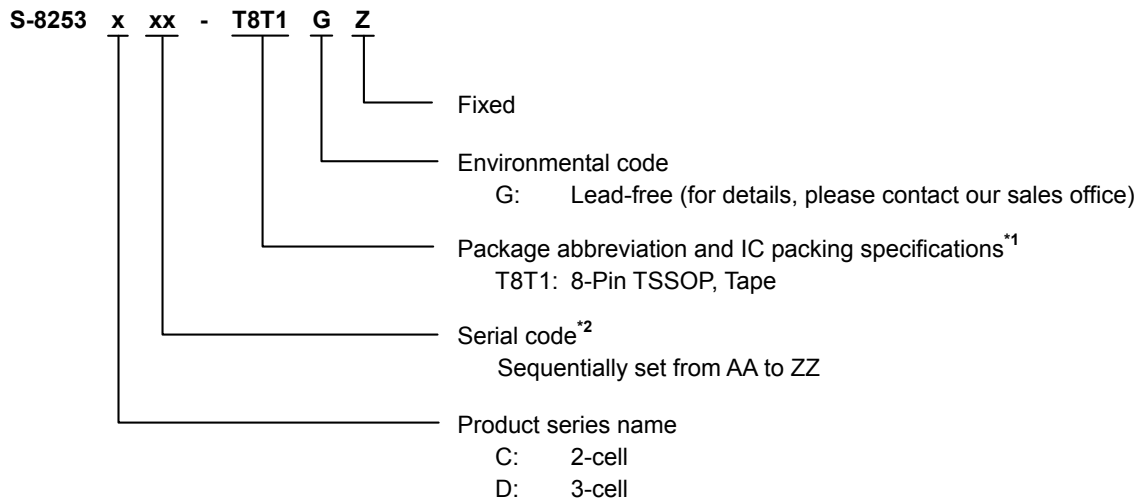
**1.1 Environmental code = U, S**



\*1. Refer to the tape drawing.

\*2. Refer to "3. Product Name List".

**1.2 Environmental code = G**



\*1. Refer to the tape drawing.

\*2. Refer to "3. Product Name List".

**2. Package**

Package Name		Drawing Code		
		Package	Tape	Reel
8-Pin TSSOP	Environmental code = G, S	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD
	Environmental code = U	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-S1

# BATTERY PROTECTION IC FOR 2-SERIES OR 3-SERIES-CELL PACK

## S-8253C/D Series

Rev.2.5\_00

### 3. Product Name List

**Table 1 S-8253C Series (For 2-Serial Cell)**

Model No.	Overcharge detection voltage [V <sub>CU</sub> ]	Overcharge release voltage [V <sub>CL</sub> ]	Overdischarge detection voltage [V <sub>DL</sub> ]	Overdischarge release voltage [V <sub>DU</sub> ]	Overcurrent detection voltage 1 [V <sub>IOV1</sub> ]	0 V battery charge function
S-8253CAA-T8T1□□	4.350 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.300 ± 0.025 V	Available
S-8253CAC-T8T1y	4.350 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.080 ± 0.025 V	Available
S-8253CAD-T8T1□□	4.250 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.120 ± 0.025 V	Available
S-8253CAH-T8T1□□	4.350 ± 0.025 V	4.150 ± 0.050 V	2.300 ± 0.080 V	2.300 ± 0.080 V	0.090 ± 0.025 V	Available
S-8253CAI-T8T1□□	4.250 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.200 ± 0.025 V	Available
S-8253CAJ-T8T1□□	4.250 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.120 ± 0.025 V	Available
S-8253CAK-T8T1□□	4.250 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.300 ± 0.025 V	Available
S-8253CAL-T8T1y	4.400 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.120 ± 0.025 V	Available
S-8253CAM-T8T1y	4.225 ± 0.025 V	4.025 ± 0.050 V	2.600 ± 0.080 V	2.900 ± 0.100 V	0.200 ± 0.025 V	Available
S-8253CAN-T8T1U	4.400 ± 0.025 V	4.100 ± 0.050 V	2.800 ± 0.080 V	3.000 ± 0.100 V	0.300 ± 0.025 V	Available
S-8253CAO-T8T1U	4.400 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.150 ± 0.025 V	Available
S-8253CAP-T8T1U	4.350 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.300 ± 0.025 V	Unavailable
S-8253CAQ-T8T1U	3.800 ± 0.025 V	3.700 ± 0.050 V	2.200 ± 0.080 V	2.400 ± 0.100 V	0.100 ± 0.025 V	Unavailable
S-8253CAR-T8T1U	4.450 ± 0.025 V	4.200 ± 0.050 V	2.800 ± 0.080 V	3.000 ± 0.100 V	0.120 ± 0.025 V	Available

**Remark 1.** □□: GZ or U

y: S or U

2. Please select products of environmental code = U for Sn 100%, halogen-free products.

**Table 2 S-8253D Series (For 3-Series Cell)**

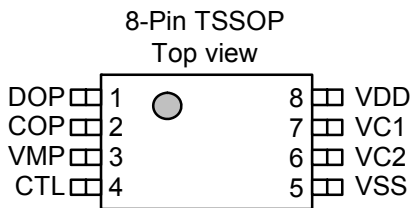
Model No.	Overcharge detection voltage [V <sub>CU</sub> ]	Overcharge release voltage [V <sub>CL</sub> ]	Overdischarge detection voltage [V <sub>DL</sub> ]	Overdischarge release voltage [V <sub>DU</sub> ]	Overcurrent detection voltage 1 [V <sub>IOV1</sub> ]	0 V battery charge function
S-8253DAA-T8T1□□	4.350 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.300 ± 0.025 V	Available
S-8253DAB-T8T1□□	4.300 ± 0.025 V	4.050 ± 0.050 V	2.700 ± 0.080 V	3.000 ± 0.100 V	0.200 ± 0.025 V	Unavailable
S-8253DAD-T8T1y	4.250 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.120 ± 0.025 V	Available
S-8253DAI-T8T1□□	4.350 ± 0.025 V	4.150 ± 0.050 V	2.200 ± 0.080 V	2.400 ± 0.100 V	0.160 ± 0.025 V	Available
S-8253DAK-T8T1y	4.350 ± 0.025 V	4.050 ± 0.050 V	2.400 ± 0.080 V	2.700 ± 0.100 V	0.300 ± 0.025 V	Available
S-8253DAL-T8T1U	4.250 ± 0.025 V	4.050 ± 0.050 V	2.600 ± 0.080 V	2.900 ± 0.100 V	0.120 ± 0.025 V	Available
S-8253DAM-T8T1U	3.800 ± 0.025 V	3.700 ± 0.050 V	2.200 ± 0.080 V	2.400 ± 0.100 V	0.100 ± 0.025 V	Unavailable
S-8253DAN-T8T1U	4.250 ± 0.025 V	4.050 ± 0.050 V	2.600 ± 0.080 V	2.900 ± 0.100 V	0.150 ± 0.025 V	Available

**Remark 1.** □□: GZ or U

y: S or U

2. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ **Pin Configuration**



**Figure 3**

**Table 3 S-8253C Series**

Pin No.	Symbol	Description
1	DOP	Connection pin for discharge control FET gate (CMOS output)
2	COP	Connection pin for charge control FET gate (Nch open-drain output)
3	VMP	Pin for voltage detection between VDD and VMP (Detection pin for overcurrent)
4	CTL	Input pin for charge / discharge control signal, Pin for shortening test time ( L : Normal operation, H : inhibit charge / discharge M ( $V_{DD} \times 1 / 2$ ) : shorten test time)
5	VSS	Input pin for negative power supply, Connection pin for negative voltage of battery 2
6	VC2	No connection *1
7	VC1	Connection pin for negative voltage of battery 1, for positive voltage of battery 2
8	VDD	Input pin for positive power supply, Connection pin for positive voltage of battery 1

**Table 4 S-8253D Series**

Pin No.	Symbol	Description
1	DOP	Connection pin for discharge control FET gate (CMOS output)
2	COP	Connection pin for charge control FET gate (Nch open-drain output)
3	VMP	Pin for voltage detection between VDD and VMP (Detection pin for overcurrent)
4	CTL	Input pin for charge / discharge control signal, pin for shortening test time ( L : Normal operation, H : inhibit charge / discharge, M ( $V_{DD} \times 1 / 2$ ) : shorten test time)
5	VSS	Input pin for negative power supply, Connection pin for negative voltage of battery 3
6	VC2	Connection pin for negative voltage of battery 2, for positive voltage of battery 3
7	VC1	Connection pin for negative voltage of battery 1, for positive voltage of battery 2
8	VDD	Input pin for positive power supply, Connection pin for positive voltage of battery 1

\*1. No connection is electrically open. This pin can be connected to VDD or VSS.

■ **Absolute Maximum Ratings**

**Table 5**

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applicable Pin	Absolute Maximum Rating	Unit
Input voltage between VDD and VSS	V <sub>DS</sub>	—	V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 26	V
Input pin voltage	V <sub>IN</sub>	VC1, VC2	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
VMP pin input voltage	V <sub>VMP</sub>	VMP	V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 26	V
DOP pin output voltage	V <sub>DOP</sub>	DOP	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
COP pin output voltage	V <sub>COP</sub>	COP	V <sub>SS</sub> - 0.3 to V <sub>VMP</sub> + 0.3	V
CTL pin input voltage	V <sub>IN,CTL</sub>	CTL	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
Power dissipation	P <sub>D</sub>	—	300 (When not mounted on board)	mW
			700 <sup>*1</sup>	mW
Operating ambient temperature	T <sub>opr</sub>	—	- 40 to + 85	°C
Storage temperature	T <sub>stg</sub>	—	- 40 to + 125	°C

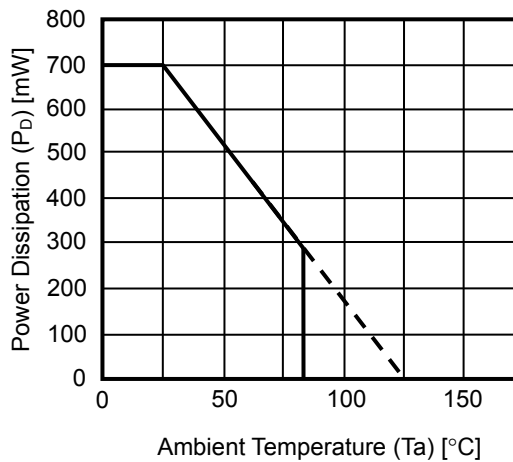
\*1. When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



**Figure 4 Power Dissipation of Package (When Mounted on Board)**

■ **Electrical Characteristics**

1. **Characteristics Other Than Detection Delay Time**

**Table 6 (1 / 2)**

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test condition	Test circuit	
<b>DETECTION VOLTAGE</b>									
Overcharge detection voltage n	$V_{CU_n}$	3.900 V to 4.400 V, Adjustable	$V_{CU_n}$ -0.025	$V_{CU_n}$	$V_{CU_n}$ +0.025	V	1	1	
Overcharge release voltage n	$V_{CL_n}$	3.800 V to 4.400 V, Adjustable	$V_{CL} \neq V_{CU}$	$V_{CL_n}$ -0.050	$V_{CL_n}$	$V_{CL_n}$ +0.050	V	1	1
			$V_{CL} = V_{CU}$	$V_{CL_n}$ -0.025	$V_{CL_n}$	$V_{CL_n}$ +0.025	V	1	1
Overdischarge detection voltage n	$V_{DL_n}$	2.000 V to 3.000 V, Adjustable	$V_{DL_n}$ -0.080	$V_{DL_n}$	$V_{DL_n}$ +0.080	V	1	1	
Overdischarge release voltage n	$V_{DU_n}$	2.000 V to 3.400 V, Adjustable	$V_{DL} \neq V_{DU}$	$V_{DU_n}$ -0.100	$V_{DU_n}$	$V_{DU_n}$ +0.100	V	1	1
			$V_{DL} = V_{DU}$	$V_{DU_n}$ -0.080	$V_{DU_n}$	$V_{DU_n}$ +0.080	V	1	1
Overcurrent detection voltage 1	$V_{IOV1}$	0.050 V to 0.300 V, Adjustable Based on $V_{DD}$	$V_{IOV1}$ -0.025	$V_{IOV1}$	$V_{IOV1}$ +0.025	V	2	1	
Overcurrent detection voltage 2	$V_{IOV2}$	Based on $V_{DD}$	0.400	0.500	0.600	V	2	1	
Overcurrent detection voltage 3	$V_{IOV3}$	Based on $V_{DD}$	0.900	1.200	1.500	V	2	1	
Temperature coefficient 1 <sup>*1</sup>	$T_{COE1}$	Ta = 0°C to 50°C <sup>*3</sup>	-1.0	0	1.0	mV / °C	—	—	
Temperature coefficient 2 <sup>*2</sup>	$T_{COE2}$	Ta = 0°C to 50°C <sup>*3</sup>	-0.5	0	0.5	mV / °C	—	—	
<b>0 V BATTERY CHARGE FUNCTION</b>									
0 V battery charge starting charger voltage	$V_{0CHA}$	0 V battery charging; available	—	0.8	1.5	V	12	5	
0 V battery charge inhibition battery voltage	$V_{0INH}$	0 V battery charging; unavailable	0.4	0.7	1.1	V	12	5	
<b>INTERNAL RESISTANCE</b>									
Resistance between VMP and VDD	$R_{VMD}$	$V1 = V2 = V3^{*4} = 3.5 V, V_{VMP} = V_{SS}$	70	95	120	kΩ	6	2	
Resistance between VMP and VSS	$R_{VMS}$	$V1 = V2 = V3^{*4} = 1.8 V, V_{VMP} = V_{DD}$	450	900	1800	kΩ	6	2	



**BATTERY PROTECTION IC FOR 2-SERIES OR 3-SERIES-CELL PACK**  
**S-8253C/D Series**

Rev.2.5\_00

**Table 6 (2 / 2)**

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test condition	Test circuit
<b>INPUT VOLTAGE</b>								
Operating voltage between VDD and VSS	V <sub>DSOP</sub>	Output voltage of DOP and COP fixed	2	—	24	V	—	—
CTL input voltage "H"	V <sub>CTLH</sub>	—	V <sub>DD</sub> -0.5	—	—	V	7	1
CTL input voltage "L"	V <sub>CTLL</sub>	—	—	—	V <sub>SS</sub> +0.5	V	7	1
<b>INPUT CURRENT</b>								
Current consumption during operation	I <sub>OPE</sub>	V1 = V2 = V3 <sup>*4</sup> = 3.5 V	—	14	28	μA	5	2
Current consumption during power-down	I <sub>PDN</sub>	V1 = V2 = V3 <sup>*4</sup> = 1.5 V	—	—	0.1	μA	5	2
VC1 pin current	I <sub>VC1</sub>	V1 = V2 = V3 <sup>*4</sup> = 3.5 V	-0.3	0	0.3	μA	9	3
VC2 pin current	I <sub>VC2</sub>	V1 = V2 = V3 <sup>*4</sup> = 3.5 V	-0.3	0	0.3	μA	9	3
CTL pin current "H"	I <sub>CTLH</sub>	V1 = V2 = V3 <sup>*4</sup> = 3.5 V, V <sub>CTL1</sub> = V <sub>DD</sub>	—	—	0.1	μA	8	3
CTL pin current "L"	I <sub>CTLL</sub>	V1 = V2 = V3 <sup>*4</sup> = 3.5 V, V <sub>CTL1</sub> = V <sub>SS</sub>	-0.4	-0.2	—	μA	8	3
<b>OUTPUT CURRENT</b>								
COP pin leakage current	I <sub>COH</sub>	V <sub>COP</sub> = 24 V	—	—	0.1	μA	10	4
COP pin sink current	I <sub>COL</sub>	V <sub>COP</sub> = V <sub>SS</sub> + 0.5 V	10	—	—	μA	10	4
DOP pin source current	I <sub>DOH</sub>	V <sub>DOP</sub> = V <sub>DD</sub> - 0.5 V	10	—	—	μA	11	4
DOP pin sink current	I <sub>DOL</sub>	V <sub>DOP</sub> = V <sub>SS</sub> + 0.5 V	10	—	—	μA	11	4

\*1. Voltage temperature coefficient 1 : Overcharge detection voltage

\*2. Voltage temperature coefficient 2 : Overcurrent detection voltage 1

\*3. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

\*4. The S-8253C Series does not have V3 because this IC is for 2-series cell battery protection.

**2. Detection Delay Time**

- (1) **S-8253CAA, S-8253CAC, S-8253CAD, S-8253CAI, S-8253CAJ, S-8253CAK, S-8253CAL, S-8253CAM, S-8253CAN, S-8253CAO, S-8253CAP, S-8253CAQ, S-8253CAR, S-8253DAA, S-8253DAB, S-8253DAD, S-8253DAK, S-8253DAL, S-8253DAM, S-8253DAN**

**Table 7**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
<b>DELAY TIME (Ta = 25°C)</b>								
Overcharge detection delay time	t <sub>CU</sub>	—	0.92	1.15	1.38	s	3	1
Overdischarge detection delay time	t <sub>DL</sub>	—	115	144	173	ms	3	1
Overcurrent detection delay time 1	t <sub>IOV1</sub>	—	7.2	9	10.8	ms	4	1
Overcurrent detection delay time 2	t <sub>IOV2</sub>	—	3.6	4.5	5.4	ms	4	1
Overcurrent detection delay time 3	t <sub>IOV3</sub>	—	220	300	380	μs	4	1

- (2) **S-8253DAI**

**Table 8**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
<b>DELAY TIME (Ta = 25°C)</b>								
Overcharge detection delay time	t <sub>CU</sub>	—	0.92	1.15	1.38	s	3	1
Overdischarge detection delay time	t <sub>DL</sub>	—	115	144	173	ms	3	1
Overcurrent detection delay time 1	t <sub>IOV1</sub>	—	3.6	4.5	5.4	ms	4	1
Overcurrent detection delay time 2	t <sub>IOV2</sub>	—	0.89	1.1	1.4	ms	4	1
Overcurrent detection delay time 3	t <sub>IOV3</sub>	—	220	300	380	μs	4	1

- (3) **S-8253CAH**

**Table 9**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
<b>DELAY TIME (Ta = 25°C)</b>								
Overcharge detection delay time	t <sub>CU</sub>	—	0.92	1.15	1.38	s	3	1
Overdischarge detection delay time	t <sub>DL</sub>	—	115	144	173	ms	3	1
Overcurrent detection delay time 1	t <sub>IOV1</sub>	—	14.5	18	22	ms	4	1
Overcurrent detection delay time 2	t <sub>IOV2</sub>	—	3.6	4.5	5.4	ms	4	1
Overcurrent detection delay time 3	t <sub>IOV3</sub>	—	220	300	380	μs	4	1

## ■ Test Circuits

### 1. Overcharge Detection Voltage 1, Overcharge Release Voltage 1, Overdischarge Detection Voltage 1, Overdischarge Release Voltage 1 (Test Condition 1, Test Circuit 1)

Confirm that  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series),  $V4 = 0\text{ V}$ ,  $V5 = 0\text{ V}$ , and the COP and DOP pins are "L" ( $V_{DD} \times 0.1\text{ V}$  or lower) (this status is referred to as the initial status).

#### 1.1 Overcharge Detection Voltage 1 ( $V_{CU1}$ ), Overcharge Release Voltage 1 ( $V_{CL1}$ )

Overcharge detection voltage 1 ( $V_{CU1}$ ) is the voltage of V1 when the voltage of the COP pin is "H" ( $V_{DD} \times 0.9\text{ V}$  or more) after the V1 voltage has been gradually increased starting at the initial status. Overcharge release voltage 1 ( $V_{CL1}$ ) is the voltage of V1 when the voltage at the COP pin is low after the V1 voltage has been gradually decreased.

#### 1.2 Overdischarge Detection Voltage 1 ( $V_{DL1}$ ), Overdischarge Release Voltage 1 ( $V_{DU1}$ )

Overdischarge detection voltage 1 ( $V_{DL1}$ ) is the voltage of V1 when the voltage of the DOP pin is high after the V1 voltage has been gradually decreased starting at the initial status. Overdischarge release voltage 1 ( $V_{DU1}$ ) is the voltage of V1 when the voltage at the DOP pin is low after the V1 voltage has been gradually increased.

By changing  $V_n$  ( $n = 2$ : S-8253C Series,  $n = 2$ ,  $3$ : S-8253D Series) the overcharge detection voltage ( $V_{CU_n}$ ), overcharge release voltage ( $V_{CL_n}$ ), overdischarge detection voltage ( $V_{DL_n}$ ), and overdischarge release voltage ( $V_{DU_n}$ ) can be measured in the same way as when  $n = 1$ .

### 2. Overcurrent Detection Voltage 1, Overcurrent Detection Voltage 2, Overcurrent Detection Voltage 3 (Test Condition 2, Test Circuit 1)

Confirm that  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series),  $V4 = 0\text{ V}$ ,  $V5 = 0\text{ V}$ , and the COP pin and DOP pin are low (this status is referred to as the initial status).

#### 2.1 Overcurrent Detection Voltage 1 ( $V_{IOV1}$ )

Overcurrent detection voltage 1 ( $V_{IOV1}$ ) is the voltage of V5 when the voltages of the COP pin and DOP pin are high after the V5 voltage has been gradually increased starting at the initial status.

#### 2.2 Overcurrent Detection Voltage 2 ( $V_{IOV2}$ )

Overcurrent detection voltage 2 ( $V_{IOV2}$ ) is a voltage at V5 when; by increasing a voltage at V5 instantaneously (within  $10\text{ }\mu\text{s}$ ) from the initial state, the voltages of the COP and DOP pin are set to "H", and its delay time is in the range of minimum to maximum value of overcurrent detection delay time 2 ( $t_{IOV2}$ ).

#### 2.3 Overcurrent Detection Voltage 3 ( $V_{IOV3}$ )

Overcurrent detection voltage 3 ( $V_{IOV3}$ ) is a voltage at V5 when; by increasing a voltage at V5 instantaneously (within  $10\text{ }\mu\text{s}$ ) from the initial state, the voltages of the COP and DOP pin are set to "H", and its delay time is in the range of minimum to maximum value of overcurrent detection delay time 3 ( $t_{IOV3}$ ).

**3. Overcharge Detection Delay Time, Overdischarge Detection Delay Time  
(Test Condition 3, Test Circuit 1)**

Confirm that  $V1 = V2 = 3.5\text{ V}$  (in S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (in S-8253D Series),  $V4 = 0\text{ V}$ ,  $V5 = 0\text{ V}$ , and the COP pin and DOP pin are low (this status is referred to as the initial status).

**3.1 Overcharge Detection Delay Time ( $t_{CU}$ )**

The overcharge detection delay time ( $t_{CU}$ ) is the time it takes for the voltage of the COP pin to change from low to high after the voltage of V1 is instantaneously changed from overcharge detection voltage 1 ( $V_{CU1} - 0.2\text{ V}$ ) to overcharge detection voltage 1 ( $V_{CU1} + 0.2\text{ V}$ ) (within  $10\text{ }\mu\text{s}$ ) starting at the initial status.

**3.2 Overdischarge Detection Delay Time ( $t_{DL}$ )**

The overdischarge detection delay time ( $t_{DL}$ ) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V1 is instantaneously changed from overdischarge detection voltage 1 ( $V_{DL1} + 0.2\text{ V}$ ) to overdischarge detection voltage 1 ( $V_{DL1} - 0.2\text{ V}$ ) (within  $10\text{ }\mu\text{s}$ ) starting at the initial status.

**4. Overcurrent Detection Delay Time 1, Overcurrent Detection Delay Time 2, Overcurrent Detection  
Delay Time 3  
(Test Condition 4, Test Circuit 1)**

Confirm that  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series),  $V4 = 0\text{ V}$ ,  $V5 = 0\text{ V}$ , and the COP pin and DOP pin are low (this status is referred to as the initial status).

**4.1 Overcurrent Detection Delay Time 1 ( $t_{OV1}$ )**

Overcurrent detection delay time 1 ( $t_{OV1}$ ) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V5 is instantaneously changed to  $0.35\text{ V}$  (within  $10\text{ }\mu\text{s}$ ) starting at the initial status.

**4.2 Overcurrent Detection Delay Time 2 ( $t_{OV2}$ )**

Overcurrent detection delay time 2 ( $t_{OV2}$ ) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V5 is instantaneously changed to  $0.7\text{ V}$  (within  $10\text{ }\mu\text{s}$ ) starting at the initial status.

**4.3 Overcurrent Detection Delay Time 3 ( $t_{OV3}$ )**

Overcurrent detection delay time 3 ( $t_{OV3}$ ) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V5 is instantaneously changed to  $1.6\text{ V}$  (within  $10\text{ }\mu\text{s}$ ) starting at the initial status.

**5. Current Consumption during Operation, Current Consumption during Power-down  
(Test Condition 5, Test Circuit 2)**

**5.1 Current Consumption during Operation ( $I_{OPE}$ )**

The current consumption during operation ( $I_{OPE}$ ) is the current of the VSS pin ( $I_{SS}$ ) when  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series),  $S1 = \text{ON}$ , and  $S2 = \text{OFF}$ .

**5.2 Current Consumption during Power-down ( $I_{PDN}$ )**

The current consumption during power-down ( $I_{PDN}$ ) is the current of the VSS pin ( $I_{SS}$ ) when  $V1 = V2 = 1.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 1.5\text{ V}$  (S-8253D Series),  $S1 = \text{OFF}$ , and  $S2 = \text{ON}$ .

**6. Resistance between VMP and VDD, Resistance between VMP and VSS  
 (Test Condition 6, Test Circuit 2)**

Confirm that  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series),  $S1 = \text{ON}$ , and  $S2 = \text{OFF}$  (this status is referred to as the initial status).

**6.1 Resistance between VMP and VDD ( $R_{VMD}$ )**

The resistance between VMP and VDD ( $R_{VMD}$ ) is determined based on the current of the VMP pin ( $I_{VMD}$ ) after  $S1$  and  $S2$  are switched to OFF and ON, respectively, starting at the initial status.

S-8253C Series :  $R_{VMD} = (V1 + V2) / I_{VMD}$

S-8253D Series :  $R_{VMD} = (V1 + V2 + V3) / I_{VMD}$

**6.2 Resistance between VMP and VSS ( $R_{VMS}$ )**

The resistance between VMP and VSS ( $R_{VMS}$ ) is determined based on the current of the VMP pin ( $I_{VMS}$ ) after  $V1 = V2 = 1.8\text{ V}$  (S-8253C Series) or  $V1 = V2 = V3 = 1.8\text{ V}$  (S-8253D Series) are set starting at the initial status.

S-8253C Series :  $R_{VMS} = (V1 + V2) / I_{VMS}$

S-8253D Series :  $R_{VMS} = (V1 + V2 + V3) / I_{VMS}$

**7. CTL Pin Input Voltage “H”  
 (Test Condition 7, Test Circuit 1)**

Confirm that  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series),  $V4 = 0\text{ V}$ ,  $V5 = 0\text{ V}$ , and the COP pin and DOP pin are low (this status is referred to as the initial status).

**7.1 CTL Pin Input Voltage “H” ( $V_{CTLH}$ )**

The CTL pin input voltage “H” ( $V_{CTLH}$ ) is the voltage of  $V4$  when the voltages of the COP pin and DOP pin are high after the voltage of  $V4$  has been gradually increased starting at the initial status.

**8. CTL Pin Input Voltage “L”  
 (Test condition 7, Test circuit 1)**

Confirm that  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series),  $V4 = 0\text{ V}$ ,  $V5 = 0.35\text{ V}$ , and the COP pin and DOP pin are high (this status is referred to as the initial status).

**8.1 CTL Pin Input Voltage “L” ( $V_{CTL L}$ )**

The CTL pin input voltage “L” ( $V_{CTL L}$ ) is the voltage of  $V4$  when the voltages of the COP pin and DOP pin are low after the voltage of  $V4$  has been gradually increased starting at the initial status.

**9. CTL Pin Current “H”, CTL Pin Current “L”  
 (Test Condition 8, Test Circuit 3)**

**9.1 CTL Pin Current “H” ( $I_{CTLH}$ ), CTL Pin Current “L” ( $I_{CTL L}$ )**

The CTL pin current “H” ( $I_{CTLH}$ ) is the current that flows through the CTL pin when  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series), and  $S3 = \text{ON}$ ,  $S4 = \text{OFF}$ . The CTL pin current “L” ( $I_{CTL L}$ ) is the current that flows through the CTL pin when  $S3 = \text{OFF}$  and  $S4 = \text{ON}$  after that.

**10. VC1 Pin Current, VC2 Pin Current**  
**(Test Condition 9, Test Circuit 3)**

**10.1 VC1 Pin Current ( $I_{VC1}$ ), VC2 Pin Current ( $I_{VC2}$ )**

The VC1 pin current ( $I_{VC1}$ ) is the current that flows through the VC1 pin when  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series), and  $S3 = \text{OFF}$ ,  $S4 = \text{ON}$ . Similarly, the VC2 pin current ( $I_{VC2}$ ) is the current that flows through the VC2 pin under these conditions (S-8253D Series only).

**11. COP Pin Leakage Current, COP Pin Sink Current**  
**(Test Condition 10, Test Circuit 4)**

**11.1 COP Pin Leakage Current ( $I_{COH}$ )**

The COP pin leakage current ( $I_{COH}$ ) is the current that flows through the COP pin when  $V1 = V2 = 12\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 8\text{ V}$  (S-8253D Series),  $S6 = S7 = S8 = \text{OFF}$ , and  $S5 = \text{ON}$ .

**11.2 COP Pin Sink Current ( $I_{COL}$ )**

The COP pin sink current ( $I_{COL}$ ) is the current that flows through the COP pin when  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series),  $V6 = 0.5\text{ V}$ ,  $S5 = S7 = S8 = \text{OFF}$ , and  $S6 = \text{ON}$ .

**12. DOP Pin Source Current, DOP Pin Sink Current**  
**(Test Condition 11, Test Circuit 4)**

**12.1 DOP Pin Source Current ( $I_{DOH}$ )**

The DOP pin source current ( $I_{DOH}$ ) is the current that flows through the DOP pin when  $V1 = V2 = 1.8\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 1.8\text{ V}$  (S-8253D Series),  $V7 = 0.5\text{ V}$ ,  $S5 = S6 = S8 = \text{OFF}$ , and  $S7 = \text{ON}$ .

**12.2 DOP Pin Sink Current ( $I_{DOL}$ )**

The DOP pin sink current ( $I_{DOL}$ ) is the current that flows through the DOP pin when  $V1 = V2 = 3.5\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 3.5\text{ V}$  (S-8253D Series),  $V8 = 0.5\text{ V}$ ,  $S5 = S6 = S7 = \text{OFF}$ , and  $S8 = \text{ON}$ .

**13. 0 V Battery Charge Starting Charger Voltage (Product with 0 V Battery Charge Function),**  
**0 V Battery Charge Inhibition Battery Voltage (Product with 0 V Battery Charge Inhibition Function)**  
**(Test Condition 12, Test Circuit 5)**

**13.1 0 V Battery Charge Starting Charger Voltage ( $V_{0CHA}$ ) (Product with 0 V Battery Charge Function)**

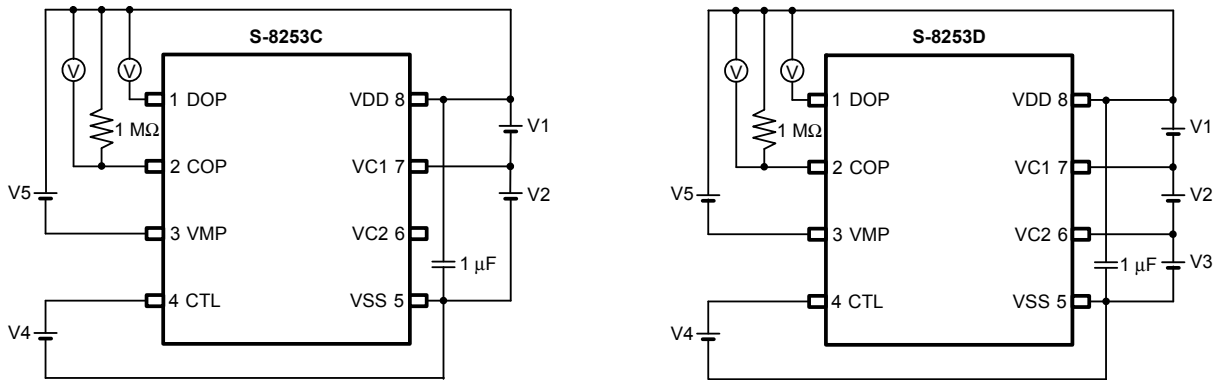
The COP pin voltage should be lower than  $V_{0CHA}\text{ max.} - 1\text{ V}$  when  $V1 = V2 = 0\text{ V}$  (S-8253C Series),  $V1 = V2 = V3 = 0\text{ V}$  (S-8253D Series), and  $V9 = V_{VMP} = V_{0CHA}\text{ max.}$

**13.2 0 V Battery Charge Inhibition Battery Voltage ( $V_{0INH}$ ) (Product with 0 V Battery Charge Inhibition Function)**

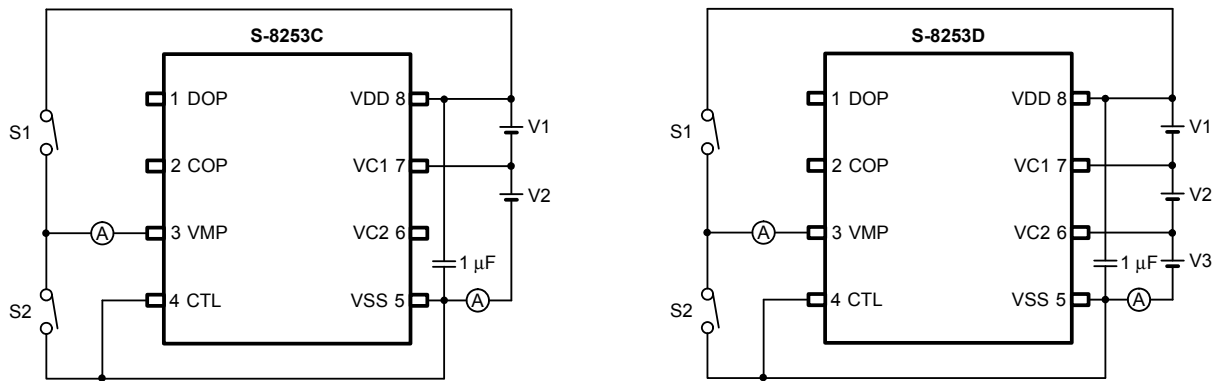
The COP pin voltage should be higher than  $V_{VMP} - 1\text{ V}$  when  $V1 = V2 = V_{0INH}\text{ min.}$  (S-8253C Series),  $V1 = V2 = V3 = V_{0INH}\text{ min.}$  (S-8253D Series), and  $V9 = V_{VMP} = 24\text{ V}$ .

**BATTERY PROTECTION IC FOR 2-SERIES OR 3-SERIES-CELL PACK**  
**S-8253C/D Series**

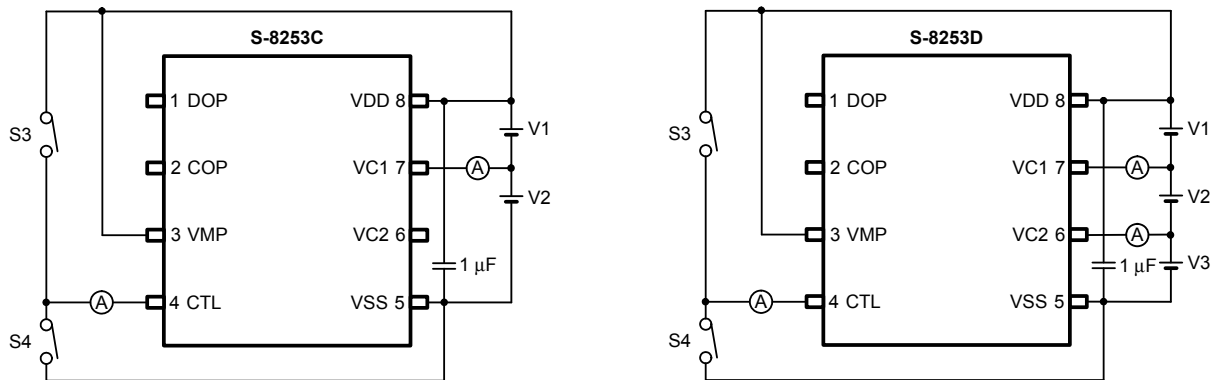
Rev.2.5\_00



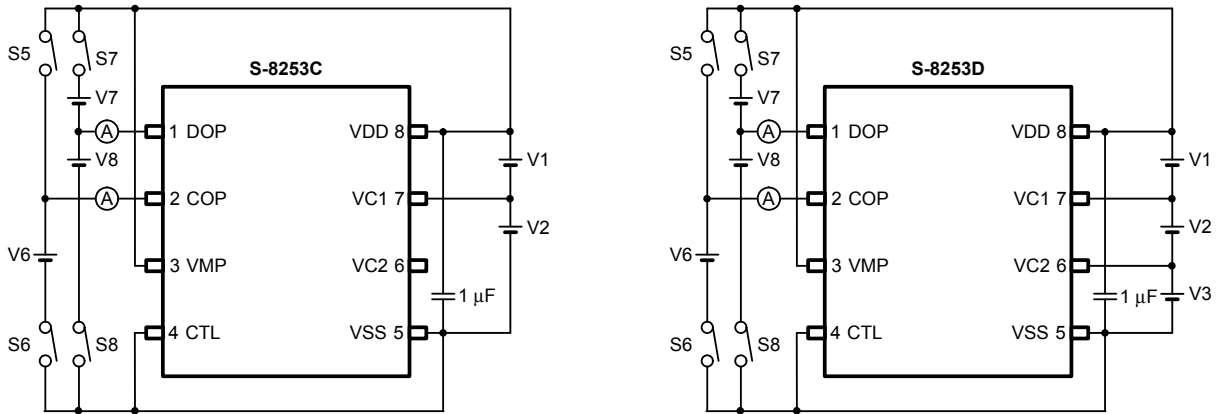
**Figure 5 Test Circuit 1**



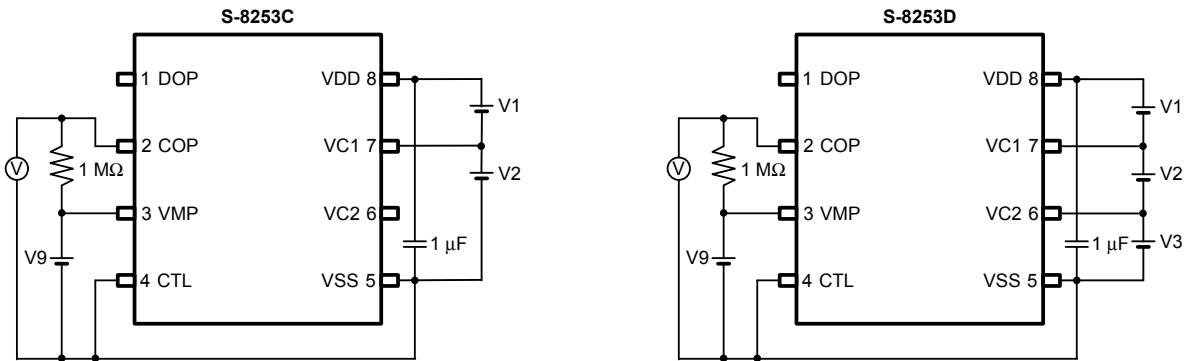
**Figure 6 Test Circuit 2**



**Figure 7 Test Circuit 3**



**Figure 8 Test Circuit 4**



**Figure 9 Test Circuit 5**



## ■ Operation

**Remark** Refer to “ ■ Battery Protection IC Connection Example”.

### 1. Normal Status

When the voltage of each of the batteries is in the range from  $V_{DLn}$  to  $V_{CUn}$  and the discharge current is lower than the specified value (the VMP pin voltage is higher than  $V_{DD} - V_{IOV1}$ ), the charging and discharging FETs are turned on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.

**Caution** When the battery is connected for the first time, discharging may not be enabled. In this case, short the VMP pin and VDD pin or connect the charger to restore the normal status.

### 2. Overcharge Status

When the voltage of one of the batteries becomes higher than  $V_{CUn}$  and the state continues for  $t_{CU}$  or longer, the COP pin becomes high impedance. Because the COP pin is pulled up to the EB+ pin voltage by an external resistor, the charging FET is turned off to stop charging. This is called the overcharge status. The overcharge status is released when one of the following two conditions holds.

- (1) The voltage of each of the batteries becomes  $V_{CLn}$  or lower.
- (2) The voltage of each of the batteries is  $V_{CUn}$  or lower, and the VMP pin voltage is  $V_{DD} - V_{IOV1}$  or lower (since the discharge current flows through the body diode of the charging FET immediately after discharging is started when the charger is removed and a load is connected, the VMP pin voltage momentarily decreases by approximately 0.6 V from the VDD pin voltage. The IC detects this voltage and releases the overcharging status).

### 3. Overdischarge Status

When the voltage of one of the batteries becomes lower than  $V_{DLn}$  and the state continues for  $t_{DL}$  or longer, the DOP pin voltage becomes  $V_{DD}$  level, and the discharging FET is turned off to stop discharging. This is called the overdischarge status.

#### 3.1 Power-down Function

When the overdischarge status is reached, the VMP pin is pulled down to the  $V_{SS}$  level by the internal  $R_{VMS}$  resistor of the IC. When the VMP pin voltage is 0.8 V typ. or lower, the power-down function starts to operate and almost every circuit in the S-8253C/D Series stops working. The conditions of each output pin are as follows.

- (1) COP pin : High-Z
- (2) DOP pin :  $V_{DD}$

The power-down function is released when the following condition holds.

- (1) The VMP pin voltage is 0.8 V typ. or higher.

The overdischarge status is released when the following two conditions hold.

- (1) In case the VMP pin voltage is 0.8 V typ. or higher and the VMP pin voltage is lower than  $V_{DD}$ , the overdischarge status is released when the voltage of each of the batteries is  $V_{DU_n}$  or higher.
- (2) In case the VMP pin voltage is 0.8 V typ. or higher and the VMP pin voltage is  $V_{DD}$  or higher, the overdischarge status is released when the voltage of each of the batteries is  $V_{DLn}$  or higher (when a charger is connected and the VMP pin voltage is  $V_{DD}$  or higher, overdischarge hysteresis is released and discharge control FET is turned on at  $V_{DLn}$ ).

#### 4. Overcurrent Status

The S-8253C/D Series has three overcurrent detection levels ( $V_{IOV1}$ ,  $V_{IOV2}$ , and  $V_{IOV3}$ ) and three overcurrent detection delay times ( $t_{IOV1}$ ,  $t_{IOV2}$ , and  $t_{IOV3}$ ) corresponding to each overcurrent detection level. When the discharging current becomes higher than the specified value (the difference of the voltages of the VMP pin and VDD pin is greater than  $V_{IOV1}$ ) and the state continues for  $t_{IOV1}$  or longer, the S-8253C/D Series enters the overcurrent status, in which the DOP pin voltage becomes  $V_{DD}$  level to turn off the discharging FET to stop discharging, the COP pin becomes high impedance and is pulled up to the EB+ pin voltage to turn off the charging FET to stop charging, and the VMP pin is pulled up to the  $V_{DD}$  voltage by the internal resistor ( $R_{VMD}$ ). Operation of overcurrent detection levels 2, 3 ( $V_{IOV2}$ ,  $V_{IOV3}$ ) and overcurrent detection delay times 2, 3 ( $t_{IOV2}$ ,  $t_{IOV3}$ ) are the same as for  $V_{IOV1}$  and  $t_{IOV1}$ . The overcurrent status is released when the following condition holds.

- (1) The VMP pin voltage is  $V_{DD} - V_{IOV1}$  or higher because a charger is connected or the load is released.

**Caution** The impedance that enables automatic restoration varies depending on the battery voltage and set value of overcurrent detection voltage 1.

#### 5. 0 V Battery Charge Function

Regarding the charging of a self-discharged battery (0 V battery), the S-8253C/D Series has two functions from which one should be selected.

- (1) 0 V battery charging is allowed (0 V battery charging is available.)  
When the charger voltage is higher than  $V_{0CHA}$ , the 0 V battery can be charged.
- (2) 0 V battery charging is inhibited (0 V battery charging is unavailable.)  
When the battery voltage is  $V_{0INH}$  or lower, the 0 V battery cannot be charged.

**Caution** When the VDD pin voltage is lower than the minimum value of  $V_{DSOP}$ , the operation of the S-8253C/D Series is not guaranteed.

## 6. Delay Circuit

The following detection delay times are determined by dividing a clock of approximately 3.57 kHz by the counter.

(Example)	Oscillator clock cycle ( $T_{CLK}$ ) :	280 $\mu$ s
	Overcharge detection delay time ( $t_{CU}$ ) :	1.15 s
	Overdischarge detection delay time ( $t_{DL}$ ) :	144 ms
	Overcurrent detection delay time 1 ( $t_{IOV1}$ ) :	9 ms
	Overcurrent detection delay time 2 ( $t_{IOV2}$ ) :	4.5 ms

**Remark** The overcurrent detection delay time 2 ( $t_{IOV2}$ ) and overcurrent detection delay time 3 ( $t_{IOV3}$ ) start when the overcurrent detection voltage 1 ( $V_{IOV1}$ ) is detected. As soon as the overcurrent detection voltage 2 ( $V_{IOV2}$ ) or overcurrent detection voltage 3 ( $V_{IOV3}$ ) is detected over the detection delay time for overcurrent 2 ( $t_{IOV2}$ ) or overcurrent 3 ( $t_{IOV3}$ ) after the detection of overcurrent 1 ( $V_{IOV1}$ ), the S-8253C/D Series turns the discharging control FET off within  $t_{IOV2}$  or  $t_{IOV3}$  of each detection.

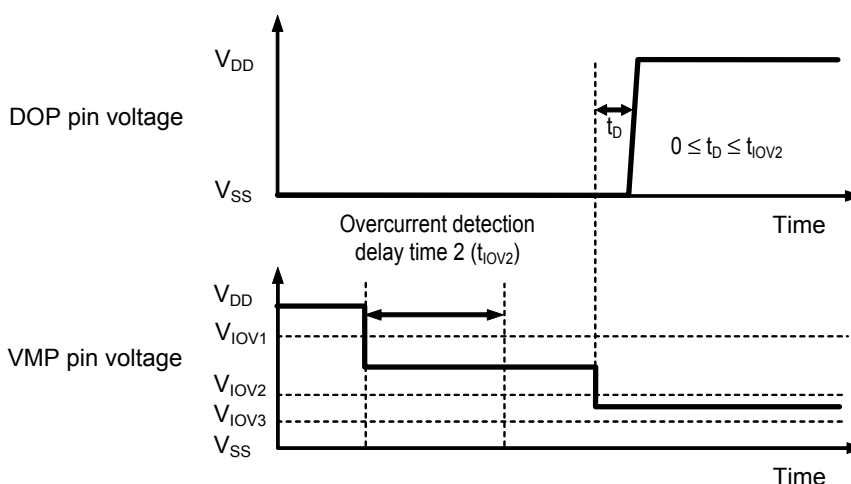


Figure 10

## 7. CTL Pin

The S-8253C/D Series has a control pin for charge / discharge control and shortening test time. The levels, “L”, “H”, and “M”, of the voltage input to the CTL pin determine the status of the S-8253C/D Series: normal operation, charge / discharge inhibition, or test time reduction. The CTL pin takes precedence over the battery protection circuit. During normal use, short the CTL pin and VSS pin.

Table 10 Conditions Set by CTL Pin

CTL Pin Potential	Status of IC	COP Pin	DOP Pin
Open	Charge / discharge inhibited status	High-Z	V <sub>DD</sub>
High ( $V_{CTL} \geq V_{CTLH}$ )	Charge / discharge inhibited status	High-Z	V <sub>DD</sub>
Middle ( $V_{CTLL} < V_{CTL} < V_{CTLH}$ )	Status to shorten delay time *1	(*)	(*)
Low ( $V_{CTLL} \geq V_{CTL}$ )	Normal status	(*)	(*)

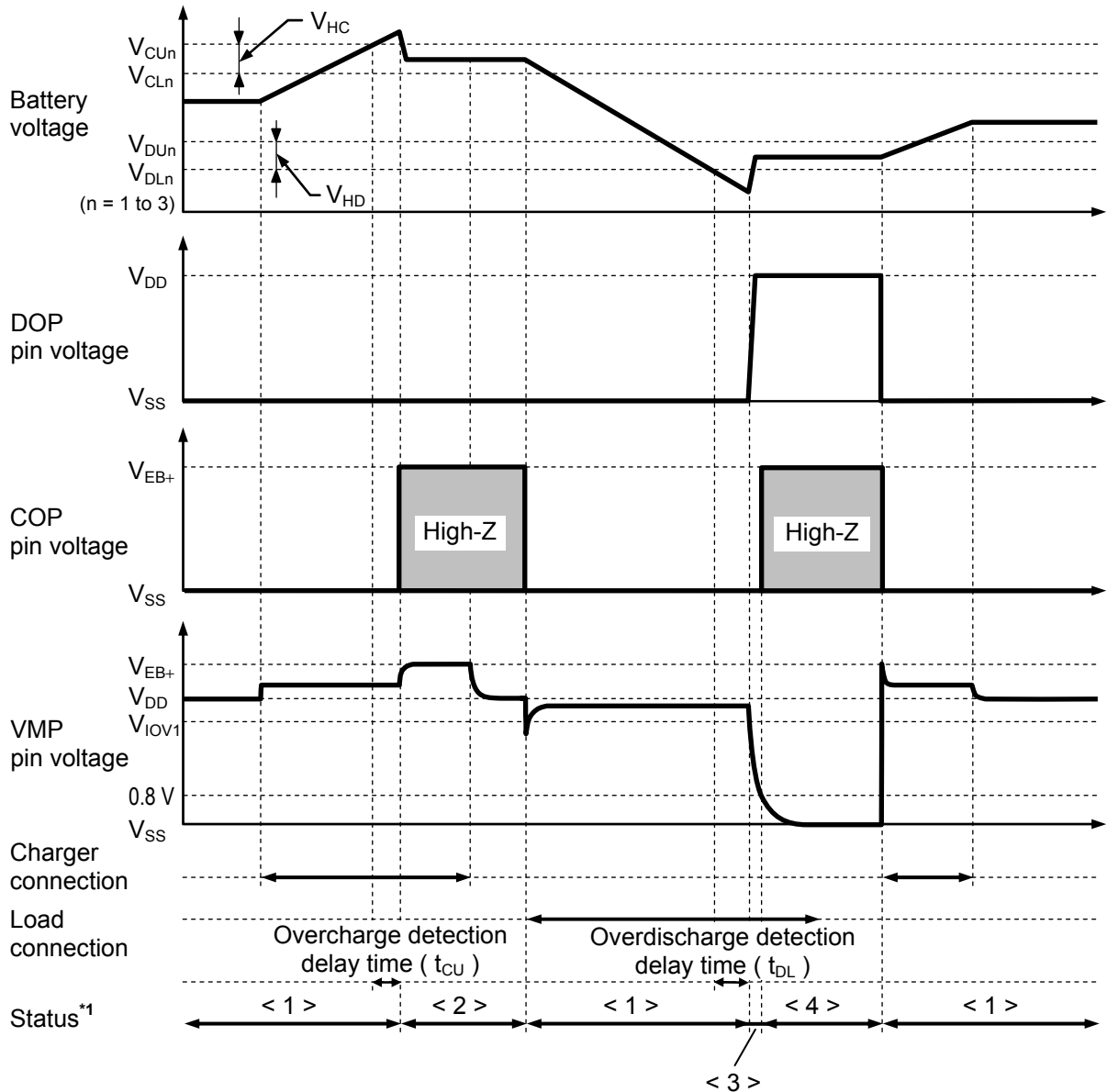
\*1. In this status that delay time is shortened, only the overcharge detection delay time is shortened in 1/60 to 1/30.

\*2. The pin status is controlled by the voltage detection circuit.

- Caution**
1. If the potential of the CTL pin is middle, overcurrent detection voltage 1 ( $V_{IOV1}$ ) does not operate.
  2. If you use the middle potential of the CTL pin, contact ABLIC Inc. marketing department.
  3. Please note unexpected behavior might occur when electrical potential difference between the CTL pin (“L” level) and VSS is generated through the external filter ( $R_{VSS}$  and  $C_{VSS}$ ) as a result of input voltage fluctuations.

■ **Timing Charts**

**1. Overcharge Detection and Overdischarge Detection**

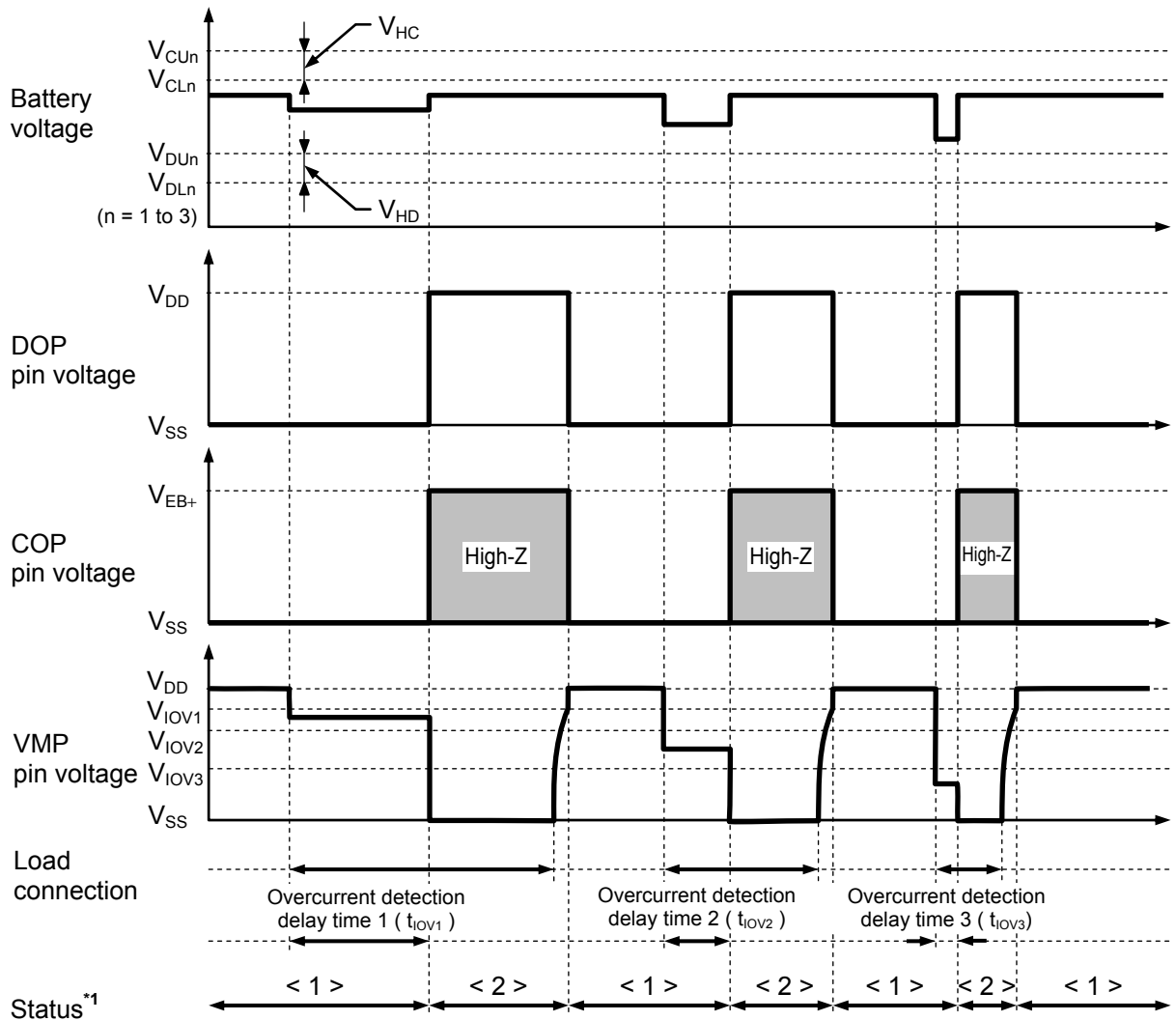


- \*1. < 1 > : Normal status
- < 2 > : Overcharge status
- < 3 > : Overdischarge status
- < 4 > : Power-down status

**Remark** The charger is assumed to charge with a constant current.  $V_{EB+}$  indicates the open voltage of the charger.

Figure 11

2. Overcurrent Detection



\*1.  $\langle 1 \rangle$  : Normal status  
 $\langle 2 \rangle$  : Overcurrent status

**Remark** The charger is assumed to charge with a constant current.  $V_{EB+}$  indicates the open voltage of the charger.

Figure 12

■ **Battery Protection IC Connection Examples**

1. **S-8253C Series**

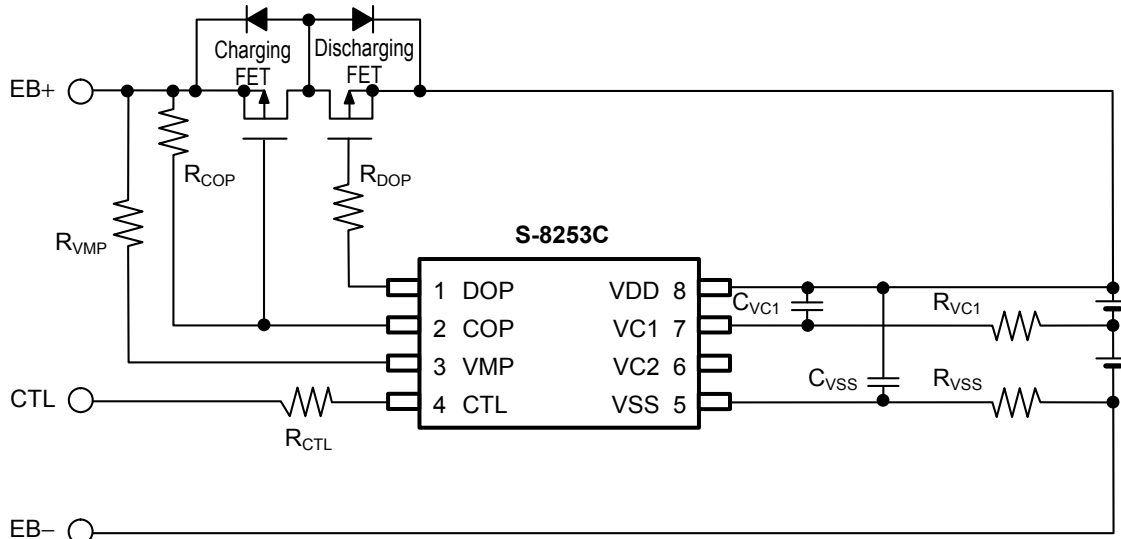


Figure 13

2. **S-8253D Series**

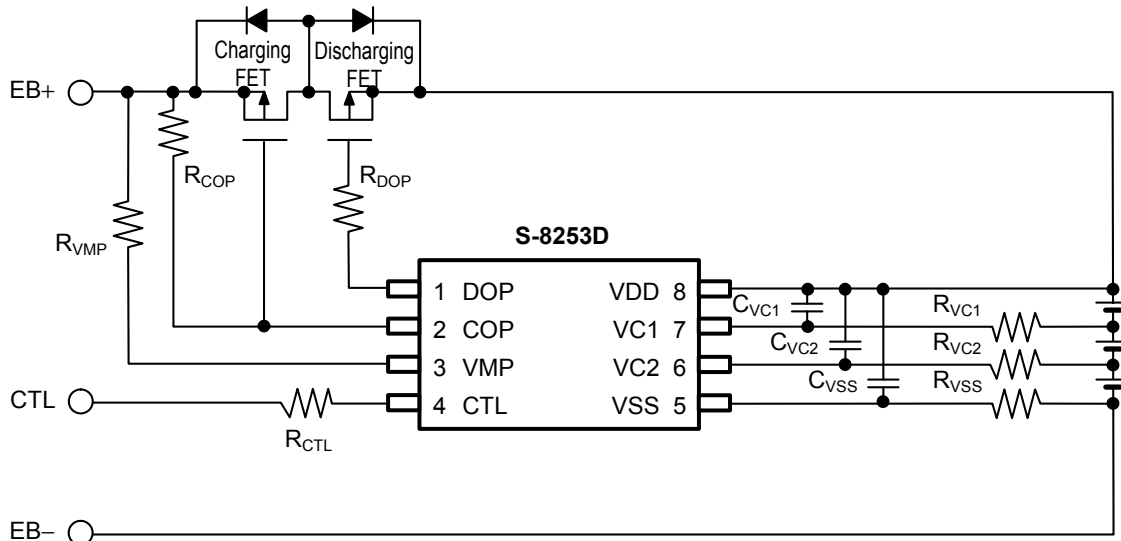


Figure 14

**Table 11 Constants for External Components**

No.	Symbol	Typ.	Range	Unit
1	R <sub>VC1</sub>	1	0.51 to 1 <sup>*1</sup>	kΩ
2	R <sub>VC2</sub>	1	0.51 to 1 <sup>*1</sup>	kΩ
3	R <sub>DOP</sub>	5.1	2 to 10	kΩ
4	R <sub>COP</sub>	1	0.1 to 1	MΩ
5	R <sub>VMP</sub>	5.1	1 to 10	kΩ
6	R <sub>CTL</sub>	1	1 to 100	kΩ
7	R <sub>VSS</sub>	51	5.1 to 51 <sup>*1</sup>	Ω
8	C <sub>VC1</sub>	0.1	0.1 to 0.47 <sup>*1</sup>	μF
9	C <sub>VC2</sub>	0.1	0.1 to 0.47 <sup>*1</sup>	μF
10	C <sub>VSS</sub>	2.2	1 to 10 <sup>*1</sup>	μF

\*1. Please set up a filter constant to be  $R_{VSS} \times C_{VSS} \geq 51 \mu\text{F} \cdot \Omega$  and to be  
 $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VSS} \times C_{VSS}$ .

**Caution 1.** The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

■ **Precautions**

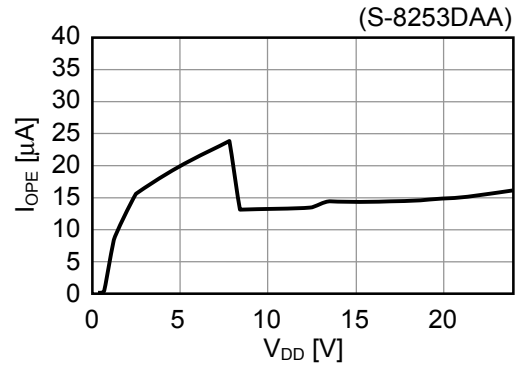
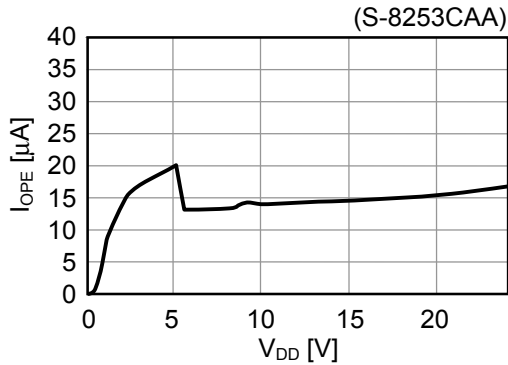
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order, however, there may be cases when discharging cannot be performed when a battery is connected. In this case, short the VMP pin and VDD pin or connect the battery charger to return to the normal mode.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.



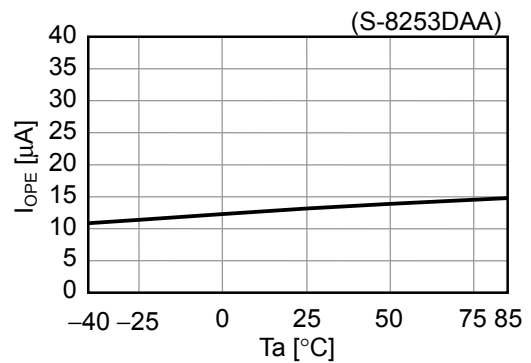
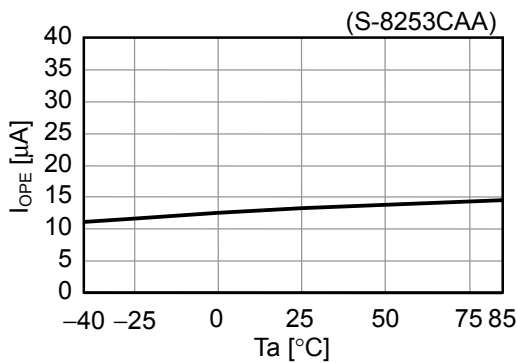
■ Characteristics (Typical Data)

1. Current Consumption

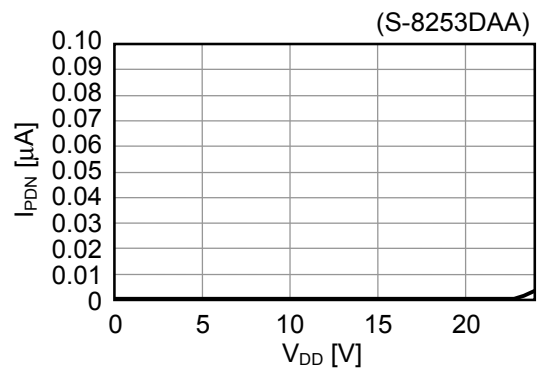
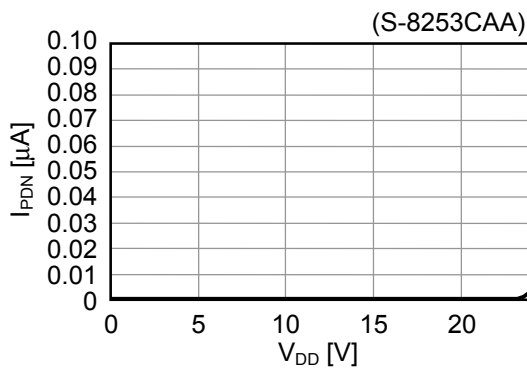
1.1  $I_{OPE}$  vs.  $V_{DD}$



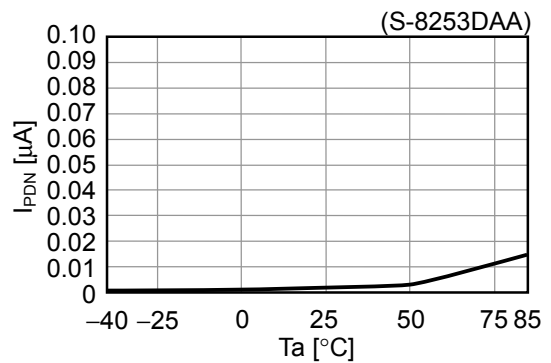
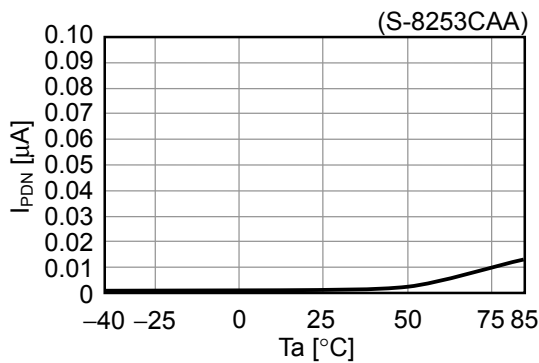
1.2  $I_{OPE}$  vs.  $T_a$



1.3  $I_{PDN}$  vs.  $V_{DD}$

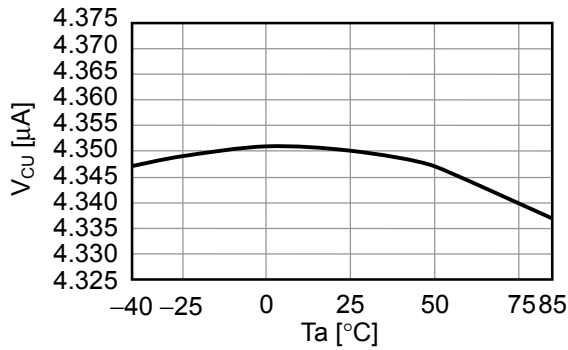


1.4  $I_{PDN}$  vs.  $T_a$

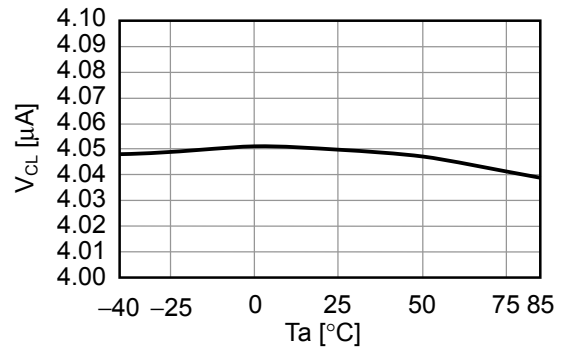


**2. Overcharge Detection / Release Voltage, Overdischarge Detection / Release Voltage, Overcurrent Detection Voltage, and Delay Times (S-8253CAA, S-8253DAA)**

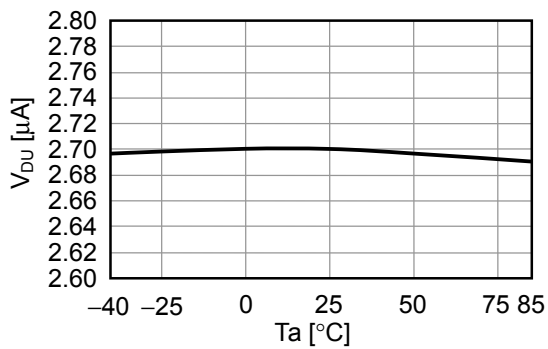
**2.1  $V_{CU}$  vs.  $T_a$**



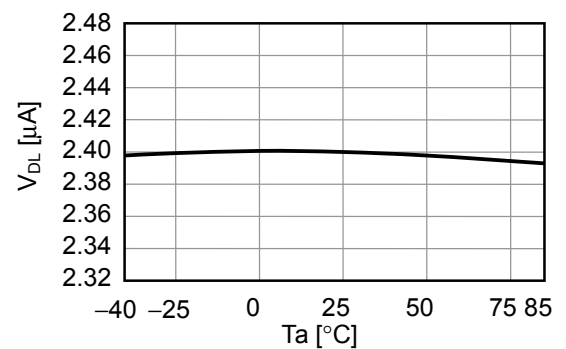
**2.2  $V_{CL}$  vs.  $T_a$**



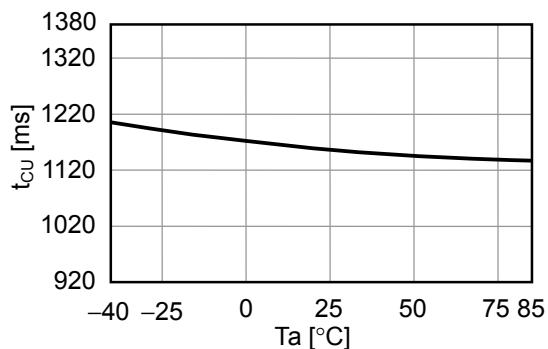
**2.3  $V_{DU}$  vs.  $T_a$**



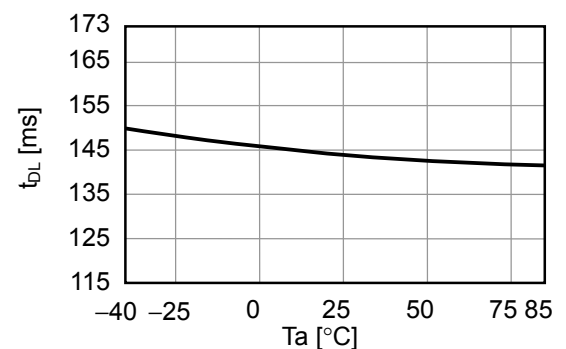
**2.4  $V_{DL}$  vs.  $T_a$**



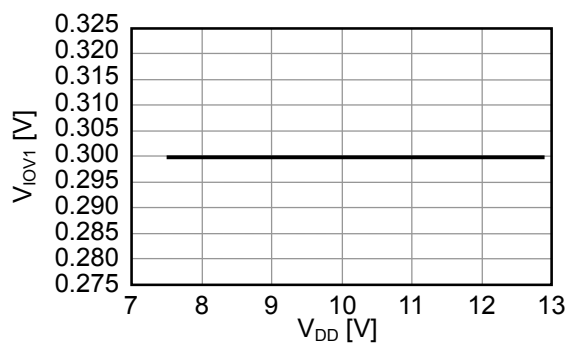
**2.5  $t_{CU}$  vs.  $T_a$**



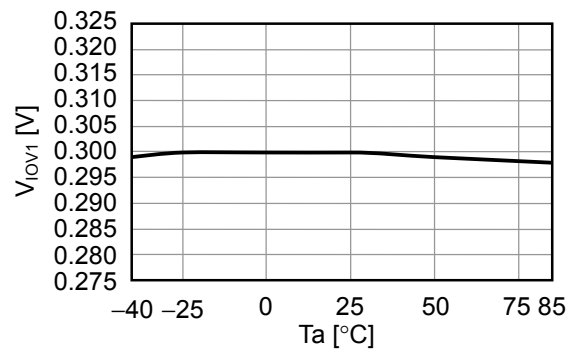
**2.6  $t_{DL}$  vs.  $T_a$**



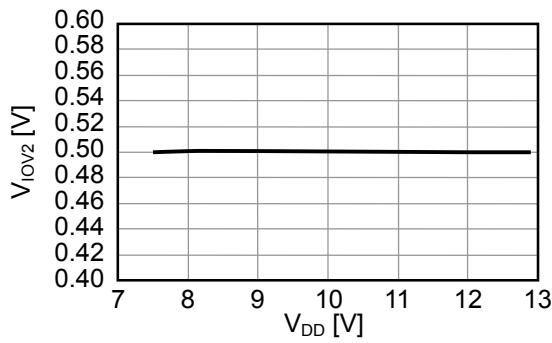
**2.7  $V_{IOV1}$  vs.  $V_{DD}$**



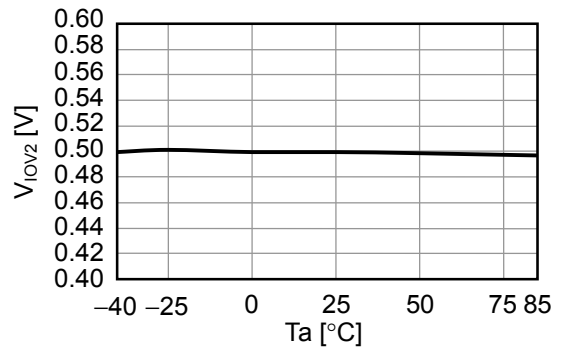
**2.8  $V_{IOV1}$  vs.  $T_a$**



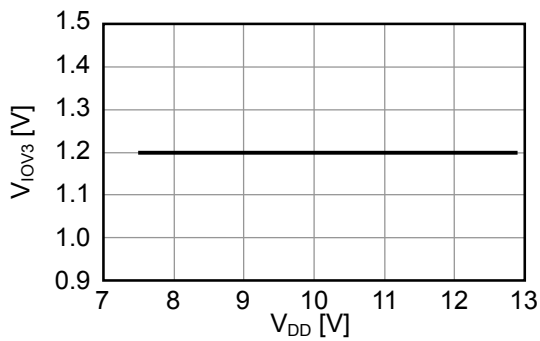
**2. 9  $V_{IOV2}$  vs.  $V_{DD}$**



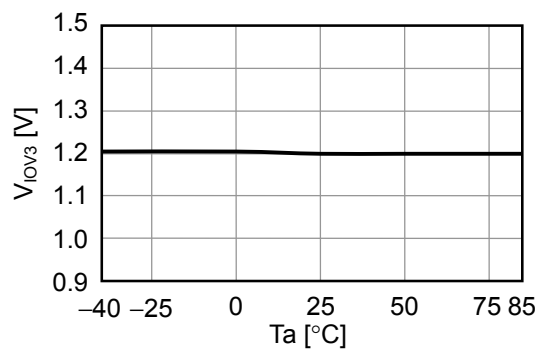
**2. 10  $V_{IOV2}$  vs.  $T_a$**



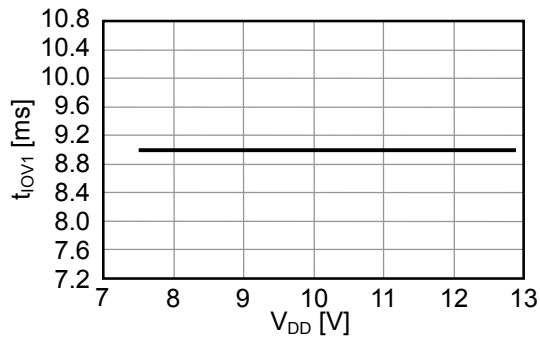
**2. 11  $V_{IOV3}$  vs.  $V_{DD}$**



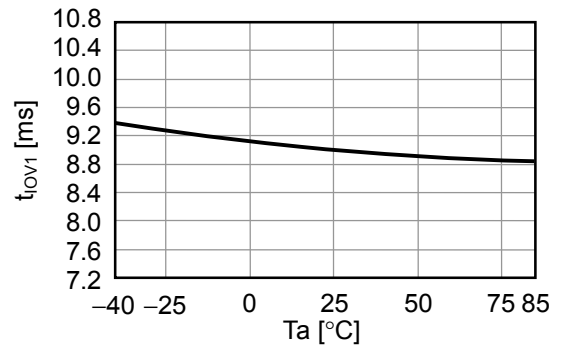
**2. 12  $V_{IOV3}$  vs.  $T_a$**



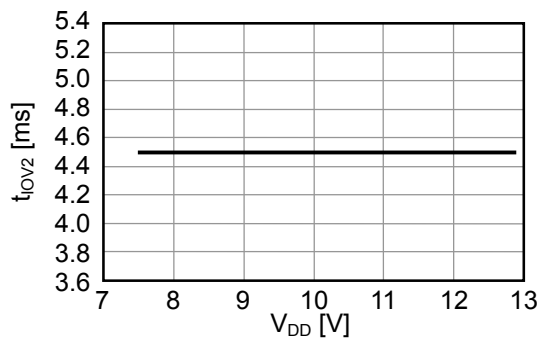
**2. 13  $t_{IOV1}$  vs.  $V_{DD}$**



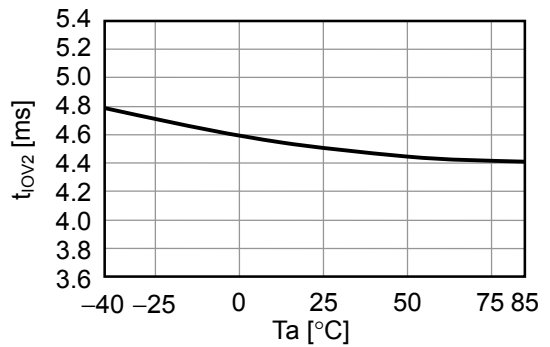
**2. 14  $t_{IOV1}$  vs.  $T_a$**



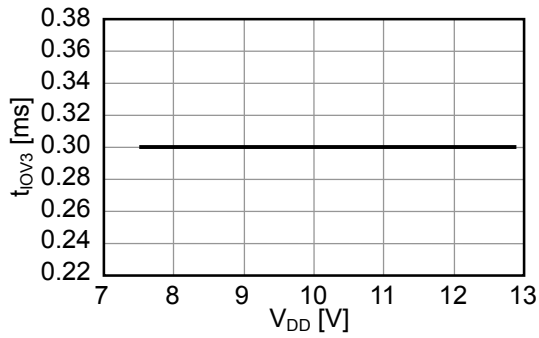
**2. 15  $t_{IOV2}$  vs.  $V_{DD}$**



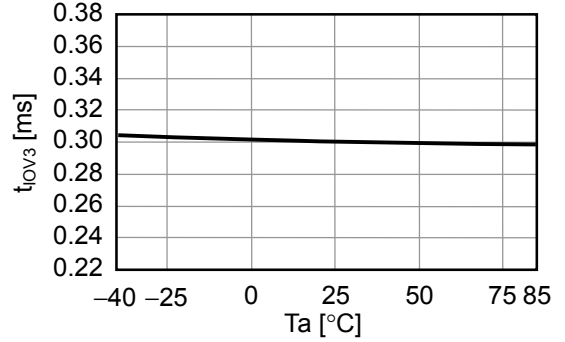
**2. 16  $t_{IOV2}$  vs.  $T_a$**



**2. 17  $t_{IOV3}$  vs.  $V_{DD}$**

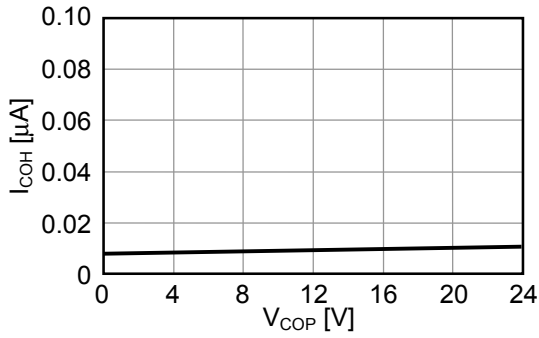


**2. 18  $t_{IOV3}$  vs.  $T_a$**

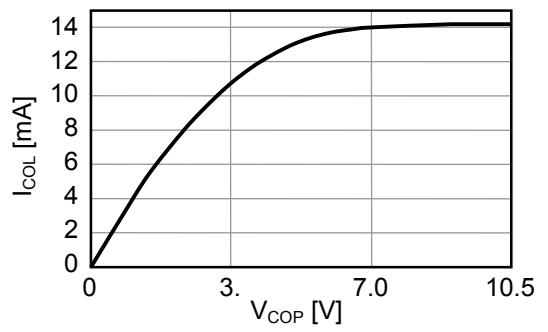


**3. COP / DOP Pin (S-8253CAA, S-8253DAA)**

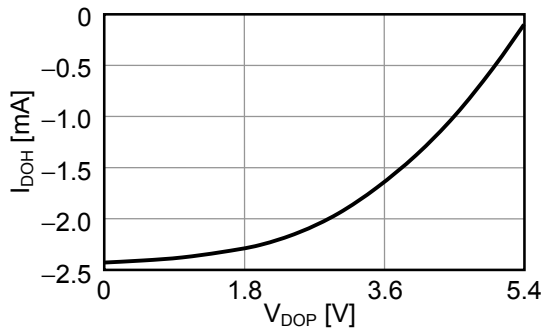
**3. 1  $I_{COH}$  vs.  $V_{COP}$**



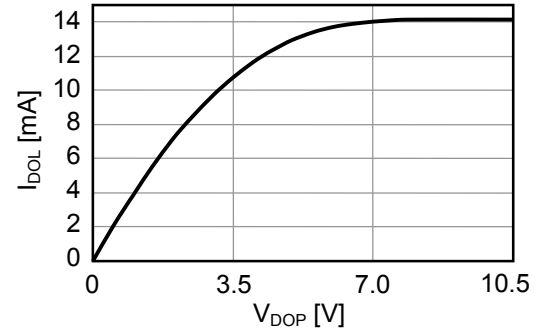
**3. 2  $I_{COL}$  vs.  $V_{COP}$**

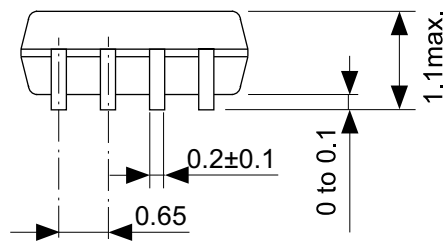
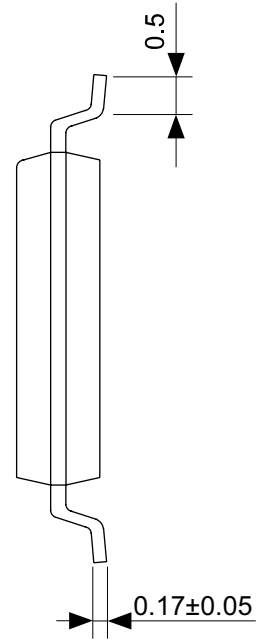
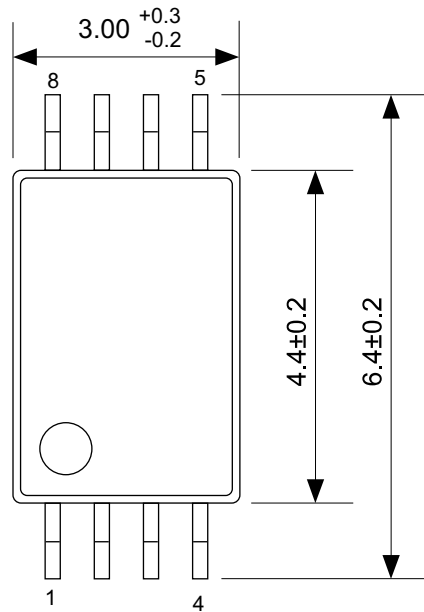


**3. 3  $I_{DOH}$  vs.  $V_{DOP}$**



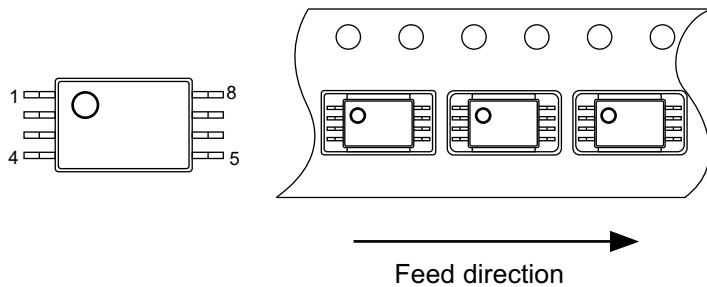
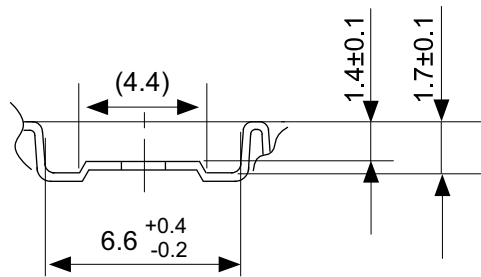
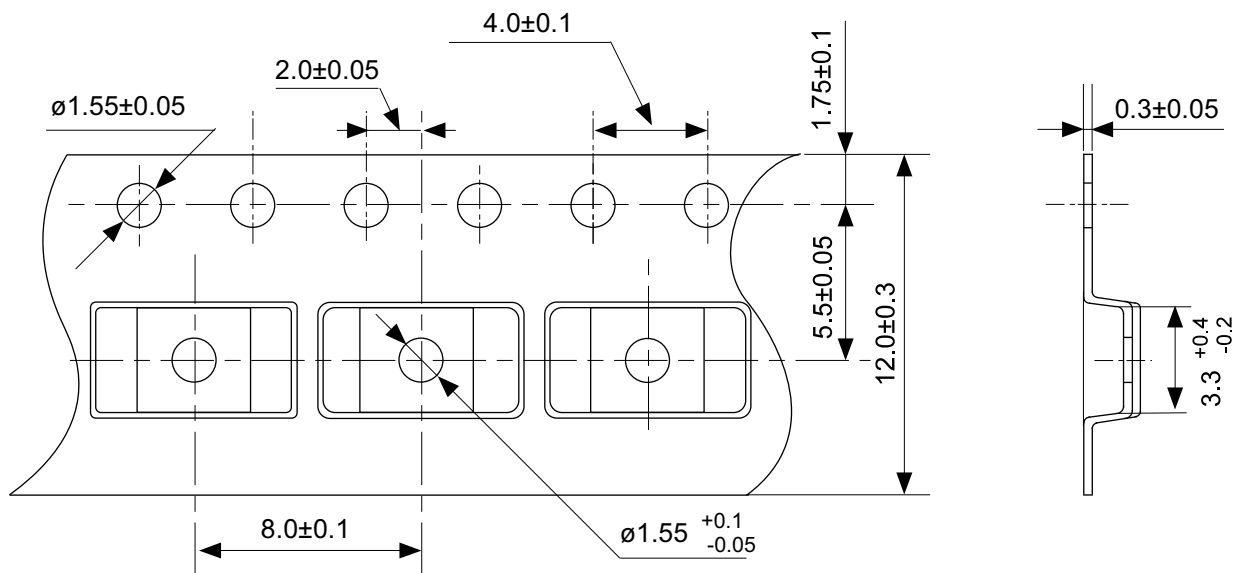
**3. 4  $I_{DOL}$  vs.  $V_{DOP}$**





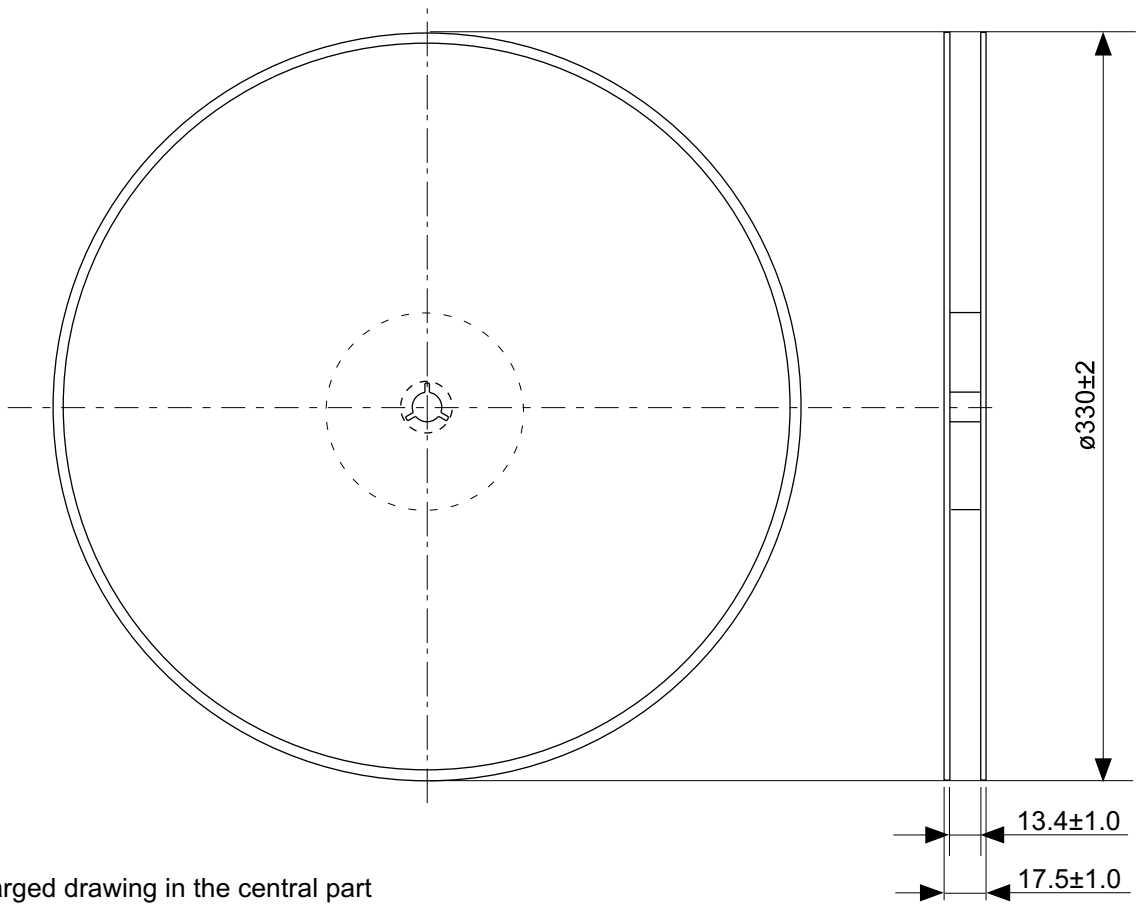
No. FT008-A-P-SD-1.2

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.2
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

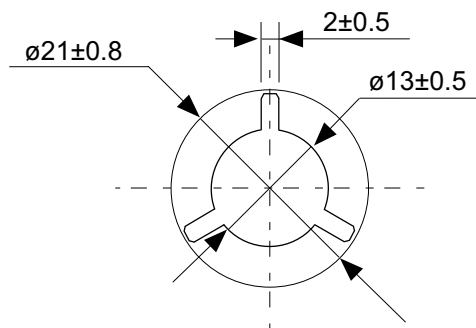


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

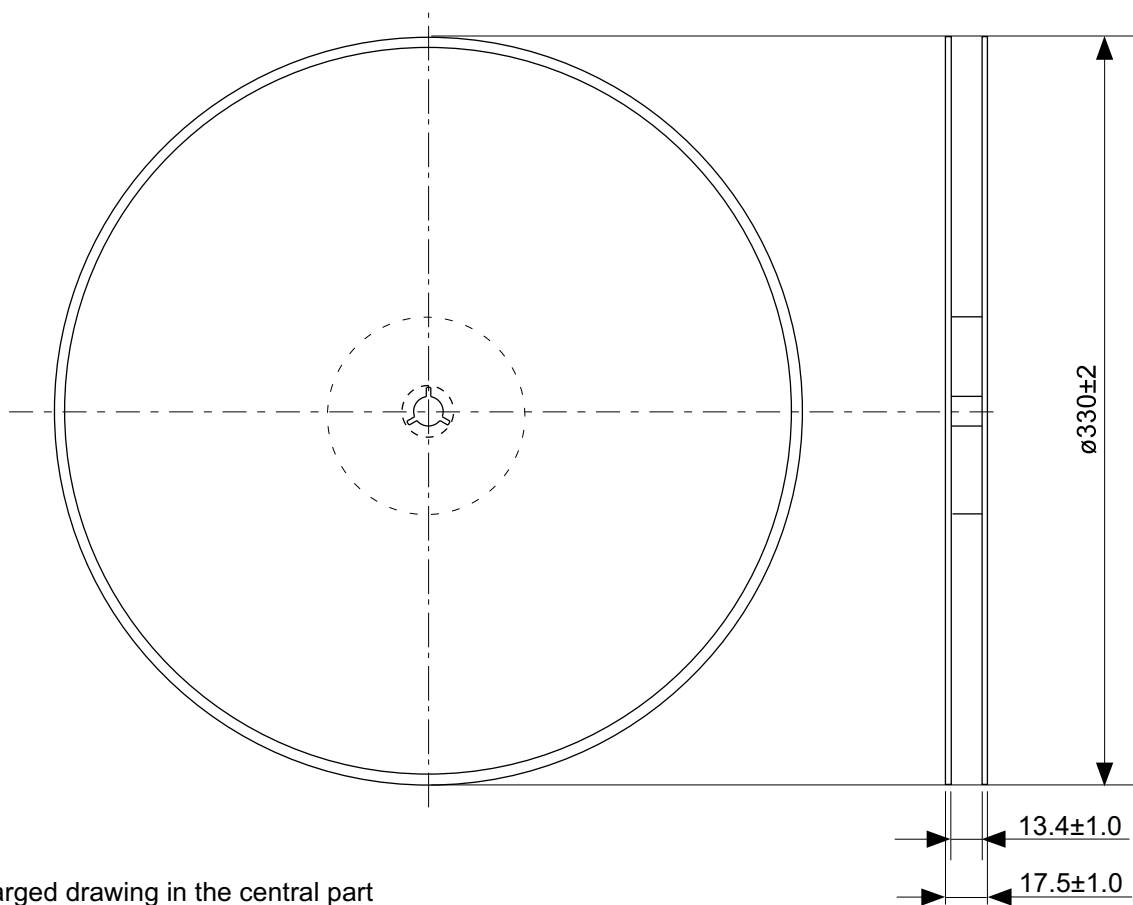


Enlarged drawing in the central part

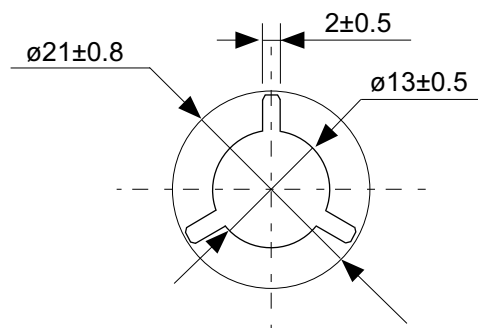


No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
<b>ABLIC Inc.</b>			



Enlarged drawing in the central part



No. FT008-E-R-S1-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-S1-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
<b>ABLIC Inc.</b>			



## Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.  
ABLIC Inc. is not responsible for damages caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not responsible for damages caused by the incorrect information described herein.
4. Be careful to use the products within their specified ranges. Pay special attention to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.  
ABLIC Inc. is not responsible for damages caused by failures and / or accidents, etc. that occur due to the use of the products outside their specified ranges.
5. When using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products must not be used or provided (exported) for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not responsible for any provision (export) to those whose purpose is to develop, manufacture, use or store nuclear, biological or chemical weapons, missiles, or other military use.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses. Do not apply the products to the above listed devices and equipments without prior written permission by ABLIC Inc. Especially, the products cannot be used for life support devices, devices implanted in the human body and devices that directly affect human life, etc.  
Prior consultation with our sales office is required when considering the above uses.  
ABLIC Inc. is not responsible for damages caused by unauthorized or unspecified use of our products.
9. Semiconductor products may fail or malfunction with some probability.  
The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.  
The entire system must be sufficiently evaluated and applied on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc.  
The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party without the express permission of ABLIC Inc. is strictly prohibited.
14. For more details on the information described herein, contact our sales office.

2.2-2018.06