The S-8209A Series is a battery protection IC with the cell-balance function. This application note is a guideline on the typical connection examples when using the S-8209A Series for applications. Refer to the datasheet for details and spec of this IC.

It is possible to configure the following applications with the S-8209A Series.

- A protection circuit with multi-serial cell: 2 cells or more
- A battery protection circuit with cell-balance function
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1. Protection circuit with S-8209A Series (without discharge cell-balance function) for multi-serial cell

In the connection of the S-8209A Series, connecting the CTLC, CTLD pins to the CO, DO pins allows to configure a protection circuit for serially connected batteries.

1.1 Connection example of battery protection IC

Figure 1 shows the example of protection circuit with S-8209A Series for multi-serial cell.

Remark Refer to "4. External components list" for constants of external components.

Caution 1. The connection example may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.
1.2 Operation

Following is about the operation of protection circuit with S-8209A Series for multi-serial cell shown in Figure 1.

1.2.1 Normal status

Following is about the operation of S-8209A Series in the normal status.

The S-8209A goes in the normal status;

In the S-8209A (3), The CTLC3, CTLD3 pins are pulled down to the level of VSS3 pin, BAT3 is more than the overdischarge detection voltage (V_DL) and less than the overdischarge detection voltage (V_CU). The CO3, DO3 pins get the level of VSS3 pin.

In the S-8209A (2), The CTLC2, CTLD2 pins are pulled down to the level of VSS3 pin by the CO3, DO3 pins, BAT2 is more than V_DL and less than V_CU. The CO2, DO2 pins get the level of VSS2 pin.

In the S-8209A (1), The CTLC1, CTLD1 pins are pulled down to the level of VSS2 pin by the CO2, DO2 pins, BAT1 is more than V_DL and less than V_CU. The CO1, DO1 pins get the level of VSS1 pin.

The status of each pin in the normal status is shown in Table 1.

<table>
<thead>
<tr>
<th>CTLC pin</th>
<th>CTLD pin</th>
<th>Status of battery</th>
<th>CO pin</th>
<th>DO pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTLC3 = VSS3</td>
<td>CTLD3 = VSS3</td>
<td>( V_{DL} &lt; \text{BAT3} &lt; V_{CU} )</td>
<td>CO3 = VSS3</td>
<td>DO3 = VSS3</td>
</tr>
<tr>
<td>CTLC2 = VSS3</td>
<td>CTLD2 = VSS3</td>
<td>( V_{DL} &lt; \text{BAT2} &lt; V_{CU} )</td>
<td>CO2 = VSS2</td>
<td>DO2 = VSS2</td>
</tr>
<tr>
<td>CTLC1 = VSS2</td>
<td>CTLD1 = VSS2</td>
<td>( V_{DL} &lt; \text{BAT1} &lt; V_{CU} )</td>
<td>CO1 = VSS1</td>
<td>DO1 = VSS1</td>
</tr>
</tbody>
</table>

The S-8209A (1) in the normal status turns on the charge control FET (CFET) and the discharge control FET (DFET) via bipolar transistors \( (Q_{CO}, Q_{DO}) \) externally set to each CO1 and DO1 pin. Therefore it is possible to charge/discharge by a charger or a load connected between \( P^+ \) and \( P^- \).
1.2.2 Status to inhibit charge

Following is about the status to inhibit charge, for example, the S-8209A (3) detects overcharge, the S-8209A (2) and (1) are in the normal status.

The S-8209A (3) goes in the overcharge status when BAT3 gets $V_{CU}$ or more by charging. The CO3 pin is set in high impedance.

The CTLC2 pin of the S-8209A (2) is pulled up to the level of VDD2 pin by the CTLC pin source current ($I_{CTLCH}$). The CTLC2 pin gets the level of VDD2 pin by the high impedance CO3 pin. Thus the S-8209A (2) goes in the overcharge status after the level of CTLC2 pin gets the CTLC pin H voltage ($V_{CTLCH}$) or more. The CO2 pin is set in high impedance.

The CTLC1 pin of the S-8209A (1) is pulled up to the level of VDD1 pin by $I_{CTLCH}$ as well. The CTLC1 pin gets the level of VDD1 pin by the high impedance CO2 pin. The S-8209A (1) also goes in the overcharge status after the level of CTLC1 pin gets $V_{CTLCH}$ or more.

The status of each pin in this case is shown in Table 2.

<table>
<thead>
<tr>
<th>CTLC pin</th>
<th>CTLD pin</th>
<th>Status of battery</th>
<th>CO pin</th>
<th>DO pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTLC3 = VSS3</td>
<td>CTLD3 = VSS3</td>
<td>$V_{CU} \leq BAT3$</td>
<td>CO3 = High-Z</td>
<td>DO3 = VSS3</td>
</tr>
<tr>
<td>CTLC2 = VDD2</td>
<td>CTLD2 = VSS3</td>
<td>$V_{DL} &lt; BAT2 &lt; V_{CU}$</td>
<td>CO2 = High-Z</td>
<td>DO2 = VSS2</td>
</tr>
<tr>
<td>CTLC1 = VDD1</td>
<td>CTLD1 = VSS2</td>
<td>$V_{DL} &lt; BAT1 &lt; V_{CU}$</td>
<td>CO1 = High-Z</td>
<td>DO1 = VSS1</td>
</tr>
</tbody>
</table>

The S-8209A (1) in the overcharge status turns off the CFET via a bipolar transistor (QCO) set externally to the CO1 pin. In this case, charging via a charger connected between P+ and P− is inhibited.

By this operation the overcharge status is transmitted from the bottom (S-8209A (3)) to the top (S-8209A (1)), from the CO pin to the CTLC pin.

Charging is also inhibited; BAT1 or BAT2 gets $V_{CU}$ or more.
1. 2. 3  Status to inhibit discharge

Following is the status to inhibit discharge, for example, the S-8209A (3) detects overdischarge, the S-8209A (2) and (1) are in the normal status. The S-8209A (3) goes in the overdischarge status when BAT3 gets $V_{DL}$ or less by discharging. The DO3 pin is set in high impedance.

The CTLD2 pin of the S-8209A (2) is pulled up to the level of VDD2 pin by the CTLD pin source current ($I_{CTLDH}$). The CTLD2 pin gets the level of VDD2 pin by the high impedance DO3 pin. Thus the S-8209A (2) goes in the overdischarge status after the level of CTLD2 pin gets the CTLD pin H voltage ($V_{CTLDH}$) or more. The DO2 pin is set in high impedance.

The CTLD1 pin of the S-8209A (1) is pulled up to the level of VDD1 pin by $I_{CTLDH}$ as well. The CTLD1 pin gets the level of VDD1 pin by the high impedance DO2 pin. The S-8209A (1) also goes in the overdischarge status after the level of CTLD1 pin gets $V_{CTLDH}$ or more.

The status of each pin in this case is shown in Table 3.

<table>
<thead>
<tr>
<th>CTLC pin</th>
<th>CTLD pin</th>
<th>Status of battery</th>
<th>CO pin</th>
<th>DO pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTLC3 = VSS3</td>
<td>CTLD3 = VSS3</td>
<td>BAT3 $\leq V_{DL}$</td>
<td>CO3 = VSS3</td>
<td>DO3 = High-Z</td>
</tr>
<tr>
<td>CTLC2 = VSS3</td>
<td>CTLD2 = VDD2</td>
<td>$V_{DL} &lt; \text{BAT2} &lt; V_{CU}$</td>
<td>CO2 = VSS2</td>
<td>DO2 = High-Z</td>
</tr>
<tr>
<td>CTLC1 = VSS2</td>
<td>CTLD1 = VDD1</td>
<td>$V_{DL} &lt; \text{BAT1} &lt; V_{CU}$</td>
<td>CO1 = VSS1</td>
<td>DO1 = High-Z</td>
</tr>
</tbody>
</table>

The S-8209A (1) in the overdischarge status turns off the DFET via a bipolar transistor ($Q_{DO}$) externally set to the DO1 pin. In this case, discharging to a load connected between $P_+$ and $P_-$ is inhibited.

By this operation the overdischarge status is transmitted from the bottom (S-8209A (3)) to the top (S-8209A (1)), from the DO pin to the CTLD pin.

Discharging is also inhibited; BAT1 or BAT2 gets $V_{DL}$ or less.
1.2.4 Charge cell-balance function

In Figure 1, the S-8209A (3) sets the CB3 pin at the level of VDD3 pin when BAT3 gets the cell-balance detection voltage (VBU) or more by charging. By this operation, the cell-balance control FET (CBFET3) is turned on so that the cell-balance control FET bypasses the charge current which flows into BAT3. At this point, if BAT1, BAT2 are less than VBU, the speed to charge BAT3 gets slower than to charge BAT1, BAT2. This is the charge cell-balance function. Even if any of battery voltages reaches VBU, the cell-balance control FET which corresponds to each battery turns on and the cell-balance is adjusted. The S-8209A Series turns off the cell-balance control FET when the battery voltage decreases to the cell-balance release voltage (VBL) or less by discharging again.

Caution If a battery having the voltage VBL or more is included among batteries when composing a protection circuit shown in Figure 1, the cell-balance control FET may turn on immediately after connecting the batteries.

1.2.5 Delay circuit

Connecting a delay capacitor only to the CDT1 pin of the S-8209A (1), as seen in Figure 1, allows to gain the detection delay time (tDET) and the release delay time (tREL). In detecting by any of batteries, each delay time is the same length.

(1) Detection delay time (tDET)

BAT3 gets VCU or more by charging, the CTLC2 pin gets the level of VDD2 pin because a capacitor is not connected to the CDT3 pin so that the CO3 pin is set in high impedance after delay of several hundred μs. After that in the S-8209A (2), the level of CTLC2 pin gets VCTLCH or more, after delay of several hundred μs the CO2 pin is set in high impedance. In the S-8209A (1), after delay of 10.0 [MΩ] (typ.) × 0.01 [μF] = 0.1 [s] (typ.), the CO1 pin is set in high impedance because connected CCDT to the CDT1 pin. Even if any of batteries detects, by this operation, users are able to gain the detection delay time almost the same to delay time of the S-8209A (1), because it defines the whole delay time in the S-8209A Series.

(2) Release delay time (tREL)

The S-8209A Series also has the release delay time (tREL), and this delay time is set its length as approx. 1/10 of the detection delay time. Connecting a delay capacitor only to the CDT1 pin of the S-8209A (1) allows having the same release delay time, as well as in the detection delay time.
1. 3  Timing chart

1. 3. 1  Overcharge detection

*1. In this period, the discharge current flows via a parasitic diode in the CFET.

Figure 2
1.3.2 Overdischarge detection

*1. In this period, the charge current flows via a parasitic diode in the DFET.

Figure 3
1. 4 Demonstration data of charge cell-balance detection

The demonstration data shows cell-balance for 3-serial lithium ion rechargeable battery using the S-8209AAA.

1. 4. 1 High ratio of bypass current to charge current

Charger: a constant current charger (0.05 C = 145 mA)

S-8209AAA charge cell-balance, 0.05 C constant current charger

Test conditions
Test circuit: Figure 1
IC: S-8209AAA (V_{CU} = 4.100 V, V_{CL} = 4.000 V, V_{BU} = 4.050 V, V_{BL} = 4.000 V, V_{DL} = 2.500 V, V_{DU} = 2.700 V)
Battery: 3-serial cell Lithium ion rechargeable battery, Nominal capacitance: 2.9 Ah, Size: 18650
R_{PASS}: 51 Ω (1 W) → Bypass current = 4.1 V / 51 Ω = 80 mA
1.4.2 Low ratio of bypass current to charge current

When the ratio of bypass current to charge current is low, repeating cell-balance cycle enables to adjust cell-balance.
Charger: a constant current charger (0.1 C = 290 mA)

![Graph showing cell voltage changes over time](image)

**Figure 5**

**Test conditions**

Test circuit: Figure 1
IC: S-8209AAA (VCU = 4.100 V, VCL = 4.000 V, VBU = 4.050 V, VBL = 4.000 V, VDL = 2.500 V, VDU = 2.700 V)
Battery: 3-serial cell lithium ion rechargeable battery, Nominal capacitance: 2.9 Ah, Size: 18650
RPASS: 51 Ω (1 W) → bypass current = 4.1 V / 51 Ω = 80 mA
2. Protection circuit with S-8209A Series (with discharge cell-balance function) for multi-serial cell

2.1 Connection example of battery protection IC

Setting bipolar transistors \((Q_{CTLD_1}, Q_{CTLD_2})\) allows adding the function to transmit the overdischarge status from the top (S-8209A (1)) to the bottom (S-8209A (3)).

Remark Refer to "4. External components list" for constants of external components.

Figure 6

Caution 1. The connection example may be changed without notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.
2. 2  Operation

Following is about the operation of protection circuit with S-8209A Series for multi-serial cell shown in Figure 6. Setting bipolar transistors (QCTLD1, QCTLD2) to the circuit in Figure 6 allows adding the function to transmit the overdischarge status from the top (S-8209A (1)) to the bottom (S-8209A (3)). By this, even if any IC among the S-8209A (1) to (3) first goes in the overdischarge status, it is possible to turn on all other cell-balance control FETs (CBFET) of the S-8209A Series. Thus cell-balance is certainly adjusted.

Following is about the operation in the status to inhibit discharge, when the S-8209A (2) detects overdischarge, and the S-8209A (1), (3) are in the normal status.

1. The S-8209A (2) goes in the overdischarge status when BAT2 decreases to VDL or less by discharging. The DO2 pin is set in high impedance.
2. The S-8209A (1) also goes in the overdischarge status via the DO2 pin to the CTLD1 pin.
3. The S-8209A (1) turns on the cell-balance control FET (CBFET1) by the discharge cell-balance function.
4. The S-8209A (1) in the overdischarge status turns off DFET via a bipolar transistor (QDO) and inhibits discharging to a load connected between P+ and P−.
5. The P− pin is pulled up by a load connected between P+ and P−.
6. QCTLD1, QCTLD2 are turned off and the CTLD3 pin of the S-8209A (3) is set in high impedance.
7. The S-8209A (3) also goes in the overdischarge status. The cell-balance control FET (CBFET3) turns on by the discharge cell-balance function.

As mentioned above, even in case that the S-8209A (2) first detects overdischarge by voltage drop in BAT2, the overdischarge status is transmitted from the S-8209A (1) to S-8209A (3) via QCTLD1, QCTLD2. As a result all (1) to (3) of the S-8209A go in the overdischarge status so that cell-balance is adjusted by the discharge cell-balance function, when each BAT is more than VDL. The cell-balance FET which corresponds to each battery turns off by the voltages of BAT1 to 3 that decreased to VDL or less.

And QCTLD1, QCTLD2 are turned on by connecting a charger between P+ and P− after inhibit discharging, and the CTLD3 pin is pulled down to the level of VSS3 pin. In this case, the cell-balance control FET (CBFET3) turns off although the voltage of BAT3 does not reach VDL or less.

Caution If a battery having the voltage VBL or more, or a battery having the overdischarge release voltage (Vou) or less is not included among batteries when composing a protection circuit shown in Figure 6, the cell-balance control FET may turn on immediately after connecting the battery. To turn off the cell-balance control FET, connect a charger between P+ and P−.
2.3 Timing chart of overdischarge detection

*1. In this period, the charge current flows via a parasitic diode in the DFET.

Figure 7
2. 4 Demonstration data of discharge cell-balance detection

The demonstration data shows cell-balance for 3-serial lithium ion rechargeable battery using the S-8209AAA.

Test conditions
Test circuit: Figure 6
IC: S-8209AAA (V_{CU} = 4.100 V, V_{CL} = 4.000 V, V_{SU} = 4.050 V, V_{BL} = 4.000 V, V_{DL} = 2.500 V, V_{DU} = 2.700 V)
Battery: 3-serial cell lithium ion rechargeable battery, Nominal capacitance: 2.9 Ah, Size: 18650
R_{PAS} = 51 \Omega (1 W) \rightarrow \text{bypass current} = 2.5 V / 51 \Omega = 49 mA
Load: 100 \Omega

Battery voltage’s oscillation
1. The cell-balance control FET turns off when the battery voltage decrease to the over discharge detection voltage (V_{DL}) or less.
2. Discharge via the cell-balance control FET stops so that the battery voltage rises.
3. The cell-balance control FET turns on when the battery voltage increases to the over discharge release voltage (V_{DU}) or more.
4. Discharge via the cell-balance control FET starts so that the battery voltage falls.

Repeating the procedures 1 to 4 enables to adjust cell-balance.
3. Examples of application circuit

The circuit examples shown in Figure 9 to Figure 11 are recommended when a low-resistance SENSE resistor is used. These circuits enable accurate overcurrent protection.

3.1 10-cell protection circuit added the discharge overcurrent protection function (Charge pin and discharge pin are integrated, S-8269B Series)

![Diagram of application circuit](image)

Remark Refer to "4. External components list" for constants of external components.
3. 2 10-serial cell protection circuit added the charge and discharge overcurrent protection functions (Charge pin and discharge pin are integrated, S-8269B Series)

Remark Refer to "4. External components list" for constants of external components.

Figure 10
3.3 10-series cell protection circuit added the charge and discharge overcurrent protection functions (Charge pin and discharge pin are separated, S-8269B Series)

Remark Refer to "4. External components list" for constants of external components.

Figure 11
3.4 10-seril cell protection circuit added the discharge overcurrent protection function
(Charge pin and discharge pin are separated, S-8239A Series active "L" product)

Remark Refer to "4. External components list" for constants of external components.
3.5 10-serail cell protection circuit added the discharge overcurrent protection function
(Charge pin and discharge pin are separated, S-8239A Series active "H" product)

Remark Refer to "4. External components list" for constants of external components.

Figure 13
3.6 5-serial cell protection circuit connected by connectors

In the application that pins are connected by connectors as seen in the application circuit below, safety is enhanced since both charge and discharge stop even if the connectors are disconnected.

Remark  Refer to "4. External components list" for constants of external components.

Figure 14
### 4. External components list

Table 4 shows external components in the connection examples in Figure 1, Figure 6 and Figure 9 to Figure 14.

<table>
<thead>
<tr>
<th>Symbol Name</th>
<th>Typical Value</th>
<th>Unit</th>
<th>Components Name</th>
<th>Maker</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1 to IC10</td>
<td>−</td>
<td>−</td>
<td>S-8209A</td>
<td>ABLIC Inc.</td>
<td>Necessary</td>
</tr>
<tr>
<td>IC11</td>
<td>−</td>
<td>−</td>
<td>S-8269B1</td>
<td>ABLIC Inc.</td>
<td>Necessary</td>
</tr>
<tr>
<td>IC12</td>
<td>−</td>
<td>−</td>
<td>S-812C50A</td>
<td>ABLIC Inc.</td>
<td>Necessary</td>
</tr>
<tr>
<td>IC13</td>
<td>−</td>
<td>−</td>
<td>S-8239A1</td>
<td>ABLIC Inc.</td>
<td>Necessary</td>
</tr>
<tr>
<td>CBFET1 to CBFET10</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>User setting</td>
</tr>
<tr>
<td>CFET</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>User setting</td>
</tr>
<tr>
<td>DFET</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>User setting</td>
</tr>
<tr>
<td>CCDT</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>User setting</td>
</tr>
<tr>
<td>CIN</td>
<td>0.1</td>
<td>μF</td>
<td>GRM188</td>
<td>Murata Manufacturing Co., Ltd.</td>
<td>User setting</td>
</tr>
<tr>
<td>CL</td>
<td>0.1</td>
<td>μF</td>
<td>GRM188</td>
<td>Murata Manufacturing Co., Ltd.</td>
<td>User setting</td>
</tr>
<tr>
<td>CVDD</td>
<td>0.1</td>
<td>μF</td>
<td>GRM188</td>
<td>Murata Manufacturing Co., Ltd.</td>
<td>Recommended</td>
</tr>
<tr>
<td>C101</td>
<td>0.1</td>
<td>μF</td>
<td>−</td>
<td>−</td>
<td>Recommended</td>
</tr>
<tr>
<td>C201</td>
<td>1</td>
<td>μF</td>
<td>−</td>
<td>−</td>
<td>Recommended</td>
</tr>
<tr>
<td>N101</td>
<td>−</td>
<td>−</td>
<td>SSM3K7002KF</td>
<td>Toshiba Electronic Devices &amp; Storage Corporation</td>
<td>Recommended</td>
</tr>
<tr>
<td>N102</td>
<td>−</td>
<td>−</td>
<td>SSM3K7002KF</td>
<td>Toshiba Electronic Devices &amp; Storage Corporation</td>
<td>Recommended</td>
</tr>
<tr>
<td>N103</td>
<td>−</td>
<td>−</td>
<td>SSM3K7002KF</td>
<td>Toshiba Electronic Devices &amp; Storage Corporation</td>
<td>Recommended</td>
</tr>
<tr>
<td>N104</td>
<td>−</td>
<td>−</td>
<td>SSM3K7002KF</td>
<td>Toshiba Electronic Devices &amp; Storage Corporation</td>
<td>Recommended</td>
</tr>
<tr>
<td>N201</td>
<td>−</td>
<td>−</td>
<td>SSM3J168F</td>
<td>Toshiba Electronic Devices &amp; Storage Corporation</td>
<td>Recommended</td>
</tr>
<tr>
<td>N202</td>
<td>−</td>
<td>−</td>
<td>SSM3J168F</td>
<td>Toshiba Electronic Devices &amp; Storage Corporation</td>
<td>Recommended</td>
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<td>P101</td>
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<td>Recommended</td>
</tr>
<tr>
<td>P102</td>
<td>−</td>
<td>−</td>
<td>SSM3K7002KF</td>
<td>Toshiba Electronic Devices &amp; Storage Corporation</td>
<td>Recommended</td>
</tr>
<tr>
<td>QCO</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>Recommended</td>
</tr>
<tr>
<td>QDO</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
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Table 4 (2 / 2)

<table>
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<tr>
<th>Symbol</th>
<th>Typical</th>
<th>Unit</th>
<th>Components name</th>
<th>Maker</th>
<th>Remark</th>
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<tr>
<td>(R_{\text{VDD}})</td>
<td>470</td>
<td>(\Omega)</td>
<td>MCR03</td>
<td>ROHM CO., LTD.</td>
<td>Recommended</td>
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<td>(R_{\text{VM}})</td>
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<td>k(\Omega)</td>
<td>MCR03</td>
<td>ROHM CO., LTD.</td>
<td>Recommended</td>
</tr>
<tr>
<td>(R_{101})</td>
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<td>(\Omega)</td>
<td>MCR03</td>
<td>ROHM CO., LTD.</td>
<td>Recommended</td>
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<td>(R_{102})</td>
<td>5.1</td>
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<td>(R_{104})</td>
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<td>(R_{105})</td>
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<td>M(\Omega)</td>
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<tr>
<td>(R_{201}^*)</td>
<td>1</td>
<td>k(\Omega)</td>
<td>MCR03</td>
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<td>Recommended</td>
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<tr>
<td>(R_{202})</td>
<td>100</td>
<td>(\Omega)</td>
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<td>Recommended</td>
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<td>TB</td>
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<td>(Z_{\text{INI}})</td>
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<td>(Z_{\text{VM}}^*)</td>
<td>1SB5930B Diodes Incorporated</td>
<td>User setting</td>
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</table>

*1. Select this product according to the overcurrent detection voltage that you will use. For details, refer to datasheet of each product.

*2. At the moment when the S-8269B Series (Figure 9 to Figure 11) or S-8239A Series (Figure 12, Figure 13) detects the overcurrent and turns off DFET, a spike voltage generated in BAT8 (Figure 9 to Figure 11) or BAT9 (Figure 12, Figure 13) may result in transient change of the power supply of the S-8269B Series or S-8239A Series through \(C_{201}\) and \(R_{201}\). The constant of \(C_{201}\) and \(R_{201}\) is normally \(1 \mu F \times 1 k\Omega = 1 mF \times \Omega\). However, since the spike voltage generated in BAT8 or BAT9 differs depending on each application, perform thorough evaluation about the power supply transient change and overcurrent protection function of the S-8269B Series or S-8239A Series using the actual application to set \(C_{201}\) and \(R_{201}\).

*3. Set the resistance with attention to VGS rated value of FET.

*4. In order to prevent from damage when an overvoltage is applied to the IC, select \(R_{\text{CTLC}}\) and \(R_{\text{CTLD}}\) from 1 k\(\Omega\) to 100 k\(\Omega\).

*5. Pay attention to the rated electric powers.

*6. TB: Thermal Breaker
   When a TB is not necessary, connect the same protection resistor as \(R_{\text{CTLC}}\) or \(R_{\text{CTLD}}\).

*7. When building a protection circuit for 10-serial or more cells, connect \(Z_{\text{VM}}\) so that the VM pin voltage does not exceed the absolute maximum rating.

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

3. Set \(V_{\text{VM}}\) as follows to release the S-8269B Series from the discharge overcurrent status when a load is open.

   · "3. 1 10-serial cell protection circuit added the discharge overcurrent protection function (Charge pin and discharge pin are integrated, S-8269B Series)" or "3. 2 10-serial cell protection circuit added the charge and discharge overcurrent protection functions (Charge pin and discharge pin are integrated, S-8269B Series)"

   \[
   V_{\text{VM}} = V_{P+} \times \frac{R_{\text{VMS}}}{R_{\text{CO1}} + R_{\text{CO4}} + R_{\text{VM}} + R_{\text{VMS}}} \leq V_{\text{RIOV}} \text{ or } V_{\text{DIOV1}}
   \]

   · "3. 3 10-serial cell protection circuit added the charge and discharge overcurrent protection functions (Charge pin and discharge pin are separated, S-8269B Series)"

   \[
   V_{\text{VM}} = V_{P+} \times \frac{R_{\text{VMS}}}{R_{\text{EB}} + R_{\text{CO1}} + R_{\text{CO4}} + R_{\text{VM}} + R_{\text{VMS}}} \leq V_{\text{RIOV}} \text{ or } V_{\text{DIOV1}}
   \]

4. Set \(V_{\text{VM}}\) as follows to release the S-8239A Series from the discharge overcurrent status when a load is open.

   · "3. 4 10-serial cell protection circuit added the discharge overcurrent protection function (Charge pin and discharge pin are separated, S-8239A Series active "L" product)" or "3. 5 10-serial cell protection circuit added the charge overcurrent protection function (Charge pin and discharge pin are separated, S-8239A Series active "H" product)"

   \[
   V_{\text{VM}} = V_{P+} \times \frac{R_{\text{VMS}}}{R_{\text{CO1}} + R_{\text{CO4}} + R_{\text{VM}} + R_{\text{VMS}}} \leq V_{\text{DD11}} - V_{\text{RIOV}}
   \]

Remark

\(V_{\text{VM}}\): VM pin input voltage
\(V_{P+}\): P+ pin voltage
\(R_{\text{VMS}}\): Resistance between VM pin and VSS pin
\(V_{\text{RIOV}}\) or \(V_{\text{DIOV1}}\): Release voltage of discharge overcurrent status
\(V_{\text{DD11}}\): Input voltage between VDD pin and VSS pin of the S-8239A Series

ABLIC Inc.
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6. Related source

Refer to the following datasheet for details of the S-8209A Series.

S-8209A Series Datasheet

The information described in this application note and the datasheet is subject to change without notice. Contact our sales representatives for details. Regarding the newest version, select product category and product name on our website, and download the PDF file.

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