S-8203A Series

BATTERY PROTECTION IC FOR 3-SERIES CELL PACK

www.ablic.com

Rev.1.1_00

The S-8203A Series includes high-accuracy voltage detection circuits and delay circuits, in single use, makes it possible for users to monitor the status of 3-series cell lithium-ion rechargeable battery.
The S-8203A Series is suitable for protecting lithium-ion rechargeable battery pack from overcharge, overdischarge, and overcurrent.

■ Features

- High-accuracy voltage detection function for each cell
  - Overcharge detection voltage n (n = 1 to 3) 3.55 V to 4.50 V*1 (50 mV step) Accuracy ±25 mV
  - Overcharge release voltage n (n = 1 to 3) 3.30 V to 4.50 V*2 Accuracy ±50 mV
  - Overdischarge detection voltage n (n = 1 to 3) 2.0 V to 3.2 V*1 (100 mV step) Accuracy ±80 mV
  - Overdischarge release voltage n (n = 1 to 3) 2.0 V to 3.4 V*3 Accuracy ±100 mV
- Discharge overcurrent detection in 2-step
  - Discharge overcurrent detection voltage 0.05 V to 0.30 V*4 (50 mV step) Accuracy ±15 mV
  - Short-circuiting detection voltage 0.50 V to 1.0 V*4 (100 mV step) Accuracy ±100 mV
- Charge overcurrent detection function
  - Charge overcurrent detection voltage −0.30 V to −0.05 V (50 mV step) Accuracy ±30 mV
- Settable by external capacitor; overcharge detection delay time, overdischarge detection delay time, discharge overcurrent detection delay time, charge overcurrent detection delay time
  (Load short-circuiting detection delay time is internally fixed.)
- Independent charge and discharge control by the control pins
- 0 V battery charge: Enabled, inhibited
- Power-down function: Available, unavailable
- High-withstand voltage: Absolute maximum rating 28 V
- Wide operation voltage range: 2 V to 24 V
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  - During operation: 40 μA max. (Ta = +25°C)
  - During power-down: 0.1 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** The overcharge detection voltage n (n = 1 to 3) and overdischarge detection voltage (n = 1 to 3) cannot be selected if the voltage difference between them is 0.6 V or lower.
***2.** Overcharge hysteresis voltage n (n = 1 to 3) can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.
(Overcharge hysteresis voltage = Overcharge detection voltage − Overcharge release voltage)
***3.** Overdischarge hysteresis voltage n (n = 1 to 3) can be selected as 0 V or from a range of 0.2 V to 0.7 V in 100 mV step.
(Overdischarge hysteresis voltage = Overdischarge release voltage − Overdischarge detection voltage)
***4.** The discharge overcurrent detection voltage and load short-circuiting detection voltage cannot be selected if the voltage difference between them is 0.3 V or lower.

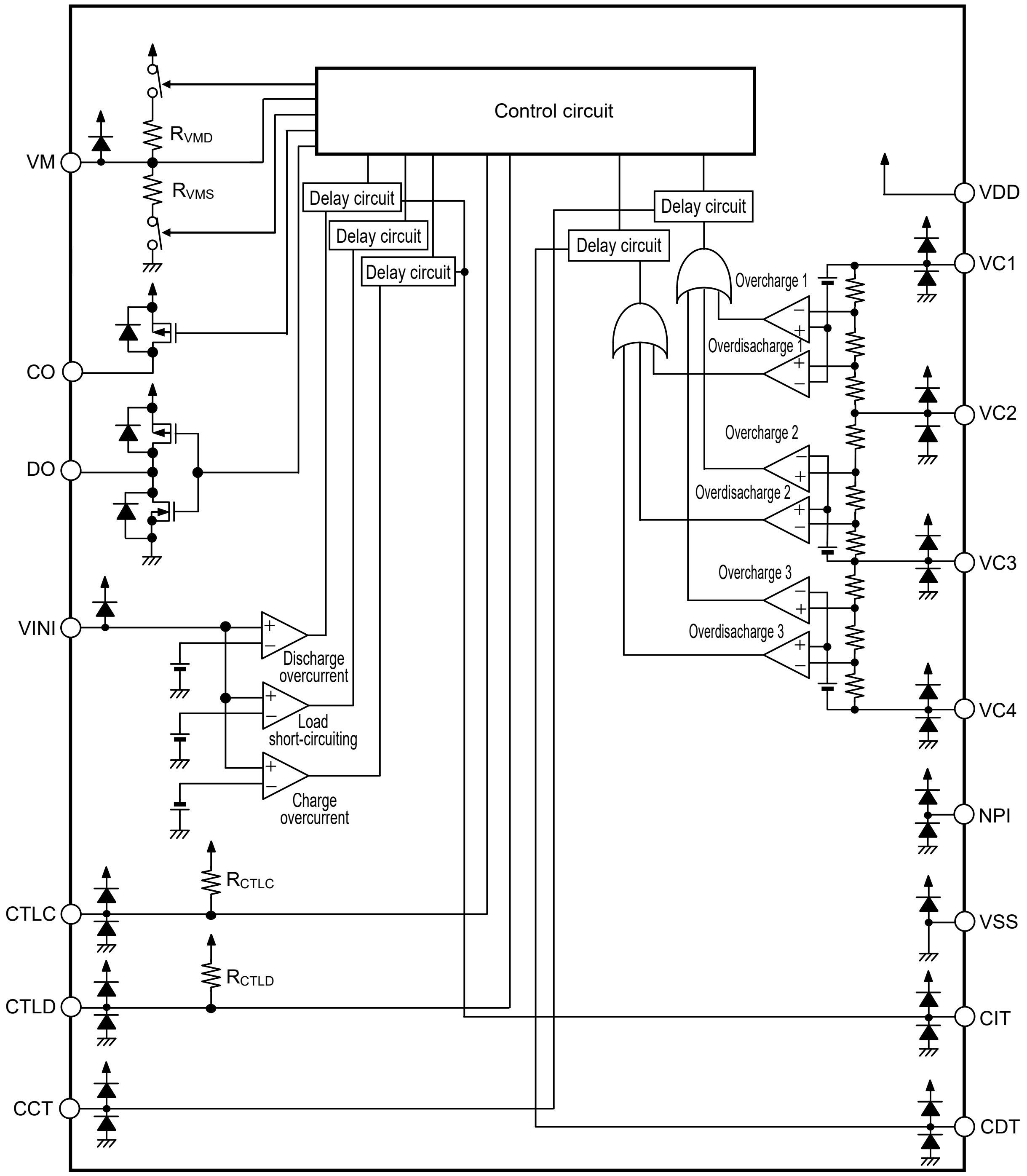
■ Application

- Rechargeable lithium-ion battery pack

■ Package

- 16-Pin TSSOP

■ Block Diagram



Remark Diodes in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name

S-8203A xx - TCT1 U

- U — Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- TCT1 — Package abbreviation and IC packing specifications*1
  - TCT1: 16-Pin TSSOP, Tape
- xx — Serial code*2
  - Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Code

Package Name	Dimension	Tape	Reel
16-Pin TSSOP	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-S1

3. Product name list

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent Detection Voltage [V_{DIOV}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]	0 V Battery Charge	Power-down Function	Delay Time*1
S-8203AAA-TCT1U	4.250 V	4.150 V	2.70 V	3.00 V	0.20 V	0.50 V	−0.10 V	Enabled	Available	(2)
S-8203AAB-TCT1U	4.250 V	4.150 V	2.50 V	3.00 V	0.10 V	0.50 V	−0.05 V	Enabled	Available	(2)
S-8203AAC-TCT1U	4.250 V	4.150 V	2.50 V	3.00 V	0.10 V	0.50 V	−0.05 V	Enabled	Unavailable	(2)
S-8203AAD-TCT1U	4.250 V	4.100 V	3.00 V	3.20 V	0.15 V	0.50 V	−0.10 V	Enabled	Available	(2)
S-8203AAE-TCT1U	4.350 V	4.150 V	2.40 V	3.00 V	0.15 V	0.50 V	−0.10 V	Enabled	Available	(2)
S-8203AAF-TCT1U	4.350 V	4.150 V	2.80 V	3.00 V	0.20 V	0.50 V	−0.10 V	Enabled	Available	(2)
S-8203AAG-TCT1U	4.425 V	4.225 V	2.50 V	2.90 V	0.15 V	0.50 V	−0.10 V	Enabled	Available	(2)
S-8203AAH-TCT1U	3.650 V	3.500 V	2.20 V	2.30 V	0.10 V	0.50 V	−0.05 V	Enabled	Available	(2)
S-8203AAI-TCT1U	3.750 V	3.600 V	2.00 V	2.50 V	0.15 V	0.50 V	−0.10 V	Enabled	Available	(2)
S-8203AAJ-TCT1U	4.425 V	4.225 V	2.80 V	3.00 V	0.15 V	0.50 V	−0.10 V	Enabled	Available	(2)
S-8203AAK-TCT1U	4.250 V	4.150 V	2.50 V	3.00 V	0.10 V	0.50 V	−0.05 V	Inhibited	Available	(2)

***1.** The delay time is set by the external capacitor.
But the discharge overcurrent release delay time (t_{DIOVR}) and charge overcurrent release delay time (t_{CIOVR}) are calculated by discharge overcurrent detection delay time (t_{DIOV}) and charge overcurrent detection delay time (t_{CIOV}) as the following equations. 1 [ms] (typ.) is the internal delay time of the S-8203A Series.

(1) $t_{DIOVR} = t_{DIOV} \times 10 + 1$ [ms] (typ.), $t_{CIOVR} = t_{CIOV} \times 10 + 1$ [ms] (typ.)
(2) $t_{DIOVR} = t_{DIOV} \times 0.05 + 1$ [ms] (typ.), $t_{CIOVR} = t_{CIOV} \times 0.05 + 1$ [ms] (typ.)

Moreover, refer to "**7. Delay time setting**" in "**■ Operation**" for calculational methods of delay times.

Remark Please contact our sales representatives for products other than the above.

■ Pin Configuration

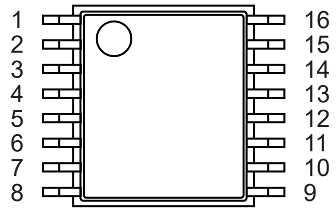


Figure 2

Table 3

Pin No.	Symbol	Description
1	VM	Voltage detection pin between VSS pin and VM pin
2	CO	FET gate connection pin for charge control (Pch open-drain output) Pin for voltage detection between VSS pin and CO pin
3	DO	FET gate connection pin for discharge control (CMOS output)
4	VINI	Voltage detection pin between VSS pin and VINI pin
5	CTLC	Control pin for charge FET
6	CTLD	Control pin for discharge FET
7	CCT	Capacitor connection pin for delay for overcharge detection voltage
8	CDT	Capacitor connection pin for delay for overdischarge detection voltage
9	CIT	Capacitor connection pin for delay for discharge overcurrent detection, charge overcurrent detection
10	VSS	Input pin for negative power supply*1
11	NPI	Input pin for negative power supply*1
12	VC4	Connection pin for battery 3's negative voltage Input pin for negative power supply
13	VC3	Connection pin for battery 2's negative voltage Connection pin for battery 3's positive voltage
14	VC2	Connection pin for battery 1's negative voltage Connection pin for battery 2's positive voltage
15	VC1	Connection pin for battery 1's positive voltage
16	VDD	Input pin for positive power supply Connection pin for battery 1's positive voltage

***1.** Be sure to short the VSS pin and the NPI pin when using them.

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 28	V
Input pin voltage 1	V_{IN1}	VC1, VC2, VC3, VC4, NPI, CTLC, CTLD, CCT, CDT, CIT	V_{SS} − 0.3 to V_{DD} + 0.3	V
Input pin voltage 2	V_{IN2}	VM, VINI	V_{DD} − 28 to V_{DD} + 0.3	V
DO pin output voltage	V_{DO}	DO	V_{SS} − 0.3 to V_{DD} + 0.3	V
CO pin input and output voltage	V_{CO}	CO	V_{DD} − 28 to V_{DD} + 0.3	V
Power dissipation	P_D	−	1100*1	mW
Operation ambient temperature	T_{opr}	−	−40 to +85	°C
Storage temperature	T_{stg}	−	−40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

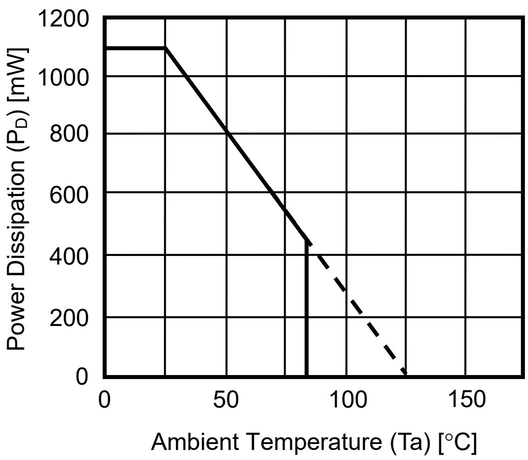


Figure 3 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 5 (1 / 2)

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n (n = 1, 2, 3)	V_{CUn}	V1 = V2 = V3 = V_{CU} − 0.05 V	V_{CU} − 0.025	V_{CU}	V_{CU} + 0.025	V	2
Overcharge release voltage n (n = 1, 2, 3)	V_{CLn}	–	V_{CL} − 0.05	V_{CL}	V_{CL} + 0.05	V	2
Overdischarge detection voltage n (n = 1, 2, 3)	V_{DLn}	–	V_{DL} − 0.08	V_{DL}	V_{DL} + 0.08	V	2
Overdischarge release voltage n (n = 1, 2, 3)	V_{DUn}	–	V_{DU} − 0.10	V_{DU}	V_{DU} + 0.10	V	2
Discharge overcurrent detection voltage	V_{DIOV}	–	V_{DIOV} − 0.015	V_{DIOV}	V_{DIOV} + 0.015	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} − 0.10	V_{SHORT}	V_{SHORT} + 0.10	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} − 0.03	V_{CIOV}	V_{CIOV} + 0.03	V	2
Temperature coefficient 1*1	T_{COE1}	Ta = 0°C to +50°C*3	−1.0	0	1.0	mV/°C	–
Temperature coefficient 2*2	T_{COE2}	Ta = 0°C to +50°C*3	−0.5	0	0.5	mV/°C	–
Delay Time Function*4							
CCT pin internal resistance	R_{CCT}	V1 = 4.5 V, V2 = V3 = 3.5 V	6.15	8.31	10.2	MΩ	3
CDT pin internal resistance	R_{CDT}	V1 = 1.5 V, V2 = V3 = 3.5 V	615	831	1020	kΩ	3
CIT pin internal resistance	R_{CIT}	–	123	166	204	kΩ	3
CCT pin detection voltage	V_{CCT}	V1 = 4.5 V, V2 = V3 = 3.5 V	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	3
CDT pin detection voltage	V_{CDT}	V1 = 1.5 V, V2 = V3 = 3.5 V	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	3
CIT pin detection voltage	V_{CIT}	V6 = V_{DIOV} + 0.015 V	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	3
Load short-circuiting detection delay time	t_{SHORT}	–	100	300	600	μs	2
CTLC pin response time	t_{CTLC}	–	–	–	2.5	ms	2
CTLD pin response time	t_{CTLD}	–	–	–	2.5	ms	2
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled V1 = V2 = V3 = 0 V	–	0.8	1.5	V	4
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge inhibited	0.4	0.7	1.1	V	2
Internal Resistance							
CTLC pin internal resistance	R_{CTLC}	–	7	10	13	MΩ	5
CTLD pin internal resistance	R_{CTLD}	–	7	10	13	MΩ	5
Resistance between VM pin and VDD pin *5	R_{VMD}	V1 = V2 = V3 = 1.8 V	450	900	1800	kΩ	5
Resistance between VM pin and VSS pin	R_{VMS}	–	250	500	750	kΩ	5

Table 5 (2 / 2)

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Input Voltage							
Operation voltage between VDD pin and VSS pin [*6]	V_{DSOP}	Fixed output voltage of DO pin and CO pin	2	–	24	V	–
CTLC pin change voltage[*6]	V_{CTLC}	–	2.1	3.0	4.0	V	2
CTLD pin change voltage[*6]	V_{CTLD}	–	2.1	3.0	4.0	V	2
Input Current							
Current consumption during operation	I_{OPE}	–	–	20	40	μA	1
Current consumption during power-down[*5]	I_{PDN}	V1 = V2 = V3 = 1.5 V	–	–	0.1	μA	1
VC1 pin current	I_{VC1}	–	0	0.8	2.0	μA	5
VC2 pin current	I_{VC2}	–	–0.3	0	0.3	μA	5
VC3 pin current	I_{VC3}	–	–0.3	0	0.3	μA	5
VC4 pin current	I_{VC4}	–	–2.0	–0.8	0	μA	5
Output Current							
CO pin source current	I_{COH}	V13 = 0.5 V	10	–	–	μA	5
CO pin leakage current	I_{COL}	V1 = V2 = V3 = 8 V	–	–	0.1	μA	5
DO pin source current	I_{DOH}	V14 = 0.5 V	10	–	–	μA	5
DO pin sink current	I_{DOL}	V15 = 0.5 V	–	–	–10	μA	5

***1.** Voltage temperature coefficient 1: Overcharge detection voltage
***2.** Voltage temperature coefficient 2: Discharge overcurrent detection voltage
***3.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.
***4.** Refer to "■ **Operation**" for details of delay time function.
***5.** For products with power-down function
***6.** The S-8203A Series does not operate detection if the operation voltage between VDD pin and VSS pin (V_{DSOP}) is CTLC pin change voltage (V_{CTLC}) or CTLD pin change voltage (V_{CTLD}) or lower.

■ Test Circuits

1. Current consumption during operation, current consumption during power-down (Test circuit 1)

Set S1 and S2 to OFF.

1. 1 Current consumption during operation (I_{OPE})

Set V1 = V2 = V3 = 3.5 V, S2 to ON. I_{SS} is the current consumption during operation (I_{OPE}) at that time.

1. 2 Current consumption during power-down (I_{PDN}) (With power-down function)

Set V1 = V2 = V3 = 1.5 V, S1 to ON. I_{SS} is the current consumption during power-down (I_{PDN}) at that time.

2. Overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, overdischarge release voltage, discharge overcurrent detection voltage, load short-circuiting detection voltage, charge overcurrent detection voltage, CTLC pin change voltage, CTLD pin change voltage, load short-circuiting detection delay time, CTLC pin response time, CTLD pin response time (Test circuit 2)

Set S3 to OFF.
Confirm both V_{CO} and V_{DO} are in "H" (the voltage level is $V_{DS} \times 0.9$ V or higher) after setting V1 = V2 = V3 = 3.5 V, V6 = V7 = V8 = 0 V (this status is referred to as initial status 1).

2. 1 Overcharge detection voltage (V_{CU1}), Overcharge release voltage (V_{CL1})

The overcharge detection voltage (V_{CU1}) is V1 when the V_{CO} is set to "L" (the voltage level is $V_{DS} \times 0.1$ V or lower) after increasing V1 gradually after setting V1 = V2 = V3 = $V_{CU} - 0.05$ V from the initial status 1. After that, decreasing V1 gradually, V1 is the overcharge release voltage (V_{CL1}) when the V_{CO} is set to "H" after setting V2 = V3 = 3.5 V.

2. 2 Overdischarge detection voltage (V_{DL1}), overdischarge release voltage (V_{DU1})

The overdischarge detection voltage (V_{DL1}) is V1 when the V_{DO} is set to "L" after decreasing V1 gradually from the initial status 1. After that, increasing V1 gradually, V1 is the overdischarge release voltage (V_{DU1}) when V_{DO} is set to "H".

By changing Vn (n = 2 to 3), users can define the overcharge detection voltage (V_{CUn}), the overcharge release voltage (V_{CLn}), the overdischarge detection voltage (V_{DLn}), the overdischarge release voltage (V_{DUn}) as well when n = 1.

2. 3 Discharge overcurrent detection voltage (V_{DIOV})

The discharge overcurrent detection voltage (V_{DIOV}) is V6 when V_{DO} is set to "L" after increasing V6 gradually from the initial status 1.

2. 4 Load short-circuiting detection voltage (V_{SHORT})

The load short-circuiting detection voltage (V_{SHORT}) is V6 when V_{DO} is set to "L" after increasing V6 gradually after setting S3 to ON from the initial status 1.

2. 5 Charge overcurrent detection voltage (V_{CIOV})

The charge overcurrent detection voltage (V_{CIOV}) is V6 when V_{CO} is set to "L" after decreasing V6 gradually from the initial status 1.

2. 6 CTLC pin change voltage (V_{CTLC})

The CTLC pin change voltage (V_{CTLC}) is V7 when V_{CO} is set to "L" after increasing V7 gradually from the initial status 1.

2. 7 CTLD pin change voltage (V_{CTLD})

The CTLD pin change voltage (V_{CTLD}) is V8 when V_{DO} is set to "L" after increasing V8 gradually from the initial status 1.

2. 8 Load short-circuiting detection delay time (t_{SHORT})

Load short-circuiting detection delay time (t_{SHORT}) is a period in which V_{DO} changes to "L" after changing V6 to 1.5 V instantaneously, after setting S3 to ON from the initial status 1.

2. 9 CTLC pin response time (t_{CTLC})

CTLC pin response time (t_{CTLC}) is a period in which V_{CO} changes to "L" after changing V7 = V_{DS} instantaneously from the initial status 1.

2. 10 CTLD pin response time (t_{CTLD})

CTLD pin response time (t_{CTLD}) is a period in which V_{DO} changes to "L" after changing V8 = V_{DS} instantaneously from the initial status 1.

3. CCT pin internal resistance, CDT pin internal resistance, CIT pin internal resistance, CCT pin detection voltage, CDT pin detection voltage, CIT pin detection voltage (Test circuit 3)

Confirm both V_{CO} and V_{DO} are in "H" after setting V1 = V2 = V3 = 3.5 V, V6 = V9 = V10 = V11 = 0 V (this status is referred to as initial status 2).

3. 1 CCT pin internal resistance (R_{CCT})

The CCT pin internal resistance (R_{CCT}) can be defined by $R_{CCT} = V_{DS} / I_{CCT}$ by using I_{CCT} when setting V1 = 4.5 V from the initial status 2.

3. 2 CDT pin internal resistance (R_{CDT})

The CDT pin internal resistance (R_{CDT}) can be defined by $R_{CDT} = V_{DS} / I_{CDT}$ by using I_{CDT} when setting V1 = 1.5 V from the initial status 2.

3. 3 CIT pin internal resistance (R_{CIT})

The CIT pin internal resistance (R_{CIT}) can be defined by $R_{CIT} = V_{DS} / I_{CIT}$ by using I_{CIT} when setting V6 = V_{DIOV} + 0.015 V from the initial status 2.

3. 4 CCT pin detection voltage (V_{CCT})

The CCT pin detection voltage (V_{CCT}) is V9 when V_{CO} is set to "L" after increasing V9 gradually, after setting V1 = 4.5 V from the initial status 2.

3. 5 CDT pin detection voltage (V_{CDT})

The CDT pin detection voltage (V_{CDT}) is V10 when V_{DO} is set to "L" after increasing V10 gradually, after setting V1 = 1.5 V from the initial status 2.

3. 6 CIT pin detection voltage (V_{CIT})

The CIT pin detection voltage (V_{CIT}) is V11 when V_{DO} is set to "L" after increasing V11 gradually, after setting V6 = V_{DIOV} + 0.015 V from the initial status 2.

4. 0 V battery charge starting charger voltage (0 V battery charge enabled) (Test circuit 4), 0 V battery charge inhibition battery voltage (0 V battery charge inhibited) (Test circuit 2)

4. 1 0 V battery charge starting charger voltage (V_{0CHA}) (0 V battery charge enabled)

The 0 V battery charge starting charger voltage (V_{0CHA}) is V12 when V_{CO} is 0.1 V or higher after increasing V12 gradually after setting V1 = V2 = V3 = 0 V, V12 = 0 V.

4. 2 0 V Battery charge inhibition battery voltage (V_{0INH}) (0 V battery charge inhibited)

The 0 V battery charge inhibition battery voltage (V_{0INH}) is V1 when V_{CO} is set to "L" after decreasing V1 gradually from the initial status 1.

5. CTLC pin internal resistance, CTLD pin internal resistance, resistance between VM pin and VDD pin, resistance between VM pin and VSS pin, VC1 pin current, VC2 pin current, VC3 pin current, VC4 pin current, CO pin source current, CO pin leakage current, DO pin source current, DO pin sink current (Test circuit 5)

Set S1, S5, S6 and S7 to OFF, set S2 and S4 to ON.
Set V1 = V2 = V3 = 3.5 V, V6 = V13 = V14 = V15 = V16 = 0 V (this status is referred to as initial status 3).

5. 1 CTLC pin internal resistance (R_{CTLC})

In the initial status 3, the CTLC pin internal resistance (R_{CTLC}) can be defined by $R_{CTLC} = V_{DS} / I_{CTLC}$ by using I_{CTLC}.

5. 2 CTLD pin internal resistance (R_{CTLD})

In the initial status 3, the CTLD pin internal resistance (R_{CTLD}) can be defined by $R_{CTLD} = V_{DS} / I_{CTLD}$ by using I_{CTLD}.

5. 3 Resistance between VM pin and VDD pin (R_{VMD}) (With power-down function)

The resistance between VM pin and VDD pin (R_{VMD}) can be defined by $R_{VMD} = V_{DS} / I_{VM}$ by using I_{VM} when setting V1 = V2 = V3 = 1.8 V from the initial status 3.

5. 4 Resistance between VM pin and VSS pin (R_{VMS})

The resistance between VM pin and VSS pin (R_{VMS}) can be defined by $R_{VMS} = V_{DS} / I_{VM}$ by using I_{VM} when setting V6 = 1.5 V, S2 to OFF, S1 to ON from the initial status 3.

5. 5 VC1 pin current (I_{VC1}), VC2 pin current (I_{VC2}), VC3 pin current (I_{VC3}), VC4 pin current (I_{VC4})

In the initial status 3, I_1 is the VC1 pin current (I_{VC1}), I_2 is the VC2 pin current (I_{VC2}), I_3 is the VC3 pin current (I_{VC3}), I_4 is the VC4 pin current (I_{VC4}).

5. 6 CO pin source current (I_{COH}), CO pin leakage current (I_{COL})

The CO pin source current (I_{COH}) is I_{CO} when setting V13 = 0.5 V from the initial status 3. After that, the CO pin leakage current (I_{COL}) is I_{CO} when setting V1 = V2 = V3 = 8 V, S4 to OFF, S5 to ON.

5. 7 DO pin source current (I_{DOH}), DO pin sink current (I_{DOL})

The DO pin source current (I_{DOH}) is I_{DO} when setting V14 = 0.5 V, S6 to ON from the initial status 3. After that, the DO pin sink current (I_{DOL}) is I_{DO} when setting V1 = V2 = V3 = 1.8 V, V15 = 0.5 V, S6 to OFF, S7 to ON.

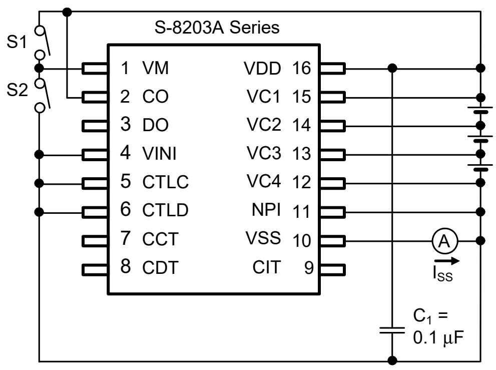


Figure 4 Test Circuit 1

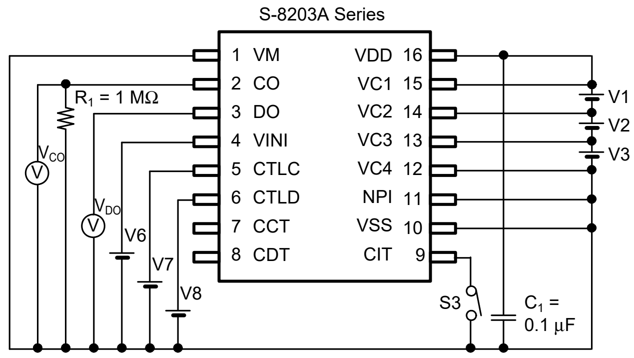


Figure 5 Test Circuit 2

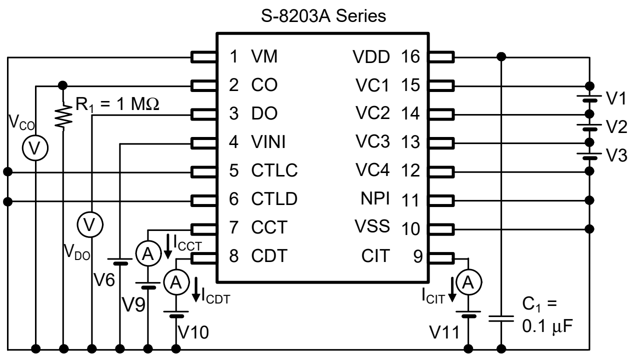


Figure 6 Test Circuit 3

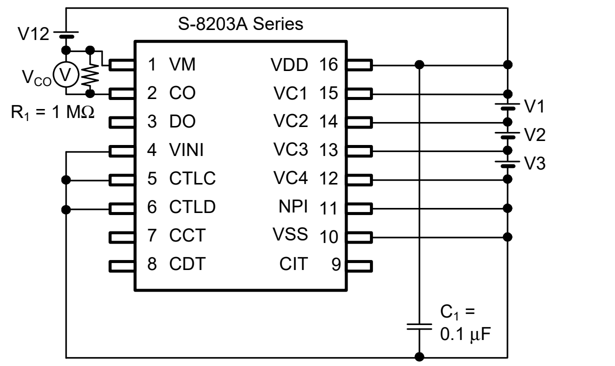


Figure 7 Test Circuit 4

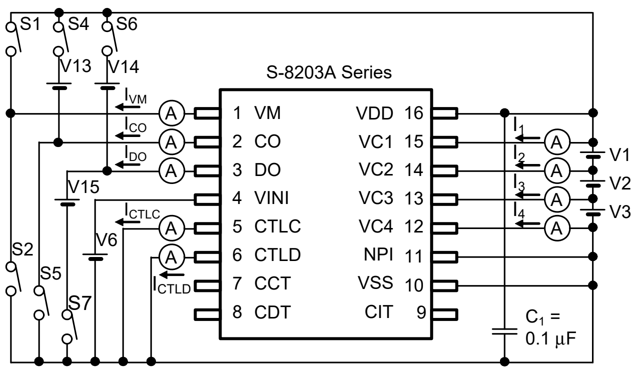


Figure 8 Test Circuit 5

■ Operation

Remark Refer to "**■ Connection Example of Battery Protection IC**".

1. Normal status

In the S-8203A Series, when the voltage of each of the batteries is in the range from overdischarge detection voltage (V_{DLn}) to overcharge detection voltage (V_{CUn}), and the VINI pin voltage is in the range from charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent detection voltage (V_{DIOV}), both of CO pin and DO pin get the V_{DD} level. This is the normal status. At this time, the charge and discharge FETs are on.

2. Overcharge status

In the S-8203A Series, when the voltage of one of the batteries increases to the level of higher than V_{CUn}, the CO pin is set in high impedance. This is the overcharge status. The CO pin is pulled down to EB– by an external resistor so that the charge FET is turned off and it stops charging.

The overcharge status is released if either condition mentioned below is satisfied;

(1) In case that the CO pin voltage is $1 / 50 \times V_{DS}$ or lower, and the voltage of each of the batteries which are V_{CUn} or higher is in the level of overcharge release voltage (V_{CLn}) or lower.
(2) In case that the CO pin voltage is $1 / 50 \times V_{DS}$ or higher, and the voltage of each of the batteries is in the level of V_{CUn} or lower.

3. Overdischarge status

In The S-8203A Series, when the voltage of one of the batteries decreases to the level of V_{DLn} or lower, the DO pin voltage gets the V_{SS} level. This is the overdischarge status. The discharge FET is turned off and it stops discharging.

The overdischarge status is released if either condition mentioned below is satisfied;

(1) In case that the VM pin voltage is in the level of lower than V_{SS}, and the voltage of each of the batteries is in the level of V_{DLn} or higher.
(2) In case that the VM pin voltage is V_{DS} / 5 (typ.) or lower and the VM pin voltage is in the level of higher than V_{SS}, and the voltage of each of the batteries which are V_{DLn} or lower is in the level of overdischarge release voltage (V_{DUn}) or higher.

3. 1 With power-down function

In The S-8203A Series, when it reaches the overdischarge status, the VM pin is pulled up to the V_{DD} level by a resistor between VM pin and VDD pin (R_{VMD}). If the VM pin voltage and the CO pin voltage increase to the level of V_{DS} / 5 (typ.) or higher, respectively, the power-down function starts to operate and almost every circuit in the S-8203A Series stops working.

The power-down function is released if either condition mentioned below is satisfied;

(1) The VM pin voltage gets V_{DS} / 5 (typ.) or lower.
(2) The CO pin voltage gets V_{DS} / 5 (typ.) or lower.

4. Discharge overcurrent status

The discharging current increases to a certain value or higher. As a result, if the status in which the VINI pin voltage increases to the level of V_{DIOV} or higher, the DO pin gets the V_{SS} level. This is the discharge overcurrent status. The discharge control FET is turned off and it stops discharging. In the status of discharge overcurrent, the CO pin is set in high impedance. The VM pin is pulled down to the V_{SS} level by a resistor between VM pin and VSS pin (R_{VMS}).

The S-8203A Series has two levels for discharge overcurrent detection (V_{DIOV}, V_{SHORT}).
The S-8203A Series' actions against load short-circuiting detection voltage (V_{SHORT}) are as well in V_{DIOV}.

The discharge overcurrent status is released if the following condition is satisfied.

(1) The VM pin voltage gets V_{DS} / 10 (typ.) or lower.

5. Charge overcurrent status

In the S-8203A Series, the charge current increases to a certain value or higher. As a result, if the status in which the VINI pin voltage decreases to the level of V_{CIOV} or lower, the CO pin is set in high impedance. This is the charge overcurrent status. The charge control FET is turned off and it stops charging. In this charge overcurrent status, DO pin gets the V_{SS} level. The VM pin is pulled up to the V_{DD} level by resistance between VM pin and VDD pin (R_{VMD}).

The charge overcurrent status is released if the following condition is satisfied.

(1) The CO pin voltage gets 1 / 50 × V_{DS} (typ.) or higher.

6. 0 V Battery charge

In the S-8203A Series, regarding how to charge a discharged battery (0 V battery), users are able to select either function mentioned below.

(1) Enable to charge a 0 V battery
A 0 V battery is charged when charger voltage is higher than 0 V battery charge starting charger voltage (V_{0CHA}).

(2) Inhibit charging a 0 V battery
A 0 V battery is not charged when the voltage of one of the batteries is 0 V battery charge inhibition battery voltage (V_{0INH}) or lower.

Caution When the VDD pin voltage is lower than the minimum value of operation voltage between VDD pin and VSS pin (V_{DSOP}), the S-8203A Series' action is not assured.

7. Delay time setting

In the S-8203A Series, users are able to set delay time for the period; from detecting the voltage of one of the batteries or detecting changes in the voltage at the VINI pin, to the output to the CO pin, DO pin. Each delay time is determined by a resistor in the IC and an external capacitor.

In the overchage detection, when the voltage of one of the batteries gets V_{CUn} or higher, the S-8203A Series starts charging to the CCT pin's capacitor (C_{CCT}) via the CCT pin's internal resistor (R_{CCT}). After a certain period, the CO pin is set in high impedance if the voltage at the CCT pin reaches the CCT pin detection voltage (V_{CCT}). This period is overcharge detection delay time (t_{CU}).

t_{CU} is calculated using the following equation ($V_{DS} = V1 + V2 + V3$).

$$t_{CU}\ [s] = -\ln(1 - V_{CCT} / V_{DS}) \times C_{CCT}\ [\mu F] \times R_{CCT}\ [M\Omega]$$
$$= -\ln(1 - 0.7\ (typ.)) \times C_{CCT}\ [\mu F] \times 8.31\ [M\Omega]\ (typ.)$$
$$= 10.0\ [M\Omega]\ (typ.) \times C_{CCT}\ [\mu F]$$

Overdischarge detection delay time (t_{DL}), discharge overcurrent detection delay time (t_{DIOV}), charge overcurrent detection delay time (t_{CIOV}) are calculated using the following equations as well.

$$t_{DL}\ [ms] = -\ln(1 - V_{CDT} / V_{DS}) \times C_{CDT}\ [\mu F] \times R_{CDT}\ [k\Omega]$$
$$t_{DIOV}\ [ms] = -\ln(1 - V_{CIT} / V_{DS}) \times C_{CIT}\ [\mu F] \times R_{CIT}\ [k\Omega]$$
$$t_{CIOV}\ [ms] = -\ln(1 - V_{CIT} / V_{DS}) \times C_{CIT}\ [\mu F] \times R_{CIT}\ [k\Omega]$$

In case $C_{CCT} = C_{CDT} = C_{CIT} = 0.1\ [\mu F]$, each delay time t_{CU}, t_{DL}, t_{DIOV}, t_{CIOV} is calculated as follows.

$$t_{CU}\ [s] = 10.0\ [M\Omega]\ (typ.) \times 0.1\ [\mu F] = 1.0\ [s]\ (typ.)$$
$$t_{DL}\ [ms] = 1000\ [k\Omega]\ (typ.) \times 0.1\ [\mu F] = 100\ [ms]\ (typ.)$$
$$t_{DIOV}\ [ms] = 200\ [k\Omega]\ (typ.) \times 0.1\ [\mu F] = 20\ [ms]\ (typ.)$$
$$t_{CIOV}\ [ms] = 200\ [k\Omega]\ (typ.) \times 0.1\ [\mu F] = 20\ [ms]\ (typ.)$$

Discharge overcurrent release delay time (t_{DIOVR}) and charge overcurrent release delay time (t_{CIOVR}) can be selected from two types, and they are calculated by t_{DIOV} and t_{CIOV} as the following equations. 1 [ms] (typ.) is the internal delay time of the S-8203A Series.

(1) $t_{DIOVR} = t_{DIOV} \times 10 + 1$ [ms] (typ.), $t_{CIOVR} = t_{CIOV} \times 10 + 1$ [ms] (typ.)

(2) $t_{DIOVR} = t_{DIOV} \times 0.05 + 1$ [ms] (typ.), $t_{CIOVR} = t_{CIOV} \times 0.05 + 1$ [ms] (typ.)

Load short-circuiting detection delay time (t_{SHORT}) is fixed internally.

8. CTLC pin and CTLD pin

The S-8203A Series has two pins to control.
The CTLC pin controls the CO pin, the CTLD pin controls the DO pin. Thus it is possible for users to control the CO pin and DO pin independently. These controls precede the battery protection circuit.

Table 6 Conditions Set by CTLC Pin

CTLC Pin	CO Pin
CTLC pin voltage ≥ V_{CTLC}	High-Z
Open*1	High-Z
CTLC pin voltage < V_{CTLC}	Normal status*2

***1.** Pulled up by R_{CTLC} when CTLC pin is open.
***2.** The status is controlled by the voltage detection circuit.

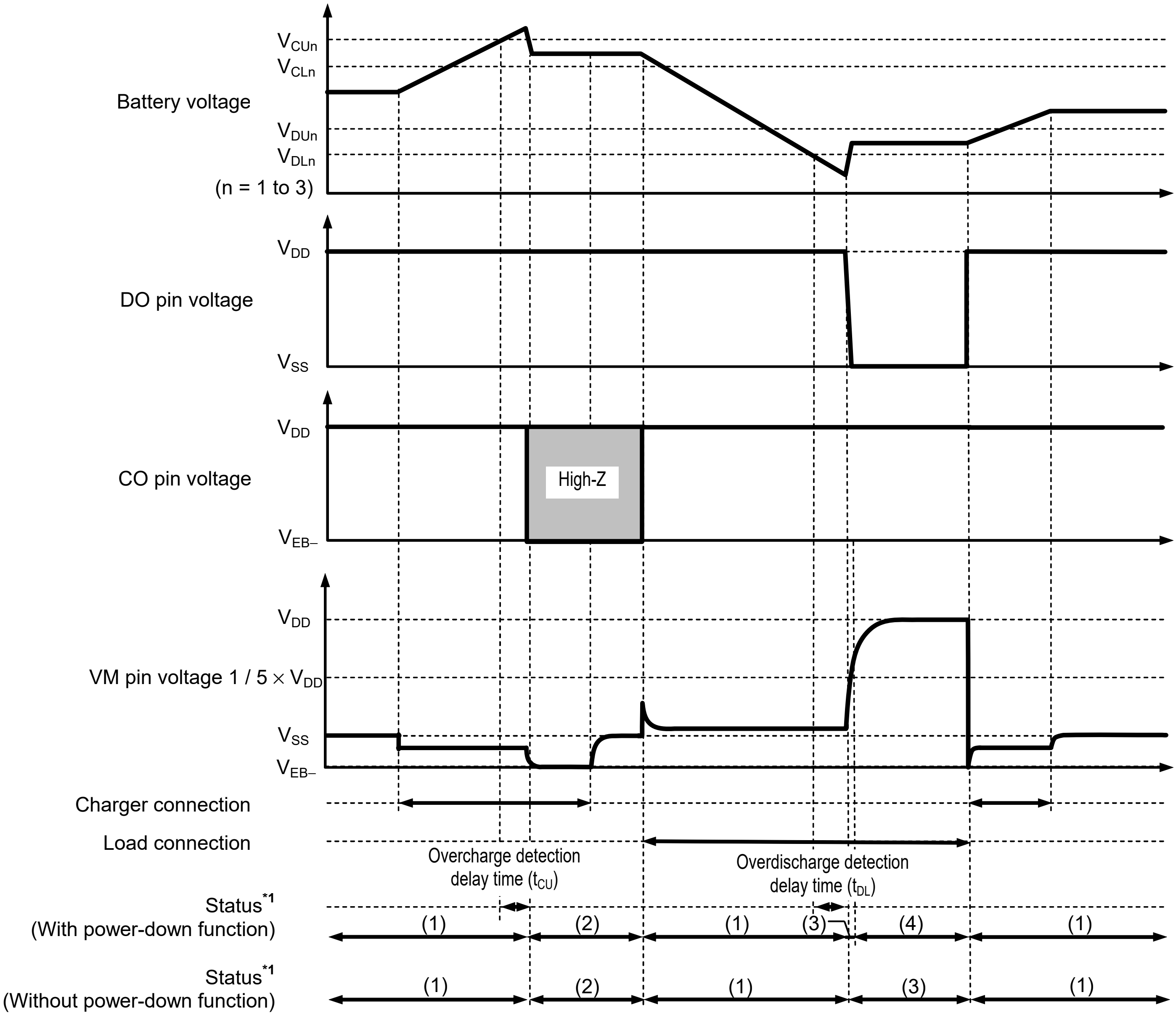
Table 7 Conditions Set by CTLD Pin

CTLD Pin	DO Pin
CTLD pin voltage ≥ V_{CTLD}	V_{SS} level
Open*1	V_{SS} level
CTLD pin voltage < V_{CTLD}	Normal status*2

***1.** Pulled up by R_{CTLD} when CTLD pin is open.
***2.** The status is controlled by the voltage detection circuit.

■ Timing Charts

1. Overcharge detection and overdischarge detection

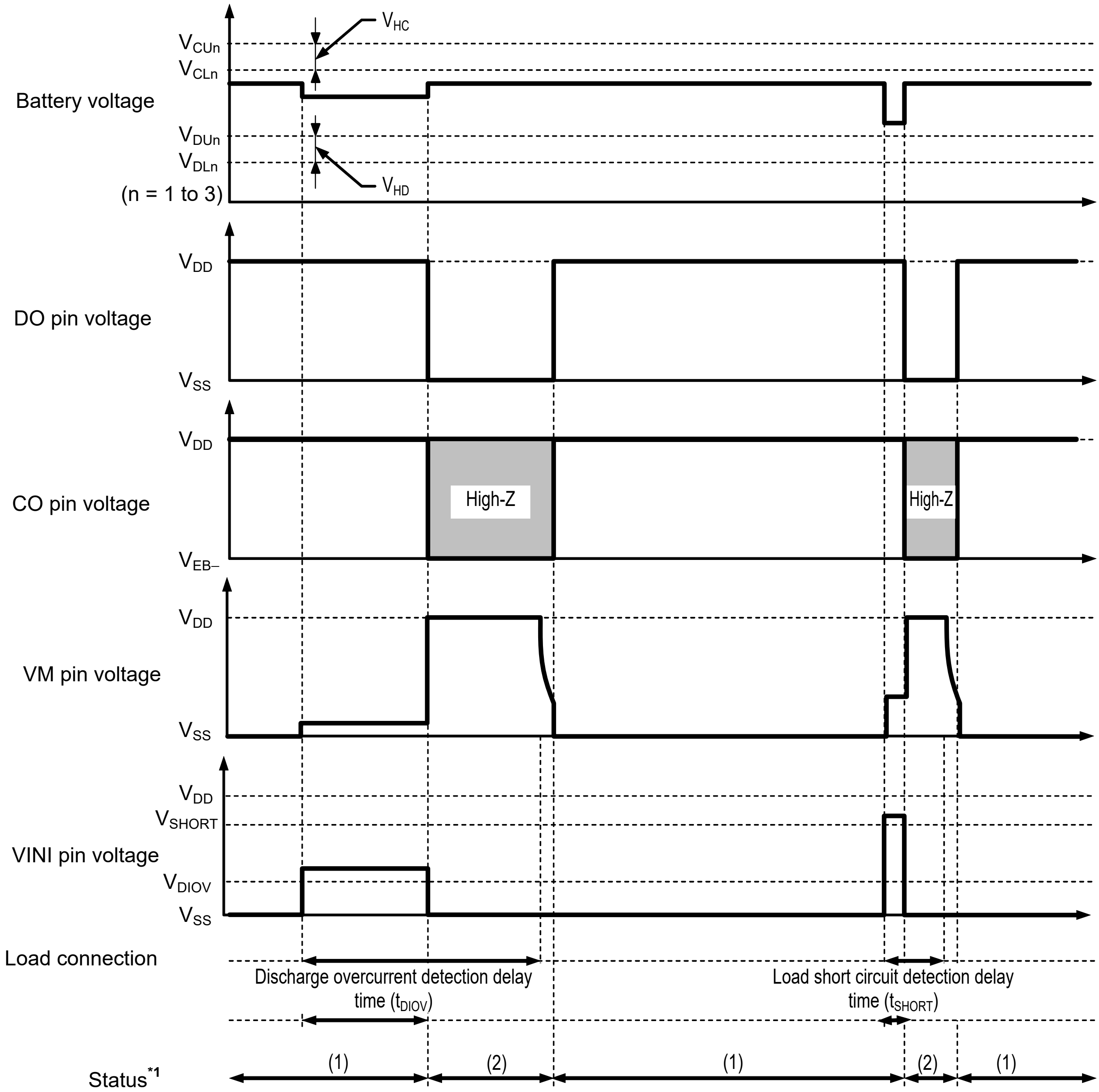


***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status
(4): Power-down status

Remark The charger is assumed to charge with a constant current. V_{EB-} indicates the open voltage of the charger.

Figure 9

2. Discharge overcurrent detection

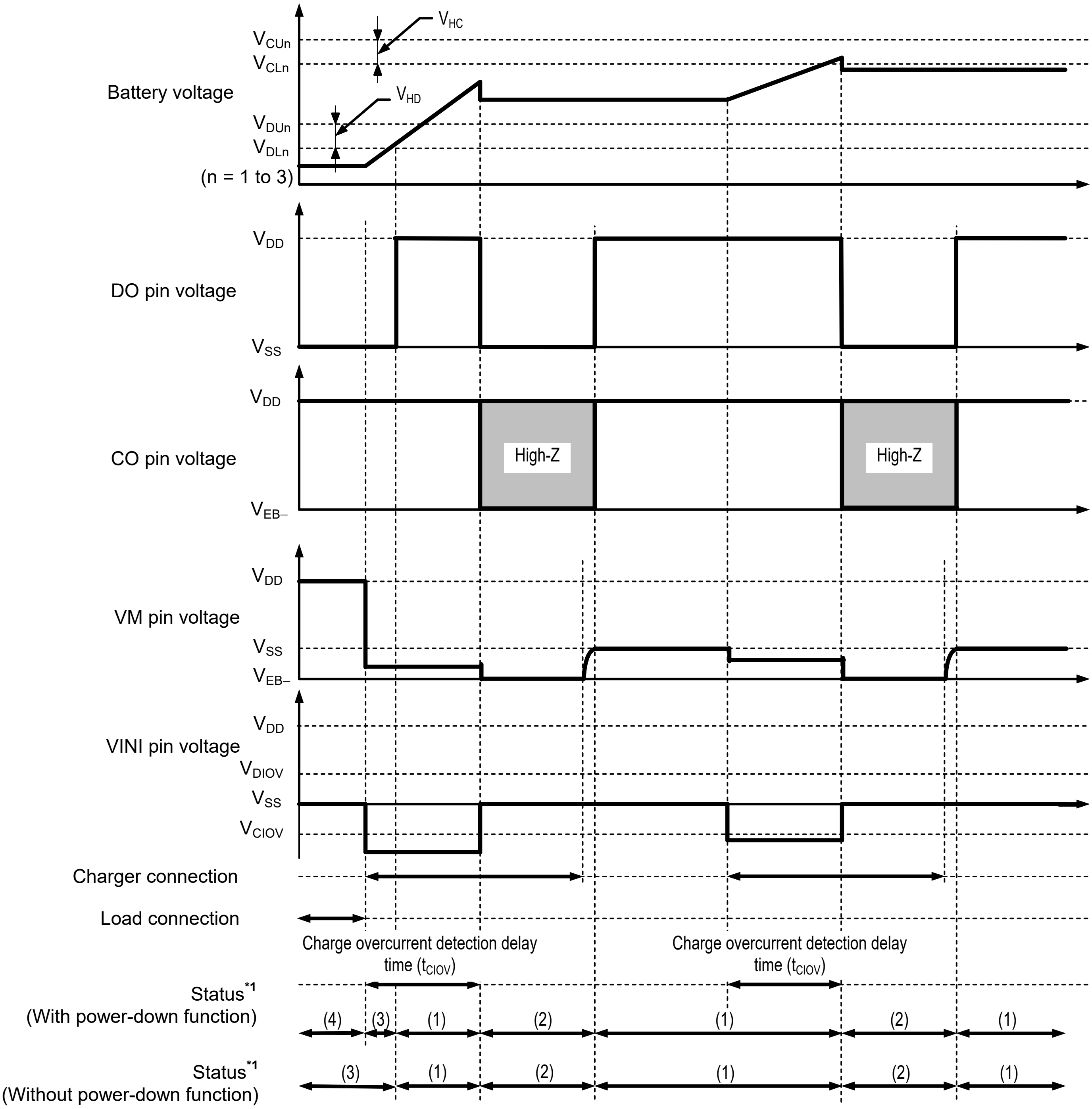


***1.** (1): Normal status
(2): Discharge overcurrent status

Remark The charger is assumed to charge with a constant current. V_{EB-} indicates the open voltage of the charger.

Figure 10

3. Charge overcurrent detection



***1.** (1): Normal status
(2): Charge overcurrent status
(3): Overdischarge status
(4): Power-down status

Remark The charger is assumed to charge with a constant current. V_{EB-} indicates the open voltage of the charger.

Figure 11

■ Connection Example of Battery Protection IC

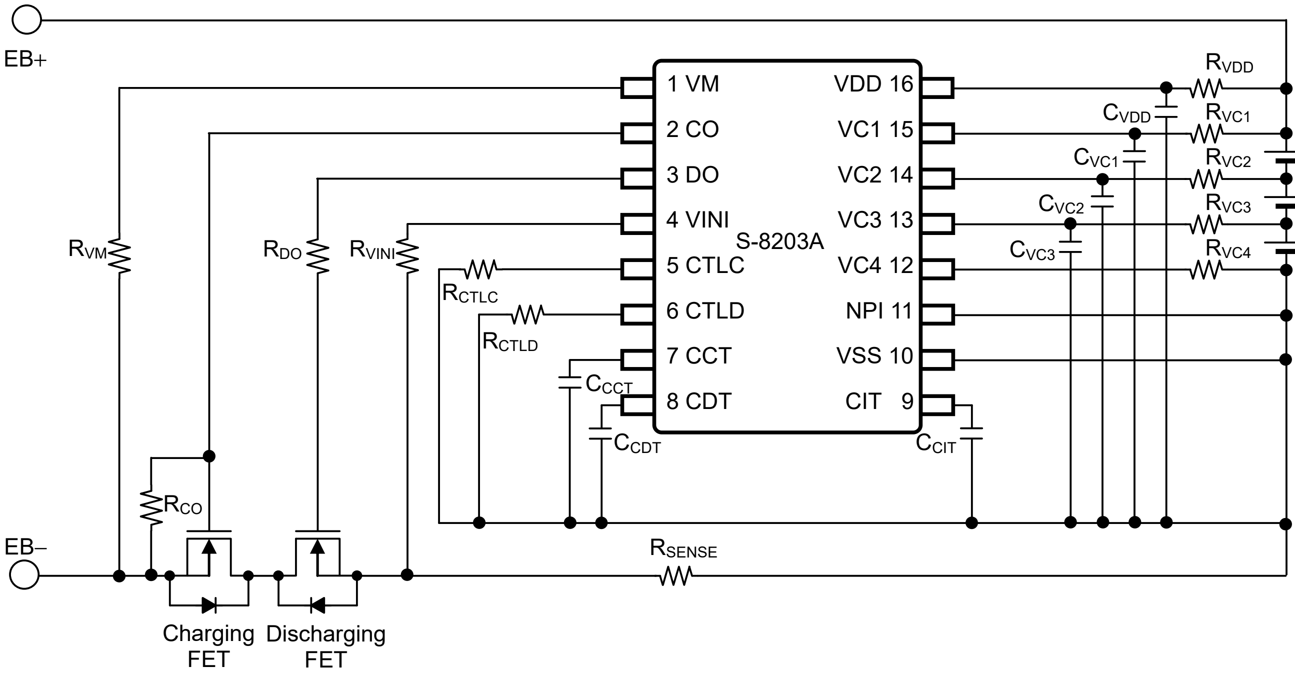


Figure 12

■ Application Circuit

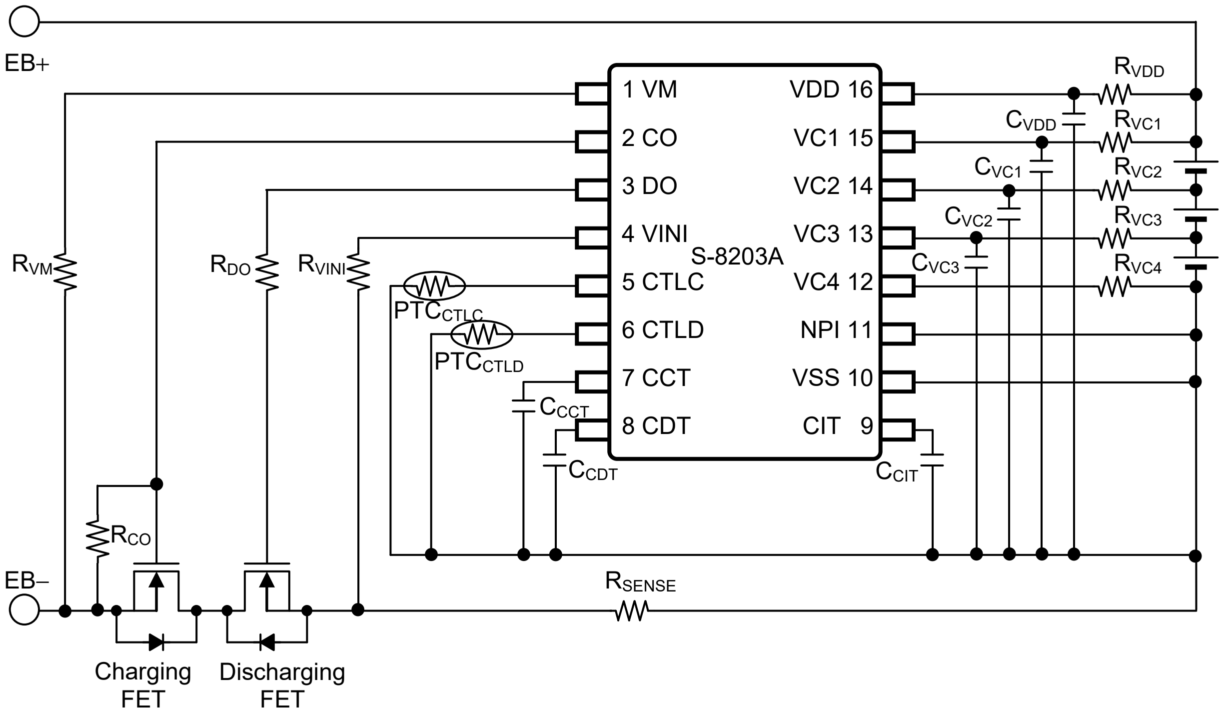


Figure 13 Overheat Protection via PTC

[For PTC, contact]

Murata Manufacturing Co., Ltd.
Thermistor Products Department
Nagaokakyo-shi, Kyoto 617-8555 Japan
TEL +81-75-955-6863
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Table 8 Constants for External Components

Symbol	Min.	Typ.	Max.	Unit
R_{VC1}*1	0.47	1	1	kΩ
R_{VC2}*1	0.47	1	1	kΩ
R_{VC3}*1	0.47	1	1	kΩ
R_{VC4}*1	0.47	1	1	kΩ
R_{DO}	1	5.1	10	kΩ
R_{CO}	0.1	1	1	MΩ
R_{VM}	3	5.1	10	kΩ
R_{CTLC}	0.1	1	1	kΩ
R_{CTLD}	0.1	1	1	kΩ
R_{VINI}	0.1	1	1	kΩ
R_{SENSE}	0	–	–	mΩ
R_{VDD}*1	43	100	100	Ω
C_{VC1}*1	0.068	0.1	1	μF
C_{VC2}*1	0.068	0.1	1	μF
C_{VC3}*1	0.068	0.1	1	μF
C_{CCT}	0.01	0.1	–	μF
C_{CDT}	0.01	0.1	–	μF
C_{CIT}	0.02	0.1	–	μF
C_{VDD}*1	0	1	10	μF

***1.** Set up a filter constant to be $R_{VDD} \times C_{VDD}$ = 68 μF•Ω or more, and to be $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VC3} \times C_{VC3} = R_{VDD} \times C_{VDD}$.

Caution 1. The constants may be changed without notice.

2. It is recommended that filter constants between VDD pin and VSS pin should be set approximately to 100 μF•Ω.

e.g., $C_{VDD} \times R_{VDD}$ = 1.0 μF × 100 Ω = 100 μF•Ω

Sufficient evaluation of transient power supply fluctuation and overcurrent protection function with the actual application is needed to determine the proper constants. Contact our sales representatives in case the constants should be set to other than 100 μF•Ω.

3. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

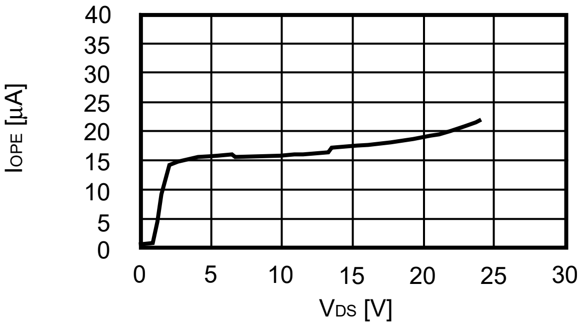
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order, however, there may be cases when discharging cannot be performed when a battery is connected. In this case, short the VM pin and VSS pin or connect the battery charger to return to the normal status.
- If both an overcharge battery and an overdischarge battery are included among the whole batteries, the condition is set in overcharge status and overdischarge status. Therefore either charging or discharging is impossible.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

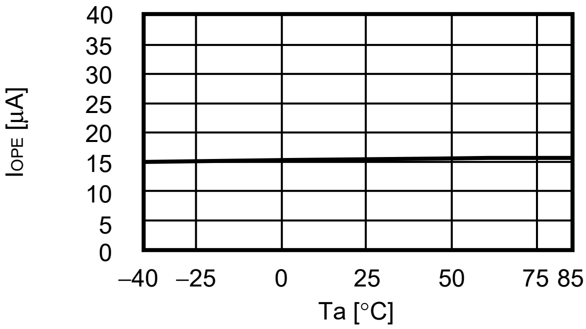
■ Characteristics (Typical Data)

1. Current consumption

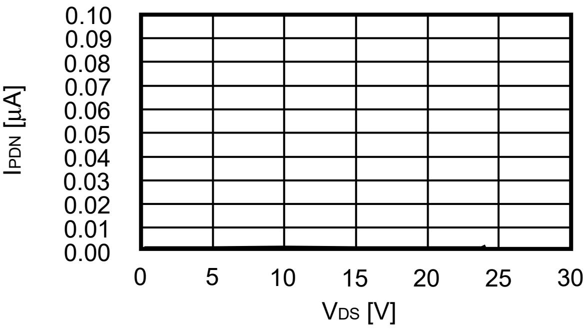
1. 1 I_{OPE} vs V_{DS}



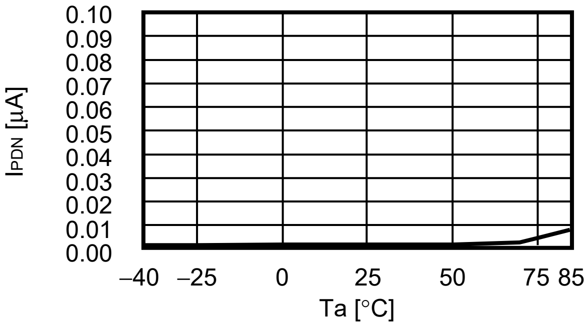
1. 2 I_{OPE} vs Ta



1. 3 I_{PDN} vs V_{DS}

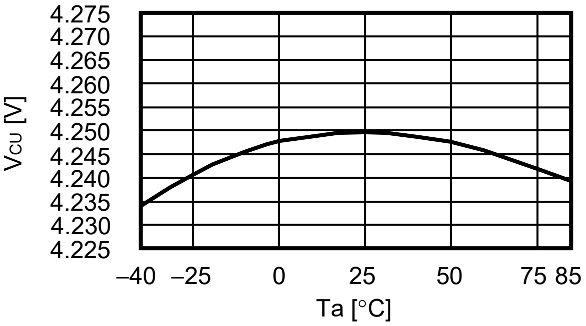


1. 4 I_{PDN} vs Ta

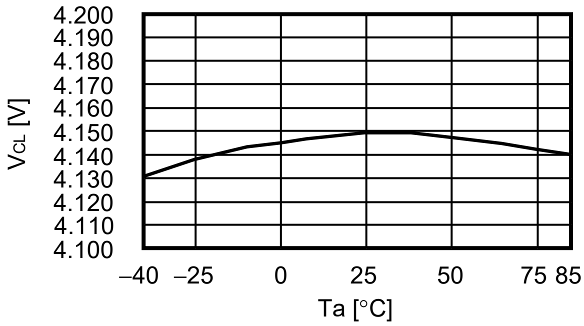


2. Overcharge detection / release voltage, overdischarge detection / release voltage, discharge overcurrent detection voltage, load short-circuiting detection voltage, charge overcurrent detection voltage

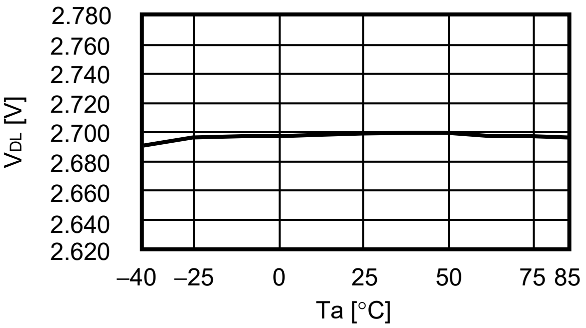
2. 1 V_{CU} vs Ta



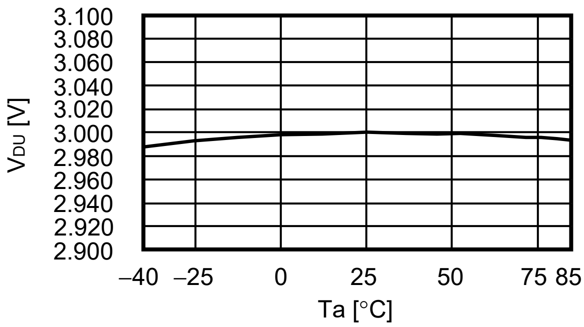
2. 2 V_{CL} vs Ta



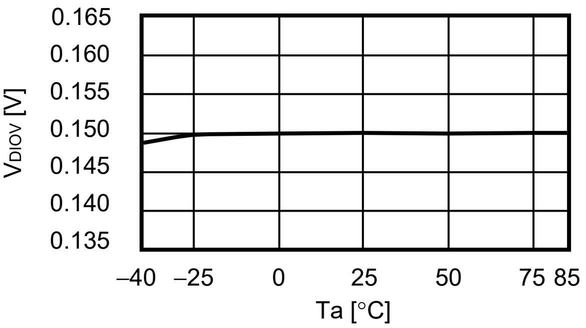
2. 3 V_{DL} vs Ta



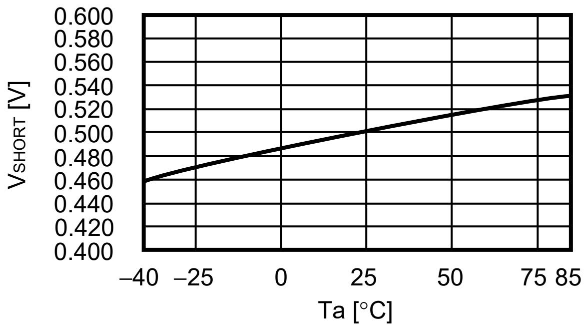
2. 4 V_{DU} vs Ta



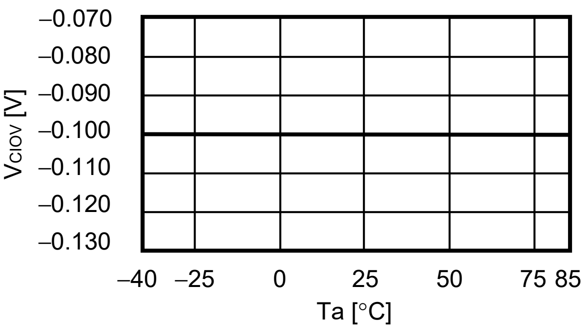
2. 5 V_{DIOV} vs Ta



2. 6 V_{SHORT} vs Ta

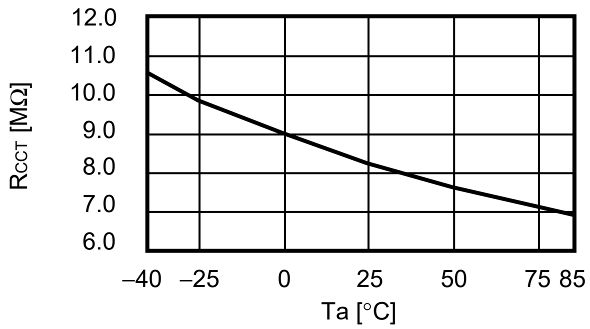


2. 7 V_{CIOV} vs Ta

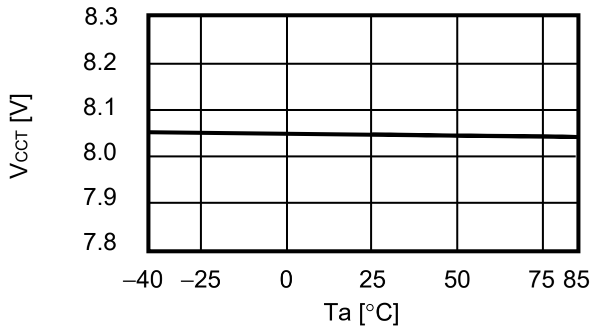


3. CCT pin internal resistance / detection voltage, CDT pin internal resistance / detection voltage, CIT pin internal resistance / detection voltage and short-circuiting detection voltage delay time

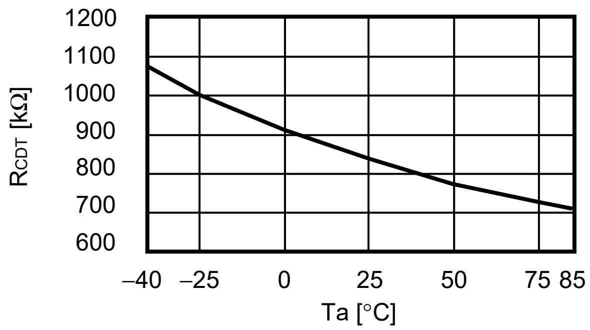
3. 1 R_{CCT} vs Ta



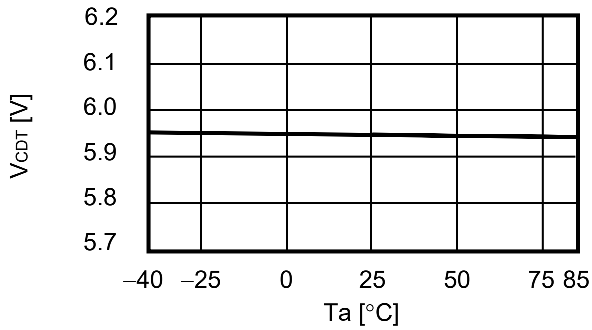
3. 2 V_{CCT} vs Ta (V_{DS} = 11.5 V)



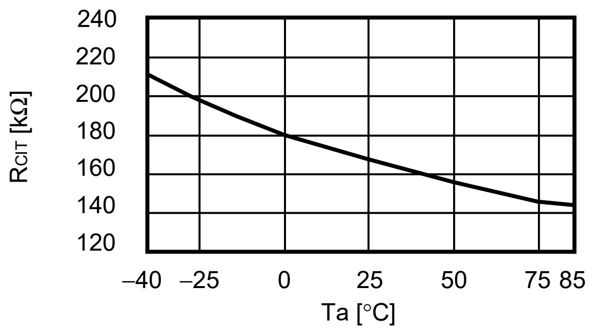
3. 3 R_{CDT} vs Ta



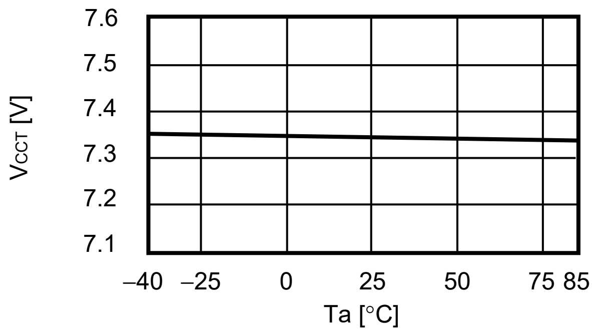
3. 4 V_{CDT} vs Ta (V_{DS} = 8.5 V)



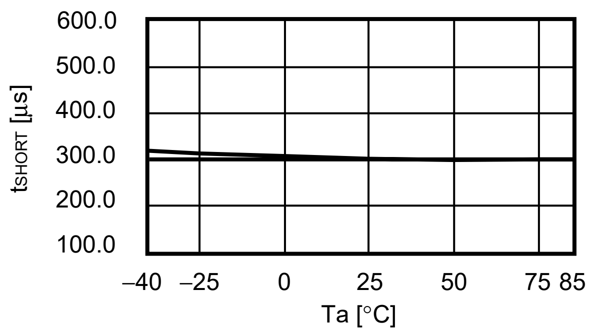
3. 5 R_{CIT} vs Ta



3. 6 V_{CIT} vs Ta (V_{DS} = 10.5 V)

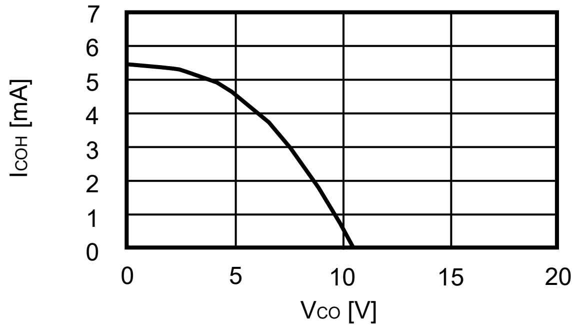


3. 7 t_{SHORT} vs Ta

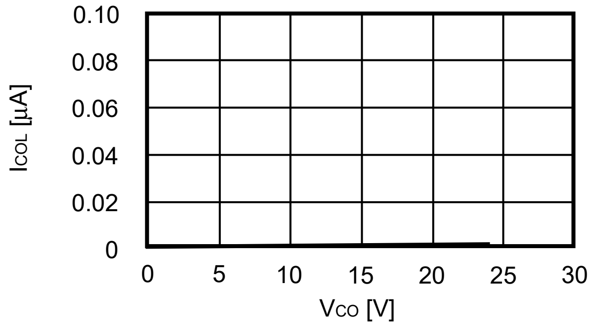


4. CO pin source / leakage current, DO pin source / sink current

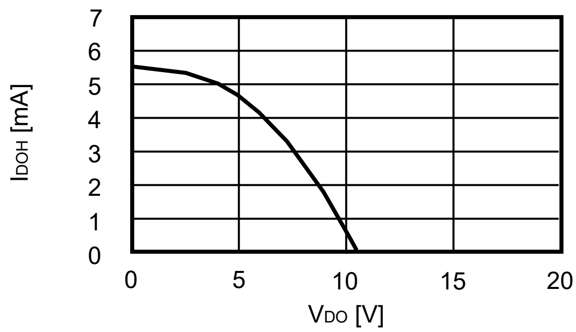
4. 1 I_{COH} vs V_{CO}



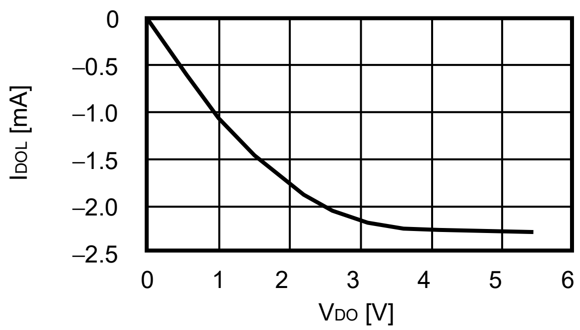
4. 2 I_{COL} vs V_{CO}

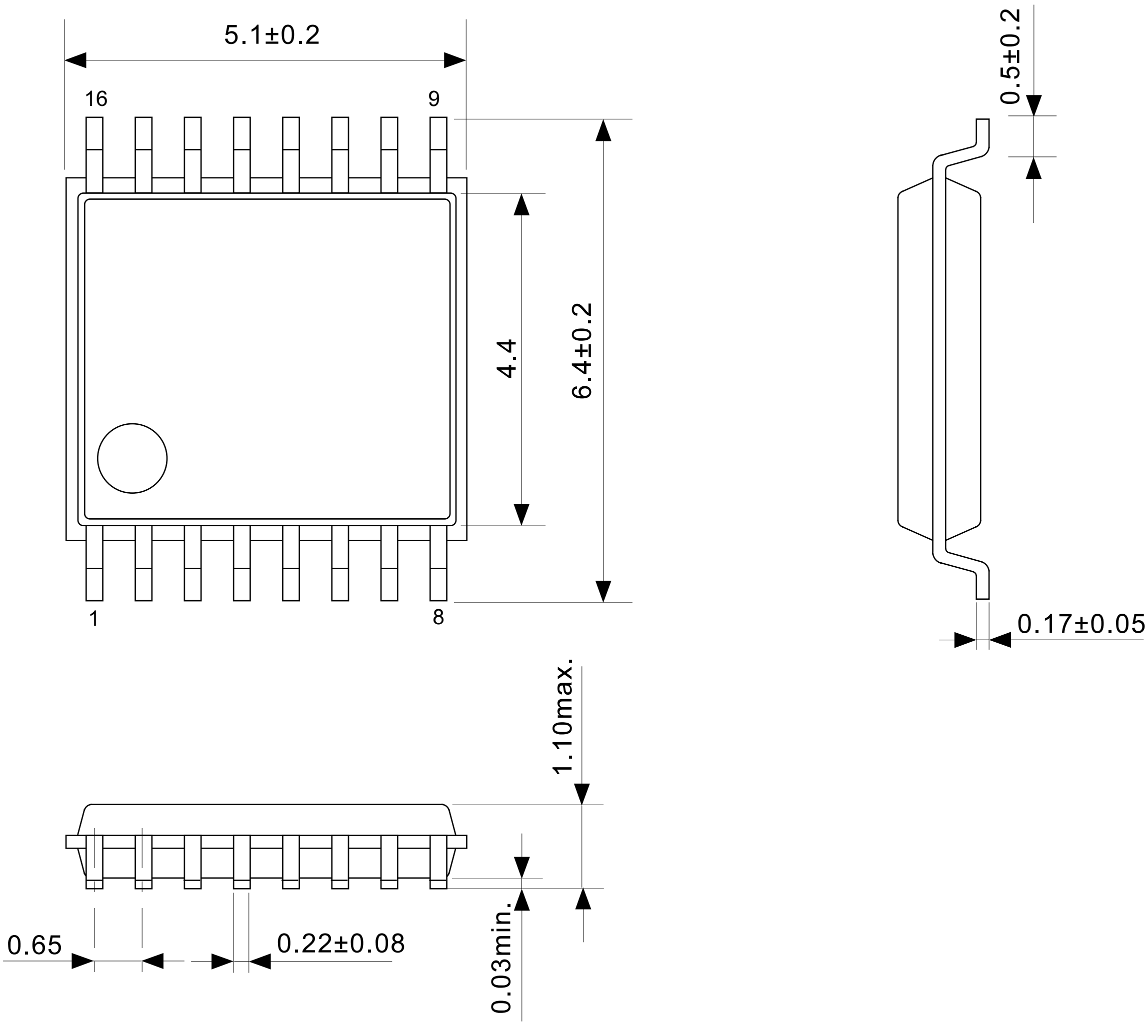


4. 3 I_{DOH} vs V_{DO}



4. 4 I_{DOL} vs V_{DO}





No. FT016-A-P-SD-1.2

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UNIT	mm

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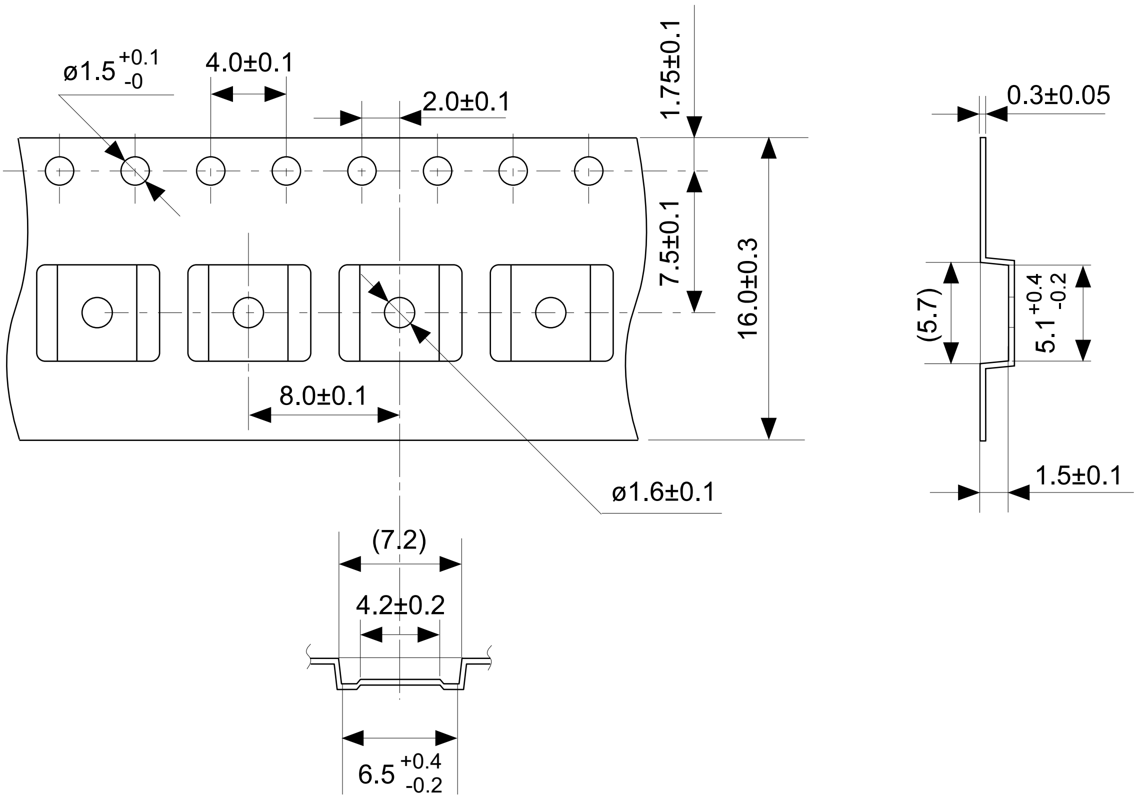

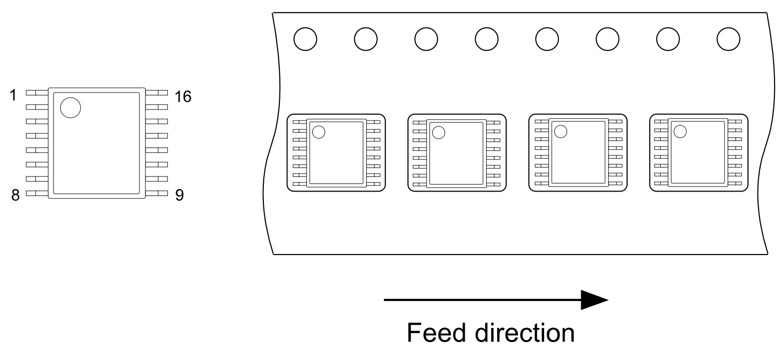

No. FT016-A-C-SD-1.1

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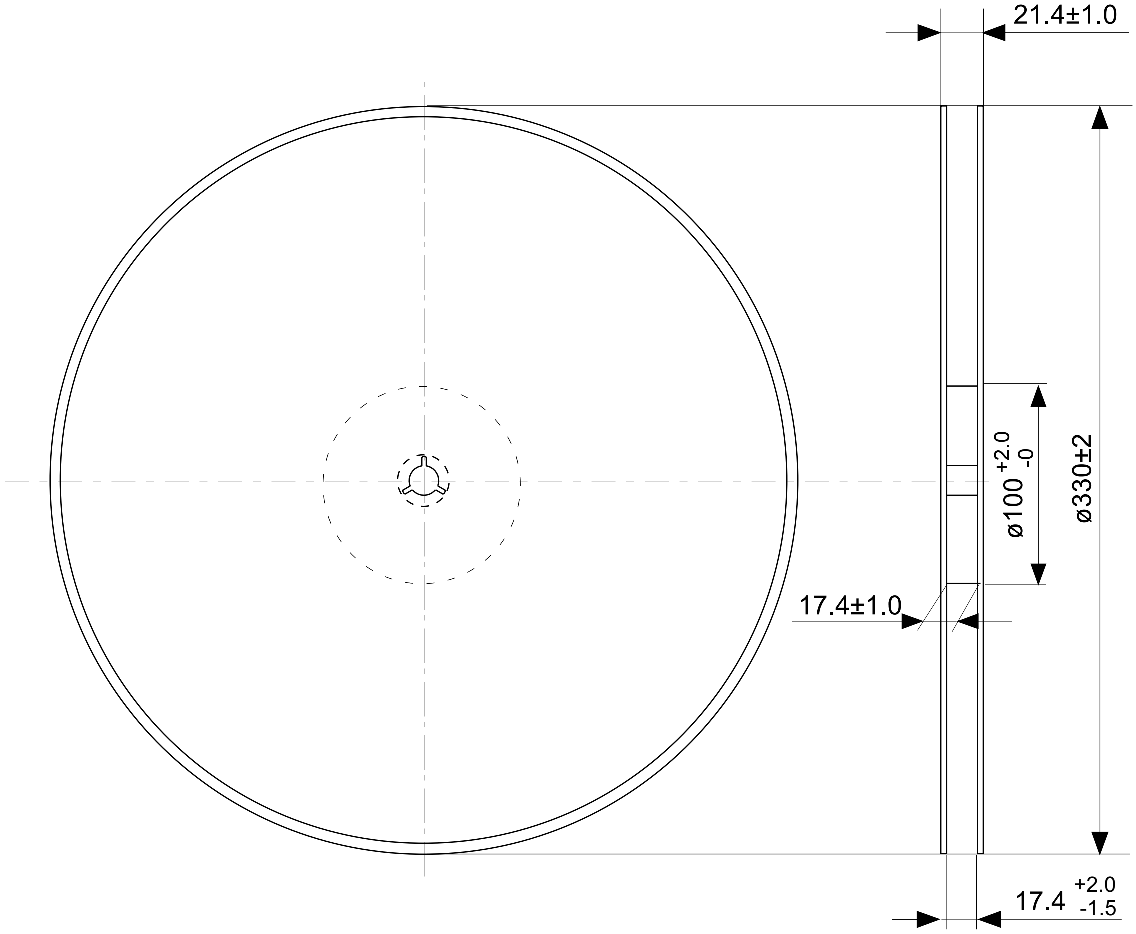
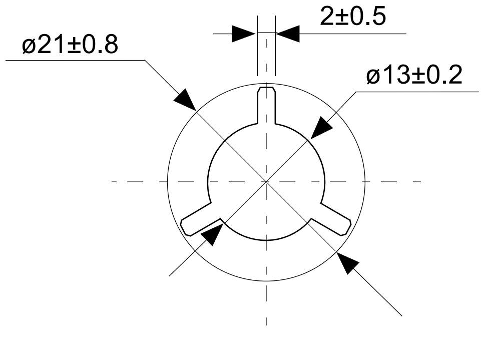
No.	FT016-A-C-SD-1.1
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FT016-A-R-S1-1.0

TITLE	TSSOP16-A- Reel		
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UNIT	mm		

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10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
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