

This IC, developed using CMOS technology, is a high-accuracy window voltage detector with the supply voltage divided output that detects undervoltage and overvoltage. The detection voltage and release voltage are fixed internally with an accuracy of  $\pm 1.5\%$ .

Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared, so the output is stable even if the SENSE pin voltage ( $V_{SENSE}$ ) falls to 0 V. The SENSE pin also has a built-in reverse connection protection circuit that reduces current in the SENSE pin during a reverse connection.

The release signal can be delayed by setting a capacitor externally, and the release delay time accuracy is  $\pm 15\%$  ( $C_D = 3.3$  nF). The output form is Nch open-drain output.

The supply voltage divided output is prepared in this IC. The supply voltage divided output is a function that divides the  $V_{SENSE}$  into  $V_{SENSE}/6$ ,  $V_{SENSE}/8$ ,  $V_{SENSE}/12$  or  $V_{SENSE}/14$  and outputs the voltage. For example, this function makes it possible that the IC connects to a low voltage microcontroller A/D converter directly and the microcontroller monitors a battery voltage.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.

For more information regarding our FIT rate calculation, contact our sales representatives.

**Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

## ■ Features

### Detector block

- |   |                                |   |
|---|--------------------------------|---|
| • Detection voltage:  | Undervoltage detection voltage | 4.0 V to 10.0 V (0.05 V step)                 |
|   | Overvoltage detection voltage  | 16.0 V to 18.0 V (0.1 V step)                 |
| • Detection voltage accuracy:                                   | Undervoltage detection voltage | $\pm 1.5\%$                                   |
|   | Overvoltage detection voltage  | $\pm 1.5\%$                                   |
| • Hysteresis width selectable from "Available" / "Unavailable": |                                | "Available": 5.0%, 10.0%<br>"Unavailable": 0% |
| • Release delay time accuracy:                                  |                                | $\pm 15\%$ ( $C_D = 3.3$ nF)                  |
| • Output form:  |                                | Nch open-drain output                         |

### Supply voltage divider block

- |                                  |  |
|----------------------------------|--|
| • Output voltage:                | $V_{PMOUT} = V_{SENSE}/6$ (S-191L Series L / M / N type)       |
|                                  | $V_{PMOUT} = V_{SENSE}/8$ (S-191L Series P / Q / R type)       |
|                                  | $V_{PMOUT} = V_{SENSE}/12$ (S-191N Series L / M / N type)      |
|                                  | $V_{PMOUT} = V_{SENSE}/14$ (S-191N Series P / Q / R type)      |
| • Output capacitor ( $C_{PM}$ ): | A ceramic capacitor can be used (0.1 $\mu$ F to 0.22 $\mu$ F). |
| • Built-in enable circuit:       | Ensures long battery life.                                     |

### Overall

- |   |   |                  |
|---|---|------------------|
| • Current consumption:                            | During supply voltage divided output operates                 | 1.3 $\mu$ A typ. |
|   | During supply voltage divided output stops                    | 0.9 $\mu$ A typ. |
| • Built-in reverse connection protection circuit: | Reduces current in the SENSE pin during a reverse connection. |                  |
| • Operation voltage range:                        | 3.0 V to 36.0 V   |                  |
| • Operation temperature range:                    | $T_a = -40^\circ\text{C}$ to $+105^\circ\text{C}$             |                  |
| • Lead-free (Sn 100%), halogen-free               |   |                  |
| • AEC-Q100 in process*1                           |   |                  |

\*1. Contact our sales representatives for details.

## ■ Applications

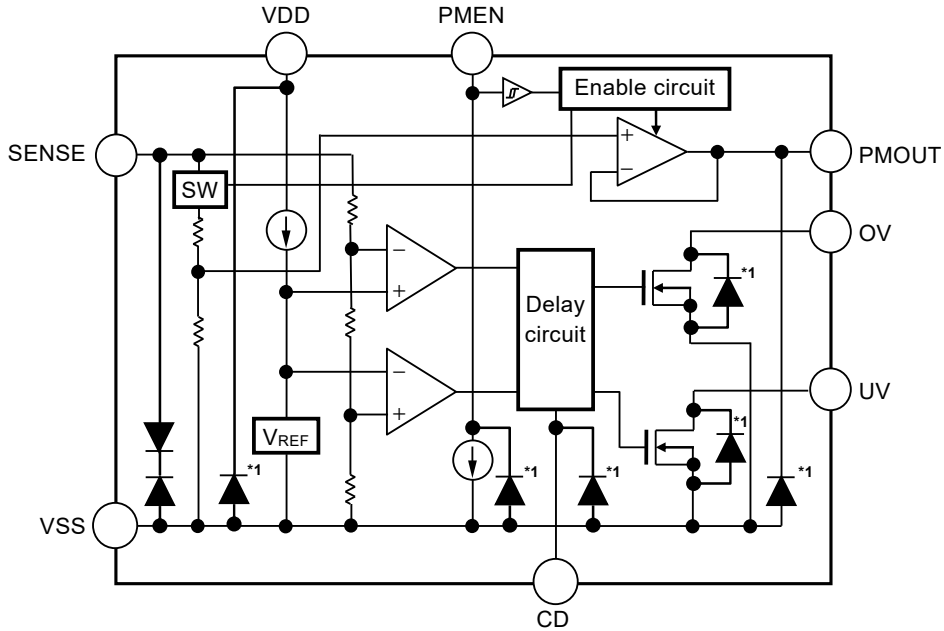
- Overvoltage detection of power supply for automotive electric component
- Automotive battery voltage detection
- For automotive use (car body, headlight, ITS, accessory, car navigation system, car audio system, etc.)

## ■ Packages

- HTMSOP-8
- HSNT-8(2030)

■ **Block Diagrams**

1. **S-191L/191N Series L / P type**



\*1. Parasitic diode

Figure 1

1.1 **S-191L Series**

Table 1

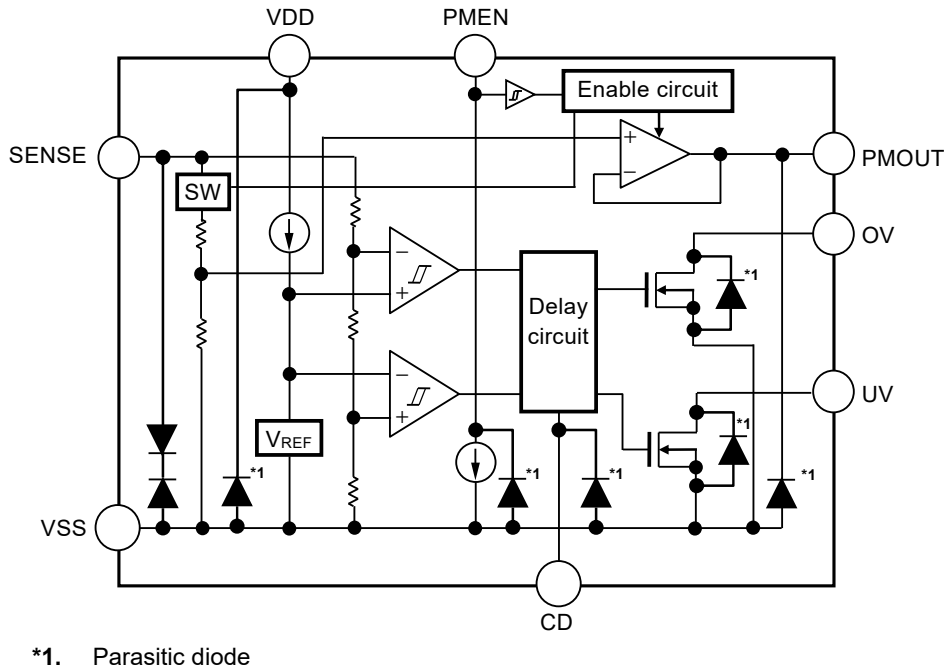
| Product Type | Output Voltage of Supply Voltage Divider Block ( $V_{PMOUT}$ ) | Hysteresis Width ( $V_{UVHYS}$ , $V_{OVHYS}$ ) | PMEN Pin Input Logic | UV, OV Pin Output Form | UV, OV Pin Output Logic |
|--------------|--|--|----------------------|------------------------|-------------------------|
| L type       | $V_{SENSE}/6$  | 0%   | Active "H"           | Nch open-drain output  | Active "L"              |
| P type       | $V_{SENSE}/8$  | 0%   | Active "H"           | Nch open-drain output  | Active "L"              |

1.2 **S-191N Series**

Table 2

| Product Type | Output Voltage of Supply Voltage Divider Block ( $V_{PMOUT}$ ) | Hysteresis Width ( $V_{UVHYS}$ , $V_{OVHYS}$ ) | PMEN Pin Input Logic | UV, OV Pin Output Form | UV, OV Pin Output Logic |
|--------------|--|--|----------------------|------------------------|-------------------------|
| L type       | $V_{SENSE}/12$   | 0%   | Active "H"           | Nch open-drain output  | Active "L"              |
| P type       | $V_{SENSE}/14$   | 0%   | Active "H"           | Nch open-drain output  | Active "L"              |

**2. S-191L/191N Series M / N / Q / R type**



**Figure 2**

**2.1 S-191L Series**

**Table 3**

| Product Type | Output Voltage of Supply Voltage Divider Block ( $V_{PMOUT}$ ) | Hysteresis Width ( $V_{UVHYS}$ , $V_{OVHYS}$ ) | PMEN Pin Input Logic | UV, OV Pin Output Form | UV, OV Pin Output Logic |
|--------------|--|--|----------------------|------------------------|-------------------------|
| M type       | $V_{SENSE}/6$  | 5.0%   | Active "H"           | Nch open-drain output  | Active "L"              |
| N type       | $V_{SENSE}/6$  | 10.0%  | Active "H"           | Nch open-drain output  | Active "L"              |
| Q type       | $V_{SENSE}/8$  | 5.0%   | Active "H"           | Nch open-drain output  | Active "L"              |
| R type       | $V_{SENSE}/8$  | 10.0%  | Active "H"           | Nch open-drain output  | Active "L"              |

**2.2 S-191N Series**

**Table 4**

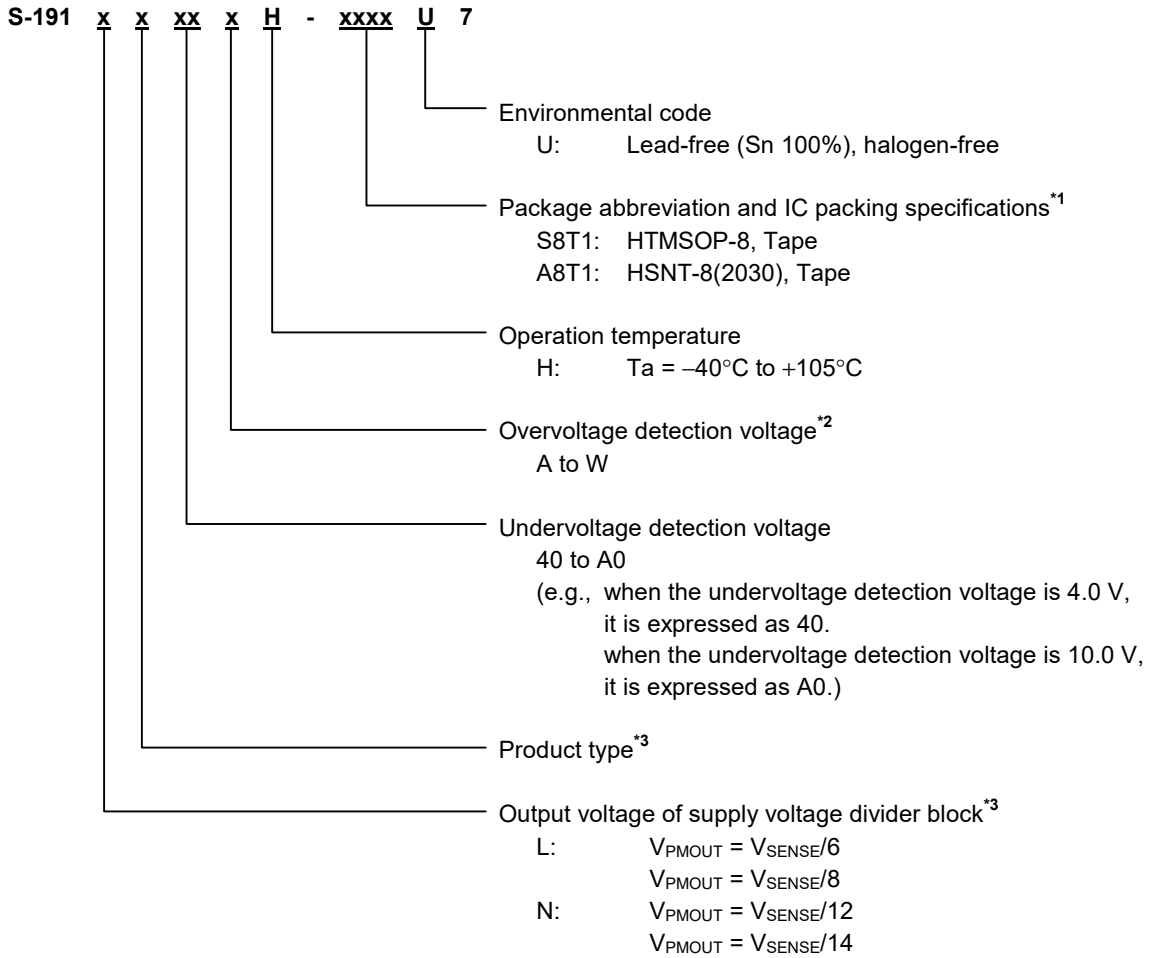
| Product Type | Output Voltage of Supply Voltage Divider Block ( $V_{PMOUT}$ ) | Hysteresis Width ( $V_{UVHYS}$ , $V_{OVHYS}$ ) | PMEN Pin Input Logic | UV, OV Pin Output Form | UV, OV Pin Output Logic |
|--------------|--|--|----------------------|------------------------|-------------------------|
| M type       | $V_{SENSE}/12$   | 5.0%   | Active "H"           | Nch open-drain output  | Active "L"              |
| N type       | $V_{SENSE}/12$   | 10.0%  | Active "H"           | Nch open-drain output  | Active "L"              |
| Q type       | $V_{SENSE}/14$   | 5.0%   | Active "H"           | Nch open-drain output  | Active "L"              |
| R type       | $V_{SENSE}/14$   | 10.0%  | Active "H"           | Nch open-drain output  | Active "L"              |

■ **AEC-Q100 in Process**

Contact our sales representatives for details of AEC-Q100 reliability specification.

■ **Product Name Structure**

1. **Product name**



\*1. Refer to the tape drawing.  
 \*2. Refer to **Table 5** for the overvoltage detection voltage.  
 \*3. Refer to "**2. Function list of product types**".

**Table 5**

| Overvoltage Detection Voltage | Symbol |
|-------------------------------|--------|
| 16.0 V                        | A      |
| 16.1 V                        | B      |
| 16.2 V                        | C      |
| 16.3 V                        | D      |
| 16.4 V                        | E      |
| 16.5 V                        | F      |
| 16.6 V                        | G      |

| Overvoltage Detection Voltage | Symbol |
|-------------------------------|--------|
| 16.7 V                        | H      |
| 16.8 V                        | J      |
| 16.9 V                        | K      |
| 17.0 V                        | L      |
| 17.1 V                        | M      |
| 17.2 V                        | N      |
| 17.3 V                        | P      |

| Overvoltage Detection Voltage | Symbol |
|-------------------------------|--------|
| 17.4 V                        | Q      |
| 17.5 V                        | R      |
| 17.6 V                        | S      |
| 17.7 V                        | T      |
| 17.8 V                        | U      |
| 17.9 V                        | V      |
| 18.0 V                        | W      |

## 2. Function list of product types

### 2.1 S-191L Series

**Table 6**

| Product Type | Output Voltage of Supply Voltage Divider Block (V <sub>PMOUT</sub> ) | Hysteresis Width (V <sub>UVHYS</sub> , V <sub>OVHYS</sub> ) | PMEN Pin Input Logic | UV, OV Pin Output Form | UV, OV Pin Output Logic |
|--------------|--|---|----------------------|------------------------|-------------------------|
| L type       | V <sub>SENSE</sub> /6  | 0%  | Active "H"           | Nch open-drain output  | Active "L"              |
| M type       | V <sub>SENSE</sub> /6  | 5.0%  | Active "H"           | Nch open-drain output  | Active "L"              |
| N type       | V <sub>SENSE</sub> /6  | 10.0%   | Active "H"           | Nch open-drain output  | Active "L"              |
| P type       | V <sub>SENSE</sub> /8  | 0%  | Active "H"           | Nch open-drain output  | Active "L"              |
| Q type       | V <sub>SENSE</sub> /8  | 5.0%  | Active "H"           | Nch open-drain output  | Active "L"              |
| R type       | V <sub>SENSE</sub> /8  | 10.0%   | Active "H"           | Nch open-drain output  | Active "L"              |

### 2.2 S-191N Series

**Table 7**

| Product Type | Output Voltage of Supply Voltage Divider Block (V <sub>PMOUT</sub> ) | Hysteresis Width (V <sub>UVHYS</sub> , V <sub>OVHYS</sub> ) | PMEN Pin Input Logic | UV, OV Pin Output Form | UV, OV Pin Output Logic |
|--------------|--|---|----------------------|------------------------|-------------------------|
| L type       | V <sub>SENSE</sub> /12   | 0%  | Active "H"           | Nch open-drain output  | Active "L"              |
| M type       | V <sub>SENSE</sub> /12   | 5.0%  | Active "H"           | Nch open-drain output  | Active "L"              |
| N type       | V <sub>SENSE</sub> /12   | 10.0%   | Active "H"           | Nch open-drain output  | Active "L"              |
| P type       | V <sub>SENSE</sub> /14   | 0%  | Active "H"           | Nch open-drain output  | Active "L"              |
| Q type       | V <sub>SENSE</sub> /14   | 5.0%  | Active "H"           | Nch open-drain output  | Active "L"              |
| R type       | V <sub>SENSE</sub> /14   | 10.0%   | Active "H"           | Nch open-drain output  | Active "L"              |

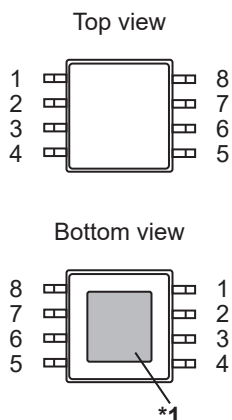
## 3. Packages

**Table 8 Package Drawing Codes**

| Package Name | Dimension    | Tape         | Reel         | Land         |
|--------------|--------------|--------------|--------------|--------------|
| HTMSOP-8     | FP008-A-P-SD | FP008-A-C-SD | FP008-A-R-SD | FP008-A-L-SD |
| HSNT-8(2030) | PP008-A-P-SD | PP008-A-C-SD | PP008-A-R-SD | PP008-A-L-SD |

## Pin Configurations

### 1. HTMSOP-8



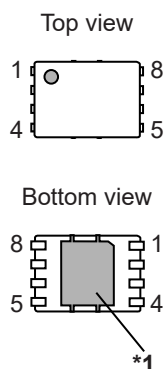
**Figure 3**

- \*1. Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.
- \*2. Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance. Moreover, the CD pin is available even when it is open.

**Table 9**

| Pin No. | Symbol | Description  |
|---------|--------|--|
| 1       | PMEN   | Supply voltage divided output enable pin                   |
| 2       | VDD    | Voltage input pin  |
| 3       | PMOUT  | Supply voltage divided output pin                          |
| 4       | SENSE  | Detection voltage input pin                                |
| 5       | CD*2   | Connection pin for release delay time adjustment capacitor |
| 6       | VSS    | GND pin  |
| 7       | UV     | Undervoltage detection output pin                          |
| 8       | OV     | Overvoltage detection output pin                           |

### 2. HSNT-8(2030)



**Figure 4**

- \*1. Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.
- \*2. Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance. Moreover, the CD pin is available even when it is open.

**Table 10**

| Pin No. | Symbol | Description  |
|---------|--------|--|
| 1       | PMEN   | Supply voltage divided output enable pin                   |
| 2       | VDD    | Voltage input pin  |
| 3       | PMOUT  | Supply voltage divided output pin                          |
| 4       | SENSE  | Detection voltage input pin                                |
| 5       | CD*2   | Connection pin for release delay time adjustment capacitor |
| 6       | VSS    | GND pin  |
| 7       | UV     | Undervoltage detection output pin                          |
| 8       | OV     | Overvoltage detection output pin                           |

## ■ Absolute Maximum Ratings

Table 11

(Ta = -40°C to +105°C unless otherwise specified)

| Item                          |                              | Symbol            | Absolute Maximum Rating                            | Unit |
|-------------------------------|------------------------------|-------------------|--|------|
| Power supply voltage          |                              | $V_{DD} - V_{SS}$ | $V_{SS} - 0.3$ to $V_{SS} + 45.0$                  | V    |
| SENSE pin voltage             | S-191L Series L / M / N type | $V_{SENSE}$       | $V_{SS} - 30.0$ to $V_{SS} + 42.0$                 | V    |
|                               | S-191L Series P / Q / R type |                   | $V_{SS} - 30.0$ to $V_{SS} + 45.0$                 | V    |
|                               | S-191N Series L / M / N type |                   | $V_{SS} - 30.0$ to $V_{SS} + 45.0$                 | V    |
|                               | S-191N Series P / Q / R type |                   | $V_{SS} - 30.0$ to $V_{SS} + 45.0$                 | V    |
| CD pin input voltage          |                              | $V_{CD}$          | $V_{SS} - 0.3$ to $V_{DD} + 0.3 \leq V_{SS} + 7.0$ | V    |
| PMEN pin input voltage        |                              | $V_{PMEN}$        | $V_{SS} - 0.3$ to $V_{SS} + 45.0$                  | V    |
| Output voltage                | Detector block               | $V_{UV}$          | $V_{SS} - 0.3$ to $V_{SS} + 45.0$                  | V    |
|                               |                              | $V_{OV}$          | $V_{SS} - 0.3$ to $V_{SS} + 45.0$                  | V    |
|                               | Supply voltage divider block | $V_{PMOUT}$       | $V_{SS} - 0.3$ to $V_{DD} + 0.3 \leq V_{SS} + 7.0$ | V    |
| Output current                |                              | $I_{UV}$          | 25   | mA   |
|                               |                              | $I_{OV}$          | 25   | mA   |
|                               |                              | $I_{PMOUT}$       | 2  | mA   |
| Junction temperature          |                              | $T_j$             | -40 to +150  | °C   |
| Operation ambient temperature |                              | $T_{opr}$         | -40 to +105  | °C   |
| Storage temperature           |                              | $T_{stg}$         | -40 to +150  | °C   |

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Thermal Resistance Value

Table 12

| Item                                     | Symbol        | Condition    | Min.    | Typ. | Max. | Unit |      |
|--|---------------|--------------|---------|------|------|------|------|
| Junction-to-ambient thermal resistance*1 | $\theta_{JA}$ | HTMSOP-8     | Board A | -    | 159  | -    | °C/W |
|  |               |              | Board B | -    | 113  | -    | °C/W |
|  |               |              | Board C | -    | 39   | -    | °C/W |
|  |               |              | Board D | -    | 40   | -    | °C/W |
|  |               |              | Board E | -    | 30   | -    | °C/W |
|  |               | HSNT-8(2030) | Board A | -    | 181  | -    | °C/W |
|  |               |              | Board B | -    | 135  | -    | °C/W |
|  |               |              | Board C | -    | 40   | -    | °C/W |
|  |               |              | Board D | -    | 42   | -    | °C/W |
|  |               |              | Board E | -    | 32   | -    | °C/W |

\*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ Power Dissipation" and "Test Board" for details.

## ■ Electrical Characteristics

### 1. Detector block

**Table 13**

(Ta = -40°C to +105°C unless otherwise specified)

| Item                             | Symbol             | Condition  | Min.                             | Typ.                         | Max.                             | Unit | Test Circuit |
|----------------------------------|--------------------|--|----------------------------------|------------------------------|----------------------------------|------|--------------|
| Undervoltage detection voltage*1 | V <sub>UVDET</sub> | V <sub>DD</sub> = 13.5 V,<br>4.0 V ≤ V <sub>UVDET(S)</sub> ≤ 10.0 V  | V <sub>UVDET(S)</sub><br>× 0.985 | V <sub>UVDET(S)</sub>        | V <sub>UVDET(S)</sub><br>× 1.015 | V    | 1            |
| Overvoltage detection voltage*2  | V <sub>OVDET</sub> | V <sub>DD</sub> = 13.5 V,<br>16.0 V ≤ V <sub>OVDET(S)</sub> ≤ 18.0 V   | V <sub>OVDET(S)</sub><br>× 0.985 | V <sub>OVDET(S)</sub>        | V <sub>OVDET(S)</sub><br>× 1.015 | V    | 1            |
| Undervoltage hysteresis width*3  | V <sub>UVHYS</sub> | L / P type<br>(V <sub>UVHYS</sub> = 0%)  | –                                | V <sub>UVDET</sub><br>× 0.00 | –                                | V    | 1            |
|                                  |                    | M / Q type<br>(V <sub>UVHYS</sub> = 5.0%)  | V <sub>UVDET</sub><br>× 0.04     | V <sub>UVDET</sub><br>× 0.05 | V <sub>UVDET</sub><br>× 0.06     | V    | 1            |
|                                  |                    | N / R type<br>(V <sub>UVHYS</sub> = 10.0%)   | V <sub>UVDET</sub><br>× 0.09     | V <sub>UVDET</sub><br>× 0.10 | V <sub>UVDET</sub><br>× 0.11     | V    | 1            |
| Overvoltage hysteresis width*3   | V <sub>OVHYS</sub> | L / P type<br>(V <sub>OVHYS</sub> = 0%)  | –                                | V <sub>OVDET</sub><br>× 0.00 | –                                | V    | 1            |
|                                  |                    | M / Q type<br>(V <sub>OVHYS</sub> = 5.0%)  | V <sub>OVDET</sub><br>× 0.04     | V <sub>OVDET</sub><br>× 0.05 | V <sub>OVDET</sub><br>× 0.06     | V    | 1            |
|                                  |                    | N / R type<br>(V <sub>OVHYS</sub> = 10.0%)   | V <sub>OVDET</sub><br>× 0.09     | V <sub>OVDET</sub><br>× 0.10 | V <sub>OVDET</sub><br>× 0.11     | V    | 1            |
| Operation voltage                | V <sub>DD</sub>    | –  | 3.0                              | –                            | 36.0                             | V    | 1            |
| Output current                   | I <sub>OUT</sub>   | UV pin Nch driver,<br>V <sub>DD</sub> = 3.0 V, V <sub>DS</sub> *4 = 0.1 V,<br>V <sub>SENSE</sub> = V <sub>UVDET(S)</sub> – 1 V | 0.60                             | –                            | –                                | mA   | 2            |
|                                  |                    | OV pin Nch driver,<br>V <sub>DD</sub> = 3.0 V, V <sub>DS</sub> *4 = 0.1 V,<br>V <sub>SENSE</sub> = V <sub>OVDET(S)</sub> + 1 V | 0.60                             | –                            | –                                | mA   | 2            |
| Leakage current                  | I <sub>LEAK</sub>  | UV pin Nch driver,<br>V <sub>DD</sub> = 36 V, V <sub>UV</sub> = 36 V,<br>V <sub>SENSE</sub> = 13.5 V                           | –                                | –                            | 2.0                              | μA   | 2            |
|                                  |                    | OV pin Nch driver,<br>V <sub>DD</sub> = 36 V, V <sub>OV</sub> = 36 V,<br>V <sub>SENSE</sub> = 13.5 V                           | –                                | –                            | 2.0                              | μA   | 2            |
| Detection response time*5        | t <sub>RESET</sub> | –  | –                                | 80                           | 200                              | μs   | 3            |
| Release delay time*6             | t <sub>DELAY</sub> | C <sub>D</sub> = 3.3 nF  | 8.5                              | 10.0                         | 11.5                             | ms   | 3            |
| SENSE pin resistance             | R <sub>SENSE</sub> | V <sub>PMEN</sub> = 0 V  | 6.8                              | –                            | 200                              | MΩ   | 7            |
| CD pin discharge ON resistance   | R <sub>CDD</sub>   | V <sub>DD</sub> = 3.0 V, V <sub>CD</sub> = 0.7 V   | 0.15                             | –                            | 0.90                             | kΩ   | –            |

\*1. V<sub>UVDET</sub>: Actual undervoltage detection voltage value, V<sub>UVDET(S)</sub>: Set undervoltage detection voltage value

\*2. V<sub>OVDET</sub>: Actual overvoltage detection voltage value, V<sub>OVDET(S)</sub>: Set overvoltage detection voltage value

\*3. The undervoltage release voltage (V<sub>UVREL</sub>) and the overvoltage release voltage (V<sub>OVREL</sub>) are as follows.

L / P type (hysteresis width "Unavailable"): V<sub>UVREL</sub> = V<sub>UVDET</sub>, V<sub>OVREL</sub> = V<sub>OVDET</sub>

M / N / Q / R type (hysteresis width "Available"): V<sub>UVREL</sub> = V<sub>UVDET</sub> + V<sub>UVHYS</sub>, V<sub>OVREL</sub> = V<sub>OVDET</sub> – V<sub>OVHYS</sub>

\*4. V<sub>DS</sub>: Drain-to-source voltage of the output transistor

\*5. The time period from when the pulse voltage of V<sub>UVDET(S)</sub> + 1.0 V → V<sub>UVDET(S)</sub> – 1.0 V or V<sub>OVDET(S)</sub> – 1.0 V → V<sub>OVDET(S)</sub> + 1.0 V is applied to the SENSE pin after V<sub>SENSE</sub> reaches the release voltage once, until V<sub>UV</sub> or V<sub>OV</sub> reaches 50% of V<sub>DD</sub>.

\*6. V<sub>UVREL(S)</sub>: Set undervoltage release voltage value, V<sub>OVREL(S)</sub>: Set overvoltage release voltage value

The time period from when the pulse voltage of V<sub>UVREL(S)</sub> – 1.0 V → V<sub>UVREL(S)</sub> + 1.0 V or V<sub>OVREL(S)</sub> + 1.0 V → V<sub>OVREL(S)</sub> – 1.0 V is applied to the SENSE pin to when V<sub>UV</sub> or V<sub>OV</sub> reaches 50% of V<sub>DD</sub>.



## 2. Supply voltage divider block

**Table 14**

(Ta = -40°C to +105°C unless otherwise specified)

| Item  | Symbol               | Condition   | Min.                                     | Typ.                             | Max.                   | Unit                             | Test Circuit |   |
|---|----------------------|---|--|----------------------------------|------------------------|----------------------------------|--------------|---|
| Input voltage   | V <sub>DD</sub>      | V <sub>DD</sub> ≥ V <sub>SENSE</sub> - 2.0 V  | 3.0                                      | -                                | 36.0                   | V                                | -            |   |
| SENSE pin voltage   | V <sub>SENSE</sub>   | -   | 5.0                                      | -                                | 36.0                   | V                                | -            |   |
| Output voltage of supply voltage divider block*1                      | V <sub>PMOUT</sub>   | 3.0 V ≤ V <sub>DD</sub> ≤ 18.0 V,<br>5.0 V ≤ V <sub>SENSE</sub> ≤ 18.0 V,<br>-10 μA ≤ I <sub>PMOUT</sub> ≤ 10 μA        | V <sub>SENSE</sub> /6<br>output product  | V <sub>PMOUT(S)</sub><br>× 0.980 | V <sub>SENSE</sub> /6  | V <sub>PMOUT(S)</sub><br>× 1.020 | V            | 4 |
|   |                      |   | V <sub>SENSE</sub> /8<br>output product  | V <sub>PMOUT(S)</sub><br>× 0.975 | V <sub>SENSE</sub> /8  | V <sub>PMOUT(S)</sub><br>× 1.025 | V            | 4 |
|   |                      |   | V <sub>SENSE</sub> /12<br>output product | V <sub>PMOUT(S)</sub><br>× 0.970 | V <sub>SENSE</sub> /12 | V <sub>PMOUT(S)</sub><br>× 1.030 | V            | 4 |
|   |                      | 3.0 V ≤ V <sub>DD</sub> ≤ 18.0 V,<br>5.0 V ≤ V <sub>SENSE</sub> ≤ 18.0 V,<br>-3 μA ≤ I <sub>PMOUT</sub> ≤ 3 μA          | V <sub>SENSE</sub> /14<br>output product | V <sub>PMOUT(S)</sub><br>× 0.966 | V <sub>SENSE</sub> /14 | V <sub>PMOUT(S)</sub><br>× 1.034 | V            | 4 |
| Load current  | I <sub>PMOUT</sub>   | V <sub>SENSE</sub> /6 output product,<br>V <sub>SENSE</sub> /8 output product,<br>V <sub>SENSE</sub> /12 output product | -10                                      | -                                | 10                     | μA                               | 4            |   |
|   |                      | V <sub>SENSE</sub> /14 output product   | -3                                       | -                                | 3                      | μA                               | 4            |   |
| Output impedance  | R <sub>PS</sub>      | 3.0 V ≤ V <sub>DD</sub> ≤ 18.0 V,<br>5.0 V ≤ V <sub>SENSE</sub> ≤ 18.0 V  | -  | -                                | 1000                   | Ω                                | 4            |   |
| Set-up time*2   | t <sub>PU</sub>      | V <sub>DD</sub> = 18.0 V, V <sub>SENSE</sub> = 18.0 V,<br>C <sub>PM</sub> = 0.22 μF, no load, t <sub>r</sub> = 1.0 μs   | -  | 15                               | 30                     | ms                               | 5            |   |
| PMEN pin input voltage "H"  | V <sub>PSH</sub>     | V <sub>DD</sub> = 18.0 V,<br>determined by V <sub>PMOUT</sub> output level  | 1.3                                      | -                                | -                      | V                                | 6            |   |
| PMEN pin input voltage "L"  | V <sub>PSL</sub>     | V <sub>DD</sub> = 18.0 V,<br>determined by V <sub>PMOUT</sub> output level  | -  | -                                | 0.3                    | V                                | 6            |   |
| PMEN pin input current "H"  | I <sub>PSH</sub>     | V <sub>DD</sub> = 18.0 V, V <sub>PMEN</sub> = V <sub>DD</sub>   | 0.00                                     | -                                | 0.50                   | μA                               | 6            |   |
| PMEN pin input current "L"  | I <sub>PSL</sub>     | V <sub>DD</sub> = 18.0 V, V <sub>PMEN</sub> = 0 V   | -0.1                                     | -                                | 0.1                    | μA                               | 6            |   |
| SENSE pin resistance during operation of supply voltage divider block | R <sub>PMSENSE</sub> | V <sub>PMEN</sub> = V <sub>DD</sub>   | 5.8                                      | -                                | 140                    | MΩ                               | 7            |   |
| Discharge shunt resistance during power-off                           | R <sub>PLow</sub>    | V <sub>DD</sub> = 13.5 V, V <sub>PMEN</sub> = 0 V, V <sub>PMOUT</sub> = 0.1 V   | -  | 2.8                              | -                      | kΩ                               | 8            |   |

\*1. V<sub>PMOUT</sub>: Actual output voltage value of supply voltage divider block,  
 V<sub>PMOUT(S)</sub>: Set output voltage value of supply voltage divider block

\*2. Set-up time shows the time period from when the input voltage reaches 50% until the output voltage of supply voltage divider block rises to 99%, when the PMEN pin is set to ON (t<sub>r</sub> = 1.0 μs).

## 3. Overall

**Table 15**

(Ta = -40°C to +105°C unless otherwise specified)

| Item                | Symbol            | Condition   | Min. | Typ. | Max. | Unit | Test Circuit |
|---------------------|-------------------|---|------|------|------|------|--------------|
| Current consumption | I <sub>SS1</sub>  | During supply voltage divided output stops,<br>V <sub>DD</sub> = 13.5 V, V <sub>SENSE</sub> = 13.5 V,<br>V <sub>PMEN</sub> = 0 V                          | -    | 0.9  | 3.2  | μA   | 7            |
|                     | I <sub>SSP1</sub> | During supply voltage divided output operates,<br>V <sub>DD</sub> = 13.5 V, V <sub>SENSE</sub> = 13.5 V,<br>V <sub>PMEN</sub> = V <sub>DD</sub> , no load | -    | 1.3  | 5.6  | μA   | 7            |

■ Test Circuits

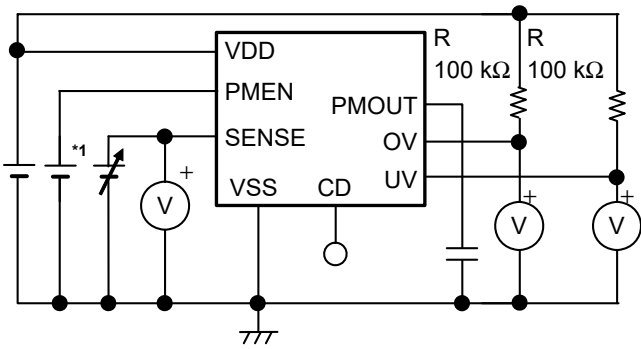


Figure 5 Test Circuit 1

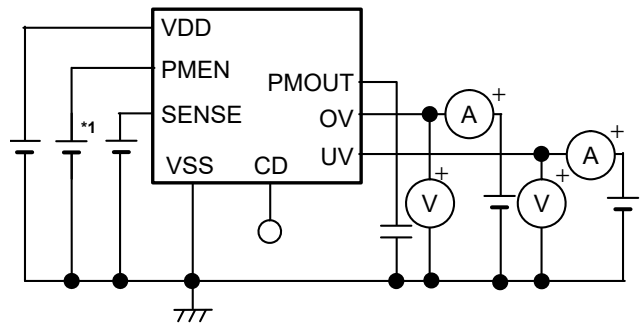


Figure 6 Test Circuit 2

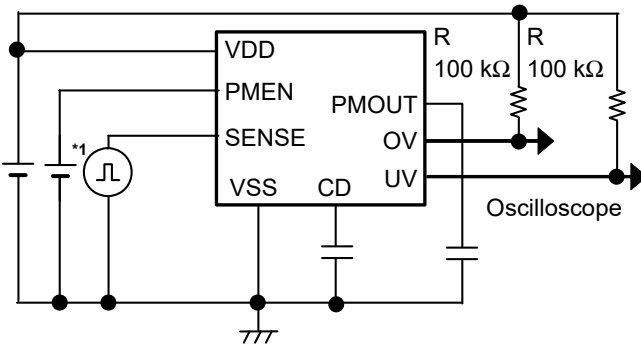


Figure 7 Test Circuit 3

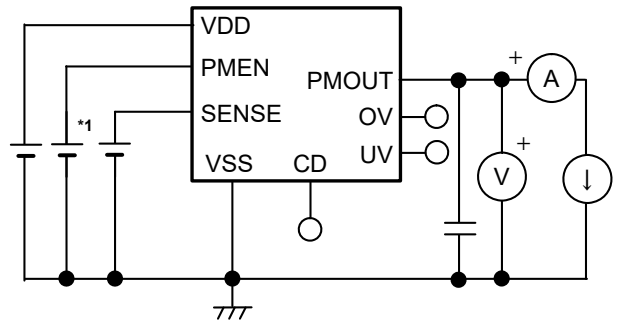


Figure 8 Test Circuit 4

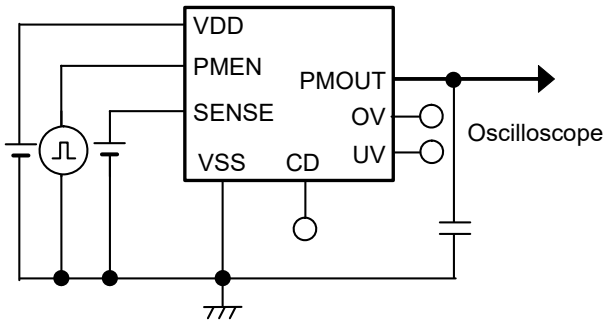


Figure 9 Test Circuit 5

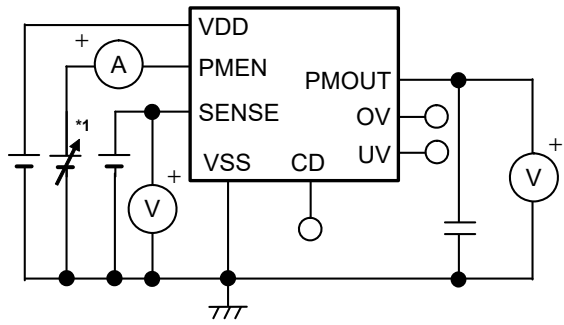


Figure 10 Test Circuit 6

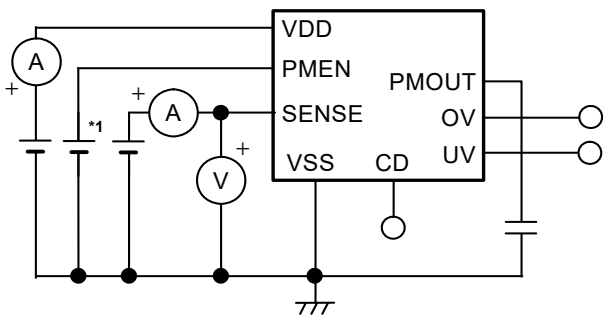


Figure 11 Test Circuit 7

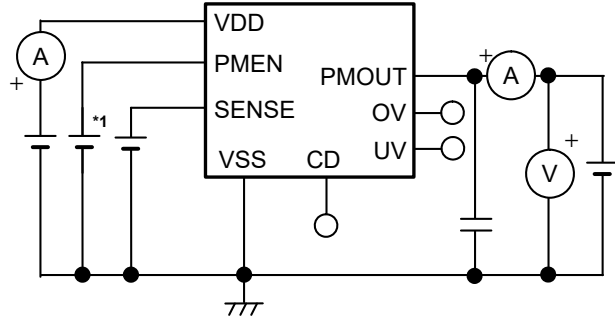
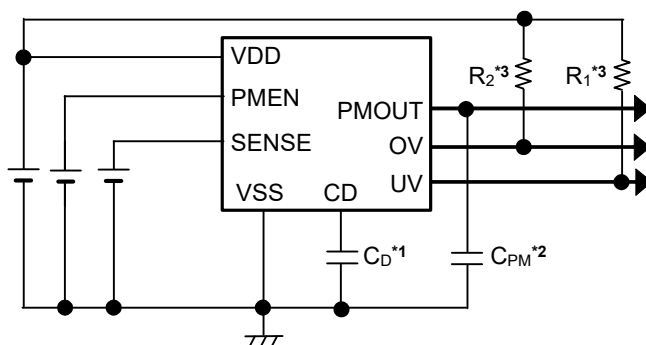


Figure 12 Test Circuit 8

## ■ Standard Circuit



- \*1.  $C_D$  is a release delay time adjustment capacitor. The  $C_D$  should be connected directly to the CD pin and the VSS pin.
- \*2.  $C_{PM}$  is a capacitor for stabilizing the output. The  $C_{PM}$  should be connected directly to the PMOUT pin and the VSS pin.
- \*3.  $R_1$ ,  $R_2$  are the external pull-up resistors for the reset output pin.

Figure 13

**Caution** The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

## ■ Condition of Application

Release delay time adjustment capacitor ( $C_D$ ): A ceramic capacitor with capacitance of 1.0 nF or more is recommended.  
 Supply voltage divider block output capacitor ( $C_{PM}$ ): A ceramic capacitor with capacitance of 0.1  $\mu\text{F}$  to 0.22  $\mu\text{F}$  is recommended.

- Caution**
1. The CD pin is available even when it is open.  
 Refer to "1. Power on sequence" in "■ Usage Precautions" when using it open.
  2. Generally, in a supply voltage divider, an oscillation may occur depending on the selection of the external parts. Perform thorough evaluation including the temperature characteristics with an actual application using the above capacitors to confirm no oscillation occurs.

## ■ Selection of Release Delay Time Adjustment Capacitor ( $C_D$ )

In this IC, the release delay time adjustment capacitor ( $C_D$ ) is necessary between the CD pin and the VSS pin to adjust the release delay time ( $t_{\text{DELAY}}$ ) of the detector. Refer to "1.4 Delay circuit" in "■ Operation" for details.

**Caution** Perform thorough evaluation including the temperature characteristics with an actual application to select  $C_D$ .

## ■ Selection of Supply Voltage Divider Block Output Capacitor ( $C_{PM}$ )

This IC requires  $C_{PM}$  between the PMOUT pin and the VSS pin for phase compensation. The operation is stabilized by a ceramic capacitor with capacitance of 0.1  $\mu\text{F}$  to 0.22  $\mu\text{F}$ . When using an OS capacitor, a tantalum capacitor or an aluminum electrolytic capacitor, the capacitance also must be 0.1  $\mu\text{F}$  to 0.22  $\mu\text{F}$ . However, an oscillation may occur depending on the equivalent series resistance (ESR).

**Caution** Perform thorough evaluation including the temperature characteristics with an actual application to select  $C_{PM}$ .

## ■ Explanation of Terms

### 1. Detector block

#### 1.1 Detection voltage ( $V_{UVDET}$ , $V_{OVDET}$ )

The detection voltage is a SENSE pin voltage at which the output voltage in **Figure 18** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum and the maximum is called the detection voltage range (Refer to "**Figure 14 Overvoltage Detection Voltage**", "**Figure 16 Undervoltage Detection Voltage**").

**Table 16**

| Detection Operation    | Detection Voltage | Output Voltage                               | Detection Voltage Range              |
|------------------------|-------------------|--|--------------------------------------|
| Undervoltage detection | $V_{UVDET}$       | $V_{UV} = \text{"H"} \rightarrow \text{"L"}$ | $V_{UVDET}$ min. to $V_{UVDET}$ max. |
| Overvoltage detection  | $V_{OVDET}$       | $V_{OV} = \text{"H"} \rightarrow \text{"L"}$ | $V_{OVDET}$ min. to $V_{OVDET}$ max. |

Example: In  $V_{UVDET} = 5.0$  V product, the detection voltage is at any point in the range of  $4.925 \text{ V} \leq V_{UVDET} \leq 5.075 \text{ V}$ .  
 This means that some  $V_{UVDET} = 5.0$  V product has  $V_{UVDET} = 4.925$  V and some has  $V_{UVDET} = 5.075$  V.

#### 1.2 Release voltage ( $V_{UVREL}$ , $V_{OVREL}$ )

The release voltage is a SENSE pin voltage at which the output voltage in **Figure 18** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum and the maximum is called the release voltage range (Refer to "**Figure 15 Overvoltage Release Voltage**", "**Figure 17 Undervoltage Release Voltage**").

The release voltage becomes the value differs from the detection voltage within the range shown below.

- M / Q type: 4% to 6% (5% typ.)
- N / R type: 9% to 11% (10% typ.)

**Table 17**

| Detection Operation    | Release Voltage | Output Voltage                               | Release Voltage Range                |
|------------------------|-----------------|--|--------------------------------------|
| Undervoltage detection | $V_{UVREL}$     | $V_{UV} = \text{"L"} \rightarrow \text{"H"}$ | $V_{UVREL}$ min. to $V_{UVREL}$ max. |
| Overvoltage detection  | $V_{OVREL}$     | $V_{OV} = \text{"L"} \rightarrow \text{"H"}$ | $V_{OVREL}$ min. to $V_{OVREL}$ max. |

Example: For N / R type,  $V_{UVDET} = 4.0$  V product, the release voltage is at any point in the range of  $4.29 \text{ V} \leq V_{UVREL} \leq 4.51 \text{ V}$  despite  $V_{UVREL} = 4.40$  V typ.  
 This means that some N / R type,  $V_{UVDET} = 4.0$  V product has  $V_{UVREL} = 4.29$  V and some has  $V_{UVREL} = 4.51$  V.

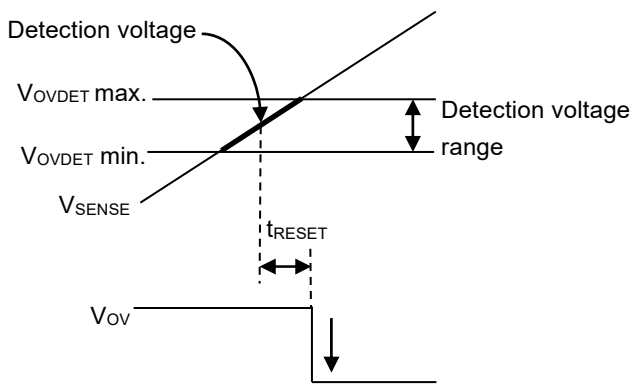


Figure 14 Overvoltage Detection Voltage

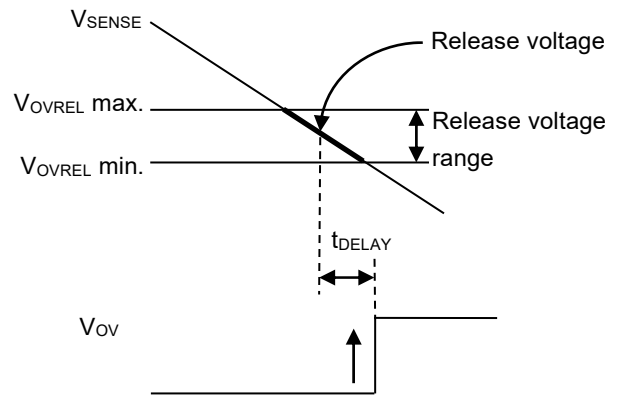


Figure 15 Overvoltage Release Voltage

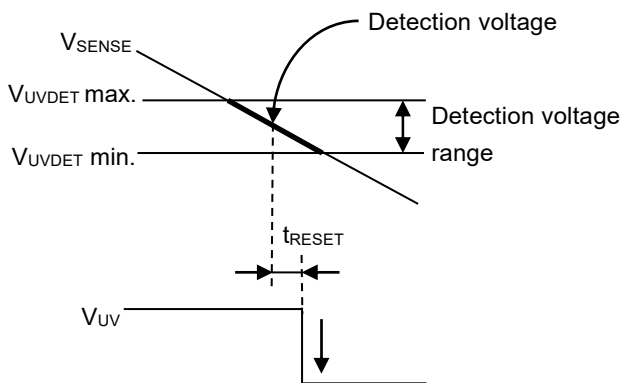


Figure 16 Undervoltage Detection Voltage

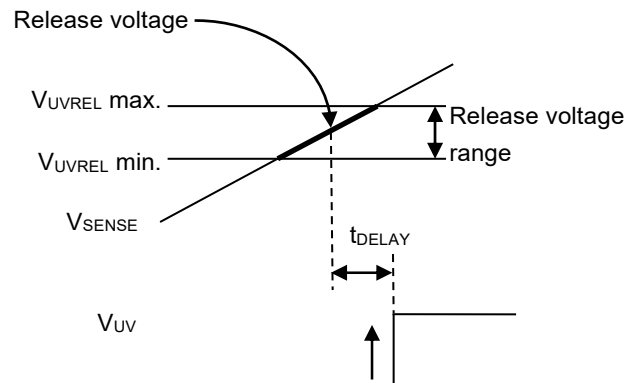


Figure 17 Undervoltage Release Voltage

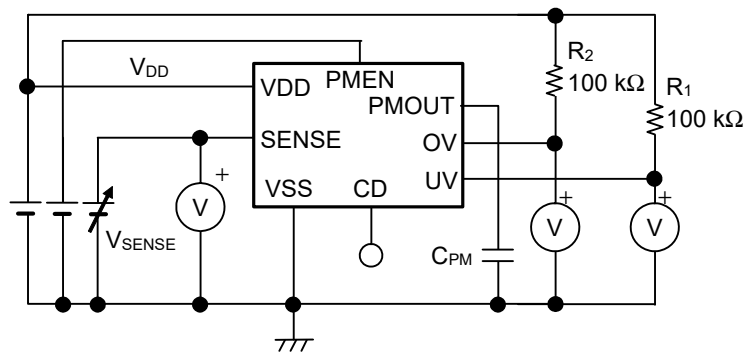


Figure 18 Test Circuit of Detection Voltage and Release Voltage

### 1.3 Hysteresis width ( $V_{UVHYS}$ , $V_{OVHYS}$ )

The hysteresis width is the voltage difference between the detection voltage and the release voltage. Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

- Undervoltage hysteresis width ( $V_{UVHYS}$ ):  $V_{UVREL} - V_{UVDET}$
- Overvoltage hysteresis width ( $V_{OVHYS}$ ):  $V_{OVDET} - V_{OVREL}$

### 1.4 Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector.

## 2. Supply voltage divider block

### 2.1 Supply voltage divided output

The supply voltage divided output is a function that divides the SENSE pin voltage ( $V_{SENSE}$ ) into  $V_{SENSE}/6$ ,  $V_{SENSE}/8$ ,  $V_{SENSE}/12$  or  $V_{SENSE}/14$  and outputs the voltage.

For example, a microcontroller can monitor a battery voltage by inputting the output voltage of supply voltage divider block ( $V_{PMOUT}$ ) to the microcontroller A/D converter.

### 2.2 Output voltage of supply voltage divider block ( $V_{PMOUT}$ )

This is the voltage of the divided  $V_{SENSE}$ . The following voltages are the outputs.

- S-191L Series L / M / N type:  $V_{SENSE}/6$
- S-191L Series P / Q / R type:  $V_{SENSE}/8$
- S-191N Series L / M / N type:  $V_{SENSE}/12$
- S-191N Series P / Q / R type:  $V_{SENSE}/14$

This voltage is the output in accuracy range of between  $\pm 2.0\%$  and  $\pm 3.4\%^{*1}$  when the power supply voltage,  $V_{SENSE}$ , temperature and load current satisfy a certain condition<sup>\*1</sup>.

<sup>\*1</sup>. Differs depending on the product type.

Example: For S-191L Series L / M / N type,  $V_{SENSE} = 15.0\text{ V}$ , the output voltage of supply voltage divider block is at any point in the range of  $2.45\text{ V} \leq V_{PMOUT} \leq 2.55\text{ V}$ .

This means that some S-191L Series L / M / N type has  $V_{PMOUT} = 2.45\text{ V}$  and some has  $V_{PMOUT} = 2.55\text{ V}$ .

**Caution** If the certain condition is not satisfied, the output voltage may exceed the accuracy range.  
Refer to Table 14 of "■ Electrical Characteristics" for details.

### 2.3 Output impedance ( $R_{PS}$ )

This is the supply voltage divider block impedance. It shows how much output offset voltage changes when the load current changes.

For example, the output impedance can be used in sampling rate calculation as signal source impedance when  $V_{PMOUT}$  from the PMOUT pin is input to the A/D converter as a microcontroller input signal.

### 2.4 Set-up time ( $t_{PU}$ )

This is the time from when the supply voltage divided output is operated until  $V_{PMOUT}$  stabilizes.

### 2.5 Discharge shunt resistance during power-off ( $R_{PLow}$ )

This is the ON resistance of the N-channel transistor built into the supply voltage divider block.

When the supply voltage divided output is stopped,  $V_{PMOUT}$  is set to the  $V_{SS}$  level by the built-in N-channel transistor.

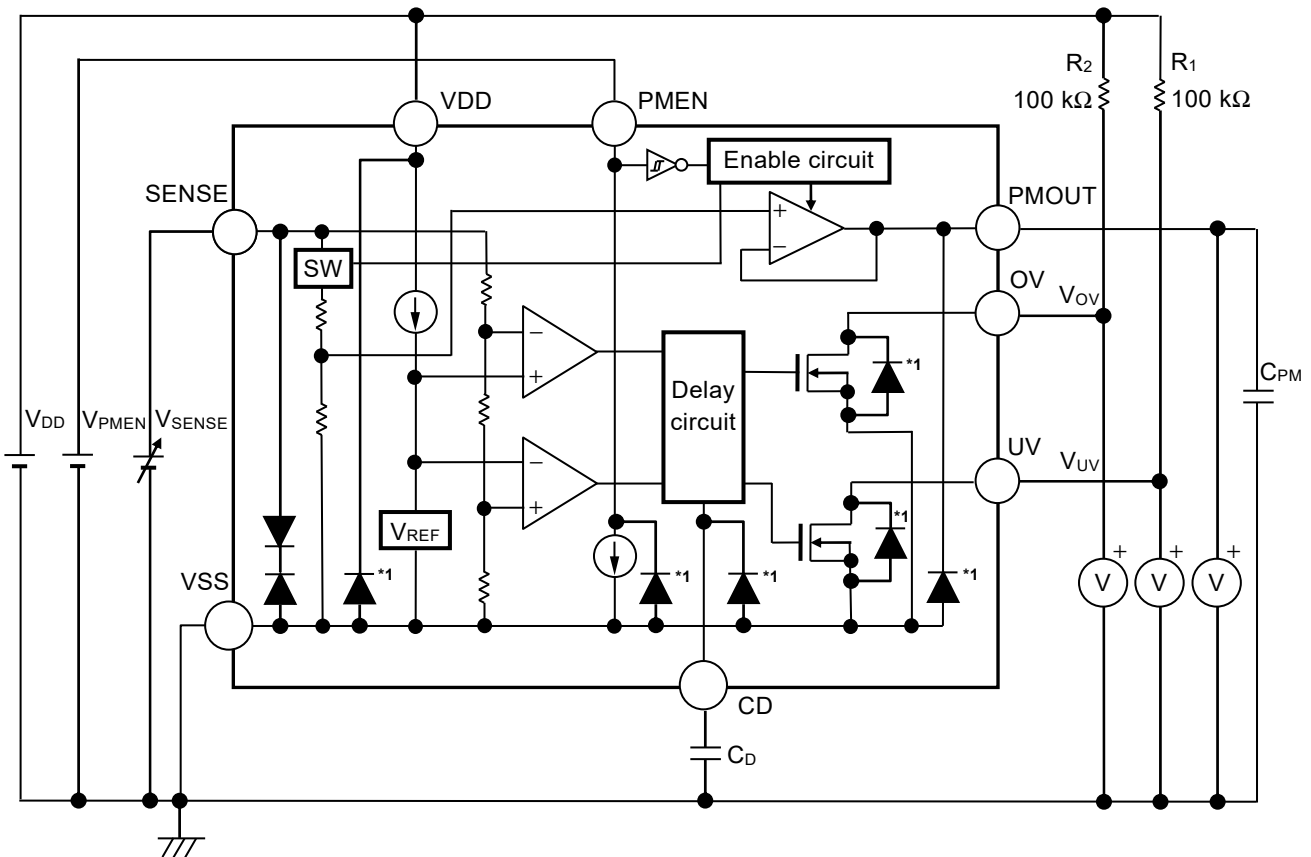
## ■ Operation

### 1. Detector block

Figure 19 and Figure 21 show that the UV and OV pins being pulled up by resistors ( $R_1$ ,  $R_2$ ) is an example of basic detector block operation.

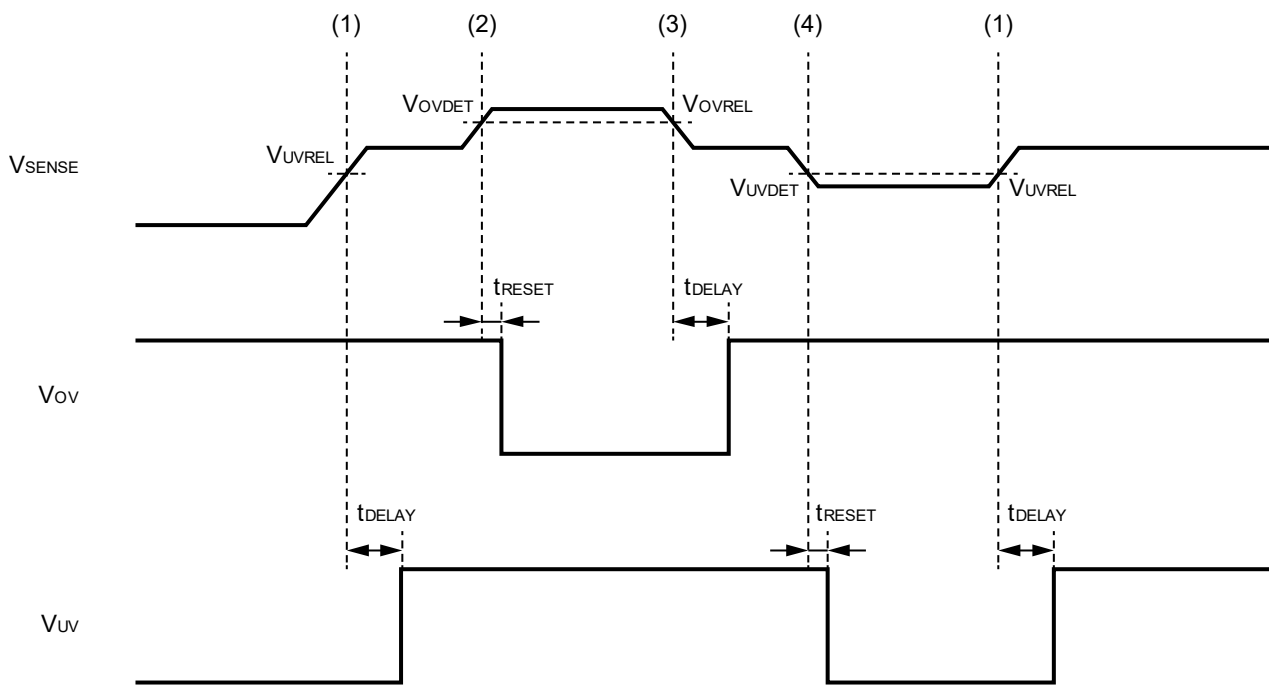
#### 1.1 S-191L/191N Series L / P type

- (1) Undervoltage detection status to release status (undervoltage release status)  
 When the SENSE pin voltage ( $V_{SENSE}$ ) exceeds the undervoltage release voltage ( $V_{UVREL} = V_{UVDET}$ ), the UV pin voltage output becomes "H" after release delay time ( $t_{DELAY}$ ). At this time, the OV pin output stays at "H".
- (2) Release status to overvoltage detection status  
 $V_{SENSE}$  rises, and when it exceeds the overvoltage detection voltage ( $V_{OVDET}$ ), the OV pin output becomes "L" after detection response time ( $t_{RESET}$ ). At this time, the UV pin stays at "H".
- (3) Overvoltage detection status to release status (overvoltage release status)  
 $V_{SENSE}$  drops, and when it goes below the overvoltage release voltage ( $V_{OVREL} = V_{OVDET}$ ), the OV pin output changes to "H" after  $t_{DELAY}$ . At this time, the UV pin output stays at "H".
- (4) Release status to undervoltage detection status  
 $V_{SENSE}$  drops, and when it goes below the undervoltage detection voltage ( $V_{UVDET}$ ), the UV pin output becomes "L" after  $t_{RESET}$  and changes to undervoltage detection status. At this time, the OV pin output stays at "H".



\*1. Parasitic diode

Figure 19 Operation of S-191L/191N Series L / P type

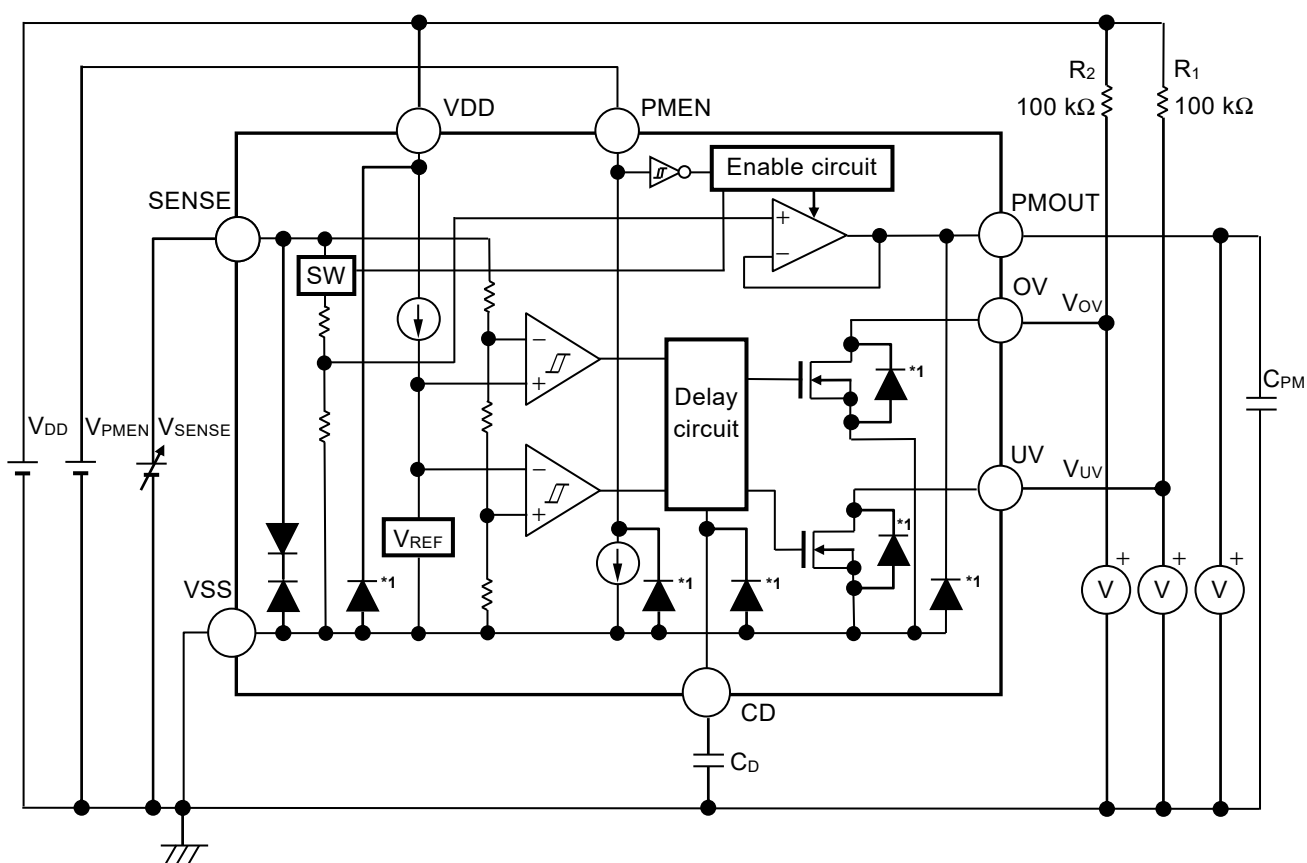


**Figure 20** Timing Chart of S-191L/191N Series L / P Type



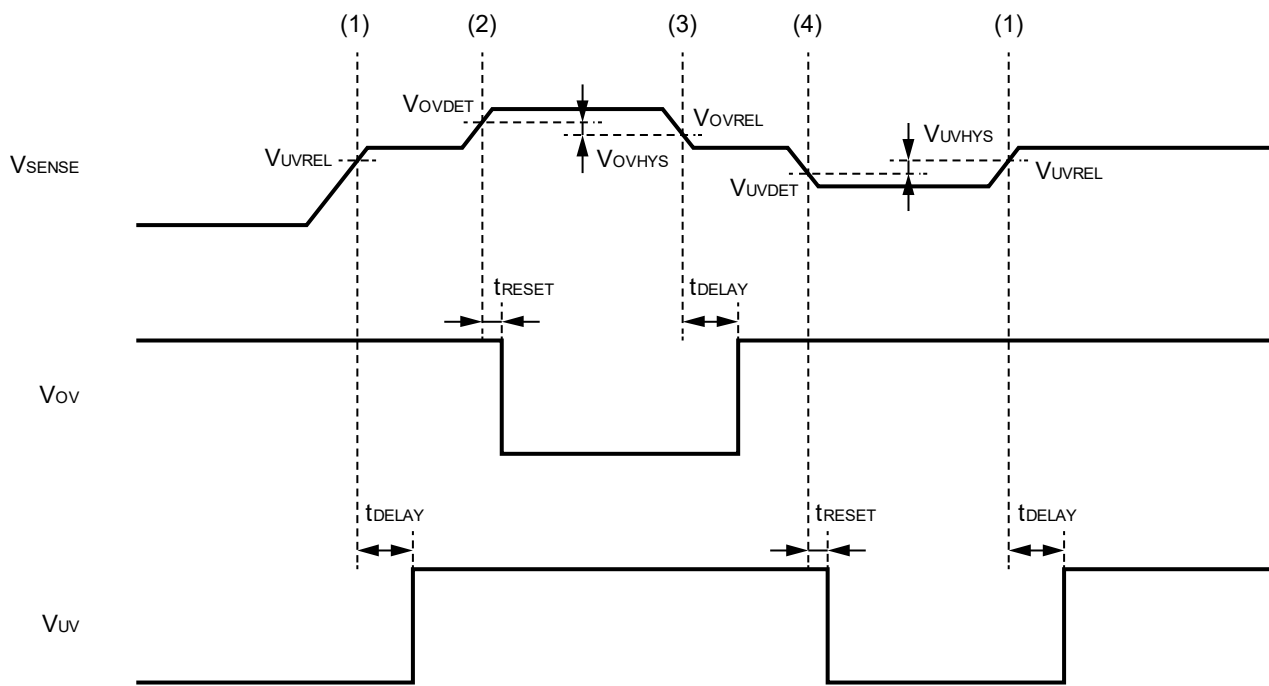
### 1.2 S-191L/191N Series M / N / Q / R type

- (1) Undervoltage detection status to release status (undervoltage release status)  
 When the SENSE pin voltage ( $V_{SENSE}$ ) exceeds the undervoltage release voltage ( $V_{UVREL} = V_{UVDET} + V_{UVHYS}$ ), the UV pin voltage output becomes "H" after release delay time ( $t_{DELAY}$ ). At this time, the OV pin output stays at "H".
- (2) Release status to overvoltage detection status  
 $V_{SENSE}$  rises, and when it exceeds the overvoltage detection voltage ( $V_{OVDET}$ ), the OV pin output becomes "L" after detection response time ( $t_{RESET}$ ). At this time, the UV pin stays at "H".
- (3) Overvoltage detection status to release status (overvoltage release status)  
 $V_{SENSE}$  drops, and when it goes below the overvoltage release voltage ( $V_{OVREL} = V_{OVDET} - V_{OVHYS}$ ), the OV pin output changes to "H" after  $t_{DELAY}$ . At this time, the UV pin output stays at "H".
- (4) Release status to undervoltage detection status  
 $V_{SENSE}$  drops, and when it goes below the undervoltage detection voltage ( $V_{UVDET}$ ), the UV pin output becomes "L" after  $t_{RESET}$  and changes to undervoltage detection status. At this time, the OV pin output stays at "H".



\*1. Parasitic diode

Figure 21 Operation of S-191L/191N Series M / N / Q / R type



**Figure 22** Timing Chart of S-191L/191N Series M / N / Q / R Type

### 1.3 SENSE pin

The SENSE pin is the input pin for the detection voltage. The power supply VDD pin and SENSE pin, for voltage detection, are divided. Therefore, as long as a voltage is supplied to the VDD pin, the reset signal will be held even if the input voltage to the SENSE pin drops below the minimum operation voltage. Also, the SENSE pin of this IC has a built-in reverse connection protection circuit. Even when the SENSE pin voltage is less than the VSS pin voltage, the voltage flowing from the VSS pin to the SENSE pin is reduced to 0.05 mA typ.

#### 1.3.1 Error when detection voltage is set externally

The undervoltage detection voltage and the overvoltage detection voltage can be set externally by connecting a node that was resistance-divided by the resistor ( $R_A$ ) and the resistor ( $R_B$ ) to the SENSE pin as shown in **Figure 23**.

For conventional products without the SENSE pin, external resistor cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if external resistor is large, problems such as oscillation or larger error in the hysteresis width may occur.

In this IC,  $R_A$  and  $R_B$  in **Figure 23** are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance ( $R_{SENSE}$ ) that will occur.

Although  $R_{SENSE}^{*1}$  in this IC is large to make the error small,  $R_A$  and  $R_B$  should be selected such that the error is within the allowable limits.

Please note that the supply voltage divided output is a function to divide and output the SENSE pin voltage so when the detection voltage is set externally, care is required as the supply voltage divider block output voltage will change.

- \*1. During supply voltage divided output stops: 6.8 M $\Omega$  min.  
During supply voltage divided output operates: 5.8 M $\Omega$  min.

**1.3.2 Selection of RA and RB**

In **Figure 23**, the relation between the external setting undervoltage detection voltage (VDUX) or the overvoltage detection voltage (VDOX) and the actual detection voltage (VUVDET, VOVDET) is ideally calculated by the equation below.

$$V_{DUX} = V_{UVDET} \times \left(1 + \frac{R_A}{R_B}\right) \dots\dots\dots(1)$$

$$V_{DOX} = V_{OVDET} \times \left(1 + \frac{R_A}{R_B}\right) \dots\dots\dots(1)$$

However, in reality there is an error in the current flowing through RSENSE. When considering this error, the relation between VDUX, VDOX and VOVDET is calculated as follows.

$$V_{DUX} = V_{UVDET} \times \left(1 + \frac{R_A}{R_B \parallel R_{SENSE}}\right)$$

$$= V_{UVDET} \times \left(1 + \frac{R_A}{\frac{R_B \times R_{SENSE}}{R_B + R_{SENSE}}}\right)$$

$$= V_{UVDET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times V_{UVDET} \dots\dots\dots(2)$$

$$V_{DOX} = V_{OVDET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times V_{OVDET} \dots\dots\dots(2)$$

By using equations (1) and (2), the error is calculated as  $V_{UVDET} \times \frac{R_A}{R_{SENSE}}$ ,  $V_{OVDET} \times \frac{R_A}{R_{SENSE}}$ . The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

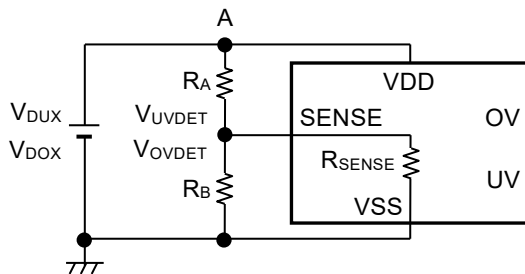
$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100 [\%] = \frac{R_A \parallel R_B}{R_{SENSE}} \times 100 [\%] \dots\dots(3)$$

As seen in equation (3), the smaller the resistance values of RA and RB compared to RSENSE, the smaller the error rate becomes.

Also, the relation between the external setting undervoltage hysteresis width (VHUX) or the overvoltage hysteresis width (VHOX) and the hysteresis width (VUVHYS, VOVHYS) is calculated by equation below. Error due to RSENSE also occurs to the relation in a similar way to the detection voltage.

$$V_{HUX} = V_{UVHYS} \times \left(1 + \frac{R_A}{R_B}\right) \dots\dots\dots(4)$$

$$V_{HOX} = V_{OVHYS} \times \left(1 + \frac{R_A}{R_B}\right) \dots\dots\dots(4)$$



**Figure 23 Detection Voltage External Setting Circuit**

**Caution** If RA and RB are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.

#### 1.4 Delay circuit

The delay circuit comes with a function for adjusting the release delay time ( $t_{\text{DELAY}}$ ) from when the SENSE pin voltage ( $V_{\text{SENSE}}$ ) enters the state in **Table 18** and until the output pin inverts.

**Table 18**

| Release operation    | Status  | Output Pin |
|----------------------|---|------------|
| Undervoltage release | Undervoltage release voltage ( $V_{\text{UVREL}} = V_{\text{UVDET}} + V_{\text{UVHYS}}$ ) or more | UV pin     |
| Overvoltage release  | Overvoltage release voltage ( $V_{\text{OVREL}} = V_{\text{OVDET}} - V_{\text{OVHYS}}$ ) or lower | OV pin     |

$t_{\text{DELAY}}$  is determined by the delay coefficient, the release delay time adjustment capacitor ( $C_{\text{D}}$ ) and the release delay time when the CD pin is open ( $t_{\text{DELAY0}}$ ). They are calculated by the equations below.

$$t_{\text{DELAY}} [\text{ms}] = \text{Delay coefficient} \times C_{\text{D}} [\text{nF}] + t_{\text{DELAY0}} [\text{ms}]$$

**Table 19**

| Operation Temperature | Delay Coefficient |      |      |
|-----------------------|-------------------|------|------|
|                       | Min.              | Typ. | Max. |
| Ta = +105°C           | 2.71              | 3.05 | 3.35 |
| Ta = +25°C            | 2.92              | 3.06 | 3.14 |
| Ta = -40°C            | 2.65              | 3.09 | 3.41 |

**Table 20**

| Operation Temperature | Release Delay Time when CD Pin is Open ( $t_{\text{DELAY0}}$ ) |      |      |
|-----------------------|--|------|------|
|                       | Min.   | Typ. | Max. |
| Ta = +105°C           | 0.05   | 0.10 | 0.17 |
| Ta = +25°C            | 0.06   | 0.11 | 0.19 |
| Ta = -40°C            | 0.06   | 0.13 | 0.25 |

- Caution 1.** Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.
2. There is no limit for the capacitance of  $C_{\text{D}}$  as long as the leakage current of the capacitor can be ignored against the built-in constant current value (approximately 160 nA). The leakage current may cause error in delay time. When the leakage current is larger than the built-in constant current, no detect or release takes place.
  3. The above equations will not guarantee successful operation. Determine the capacitance of  $C_{\text{D}}$  through thorough evaluation including temperature characteristics in the actual usage conditions.

## 2. Supply voltage divider block

### 2.1 Basic operation

**Figure 24** shows the block diagram of the supply voltage divider block to describe basic operation. Reference voltage ( $V_{refpm}$ ) is generated by dividing the SENSE pin voltage ( $V_{SENSE}$ ) using the dividing resistance ( $R_{pm1}$  and  $R_{pm2}$ ). Since the buffer amplifier constitutes a voltage follower, it can perform the feedback control so that the output voltage of supply voltage divider block ( $V_{PMOUT}$ ) and  $V_{refpm}$  are the same. Low output impedance is realized by the buffer amplifier, while outputting  $V_{PMOUT}$  according to  $V_{SENSE}$ . When "L" is input to the PMEN pin, the current which flows to  $R_{pm1}$  and  $R_{pm2}$  and the current which flows to the buffer amplifier can be stopped. The buffer amplifier output is pulled down to  $V_{SS}$  by the built-in N-channel transistor, and  $V_{PMOUT}$  is set to the  $V_{SS}$  level.

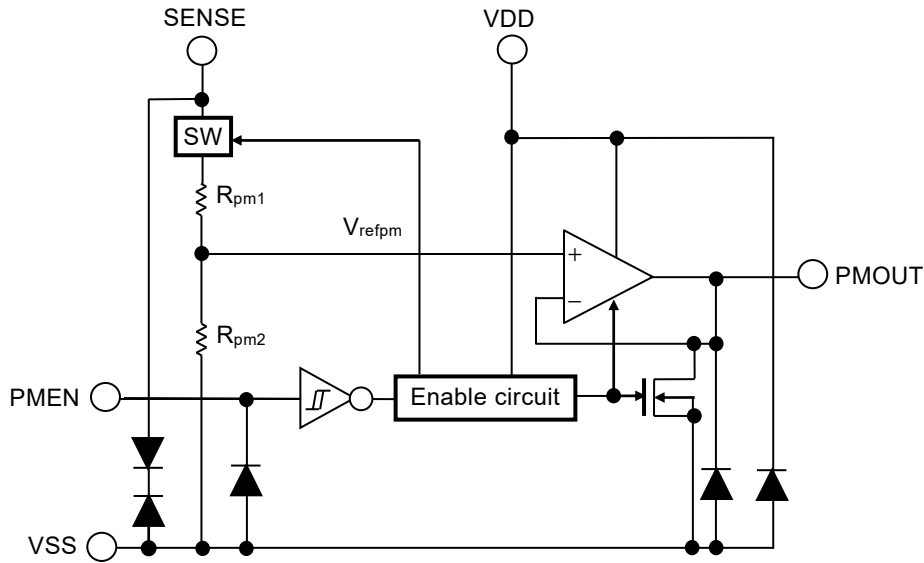


Figure 24

## 2.2 PMEN pin

Input to the PMEN pin controls the internal circuit in the supply voltage divided output, and it starts or stops the supply voltage divided output.

When the PMEN pin is set to "L" level, the internal circuit stops operating, reducing current consumption significantly. In addition, the PMEN pin has absolutely no effect on the operation of the detector block.

Note that the current consumption increases when a voltage of 0.8 V to  $V_{DD} \text{ min.} - 0.3 \text{ V}$  is applied to the PMEN pin. The PMEN pin is configured as shown in **Figure 25**.

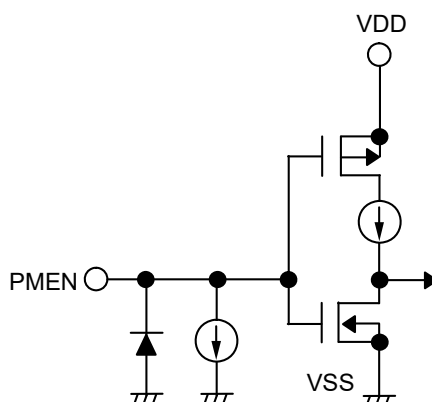
Since the PMEN pin is internally pulled down to the VSS pin in the floating status, the PMOUT pin is set to the VSS level. When the PMEN pin is set to "H" level, PMEN pin input current "H" ( $I_{PSH}$ ) in **Table 14** of "■ Electrical Characteristics" flows through the PMEN pin and care is required.

**Table 21**

| Product Type          | PMEN Pin | Internal Circuit | PMOUT Pin Output           | Current Consumption |
|-----------------------|----------|------------------|----------------------------|---------------------|
| L / M / N / P / Q / R | "H": ON  | Operate          | Constant value*1           | $I_{SSP1}$          |
| L / M / N / P / Q / R | "L": OFF | Stop             | Pulled down to $V_{SS}$ *2 | $I_{SS1}$           |

\*1. The constant value is output due to the operation based on the set output voltage value of supply voltage divider block.

\*2. The buffer amplifier output is pulled down to  $V_{SS}$  by the built-in N-channel transistor, and PMOUT pin output is set to the  $V_{SS}$  level due to resistance ( $R_{Low} = 2.8 \text{ k}\Omega \text{ typ.}$ ) of the discharge shunt circuit and a load.



**Figure 25**

### 2.3 PMEN pin voltage and output voltage of supply voltage divider block ( $V_{PMOUT}$ )

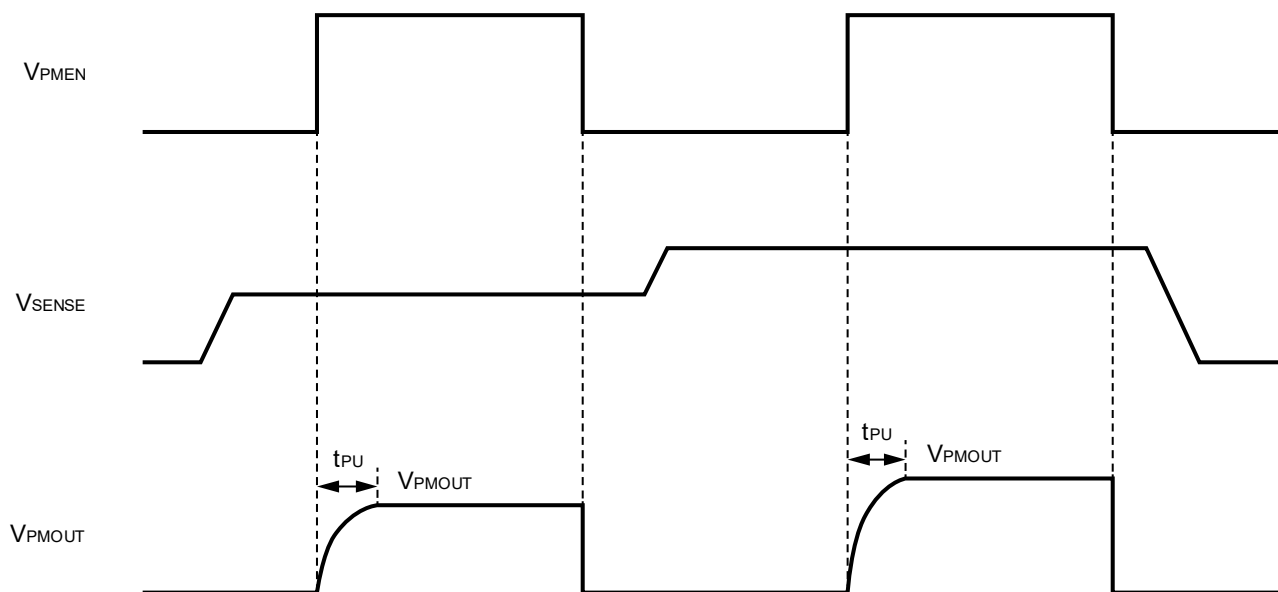
**Figure 26** shows the timing chart of the supply voltage divided output.

When "H" is input to the PMEN pin, the supply voltage divided output operates. When the set-up time ( $t_{PU}$ ) = 50 ms max.\*1 elapses,  $V_{PMOUT}$  stabilizes, the SENSE pin voltage ( $V_{SENSE}$ ) is divided at the set ratio, and the voltage is output to the PMOUT pin.

When "L" is input to the PMEN pin, the supply voltage divided output is stopped.  $V_{PMOUT}$  is set to the  $V_{SS}$  level by the built-in N-channel transistor.

By repeatedly inputting "H" and "L" to the PMEN pin, it is possible to lower current consumption when the supply voltage divided output is not needed.

\*1. When  $5\text{ V} \leq V_{SENSE} \leq 18\text{ V}$ ,  $C_{PM} = 0.22\ \mu\text{F}$ , no load



**Figure 26**

**Remark**  $V_{PMEN} = V_{DD} \leftrightarrow V_{SS}$



## ■ Usage Precautions

### 1. Power on sequence

#### 1.1 Power on when release delay time adjustment capacitor ( $C_D$ ) $\geq 1$ nF

When connecting a 1 nF or larger capacitor to the CD pin, there is no specific order for turning on the SENSE and VDD pins.

#### 1.2 Power on when release delay time adjustment capacitor ( $C_D$ ) $< 1$ nF or CD pin is open

When connecting a capacitor of less than 1 nF to the CD pin, turn on the VDD pin before the SENSE pin as shown in **Figure 27**.

When  $V_{OVDET} \geq V_{SENSE} \geq V_{UVREL}$  applies, both the overvoltage output voltage ( $V_{OV}$ ) and the undervoltage output voltage ( $V_{UV}$ ) become "H", and the detector enters release status.

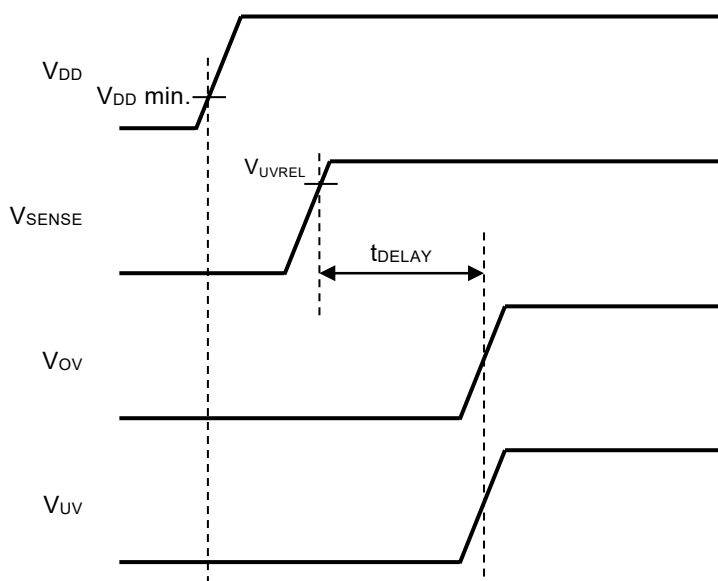


Figure 27

**Caution** When connecting a capacitor of less than 1 nF to the CD pin and the SENSE pin is turned on before the VDD pin, a release may mistakenly occur even if  $V_{SENSE}$  is less than  $V_{UVREL}$ .

## ■ Precautions

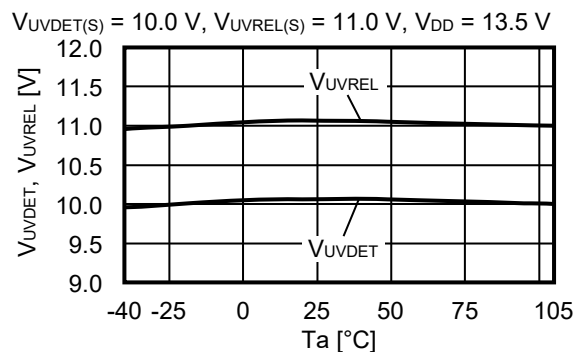
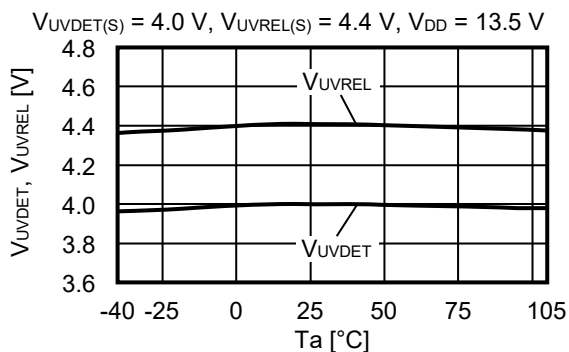
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Because the SENSE pin has a high impedance, malfunctions may occur due to noise. Be careful of wiring adjoining SENSE pin wiring in actual applications.
- In the supply voltage divided output, the values of an overshoot and an undershoot in the output voltage vary depending on the variation factors of input voltage start-up, input voltage fluctuation and load fluctuation etc., or the capacitance of  $C_{PM}$  and the value of the equivalent series resistance (ESR), which may cause a problem to the stable operation. Perform thorough evaluation including the temperature characteristics with an actual application to select  $C_{PM}$ .
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

## ■ Characteristics (Typical Data)

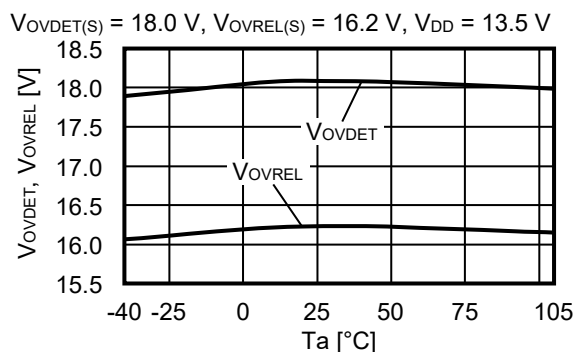
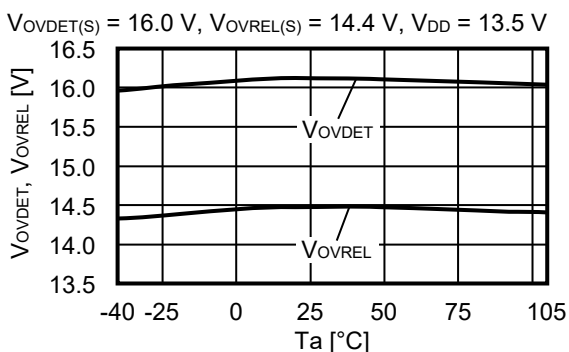
### 1. Detector block

#### 1.1 Detection voltage ( $V_{UVDET}$ , $V_{OVDET}$ ), Release voltage ( $V_{UVREL}$ , $V_{OVREL}$ ) vs. Temperature ( $T_a$ )

##### 1.1.1 Undervoltage detection

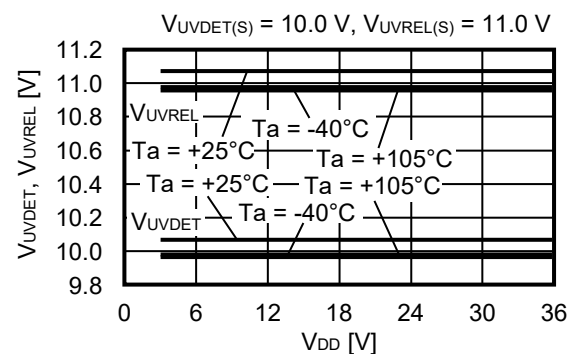
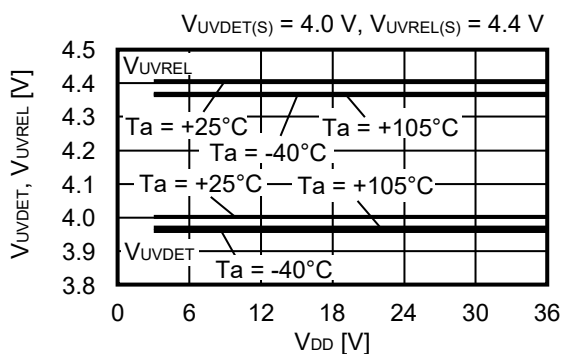


##### 1.1.2 Overvoltage detection

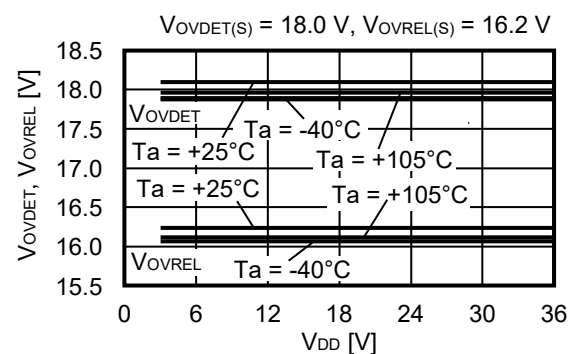
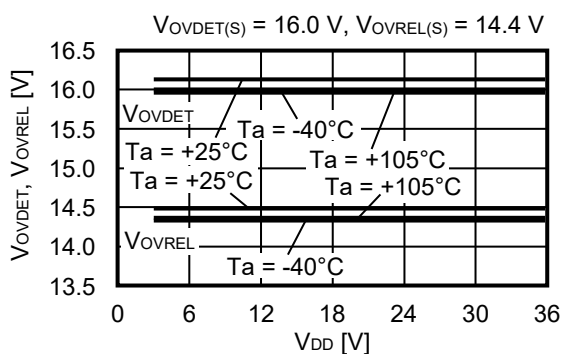


#### 1.2 Detection voltage ( $V_{UVDET}$ , $V_{OVDET}$ ), Release voltage ( $V_{UVREL}$ , $V_{OVREL}$ ) vs. Power supply voltage ( $V_{DD}$ )

##### 1.2.1 Undervoltage detection

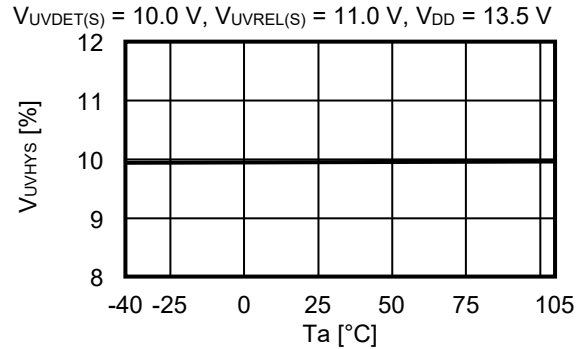
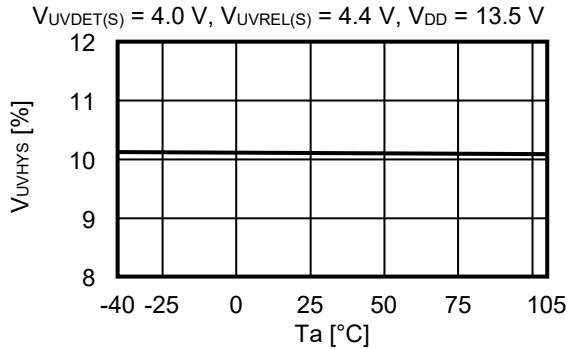


##### 1.2.2 Overvoltage detection

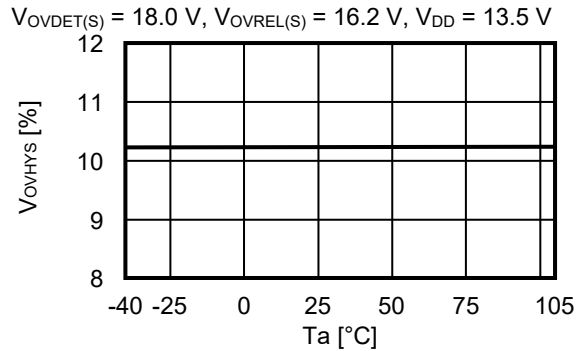
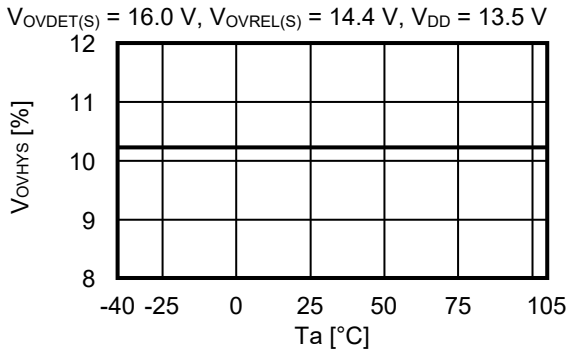


**1.3 Hysteresis width ( $V_{UVHYS}$ ,  $V_{OVHYS}$ ) vs. Temperature ( $T_a$ )**

**1.3.1 Undervoltage detection**

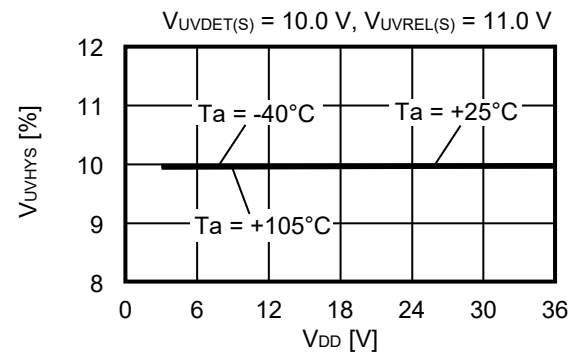
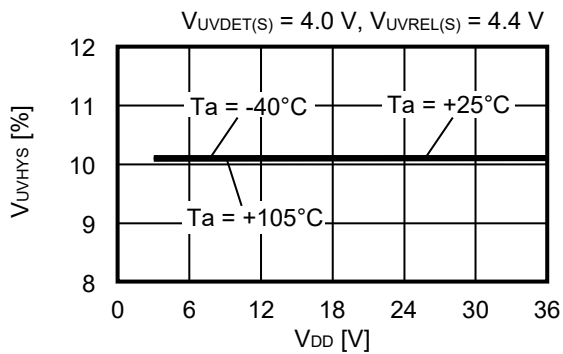


**1.3.2 Overvoltage detection**

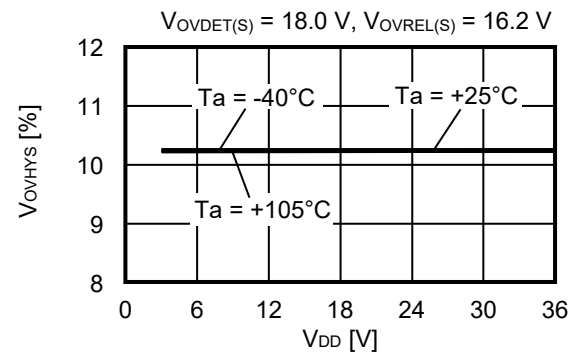
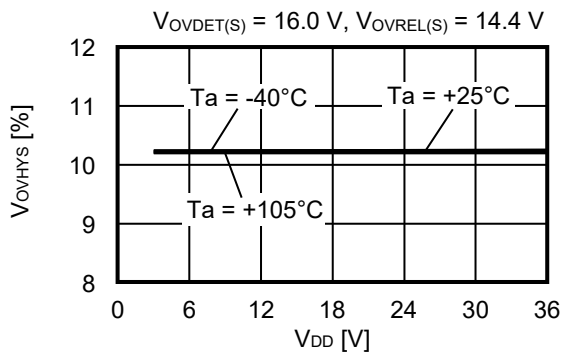


**1.4 Hysteresis width ( $V_{UVHYS}$ ,  $V_{OVHYS}$ ) vs. Power supply voltage ( $V_{DD}$ )**

**1.4.1 Undervoltage detection**

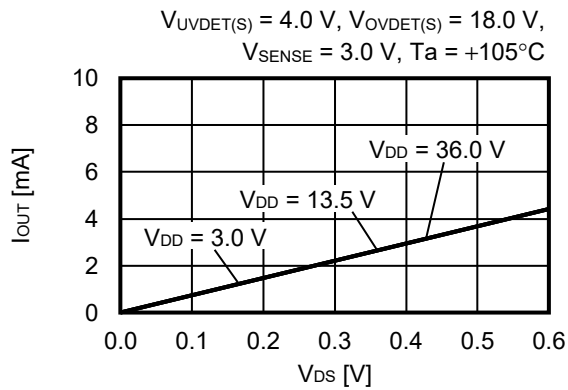
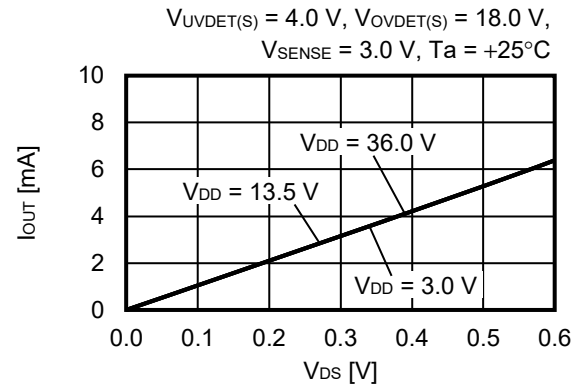
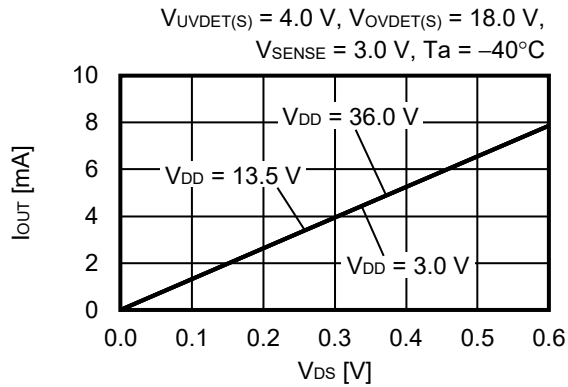


**1.4.2 Overvoltage detection**

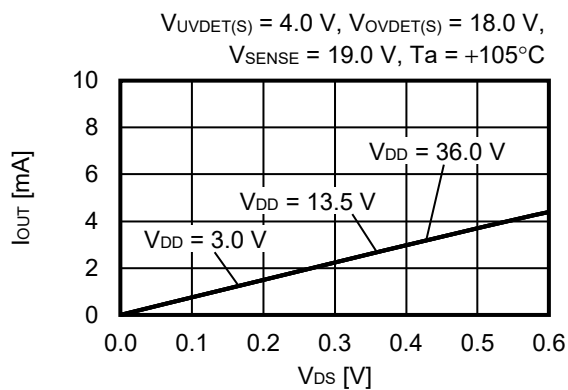
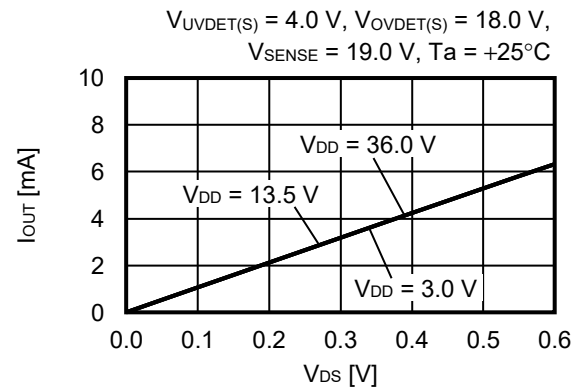
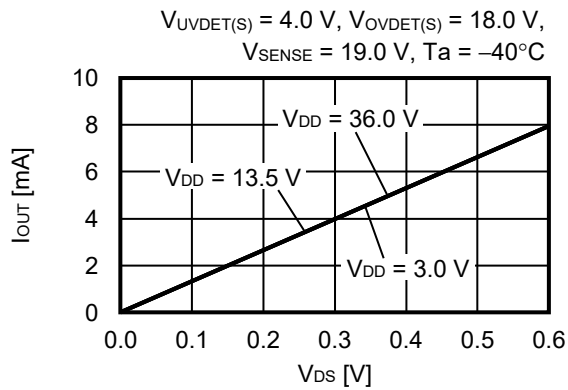


**1.5 Nch transistor output current ( $I_{OUT}$ ) vs.  $V_{DS}$**

**1.5.1 Undervoltage detection**



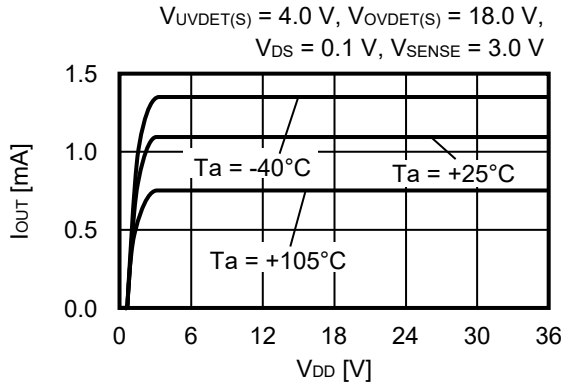
**1.5.2 Overvoltage detection**



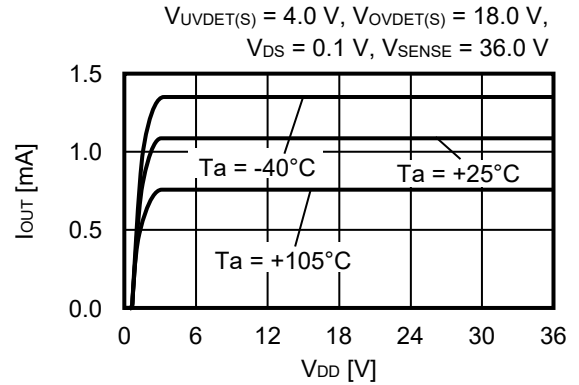
**Remark**  $V_{DS}$ : Drain-to-source voltage of the output transistor

**1.6 Nch transistor output current ( $I_{OUT}$ ) vs. Power supply voltage ( $V_{DD}$ )**

**1.6.1 Undervoltage detection**



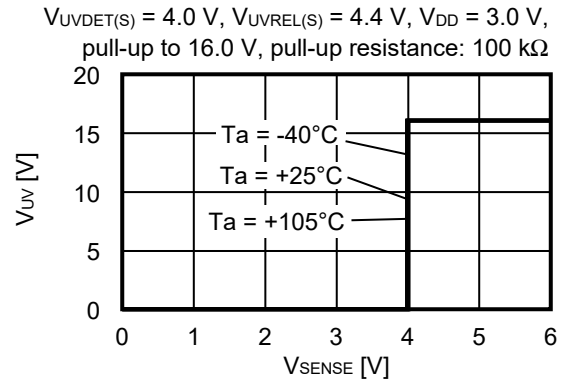
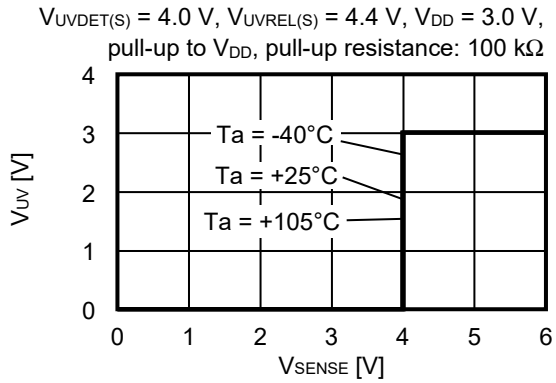
**1.6.2 Overvoltage detection**



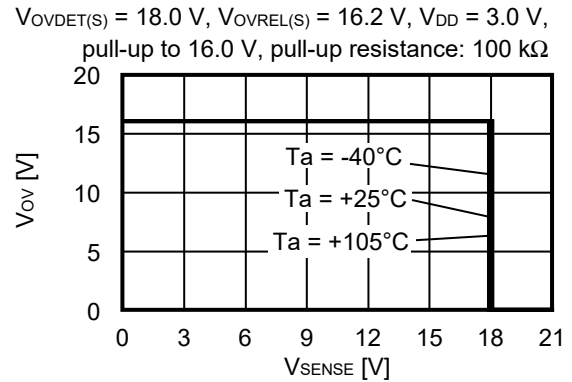
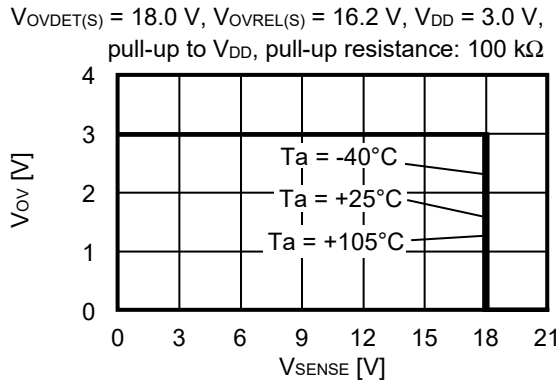
**Remark**  $V_{DS}$ : Drain-to-source voltage of the output transistor

**1.7 Output voltage ( $V_{UV}$ ,  $V_{OV}$ ) vs. SENSE pin voltage ( $V_{SENSE}$ )**

**1.7.1 Undervoltage detection**

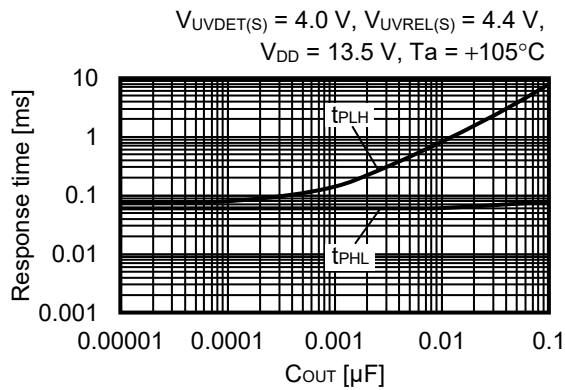
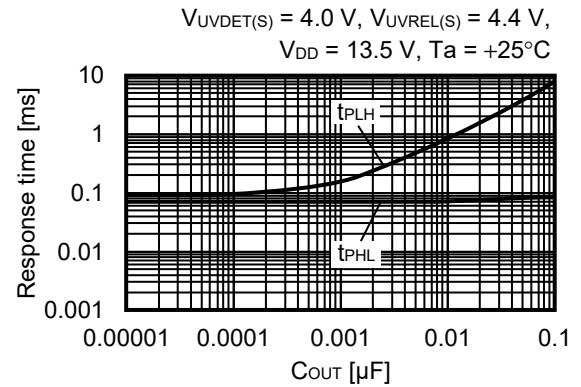
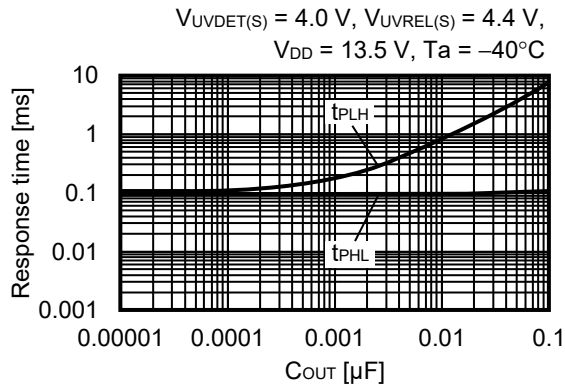


**1.7.2 Overvoltage detection**

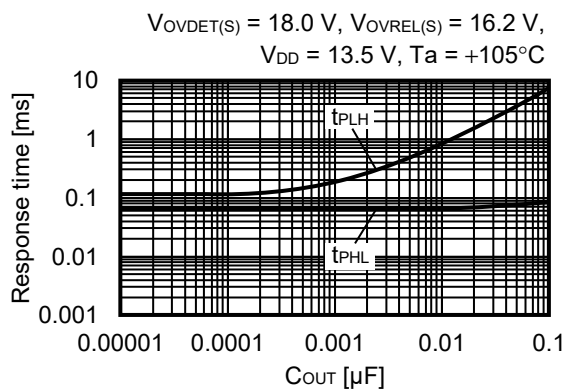
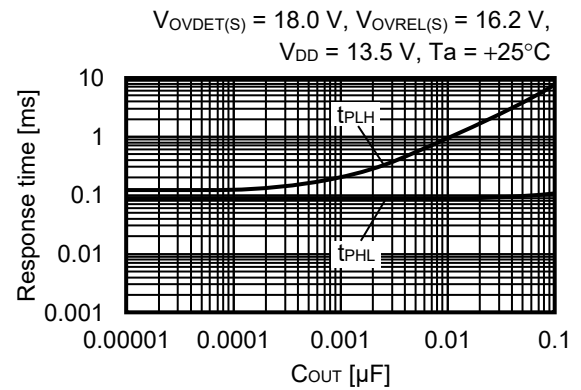
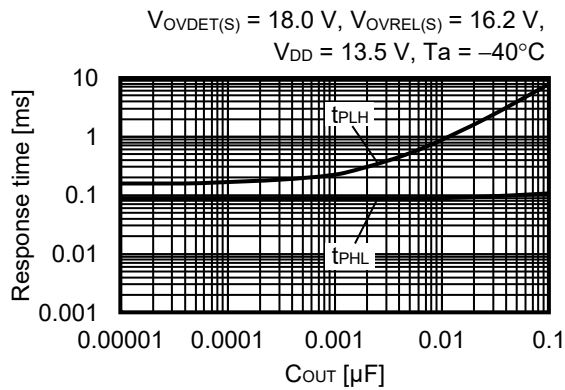


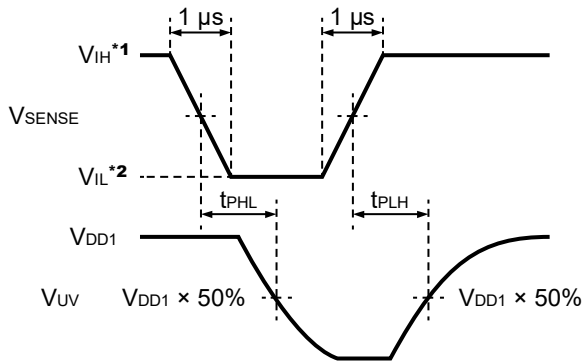
**1.8 Dynamic response vs. Output pin capacitance (C<sub>OUT</sub>) (CD pin; open)**

**1.8.1 Undervoltage detection**



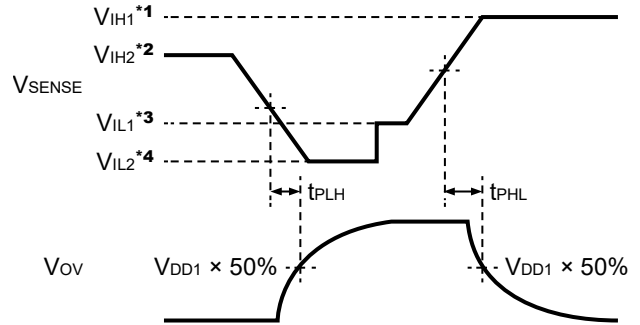
**1.8.2 Overvoltage detection**





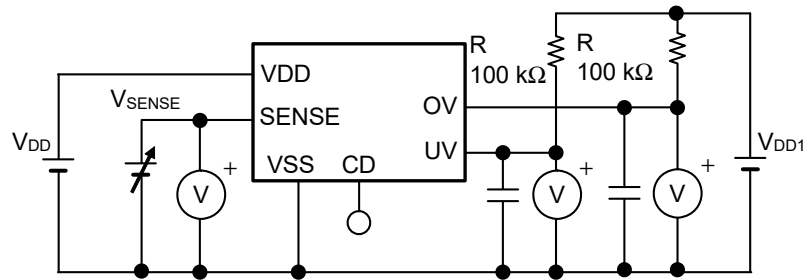
- \*1.  $V_{IH} = V_{UVDET(S)} + 1.0 \text{ V}$
- \*2.  $V_{IL} = V_{UVDET(S)} - 1.0 \text{ V}$

**Figure 28 Test Condition of Response Time (Undervoltage Detection)**



- \*1.  $V_{IH1} = V_{OVDET(S)} + 1.0 \text{ V}$
- \*2.  $V_{IH2} = V_{OVREL(S)} + 1.0 \text{ V}$
- \*3.  $V_{IL1} = V_{OVDET(S)} - 1.0 \text{ V}$
- \*4.  $V_{IL2} = V_{OVREL(S)} - 1.0 \text{ V}$

**Figure 29 Test Condition of Response Time (Overvoltage Detection)**



**Figure 30 Test Circuit of Response Time**

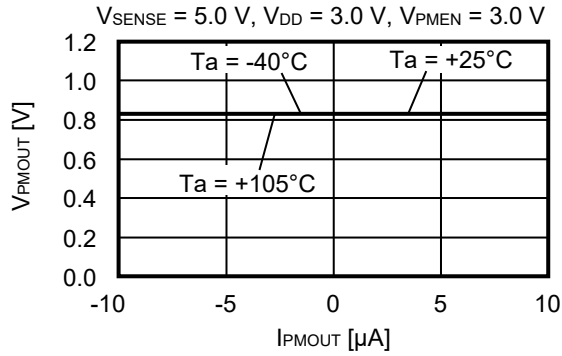
**Caution** The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.



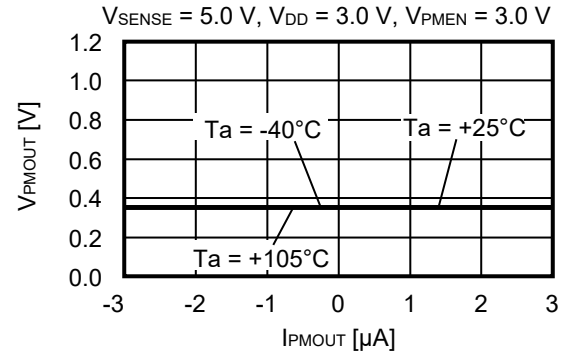
## 2. Supply voltage divider block

### 2.1 Output voltage of supply voltage divider block ( $V_{PMOUT}$ ) vs. Load current ( $I_{PMOUT}$ )

#### 2.1.1 $V_{PMOUT} = V_{SENSE}/6$

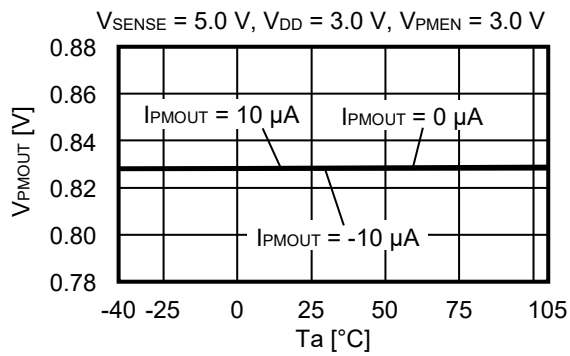


#### 2.1.2 $V_{PMOUT} = V_{SENSE}/14$

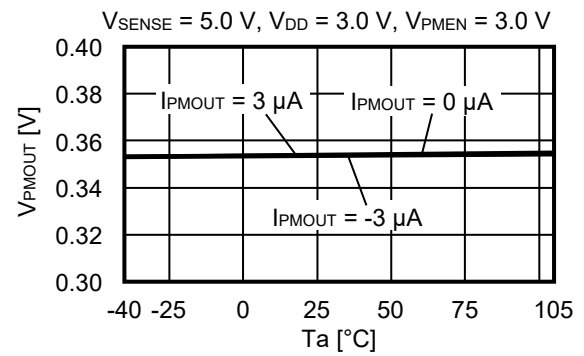


### 2.2 Output voltage of supply voltage divider block ( $V_{PMOUT}$ ) vs. Temperature ( $T_a$ )

#### 2.2.1 $V_{PMOUT} = V_{SENSE}/6$

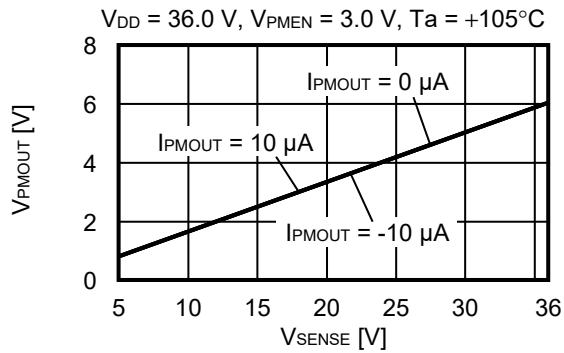
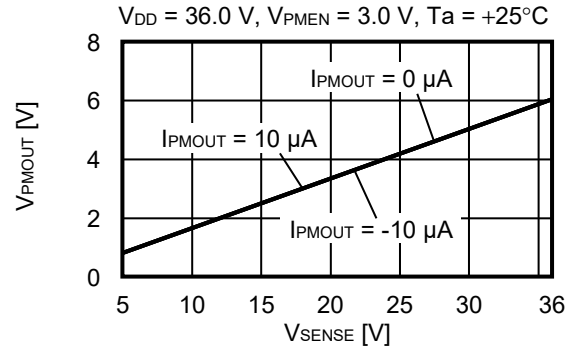
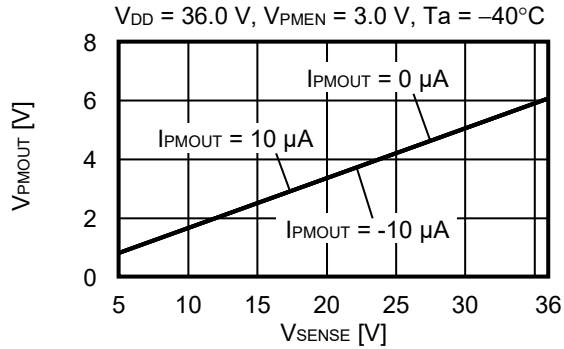


#### 2.2.2 $V_{PMOUT} = V_{SENSE}/14$

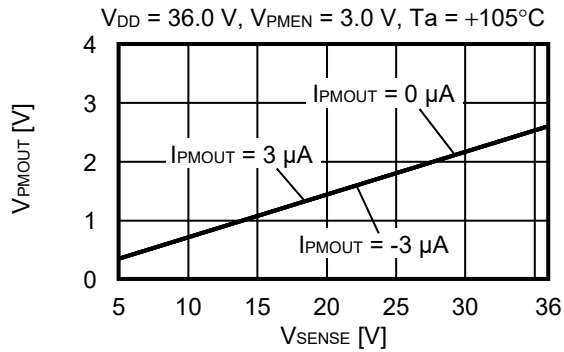
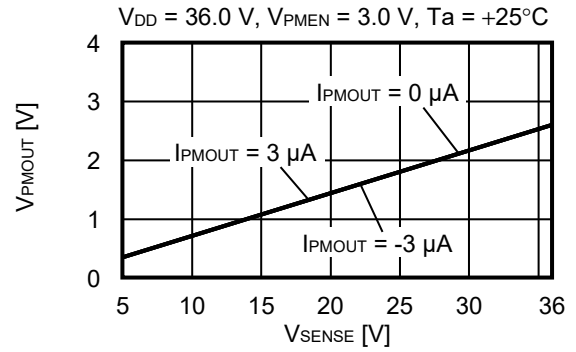
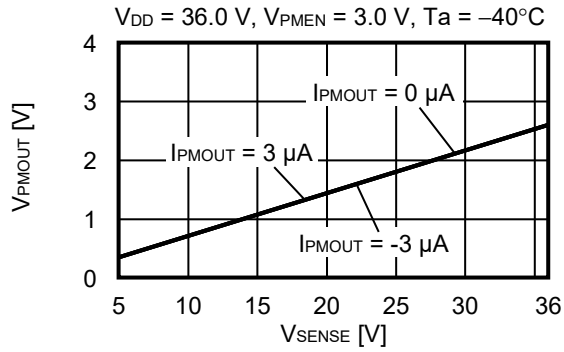


**2.3 Output voltage of supply voltage divider block ( $V_{PMOUT}$ ) vs. SENSE pin voltage ( $V_{SENSE}$ )**

**2.3.1  $V_{PMOUT} = V_{SENSE}/6$**

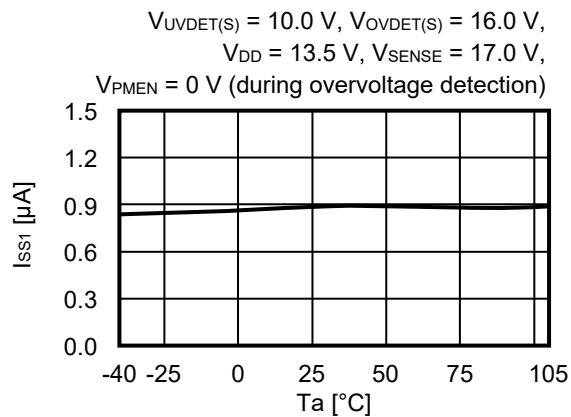
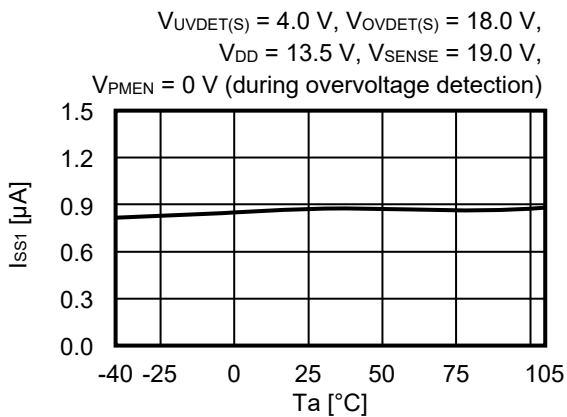
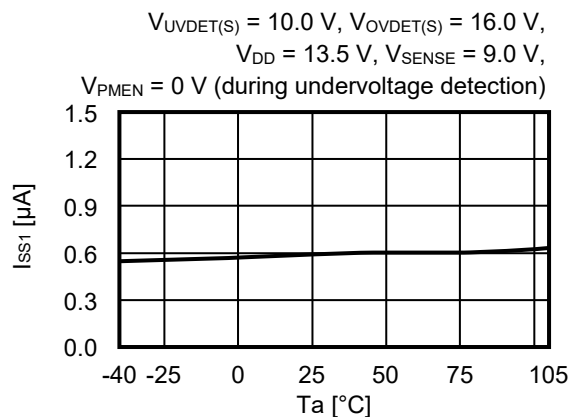
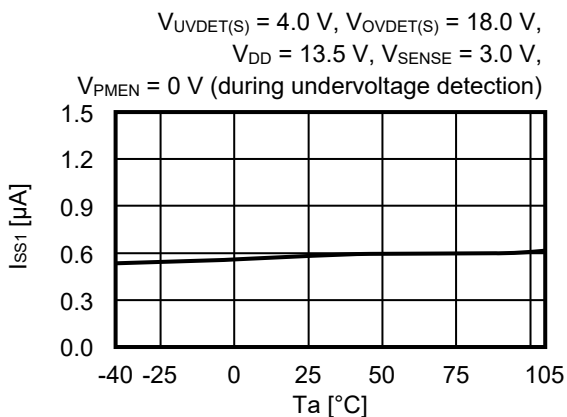
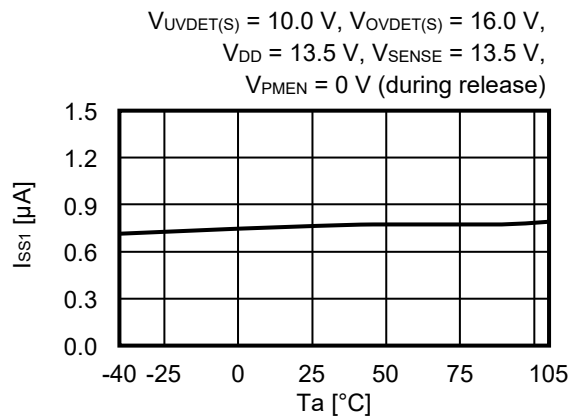
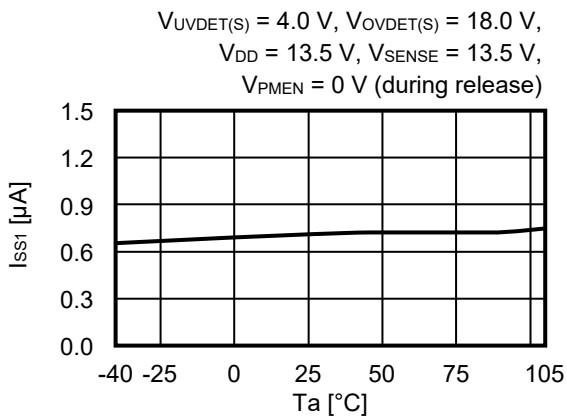


**2.3.2  $V_{PMOUT} = V_{SENSE}/14$**

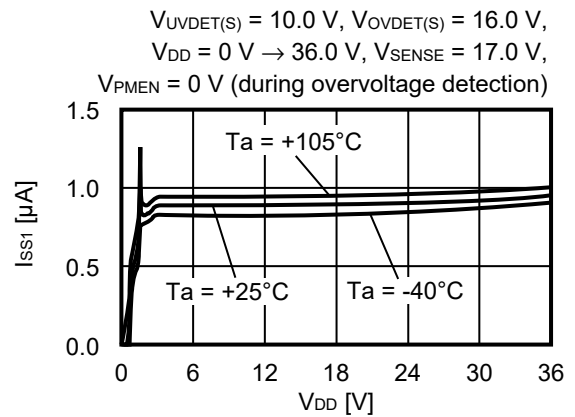
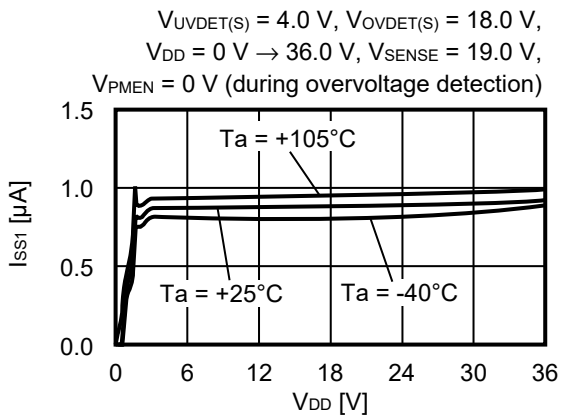
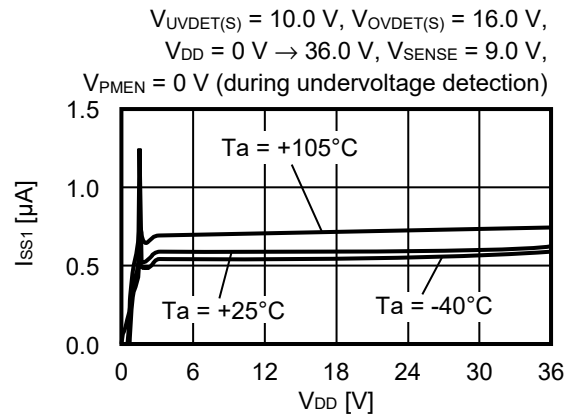
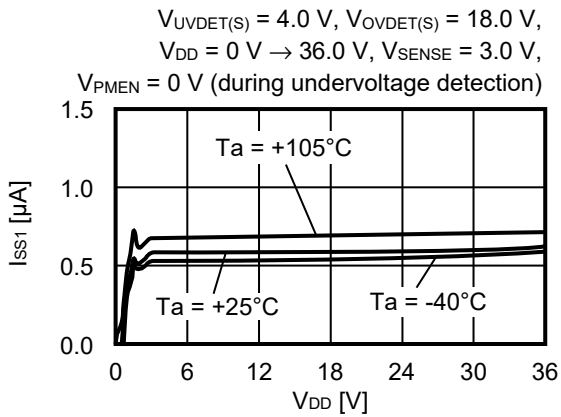
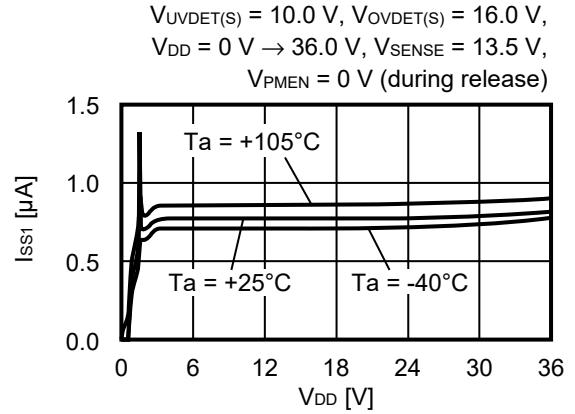
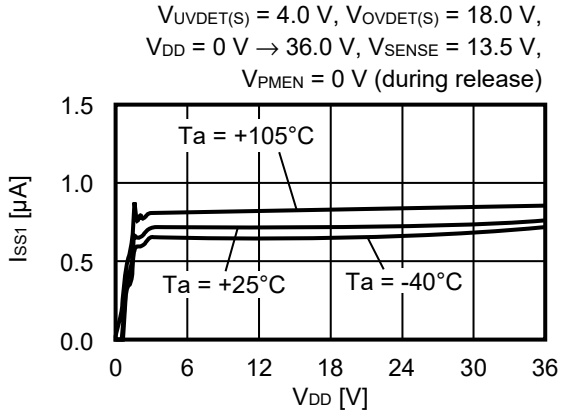


### 3. Overall

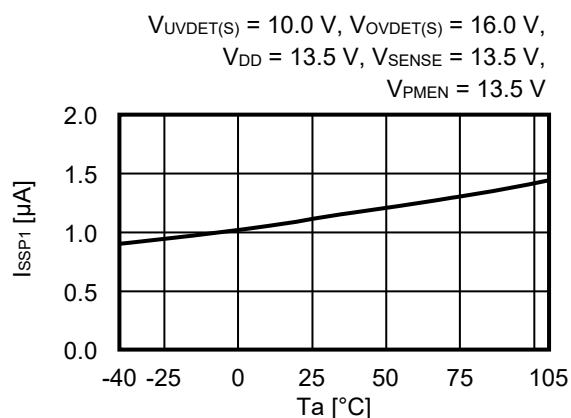
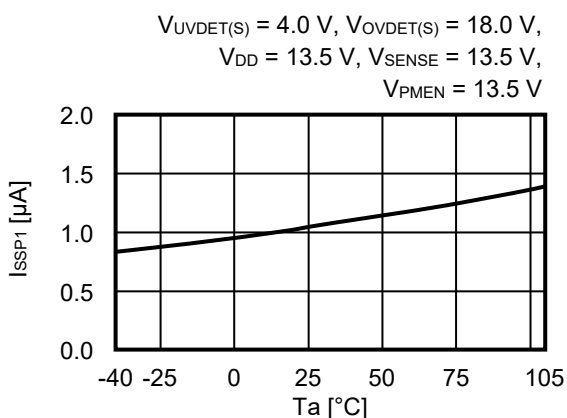
#### 3.1 Current consumption (I<sub>SS1</sub>) vs. Temperature (Ta)



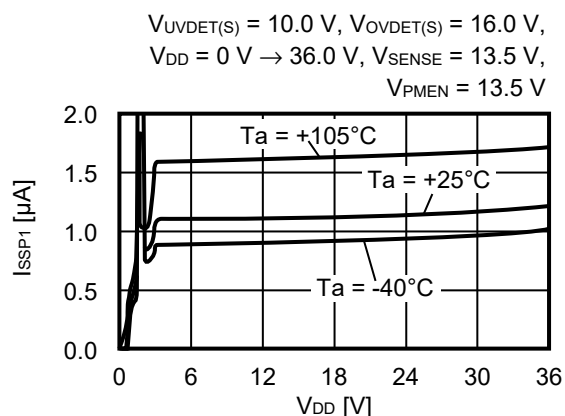
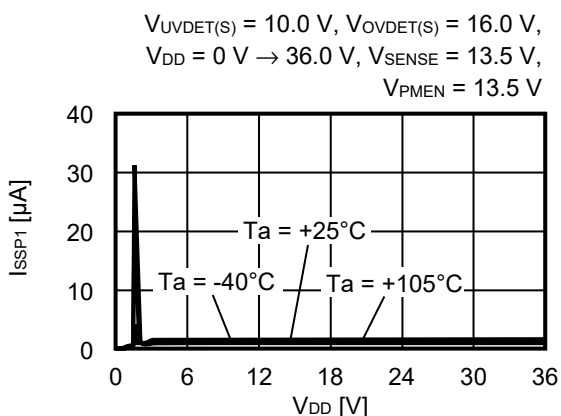
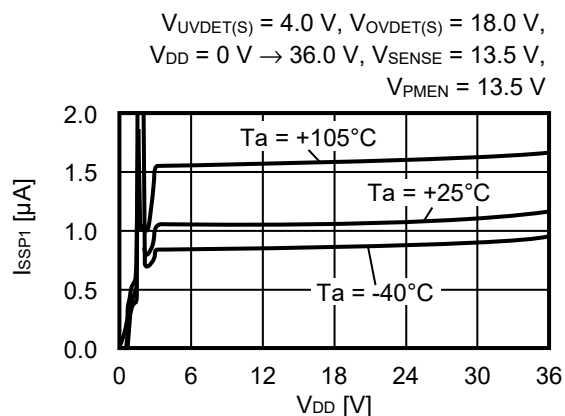
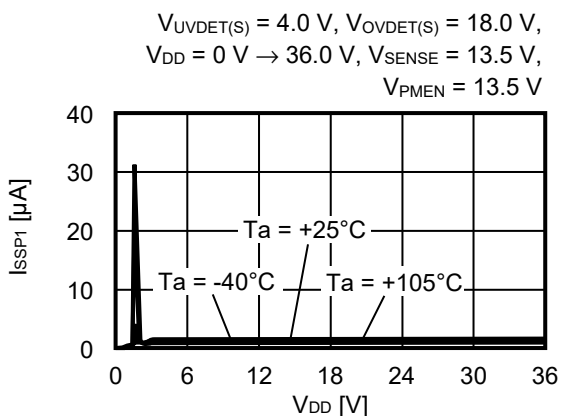
**3.2 Current consumption (I<sub>SS1</sub>) vs. Power supply voltage (V<sub>DD</sub>) (No load)**



**3.3 Current consumption ( $I_{SSP1}$ ) vs. Temperature ( $T_a$ )**  
 (No load, during supply voltage divided output operates)



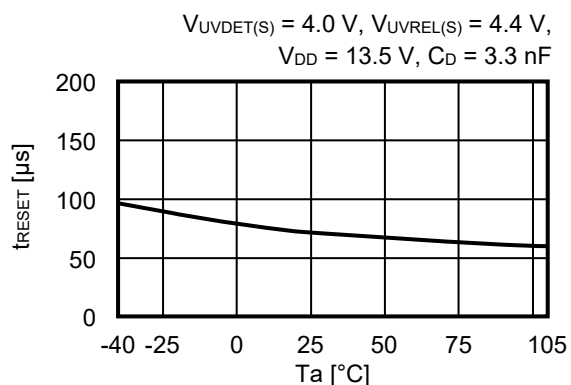
**3.4 Current consumption ( $I_{SSP1}$ ) vs. Power supply voltage ( $V_{DD}$ )**  
 (No load, during supply voltage divided output operates)



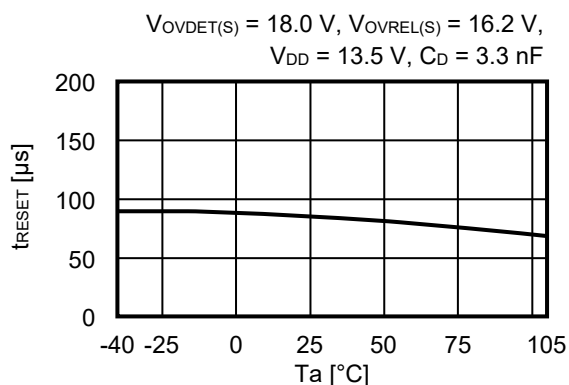
■ Reference Data

1. Detection response time ( $t_{\text{RESET}}$ ) vs. Temperature ( $T_a$ )

1.1 Undervoltage detection

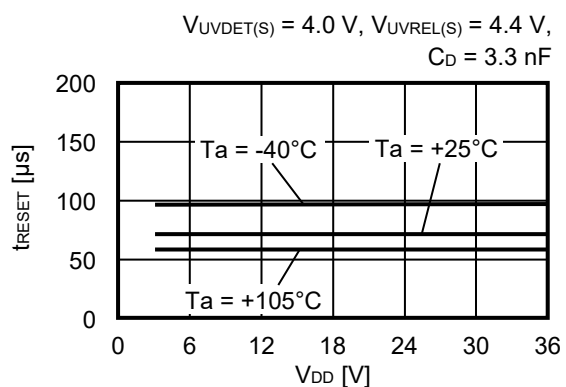


1.2 Overvoltage detection

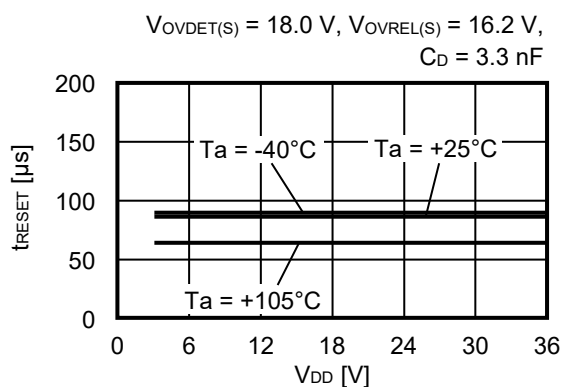


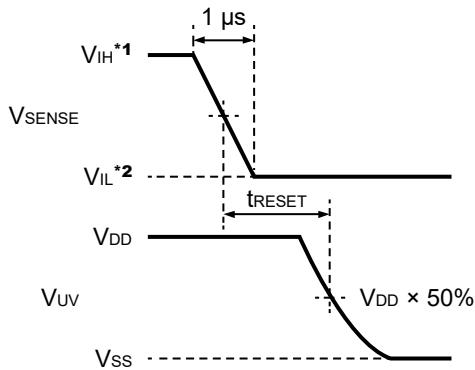
2. Detection response time ( $t_{\text{RESET}}$ ) vs. Power supply voltage ( $V_{\text{DD}}$ )

2.1 Undervoltage detection



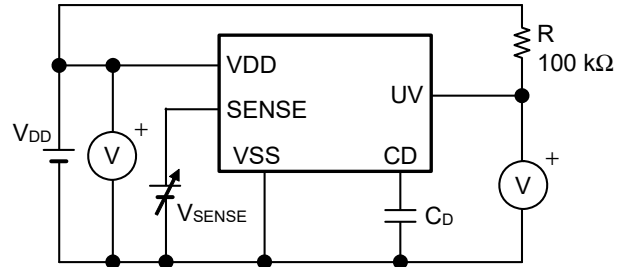
2.2 Overvoltage detection



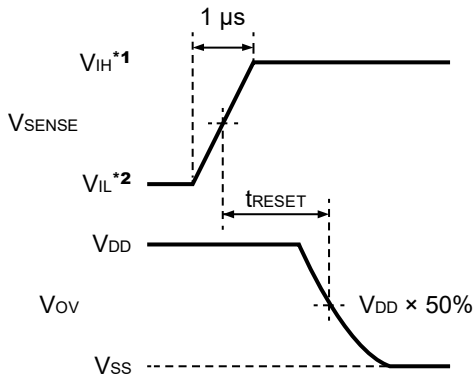


- \*1.  $V_{IH} = V_{UVDET(S)} + 1.0 \text{ V}$
- \*2.  $V_{IL} = V_{UVDET(S)} - 1.0 \text{ V}$

**Figure 31 Test Condition of Detection Response Time (Undervoltage Detection)**

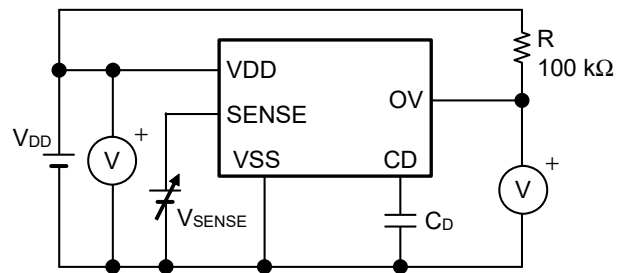


**Figure 32 Test Circuit of Detection Response Time (Undervoltage Detection)**



- \*1.  $V_{IH} = V_{OVDET(S)} + 1.0 \text{ V}$
- \*2.  $V_{IL} = V_{OVDET(S)} - 1.0 \text{ V}$

**Figure 33 Test Condition of Detection Response Time (Overvoltage Detection)**

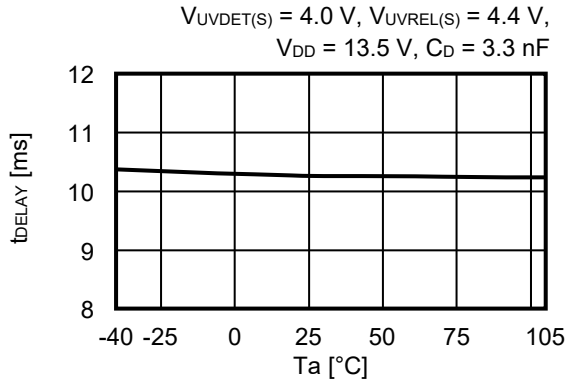


**Figure 34 Test Circuit of Detection Response Time (Overvoltage Detection)**

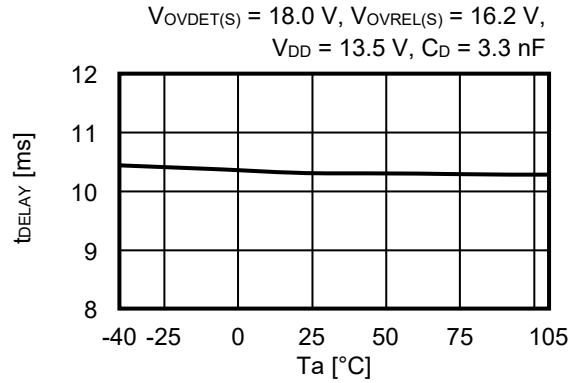
**Caution** The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

**3. Release delay time ( $t_{DELAY}$ ) vs. Temperature ( $T_a$ )**

**3.1 Undervoltage detection**

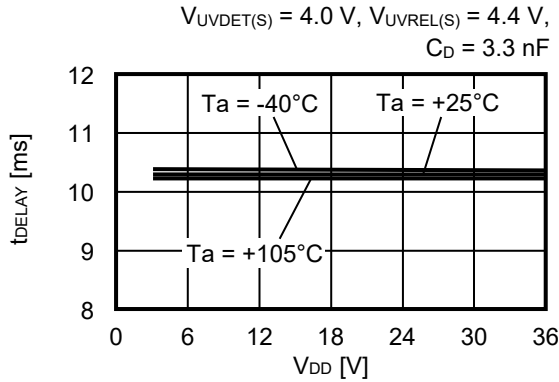


**3.2 Overvoltage detection**

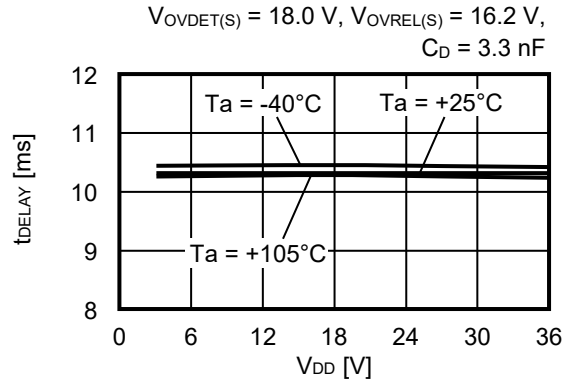


**4. Release delay time ( $t_{DELAY}$ ) vs. Power supply voltage ( $V_{DD}$ )**

**4.1 Undervoltage detection**

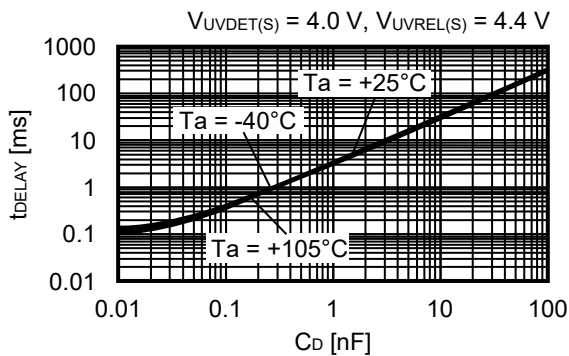


**4.2 Overvoltage detection**

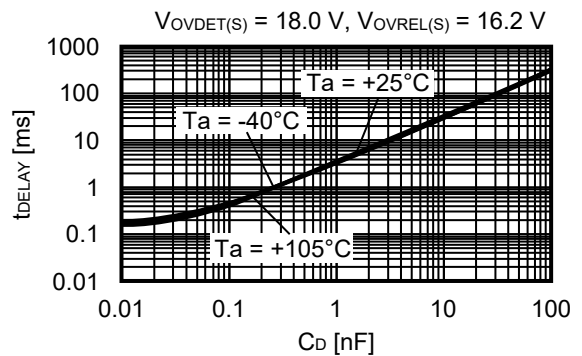


**5. Release delay time ( $t_{DELAY}$ ) vs. CD pin capacitance ( $C_D$ ) (Without output pin capacitance)**

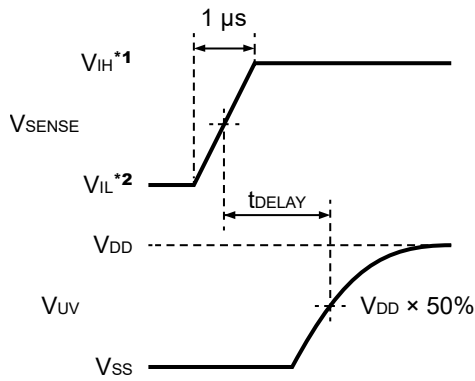
**5.1 Undervoltage detection**



**5.2 Overvoltage detection**

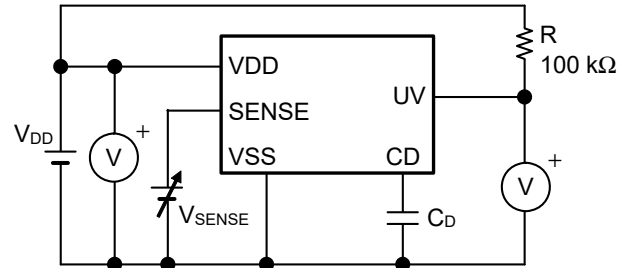




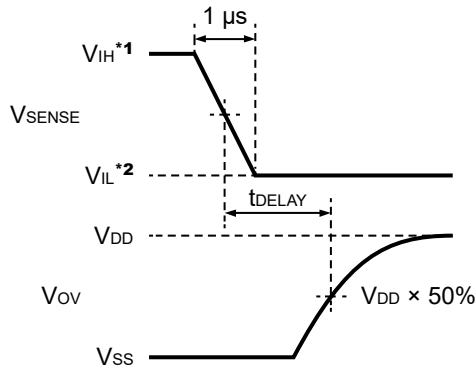


- \*1.  $V_{IH} = V_{UVREL(S)} + 1.0 \text{ V}$
- \*2.  $V_{IL} = V_{UVREL(S)} - 1.0 \text{ V}$

**Figure 35 Test Condition of Release Delay Time (Undervoltage Detection)**

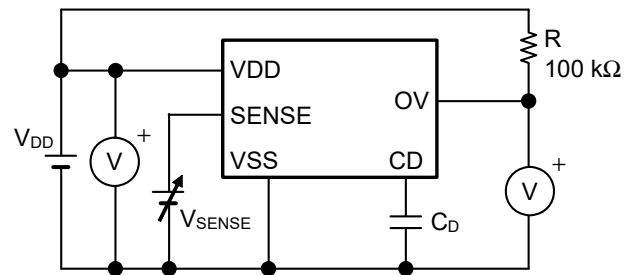


**Figure 36 Test Circuit of Release Delay Time (Undervoltage Detection)**



- \*1.  $V_{IH} = V_{OVREL(S)} + 1.0 \text{ V}$
- \*2.  $V_{IL} = V_{OVREL(S)} - 1.0 \text{ V}$

**Figure 37 Test Condition of Release Delay Time (Overvoltage Detection)**



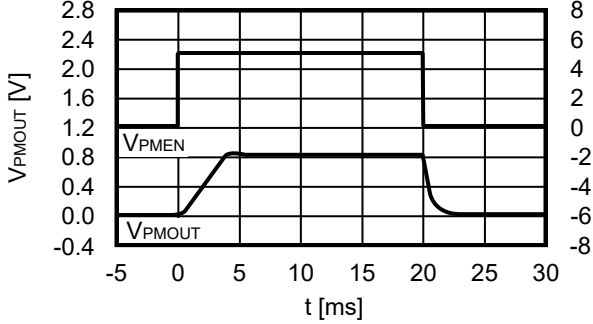
**Figure 38 Test Circuit of Release Delay Time (Overvoltage Detection)**

**Caution** The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

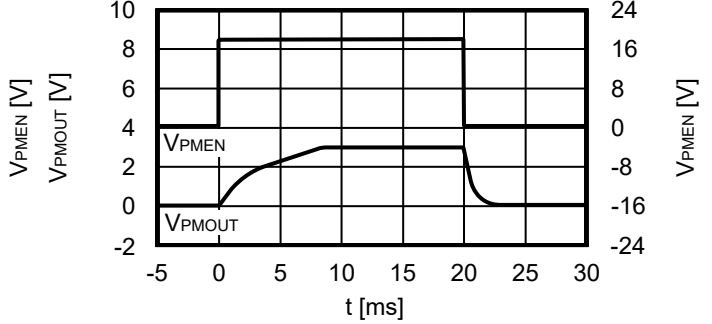
**6. Transient response characteristics of PMEN pin (Ta = +25°C)**

**6.1  $V_{PMOUT} = V_{SENSE}/6$**

$V_{DD} = V_{SENSE} = 5.0\text{ V}$ ,  $C_{PM} = 0.22\ \mu\text{F}$ ,  
 $V_{PMEN} = 0\text{ V} \leftrightarrow 5.0\text{ V}$  ( $t_r = t_f = 1.0\ \mu\text{s}$ )

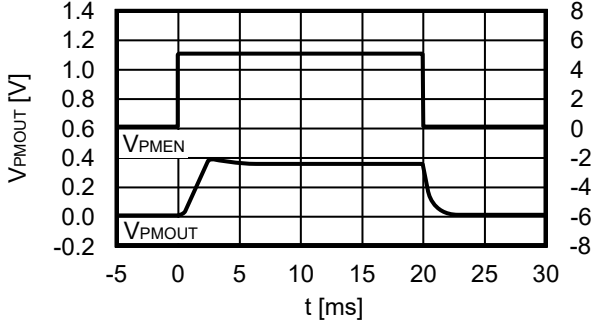


$V_{DD} = V_{SENSE} = 18.0\text{ V}$ ,  $C_{PM} = 0.22\ \mu\text{F}$ ,  
 $V_{PMEN} = 0\text{ V} \leftrightarrow 18.0\text{ V}$  ( $t_r = t_f = 1.0\ \mu\text{s}$ )

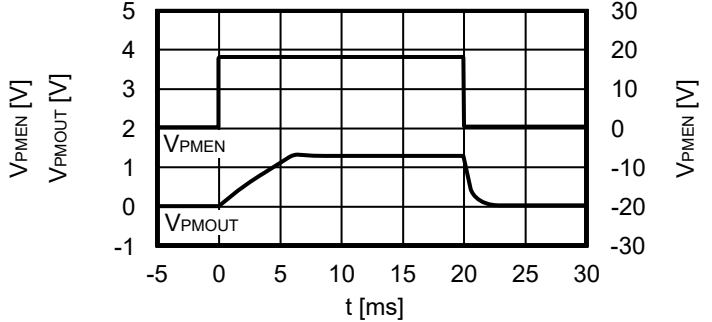


**6.2  $V_{PMOUT} = V_{SENSE}/14$**

$V_{DD} = V_{SENSE} = 5.0\text{ V}$ ,  $C_{PM} = 0.22\ \mu\text{F}$ ,  
 $V_{PMEN} = 0\text{ V} \leftrightarrow 5.0\text{ V}$  ( $t_r = t_f = 1.0\ \mu\text{s}$ )



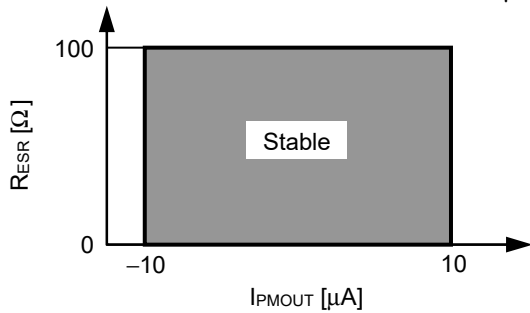
$V_{DD} = V_{SENSE} = 18.0\text{ V}$ ,  $C_{PM} = 0.22\ \mu\text{F}$ ,  
 $V_{PMEN} = 0\text{ V} \leftrightarrow 18.0\text{ V}$  ( $t_r = t_f = 1.0\ \mu\text{s}$ )



**7. Example of equivalent series resistance vs. Load current characteristics (Ta = +25°C)**

**7.1  $V_{PMOUT} = V_{SENSE}/6, V_{SENSE}/8, V_{SENSE}/12$**

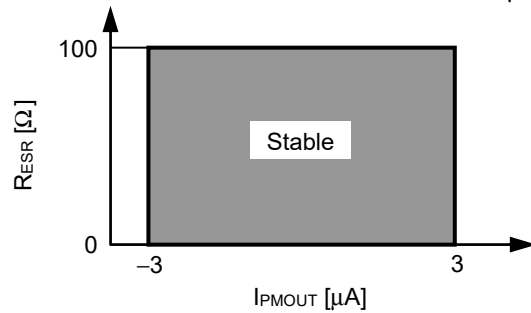
$C_{PM} = 0.1\ \mu\text{F}$



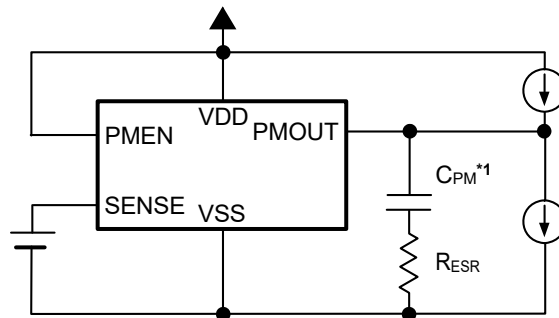
**Figure 39**

**7.2  $V_{PMOUT} = V_{SENSE}/14$**

$C_{PM} = 0.1\ \mu\text{F}$



**Figure 40**

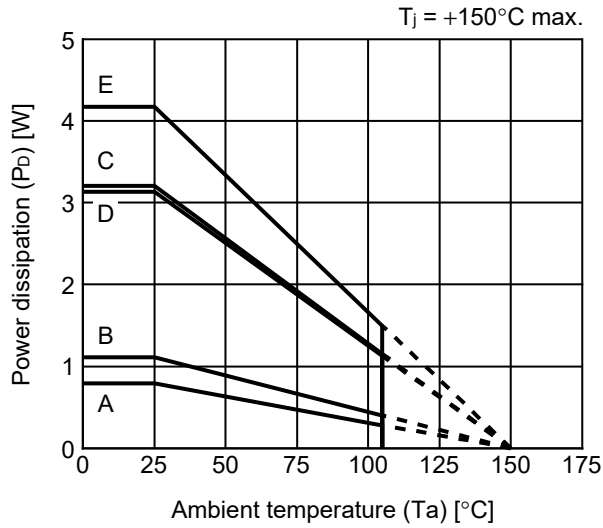


\*1. CPM: TDK Corporation CGA4J2X8R1H104K

**Figure 41**

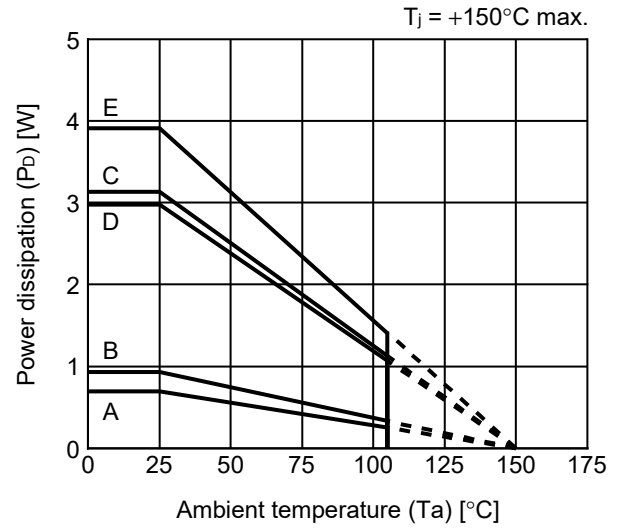
■ Power Dissipation

HTMSOP-8



| Board | Power Dissipation ( $P_D$ ) |
|-------|-----------------------------|
| A     | 0.79 W                      |
| B     | 1.11 W                      |
| C     | 3.21 W                      |
| D     | 3.13 W                      |
| E     | 4.17 W                      |

HSNT-8(2030)

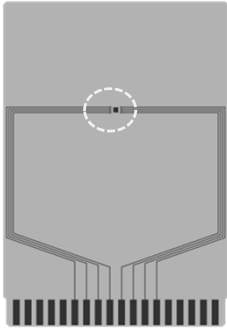


| Board | Power Dissipation ( $P_D$ ) |
|-------|-----------------------------|
| A     | 0.69 W                      |
| B     | 0.93 W                      |
| C     | 3.13 W                      |
| D     | 2.98 W                      |
| E     | 3.91 W                      |

# HTMSOP-8 Test Board

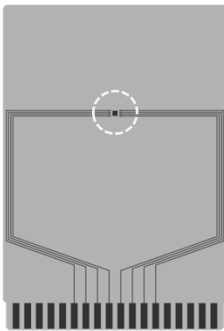
 IC Mount Area

(1) Board A



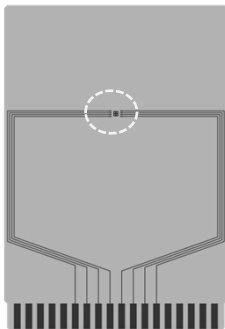
| Item                        | Specification       |   |
|-----------------------------|---------------------|---|
| Size [mm]                   | 114.3 x 76.2 x t1.6 |   |
| Material                    | FR-4                |   |
| Number of copper foil layer | 2                   |   |
| Copper foil layer [mm]      | 1                   | Land pattern and wiring for testing: t0.070 |
|                             | 2                   | -   |
|                             | 3                   | -   |
|                             | 4                   | 74.2 x 74.2 x t0.070                        |
| Thermal via                 | -                   |   |

(2) Board B



| Item                        | Specification       |   |
|-----------------------------|---------------------|---|
| Size [mm]                   | 114.3 x 76.2 x t1.6 |   |
| Material                    | FR-4                |   |
| Number of copper foil layer | 4                   |   |
| Copper foil layer [mm]      | 1                   | Land pattern and wiring for testing: t0.070 |
|                             | 2                   | 74.2 x 74.2 x t0.035                        |
|                             | 3                   | 74.2 x 74.2 x t0.035                        |
|                             | 4                   | 74.2 x 74.2 x t0.070                        |
| Thermal via                 | -                   |   |

(3) Board C



| Item                        | Specification                 |   |
|-----------------------------|-------------------------------|---|
| Size [mm]                   | 114.3 x 76.2 x t1.6           |   |
| Material                    | FR-4                          |   |
| Number of copper foil layer | 4                             |   |
| Copper foil layer [mm]      | 1                             | Land pattern and wiring for testing: t0.070 |
|                             | 2                             | 74.2 x 74.2 x t0.035                        |
|                             | 3                             | 74.2 x 74.2 x t0.035                        |
|                             | 4                             | 74.2 x 74.2 x t0.070                        |
| Thermal via                 | Number: 4<br>Diameter: 0.3 mm |   |



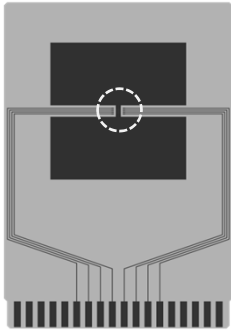
enlarged view

No. HTMSOP8-A-Board-SD-1.0

# HTMSOP-8 Test Board

 IC Mount Area

## (4) Board D

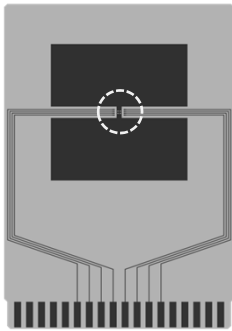


| Item                        | Specification       |  |
|-----------------------------|---------------------|--|
| Size [mm]                   | 114.3 x 76.2 x t1.6 |  |
| Material                    | FR-4                |  |
| Number of copper foil layer | 4                   |  |
| Copper foil layer [mm]      | 1                   | Pattern for heat radiation: 2000mm <sup>2</sup> t0.070 |
|                             | 2                   | 74.2 x 74.2 x t0.035                                   |
|                             | 3                   | 74.2 x 74.2 x t0.035                                   |
|                             | 4                   | 74.2 x 74.2 x t0.070                                   |
| Thermal via                 | -                   |  |



enlarged view

## (5) Board E




| Item                        | Specification                 |  |
|-----------------------------|-------------------------------|--|
| Size [mm]                   | 114.3 x 76.2 x t1.6           |  |
| Material                    | FR-4                          |  |
| Number of copper foil layer | 4                             |  |
| Copper foil layer [mm]      | 1                             | Pattern for heat radiation: 2000mm <sup>2</sup> t0.070 |
|                             | 2                             | 74.2 x 74.2 x t0.035                                   |
|                             | 3                             | 74.2 x 74.2 x t0.035                                   |
|                             | 4                             | 74.2 x 74.2 x t0.070                                   |
| Thermal via                 | Number: 4<br>Diameter: 0.3 mm |  |



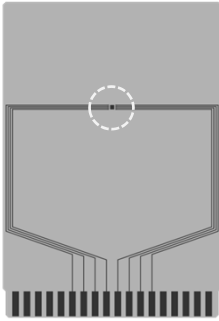
enlarged view

No. HTMSOP8-A-Board-SD-1.0

# HSNT-8(2030) Test Board

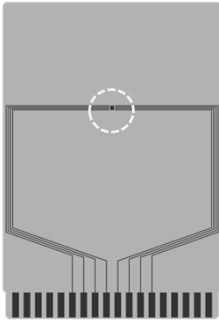
 IC Mount Area

## (1) Board A



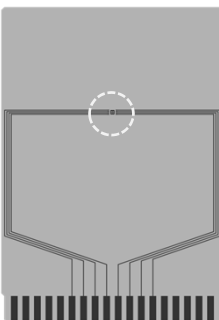
| Item                        | Specification       |   |
|-----------------------------|---------------------|---|
| Size [mm]                   | 114.3 x 76.2 x t1.6 |   |
| Material                    | FR-4                |   |
| Number of copper foil layer | 2                   |   |
| Copper foil layer [mm]      | 1                   | Land pattern and wiring for testing: t0.070 |
|                             | 2                   | -   |
|                             | 3                   | -   |
|                             | 4                   | 74.2 x 74.2 x t0.070                        |
| Thermal via                 | -                   |   |

## (2) Board B



| Item                        | Specification       |   |
|-----------------------------|---------------------|---|
| Size [mm]                   | 114.3 x 76.2 x t1.6 |   |
| Material                    | FR-4                |   |
| Number of copper foil layer | 4                   |   |
| Copper foil layer [mm]      | 1                   | Land pattern and wiring for testing: t0.070 |
|                             | 2                   | 74.2 x 74.2 x t0.035                        |
|                             | 3                   | 74.2 x 74.2 x t0.035                        |
|                             | 4                   | 74.2 x 74.2 x t0.070                        |
| Thermal via                 | -                   |   |

## (3) Board C




| Item                        | Specification                 |   |
|-----------------------------|-------------------------------|---|
| Size [mm]                   | 114.3 x 76.2 x t1.6           |   |
| Material                    | FR-4                          |   |
| Number of copper foil layer | 4                             |   |
| Copper foil layer [mm]      | 1                             | Land pattern and wiring for testing: t0.070 |
|                             | 2                             | 74.2 x 74.2 x t0.035                        |
|                             | 3                             | 74.2 x 74.2 x t0.035                        |
|                             | 4                             | 74.2 x 74.2 x t0.070                        |
| Thermal via                 | Number: 4<br>Diameter: 0.3 mm |   |



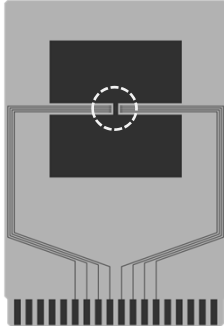
enlarged view

No. HSNT8-A-Board-SD-2.0

# HSNT-8(2030) Test Board

 IC Mount Area

## (4) Board D

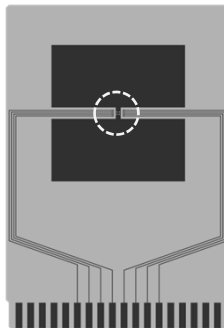


| Item                        | Specification       |  |
|-----------------------------|---------------------|--|
| Size [mm]                   | 114.3 x 76.2 x t1.6 |  |
| Material                    | FR-4                |  |
| Number of copper foil layer | 4                   |  |
| Copper foil layer [mm]      | 1                   | Pattern for heat radiation: 2000mm <sup>2</sup> t0.070 |
|                             | 2                   | 74.2 x 74.2 x t0.035                                   |
|                             | 3                   | 74.2 x 74.2 x t0.035                                   |
|                             | 4                   | 74.2 x 74.2 x t0.070                                   |
| Thermal via                 | -                   |  |



enlarged view

## (5) Board E

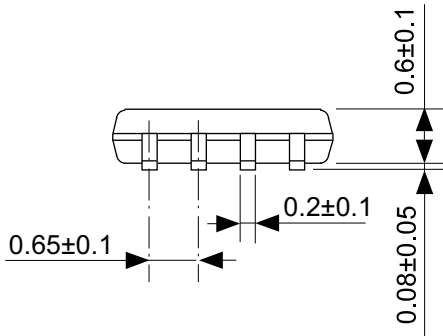
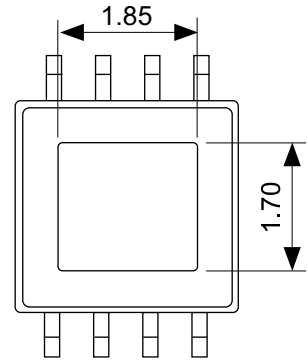
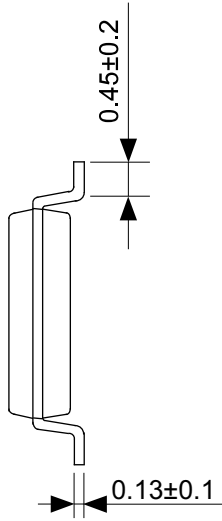
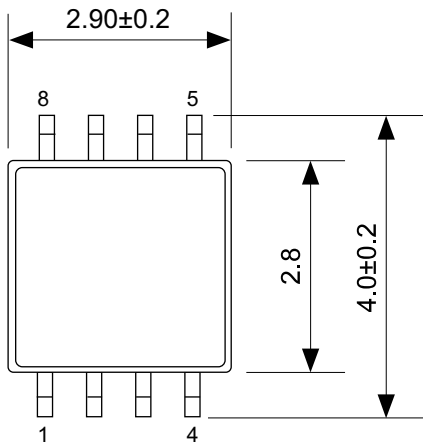


| Item                        | Specification                 |  |
|-----------------------------|-------------------------------|--|
| Size [mm]                   | 114.3 x 76.2 x t1.6           |  |
| Material                    | FR-4                          |  |
| Number of copper foil layer | 4                             |  |
| Copper foil layer [mm]      | 1                             | Pattern for heat radiation: 2000mm <sup>2</sup> t0.070 |
|                             | 2                             | 74.2 x 74.2 x t0.035                                   |
|                             | 3                             | 74.2 x 74.2 x t0.035                                   |
|                             | 4                             | 74.2 x 74.2 x t0.070                                   |
| Thermal via                 | Number: 4<br>Diameter: 0.3 mm |  |



enlarged view

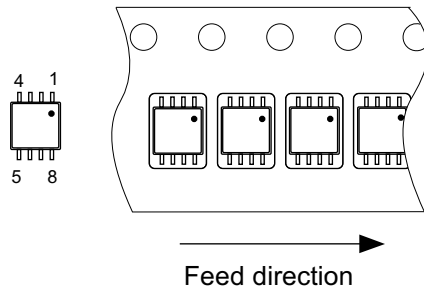
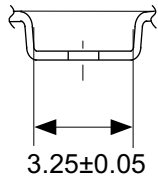
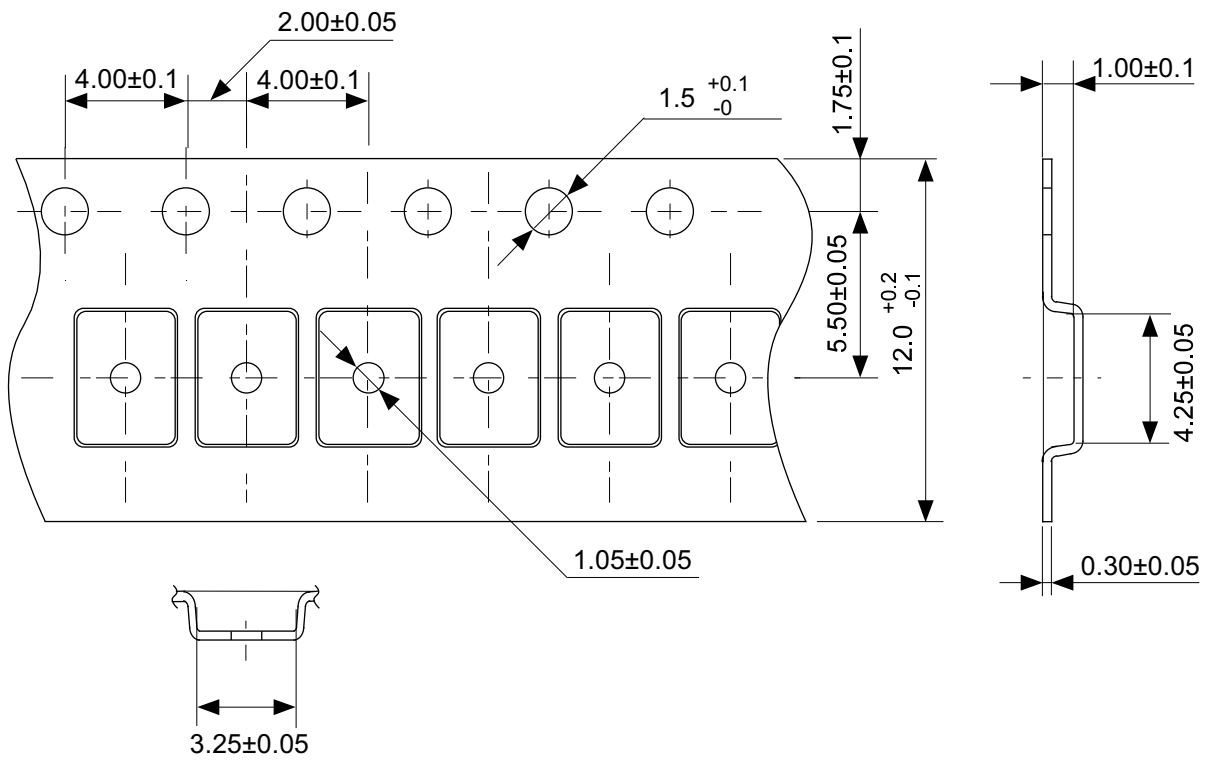
No. HSNT8-A-Board-SD-2.0



No. FP008-A-P-SD-2.0

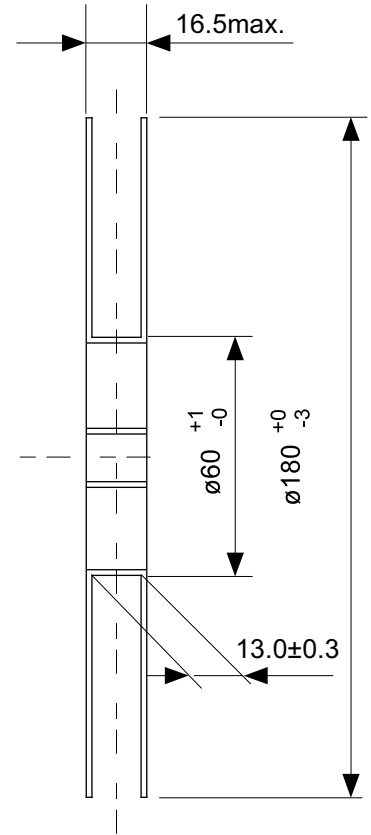
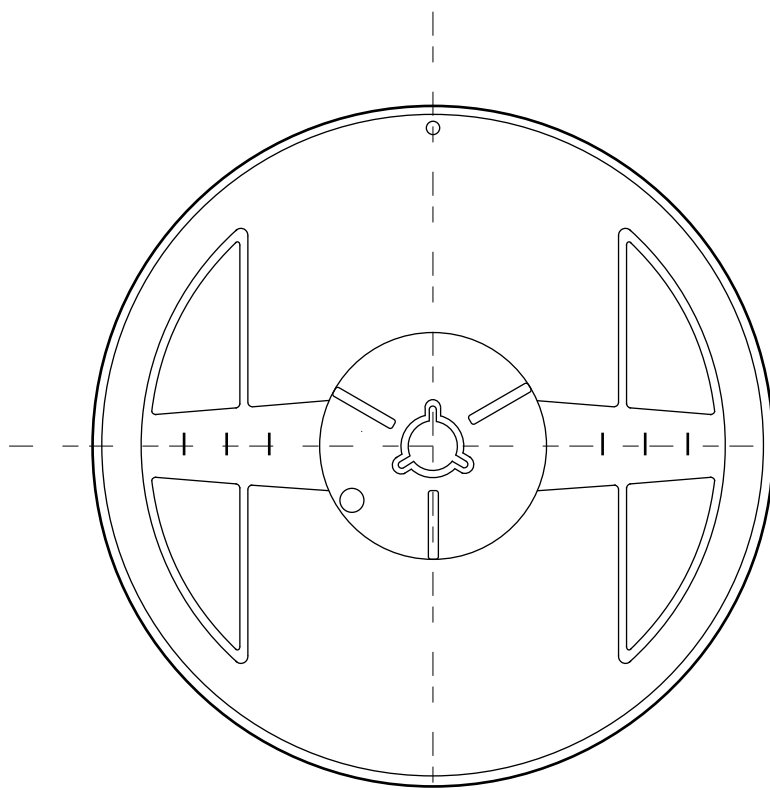
|                   |                          |
|-------------------|--------------------------|
| TITLE             | HTMSOP8-A-PKG Dimensions |
| No.               | FP008-A-P-SD-2.0         |
| ANGLE             |                          |
| UNIT              | mm                       |
| <b>ABLIC Inc.</b> |                          |



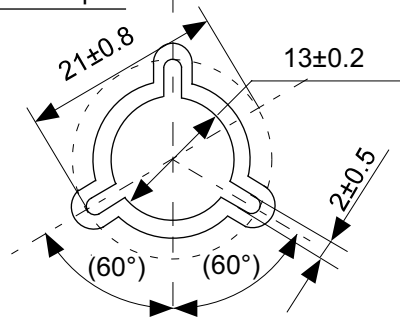


No. FP008-A-C-SD-1.0

|                   |                        |
|-------------------|------------------------|
| TITLE             | HTMSOP8-A-Carrier Tape |
| No.               | FP008-A-C-SD-1.0       |
| ANGLE             |                        |
| UNIT              | mm                     |
| <b>ABLIC Inc.</b> |                        |

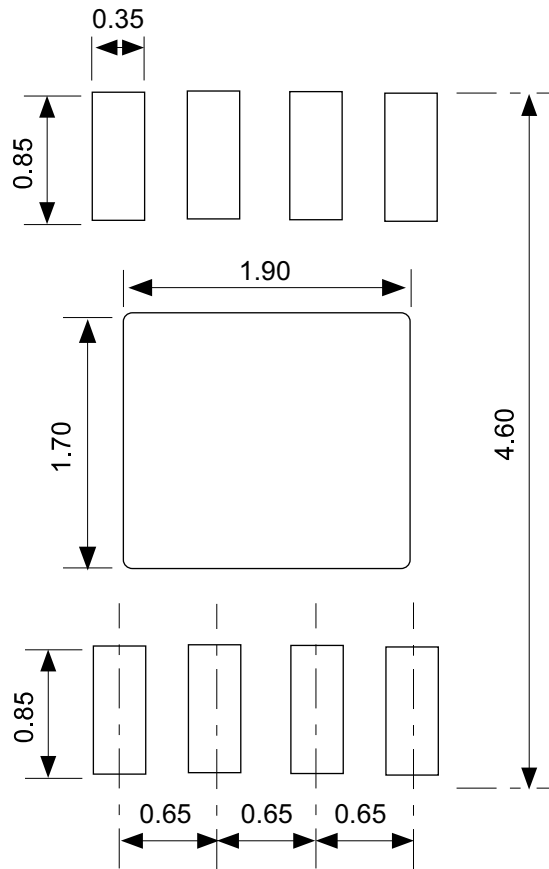


Enlarged drawing in the central part



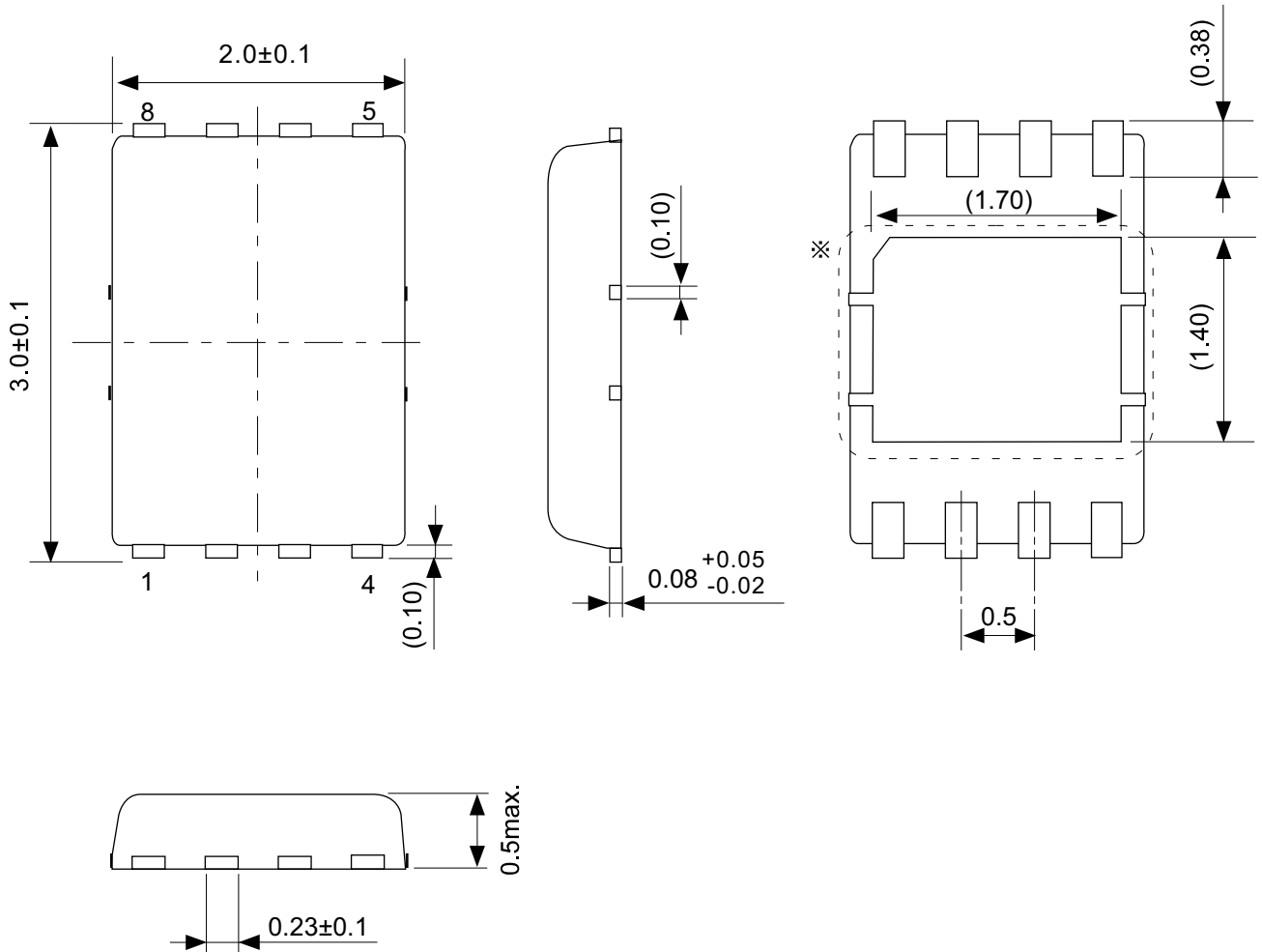
No. FP008-A-R-SD-1.0

|                   |                  |      |       |
|-------------------|------------------|------|-------|
| TITLE             | HTMSOP8-A-Reel   |      |       |
| No.               | FP008-A-R-SD-1.0 |      |       |
| ANGLE             |                  | QTY. | 4,000 |
| UNIT              | mm               |      |       |
|                   |                  |      |       |
| <b>ABLIC Inc.</b> |                  |      |       |



No. FP008-A-L-SD-2.0

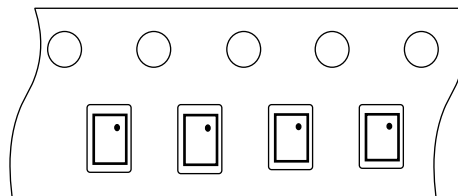
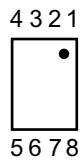
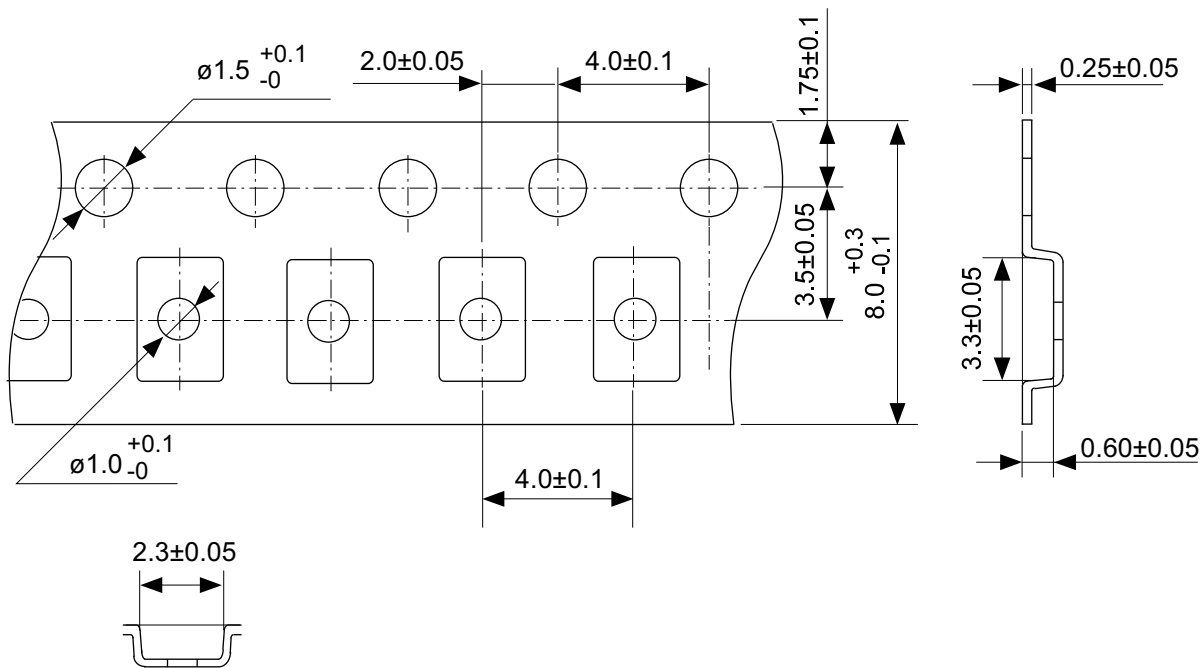
|                   |                                   |
|-------------------|-----------------------------------|
| TITLE             | HTMSOP8-A<br>-Land Recommendation |
| No.               | FP008-A-L-SD-2.0                  |
| ANGLE             |                                   |
| UNIT              | mm                                |
|                   |                                   |
| <b>ABLIC Inc.</b> |                                   |



※ The heat sink of back side has different electric potential depending on the product.  
 Confirm specifications of each product.  
 Do not use it as the function of electrode.

No. PP008-A-P-SD-2.0

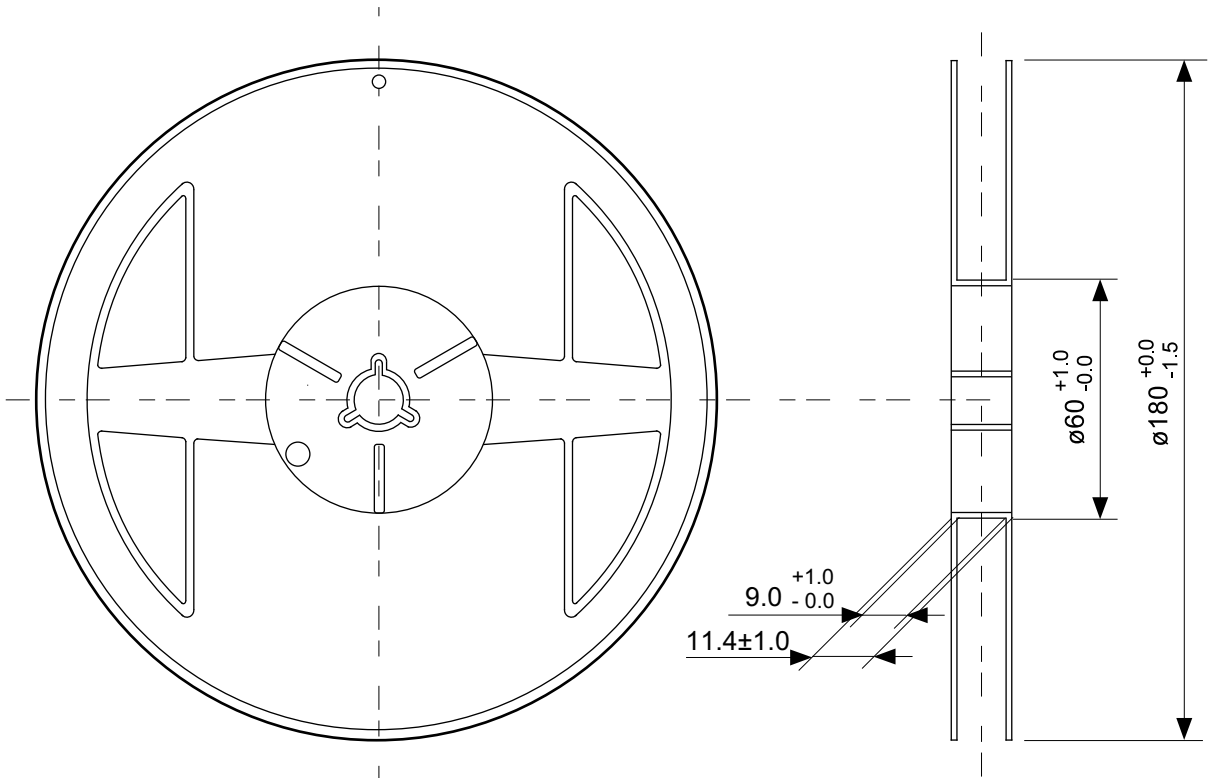
|                   |                         |
|-------------------|-------------------------|
| TITLE             | HSNT-8-A-PKG Dimensions |
| No.               | PP008-A-P-SD-2.0        |
| ANGLE             |                         |
| UNIT              | mm                      |
| <b>ABLIC Inc.</b> |                         |



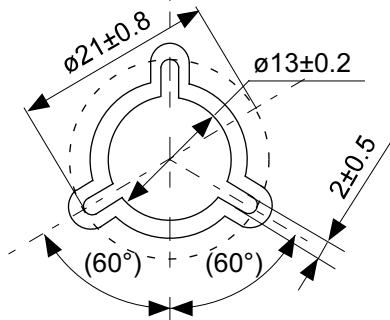
Feed direction

No. PP008-A-C-SD-1.0

|                   |                       |
|-------------------|-----------------------|
| TITLE             | HSNT-8-A-Carrier Tape |
| No.               | PP008-A-C-SD-1.0      |
| ANGLE             |                       |
| UNIT              | mm                    |
|                   |                       |
| <b>ABLIC Inc.</b> |                       |

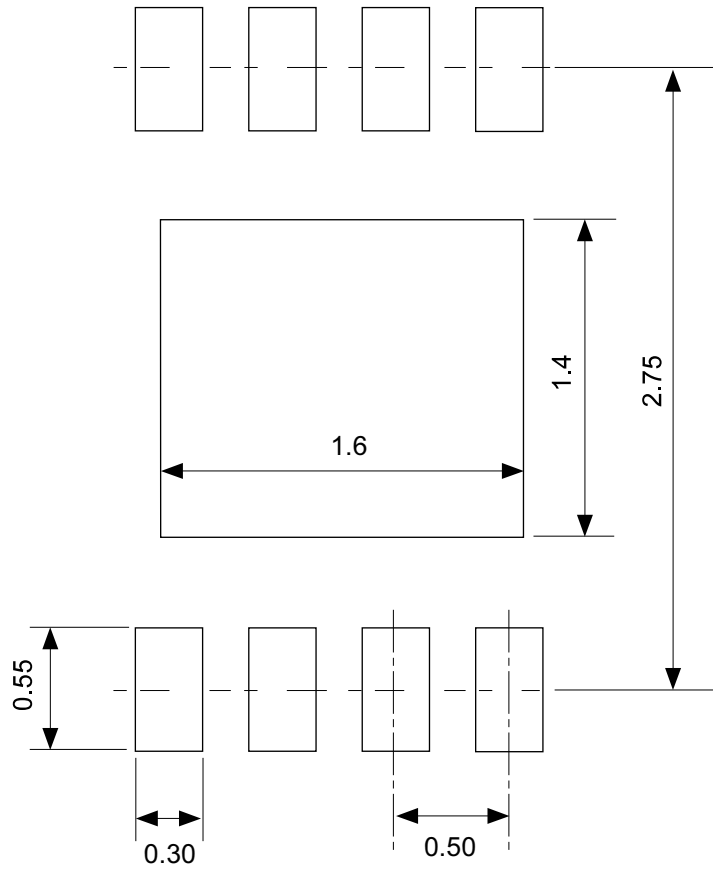


Enlarged drawing in the central part



No. PP008-A-R-SD-1.0

|                   |                  |      |       |
|-------------------|------------------|------|-------|
| TITLE             | HSNT-8-A-Reel    |      |       |
| No.               | PP008-A-R-SD-1.0 |      |       |
| ANGLE             |                  | QTY. | 5,000 |
| UNIT              | mm               |      |       |
|                   |                  |      |       |
| <b>ABLIC Inc.</b> |                  |      |       |



No. PP008-A-L-SD-1.0

|                   |                                  |
|-------------------|----------------------------------|
| TITLE             | HSNT-8-A<br>-Land Recommendation |
| No.               | PP008-A-L-SD-1.0                 |
| ANGLE             |                                  |
| UNIT              | mm                               |
|                   |                                  |
| <b>ABLIC Inc.</b> |                                  |

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2.4-2019.07