The S-19110 Series is a high-accuracy voltage detector developed using CMOS technology. The detection voltage and release voltage are fixed internally with an accuracy of ±2.0%. It operates with current consumption of 600 nA typ.

Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared in the SENSE detection product, so the output is stable even if the SENSE pin falls to 0 V.

The detection signal and release signal can be delayed by setting a capacitor externally, and the detection delay time accuracy is ±20% (CN = 3.3 nF, Ta = −40°C to +125°C), the release delay time accuracy is ±20% (CP = 3.3 nF, Ta = −40°C to +125°C).

The output form is Nch open-drain output.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.

**Features**

- Detection voltage: 5.0 V to 10.0 V (0.05 V step)
- Detection voltage accuracy: ±2.0% (Ta = −40°C to +125°C)
- Detection delay time accuracy: ±20% (CN = 3.3 nF, Ta = −40°C to +125°C)
- Release voltage: 5.25 V to 13.0 V (0.05 V step)
- Release voltage accuracy: ±2.0% (Ta = −40°C to +125°C, 5.0% ≤ VHYS ≤ 20.0%)
  ±2.5% (Ta = −40°C to +125°C, 20.0% < VHYS ≤ 30.0%)
- Release delay time accuracy: ±20% (CP = 3.3 nF, Ta = −40°C to +125°C)
- Current consumption: 600 nA typ.
- Operation voltage range: 1.8 V to 36.0 V
- Hysteresis width*1: "Available" / "unavailable" is selectable.
  5.0% to 30.0% (Ta = −40°C to +125°C)
- Output form: Nch open-drain output
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified*2

*1. When "available" is selected, the hysteresis width can be set in the range of 5.0% to 30.0%.

*2. Contact our sales office for details.

**Applications**

- Power supply monitor for microcomputer and reset for CPU
- Automotive battery voltage detection
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

**Package**

- SOT-23-6
## Block Diagrams

1. **S-19110 Series A / B type (VDD detection product)**

   - **Function** | **Status**
   - Voltage detection | VDD detection
   - Hysteresis width | Available

   *1. Parasitic diode

   ![Figure 1](image1.png)

2. **S-19110 Series C / D type (VDD detection product)**

   - **Function** | **Status**
   - Voltage detection | VDD detection
   - Hysteresis width | Unavailable

   *1. Parasitic diode

   ![Figure 2](image2.png)
3. **S-19110 Series E / F type (SENSE detection product)**

![Diagram](https://via.placeholder.com/150)

<table>
<thead>
<tr>
<th>Function</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage detection</td>
<td>SENSE detection</td>
</tr>
<tr>
<td>Hysteresis width</td>
<td>Available</td>
</tr>
</tbody>
</table>

*1. Parasitic diode

**Figure 3**

4. **S-19110 Series G / H type (SENSE detection product)**

![Diagram](https://via.placeholder.com/150)

<table>
<thead>
<tr>
<th>Function</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage detection</td>
<td>SENSE detection</td>
</tr>
<tr>
<td>Hysteresis width</td>
<td>Unavailable</td>
</tr>
</tbody>
</table>

*1. Parasitic diode

**Figure 4**
AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1. Contact our sales office for details of AEC-Q100 reliability specification.

Product Name Structure

Users can select the product type, detection voltage value and release voltage value for the S-19110 Series. Refer to "1. Product name" regarding the contents of product name, "2. Function list of product types" regarding the product types and "3. Package" regarding the package drawings.

1. Product name

S-19110 x xx A - M6T1 U 4

- Environmental code
  U : Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications
  M6T1 : SOT-23-6, Tape
- Operation temperature
  A : Ta = −40°C to +125°C
- Detection voltage value, release voltage value
  AA to ZZ
  (2-digit alphabetical option code)
- Product type
  A to H

*1. Refer to the tape drawing.
*2. Contact our sales office for details on combination of detection voltage value and release voltage value.
*3. Refer to "2. Function list of product types".
Remark 1. The difference (hysteresis width) of detection voltage \((-V_{DET}\)) and release voltage \((+V_{DET}\)) can be set in the range of 5.0% to 30.0%. The detection voltage and release voltage combination can be selected from the A area shown in Figure 5.

Example: If \(-V_{DET} = 5.0\) V, the release voltage can be set in the range of 5.25 V to 6.5 V in 50 mV step.

![Figure 5](image)

Figure 5  Detection Voltage and Release Voltage Possible Setting Area \((-V_{DET} \leq 10.0\) V)

2. The detection voltage in the S-19110 Series, which is 10.0 V max., is the release voltage in B area shown in Figure 6 in SENSE detection product with \(-V_{DET} = 10.0\) V. When setting the detection voltage exceeding 10.0 V with an external resistor, the difference of detection voltage and release voltage can be set in the range of 5.0% to 30.0%.

Refer to “2. SENSE pin” in “Operation” for details.

![Figure 6](image)

Figure 6  Detection Voltage and Release Voltage Possible Setting Area \((-V_{DET} > 10.0\) V)

2. Function list of product types

<table>
<thead>
<tr>
<th>Product Type</th>
<th>Voltage Detection</th>
<th>Output Logic</th>
<th>Hysteresis Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>VDD detection</td>
<td>Active &quot;L&quot;</td>
<td>Available</td>
</tr>
<tr>
<td>B</td>
<td>VDD detection</td>
<td>Active &quot;H&quot;</td>
<td>Available</td>
</tr>
<tr>
<td>C</td>
<td>VDD detection</td>
<td>Active &quot;L&quot;</td>
<td>Unavailable</td>
</tr>
<tr>
<td>D</td>
<td>VDD detection</td>
<td>Active &quot;H&quot;</td>
<td>Unavailable</td>
</tr>
<tr>
<td>E</td>
<td>SENSE detection</td>
<td>Active &quot;L&quot;</td>
<td>Available</td>
</tr>
<tr>
<td>F</td>
<td>SENSE detection</td>
<td>Active &quot;H&quot;</td>
<td>Available</td>
</tr>
<tr>
<td>G</td>
<td>SENSE detection</td>
<td>Active &quot;L&quot;</td>
<td>Unavailable</td>
</tr>
<tr>
<td>H</td>
<td>SENSE detection</td>
<td>Active &quot;H&quot;</td>
<td>Unavailable</td>
</tr>
</tbody>
</table>

3. Package

<table>
<thead>
<tr>
<th>Package Name</th>
<th>Dimension</th>
<th>Tape</th>
<th>Reel</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOT-23-6</td>
<td>MP006-A-P-SD</td>
<td>MP006-A-C-SD</td>
<td>MP006-A-R-SD</td>
</tr>
</tbody>
</table>
### Pin Configurations

1. **S-19110 Series A / B / C / D type (VDD detection product)**

   1. 1 SOT-23-6

   **Table 3**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Voltage input pin</td>
</tr>
<tr>
<td>2</td>
<td>NC(^1)</td>
<td>No connection</td>
</tr>
<tr>
<td>3</td>
<td>OUT</td>
<td>Voltage detection output pin</td>
</tr>
<tr>
<td>4</td>
<td>CP(^2)</td>
<td>Connection pin for release delay capacitor</td>
</tr>
<tr>
<td>5</td>
<td>VSS</td>
<td>GND pin</td>
</tr>
<tr>
<td>6</td>
<td>CN(^3)</td>
<td>Connection pin for detection delay capacitor</td>
</tr>
</tbody>
</table>

*1. The NC pin is electrically open. The NC pin can be connected to the VDD pin or the VSS pin.  
*2. Connect a capacitor between the CP pin and the VSS pin. The release delay time can be adjusted according to the capacitance. Moreover, the CP pin is available even when it is open.  
*3. Connect a capacitor between the CN pin and the VSS pin. The detection delay time can be adjusted according to the capacitance. Moreover, the CN pin is available even when it is open.

2. **S-19110 Series E / F / G / H type (SENSE detection product)**

   2. 1 SOT-23-6

   **Table 4**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Voltage input pin</td>
</tr>
<tr>
<td>2</td>
<td>SENSE</td>
<td>Detection voltage input pin</td>
</tr>
<tr>
<td>3</td>
<td>OUT</td>
<td>Voltage detection output pin</td>
</tr>
<tr>
<td>4</td>
<td>CP(^1)</td>
<td>Connection pin for release delay capacitor</td>
</tr>
<tr>
<td>5</td>
<td>VSS</td>
<td>GND pin</td>
</tr>
<tr>
<td>6</td>
<td>CN(^2)</td>
<td>Connection pin for detection delay capacitor</td>
</tr>
</tbody>
</table>

*1. Connect a capacitor between the CP pin and the VSS pin. The release delay time can be adjusted according to the capacitance. Moreover, the CP pin is available even when it is open.  
*2. Connect a capacitor between the CN pin and the VSS pin. The detection delay time can be adjusted according to the capacitance. Moreover, the CN pin is available even when it is open.
Absolute Maximum Ratings

Table 5

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Absolute Maximum Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage</td>
<td>( V_{DD} - V_{SS} )</td>
<td>( V_{SS} - 0.3 ) to ( V_{SS} + 45 )</td>
<td>V</td>
</tr>
<tr>
<td>SENSE pin input voltage</td>
<td>( V_{SENSE} )</td>
<td>( V_{SS} - 0.3 ) to ( V_{SS} + 45 )</td>
<td>V</td>
</tr>
<tr>
<td>CP pin input voltage</td>
<td>( V_{CP} )</td>
<td>( V_{SS} - 0.3 ) to ( V_{DD} + 0.3 ) to ( V_{SS} + 7.0 )</td>
<td>V</td>
</tr>
<tr>
<td>CN pin input voltage</td>
<td>( V_{CN} )</td>
<td>( V_{SS} - 0.3 ) to ( V_{DD} + 0.3 ) to ( V_{SS} + 7.0 )</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>( V_{OUT} )</td>
<td>( V_{SS} - 0.3 ) to ( V_{SS} + 45 )</td>
<td>V</td>
</tr>
<tr>
<td>Output current</td>
<td>( I_{OUT} )</td>
<td>25</td>
<td>mA</td>
</tr>
<tr>
<td>Operation ambient temperature</td>
<td>( T_{opr} )</td>
<td>( -40 ) to ( +125 )</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>( T_{stg} )</td>
<td>( -40 ) to ( +150 )</td>
<td>°C</td>
</tr>
</tbody>
</table>

Caution: The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

Thermal Resistance Value

Table 6

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction-to-ambient thermal resistance*1</td>
<td>( \theta_{JA} )</td>
<td>SOT-23-6</td>
<td>Board A</td>
<td>–</td>
<td>159</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Board B</td>
<td>–</td>
<td>124</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Board C</td>
<td>–</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Board D</td>
<td>–</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Board E</td>
<td>–</td>
<td>–</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark: Refer to “Power Dissipation” and “Test Board” for details.
Electrical Characteristics

1. VDD detection product

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Detection voltage</strong></td>
<td>(-V_{\text{DET}})</td>
<td>(5.0 \text{ V} \leq V_{\text{DET(S)}} \leq 10.0 \text{ V})</td>
<td>(-V_{\text{DET(S)}}/0.980)</td>
<td>(-V_{\text{DET(S)}}/1.020)</td>
<td></td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td><strong>Release voltage</strong></td>
<td>(+V_{\text{DET}})</td>
<td>(A / B \text{ type} ) (5.0% \leq V_{\text{HYS}} \leq 20.0%)</td>
<td>(+V_{\text{DET(S)}}/0.980)</td>
<td>(+V_{\text{DET(S)}}/1.020)</td>
<td></td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>(A / B \text{ type} ) (20.0% \leq V_{\text{HYS}} \leq 30.0%)</td>
<td>(+V_{\text{DET(S)}}/0.975)</td>
<td>(+V_{\text{DET(S)}}/1.025)</td>
<td></td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(C / D \text{ type} ) (V_{\text{HYS}} = 0%)</td>
<td>(-V_{\text{DET(S)}}/0.980)</td>
<td>(-V_{\text{DET(S)}}/1.020)</td>
<td></td>
<td>V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td><strong>Current consumption</strong></td>
<td>(I_{\text{SS}})</td>
<td>(A / B / C / D \text{ type} ) (V_{\text{DD}} = -V_{\text{DET}} - 0.1 \text{ V} \leq V_{\text{DD}} \leq 10.0 \text{ V})</td>
<td>(-0.60)</td>
<td>(-1.60)</td>
<td></td>
<td>μA</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>(A / B \text{ type} ) (V_{\text{DD}} = +V_{\text{DET}} + 0.1 \text{ V} \leq V_{\text{DD}} \leq 13.0 \text{ V})</td>
<td>(-0.60)</td>
<td>(-1.60)</td>
<td></td>
<td>μA</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td><strong>Operation voltage</strong></td>
<td>(V_{\text{DD}})</td>
<td>–</td>
<td>(1.8)</td>
<td>–</td>
<td>(36.0)</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td><strong>Output current</strong></td>
<td>(I_{\text{OUT}})</td>
<td>Output transistor Nch, (V_{\text{DS}} = 0.05 \text{ V})</td>
<td>(V_{\text{DD}} = 4.5 \text{ V}, \text{ active } &quot;L&quot;)</td>
<td>(0.45)</td>
<td>–</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{\text{DD}} = 14.0 \text{ V}, \text{ active } &quot;H&quot;)</td>
<td>(0.45)</td>
<td>–</td>
<td>–</td>
<td>mA</td>
<td>3</td>
</tr>
<tr>
<td><strong>Leakage current</strong></td>
<td>(I_{\text{LEAK}})</td>
<td>Output transistor Nch, (V_{\text{DS}} = 0.05 \text{ V})</td>
<td>(V_{\text{DD}} = 30.0 \text{ V}, V_{\text{OUT}} = 30.0 \text{ V}, \text{ active } &quot;L&quot;)</td>
<td>–</td>
<td>–</td>
<td>2.0</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{\text{DD}} = 4.5 \text{ V}, V_{\text{OUT}} = 30.0 \text{ V}, \text{ active } &quot;H&quot;)</td>
<td>–</td>
<td>–</td>
<td>2.0</td>
<td>μA</td>
<td>3</td>
</tr>
<tr>
<td><strong>Detection delay time</strong></td>
<td>(t_{\text{RESET}})</td>
<td>(C_{\text{N}} = 3.3 \text{ nF})</td>
<td>(8.0)</td>
<td>(10.0)</td>
<td>(12.0)</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td><strong>Release delay time</strong></td>
<td>(t_{\text{DELAY}})</td>
<td>(A / B \text{ type} ) (C_{\text{P}} = 3.3 \text{ nF})</td>
<td>(8.0)</td>
<td>(10.0)</td>
<td>(12.0)</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(C / D \text{ type} ) (C_{\text{P}} = 3.3 \text{ nF})</td>
<td>(8.0)</td>
<td>(10.0)</td>
<td>(12.0)</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td><strong>CP pin discharge resistance</strong></td>
<td>(R_{\text{CP}})</td>
<td>(V_{\text{DD}} = 14.0 \text{ V}, V_{\text{CP}} = 0.5 \text{ V})</td>
<td>(0.30)</td>
<td>–</td>
<td>2.60</td>
<td>kΩ</td>
<td>–</td>
</tr>
<tr>
<td><strong>CN pin discharge resistance</strong></td>
<td>(R_{\text{CN}})</td>
<td>(V_{\text{DD}} = 4.5 \text{ V}, V_{\text{CN}} = 0.5 \text{ V})</td>
<td>(0.63)</td>
<td>–</td>
<td>2.60</td>
<td>kΩ</td>
<td>–</td>
</tr>
</tbody>
</table>

*1. \(-V_{\text{DET}}\): Actual detection voltage value, \(-V_{\text{DET(S)}}\): Set detection voltage value
*2. \(+V_{\text{DET}}\): Actual release voltage value, \(+V_{\text{DET(S)}}\): Set release voltage value
*3. Although the hysteresis width can be set in the range of 5.0% to 30.0%, the release voltage accuracy differs when the setting range exceeds 20.0%.
*4. The hysteresis width is "unavailable", so release voltage = detection voltage.
*5. \(V_{\text{DS}}\): Drain-to-source voltage of the output transistor
*6. The time period from when the pulse voltage of \(-V_{\text{DET(S)}} + 1.0 \text{ V} \rightarrow -V_{\text{DET(S)}} - 1.0 \text{ V}\) is applied to the VDD pin to when \(V_{\text{OUT}}\) reaches \(V_{\text{DD}} / 2\), after the power supply voltage (\(V_{\text{DD}}\)) reaches the release voltage once.
*7. The time period from when the pulse voltage of \(+V_{\text{DET(S)}} - 1.0 \text{ V} \rightarrow +V_{\text{DET(S)}} + 1.0 \text{ V}\) is applied to the VDD pin to when \(V_{\text{OUT}}\) reaches \(V_{\text{DD}} / 2\).
*8. The time period from when the pulse voltage of \(-V_{\text{DET(S)}} - 1.0 \text{ V} \rightarrow -V_{\text{DET(S)}} + 1.0 \text{ V}\) is applied to the VDD pin to when \(V_{\text{OUT}}\) reaches \(V_{\text{DD}} / 2\).
### 2. SENSE detection product

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detection voltage&lt;sup&gt;1&lt;/sup&gt;</td>
<td>−VDET</td>
<td>VDD = 16.0 V, 5.0 V ≤ −VDET(S) ≤ 10.0 V</td>
<td>−VDET(S) × 0.980</td>
<td>−VDET(S)</td>
<td>−VDET(S) × 1.020</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Release voltage&lt;sup&gt;2&lt;/sup&gt;</td>
<td>+VDET</td>
<td>VDD = 16.0 V</td>
<td>+VDET(S) × 0.980</td>
<td>+VDET(S)</td>
<td>+VDET(S) × 1.020</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Current consumption&lt;sup&gt;3&lt;/sup&gt;</td>
<td>I&lt;sub&gt;SS&lt;/sub&gt;</td>
<td>E / F / G / H type&lt;br&gt;VDD = 16.0 V, VSENSE = −VDET − 0.1 V, 5.0 V ≤ −VDET ≤ 10.0 V</td>
<td>−</td>
<td>0.55</td>
<td>1.55</td>
<td>μA</td>
<td>2</td>
</tr>
<tr>
<td>Operation voltage</td>
<td>VDD</td>
<td>−</td>
<td>3.0</td>
<td>−</td>
<td>36.0</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Output current</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Output transistor Nch&lt;br&gt;V&lt;sub&gt;DS&lt;/sub&gt; = 0.05 V</td>
<td>VDD = 5.0 V, VSENSE = 4.5 V, active &quot;L&quot;</td>
<td>0.45</td>
<td>−</td>
<td>−</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDD = 5.0 V, VSENSE = 14.0 V, active &quot;H&quot;</td>
<td>0.45</td>
<td>−</td>
<td>−</td>
<td>mA</td>
<td>3</td>
</tr>
<tr>
<td>Leakage current</td>
<td>I&lt;sub&gt;LEAK&lt;/sub&gt;</td>
<td>Output transistor Nch&lt;br&gt;VDD = 30.0 V, VSENSE = 30.0 V, active &quot;L&quot;</td>
<td>−</td>
<td>−</td>
<td>2.0</td>
<td>μA</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDD = 30.0 V, VSENSE = 4.5 V, active &quot;H&quot;</td>
<td>−</td>
<td>−</td>
<td>2.0</td>
<td>μA</td>
<td>3</td>
</tr>
<tr>
<td>Detection delay time&lt;sup&gt;7&lt;/sup&gt;</td>
<td>t&lt;sub&gt;RESET&lt;/sub&gt;</td>
<td>CN = 3.3 nF</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td>Release delay time&lt;sup&gt;8&lt;/sup&gt;</td>
<td>t&lt;sub&gt;DELAY&lt;/sub&gt;</td>
<td>E / F type&lt;br&gt;C&lt;sub&gt;P&lt;/sub&gt; = 3.3 nF</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>G / H type&lt;br&gt;C&lt;sub&gt;P&lt;/sub&gt; = 3.3 nF</td>
<td>8.0</td>
<td>10.0</td>
<td>12.0</td>
<td>ms</td>
<td>4</td>
</tr>
<tr>
<td>SENSE pin resistance</td>
<td>R&lt;sub&gt;SENSE&lt;/sub&gt;</td>
<td>−</td>
<td>26.0</td>
<td>−</td>
<td>400</td>
<td>MΩ</td>
<td>2</td>
</tr>
<tr>
<td>CP pin discharge ON resistance</td>
<td>R&lt;sub&gt;CP&lt;/sub&gt;</td>
<td>VDD = 4.5 V, VSENSE = 14.0 V, V&lt;sub&gt;CP&lt;/sub&gt; = 0.5 V</td>
<td>0.30</td>
<td>−</td>
<td>2.60</td>
<td>kΩ</td>
<td>−</td>
</tr>
<tr>
<td>CN pin discharge ON resistance</td>
<td>R&lt;sub&gt;CN&lt;/sub&gt;</td>
<td>VDD = 4.5 V, VSENSE = 4.5 V, V&lt;sub&gt;CN&lt;/sub&gt; = 0.5 V</td>
<td>0.63</td>
<td>−</td>
<td>2.60</td>
<td>kΩ</td>
<td>−</td>
</tr>
</tbody>
</table>

<sup>1</sup> −VDET: Actual detection voltage value, −VDET(S): Set detection voltage value

<sup>2</sup> +VDET: Actual release voltage value, +VDET(S): Set release voltage value

<sup>3</sup> Although the hysteresis width can be set in the range of 5.0% to 30.0%, the release voltage accuracy differs when the setting range exceeds 20.0%.

<sup>4</sup> The hysteresis width is "unavailable", so release voltage = detection voltage.

<sup>5</sup> The current flowing through the SENSE pin resistance is not included.

<sup>6</sup> V<sub>DS</sub>: Drain-to-source voltage of the output transistor

<sup>7</sup> The time period from when the pulse voltage of −VDET(S) + 1.0 V → −VDET(S) − 1.0 V is applied to the SENSE pin to when VOUT reaches VDD / 2, after voltage of 16.0 V is applied to the VDD pin and the SENSE pin input voltage (VSENSE) reaches the release voltage once.

<sup>8</sup> The time period from when voltage of 16.0 V is applied to the VDD pin and the pulse voltage of +VDET(S) − 1.0 V → +VDET(S) + 1.0 V is applied to the SENSE pin to when VOUT reaches VDD / 2.

<sup>9</sup> The time period from when voltage of 16.0 V is applied to the VDD pin and the pulse voltage of −VDET(S) − 1.0 V → −VDET(S) + 1.0 V is applied to the SENSE pin to when VOUT reaches VDD / 2.
### Test Circuits

**Figure 9** Test Circuit 1 (VDD Detection Product)

**Figure 10** Test Circuit 1 (SENSE Detection Product)

**Figure 11** Test Circuit 2 (VDD Detection Product)

**Figure 12** Test Circuit 2 (SENSE Detection Product)

**Figure 13** Test Circuit 3 (VDD Detection Product)

**Figure 14** Test Circuit 3 (SENSE Detection Product)

**Figure 15** Test Circuit 4 (VDD Detection Product)

**Figure 16** Test Circuit 4 (SENSE Detection Product)
### Standard Circuits

1. **VDD detection product**

![Figure 17](image1.png)

*1. The delay capacitor (Cp) should be connected directly to the CP pin and the VSS pin.
*2. The delay capacitor (Cn) should be connected directly to the CN pin and the VSS pin.

Figure 17

2. **SENSE detection product**

![Figure 18](image2.png)

*1. The delay capacitor (Cp) should be connected directly to the CP pin and the VSS pin.
*2. The delay capacitor (Cn) should be connected directly to the CN pin and the VSS pin.

Figure 18

**Caution** The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.
Explanation of Terms

1. Detection voltage (−V_{DET})

The detection voltage is a voltage at which the output in Figure 23 or Figure 24 turns to "H" for active "H", and "L" for active "L" (VDD detection product: V_{DD}, SENSE detection product: V_{SENSE}). The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum (−V_{DET \ min.}) and the maximum (−V_{DET \ max.}) is called the detection voltage range (Refer to Figure 19, Figure 21).

Example: In −V_{DET} = 5.0 V product, the detection voltage is either one in the range of 4.900 V ≤ −V_{DET} ≤ 5.100 V. This means that some −V_{DET} = 5.0 V product have −V_{DET} = 4.900 V and some have −V_{DET} = 5.100 V.

2. Release voltage (+V_{DET})

The release voltage is a voltage at which the output in Figure 23 or Figure 24 turns to "L" for active "H", and "H" for active "L" (VDD detection product: V_{DD}, SENSE detection product: V_{SENSE}). The difference of detection voltage and release voltage can be set in the range of 5.0% to 30.0% (Refer to "Figure 5 Detection Voltage and Release Voltage Possible Setting Area (−V_{DET} ≤ 10.0 V)").

The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum (+V_{DET \ min.}) and the maximum (+V_{DET \ max.}) is called the release voltage range (Refer to Figure 20, Figure 22).

Release voltage accuracy is ±2.0% when hysteresis width = 5.0% to 20.0%, and ±2.5% when hysteresis width = 20.0% to 30.0%.

In the S-19110 Series C / D / G / H type, the release voltage (+V_{DET}) is the same value as the actual detection voltage (−V_{DET}) of a product.

Example 1: For −V_{DET} = 6.0 V, +V_{DET} = 6.6 V product (hysteresis width = 10.0%), the release voltage is either one in the range of 6.468 V ≤ +V_{DET} ≤ 6.732 V.

This means that some −V_{DET} = 6.0 V, +V_{DET} = 6.6 V product have +V_{DET} = 6.468 V and some have +V_{DET} = 6.732 V.

Example 2: For −V_{DET} = 10.0 V, +V_{DET} = 13.0 V product (hysteresis width = 30.0%), the release voltage is either one in the range of 12.675 V ≤ +V_{DET} ≤ 13.325 V.

This means that some −V_{DET} = 10.0 V, +V_{DET} = 13.0 V product have +V_{DET} = 12.675 V and some have +V_{DET} = 13.325 V.
3. Hysteresis width ($V_{HYS}$)

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B – the voltage at point A = $V_{HYS}$ in Figure 26, Figure 28, Figure 34 and Figure 36). Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

4. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector.
Operation

1. Basic operation

1.1 S-19110 Series A type

(1) When the power supply voltage (V_{DD}) is the release voltage (+V_{DET}) or higher, the Nch transistor is turned off to output V_{DD} ("H") when the output is pulled up.

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is \( \frac{(R_A + R_C) \cdot V_{DD}}{R_A + R_B + R_C} \).

(2) Even if V_{DD} decreases to +V_{DET} or lower, V_{DD} is output when V_{DD} is higher than the detection voltage (–V_{DET}). When V_{DD} decreases to –V_{DET} or lower (point A in Figure 26), the Nch transistor is turned on. And then V_{SS} ("L") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}).

At this time, N1 is turned on, and the input voltage to the comparator is \( \frac{R_B \cdot V_{DD}}{R_A + R_B} \).

(3) The output is unstable when V_{DD} decreases to the IC’s minimum operation voltage or lower. V_{DD} is output when the output is pulled up.

(4) V_{SS} is output by increasing V_{DD} to the minimum operation voltage or higher. Even if V_{DD} exceeds +V_{DET}, V_{SS} is output when V_{DD} is lower than –V_{DET}.

(5) When V_{DD} increases to +V_{DET} or higher (point B in Figure 26), the Nch transistor is turned off. And then V_{DD} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}) when the output is pulled up.

Remark When V_{DD} is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.
1.2 S-19110 Series B type

(1) When the power supply voltage ($V_{DD}$) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned on to output $V_{SS}$ ("L").

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is
\[
\frac{(R_B + R_C)}{R_A + R_B + R_C} \cdot V_{DD}.
\]

(2) Even if $V_{DD}$ decreases to $+V_{DET}$ or lower, $V_{SS}$ is output when $V_{DD}$ is higher than the detection voltage ($-V_{DET}$). When $V_{DD}$ decreases to $-V_{DET}$ or lower (point A in Figure 28), the Nch transistor is turned off. And then $V_{DD}$ ("H") is output from the OUT pin after the elapse of the detection delay time ($t_{RESET}$).

At this time, N1 is turned on, and the input voltage to the comparator is \[
\frac{R_B \cdot V_{DD}}{R_A + R_B}.
\]

(3) The output is unstable when $V_{DD}$ decreases to the IC’s minimum operation voltage or lower. $V_{DD}$ is output when the output is pulled up.

(4) $V_{DD}$ is output by increasing $V_{DD}$ to the minimum operation voltage or higher. Even if $V_{DD}$ exceeds $-V_{DET}$, $V_{DD}$ is output when $V_{DD}$ is lower than $+V_{DET}$.

(5) When $V_{DD}$ increases to $+V_{DET}$ or higher (point B in Figure 28), the Nch transistor is turned on. And then $V_{SS}$ is output from the OUT pin after the elapse of the release delay time ($t_{DELAY}$).

*1. Parasitic diode

Figure 27 Operation of S-19110 Series B Type

Remark When $V_{DD}$ is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

Figure 28 Timing Chart of S-19110 Series B Type
1. 3 S-19110 Series C type

(1) When the power supply voltage (VDD) is the release voltage (+VDET) or higher, the Nch transistor is turned off to output VDD ("H") when the output is pulled up. At this time, the input voltage to the comparator is:

\[ \frac{(R_B + R_C) \cdot VDD}{R_A + R_B + R_C} \]

(2) When VDD decreases to the detection voltage (−VDET) or lower (point A in Figure 30), the Nch transistor is turned on. And then VSS ("L") is output from the OUT pin after the elapse of the detection delay time (tRESET).

(3) The output is unstable when VDD decreases to the IC's minimum operation voltage or lower. VDD is output when the output is pulled up.

(4) VSS is output by increasing VDD to the minimum operation voltage or higher.

(5) When VDD increases to +VDET or higher (point B in Figure 30), the Nch transistor is turned off. And then VDD is output from the OUT pin after the elapse of the release delay time (tDELAY) when the output is pulled up.

Figure 29 Operation of S-19110 Series C Type

Remark 1. When VDD is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

2. The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 30 Timing Chart of S-19110 Series C Type
1.4 S-19110 Series D type

(1) When the power supply voltage (V_{DD}) is the release voltage (+V_{DET}) or higher, the Nch transistor is turned on to output V_{SS} ("L"). At this time, the input voltage to the comparator is \((R_B + R_C) \cdot V_{DD} \over R_A + R_B + R_C\).

(2) When V_{DD} decreases to the detection voltage (−V_{DET}) or lower (point A in Figure 32), the Nch transistor is turned off. And then V_{DD} ("H") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}) when the output is pulled up.

(3) The output is unstable when V_{DD} decreases to the IC's minimum operation voltage or lower. V_{DD} is output when the output is pulled up.

(4) V_{DD} is output by increasing V_{DD} to the minimum operation voltage or higher.

(5) When V_{DD} increases to +V_{DET} or higher (point B in Figure 32), the Nch transistor is turned on. And then V_{SS} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}).

\[\begin{align*}
V_{DD} & \quad \text{VDD} \\
V_{SS} & \quad \text{VSS} \\
R & \quad 100 \text{ k\Omega} \\
\text{OUT} & \\
\end{align*}\]

*1. Parasitic diode

Figure 31 Operation of S-19110 Series D Type

Detection voltage (−V_{DET})

Release voltage (+V_{DET})

Minimum operation voltage

Output from OUT pin

Remark 1. When V_{DD} is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

2. The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.
1. 5 S-19110 Series E type

(1) When the power supply voltage (VDD) is the minimum operation voltage or higher, and the SENSE pin voltage (VSENSE) is the release voltage (+VDET) or higher, the Nch transistor is turned off to output VDD ("H") when the output is pulled up.

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is \( \frac{(R_b + R_c) \cdot V_{SENSE}}{R_A + R_b + R_c} \).

(2) Even if VSENSE decreases to +VDET or lower, VDD is output when VSENSE is higher than the detection voltage (−VDET).

When VSENSE decreases to −VDET or lower (point A in Figure 34), the Nch transistor is turned on. And then VSS ("L") is output from the OUT pin after the elapse of the detection delay time (tRESET).

At this time, N1 is turned on, and the input voltage to the comparator is \( \frac{R_b \cdot V_{SENSE}}{R_A + R_b} \).

(3) Even if VSENSE further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when VDD is minimum operation voltage or higher.

(4) Even if VSENSE exceeds −VDET, VSS is output when VSENSE is lower than +VDET.

(5) When VSENSE increases to +VDET or higher (point B in Figure 34), the Nch transistor is turned off. And then VDD is output from the OUT pin after the elapse of the release delay time (tDELAY) when the output is pulled up.

Figure 33 Operation of S-19110 Series E Type

Figure 34 Timing Chart of S-19110 Series E Type
1. 6 S-19110 Series F type

(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage (+V_{DET}) or higher, the Nch transistor is turned on to output V_{SS} ("L").

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is \( \frac{(R_B + R_C) \cdot V_{SENSE}}{R_A + R_B + R_C} \).

(2) Even if V_{SENSE} decreases to +V_{DET} or lower, V_{SS} is output when V_{SENSE} is higher than the detection voltage (−V_{DET}).

When V_{SENSE} decreases to −V_{DET} or lower (point A in Figure 36), the Nch transistor is turned off. And then V_{DD} ("H") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}) when the output is pulled up.

At this time, N1 is turned on, and the input voltage to the comparator is \( \frac{R_B \cdot V_{SENSE}}{R_A + R_B} \).

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or higher.

(4) Even if V_{SENSE} exceeds −V_{DET}, V_{DD} is output when V_{SENSE} is lower than +V_{DET}.

(5) When V_{SENSE} increases to +V_{DET} or higher (point B in Figure 36), the Nch transistor is turned on. And then V_{SS} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}).

![Figure 35 Operation of S-19110 Series F Type](image)

![Figure 36 Timing Chart of S-19110 Series F Type](image)

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1.7 S-19110 Series G type

(1) When the power supply voltage (V_DD) is the minimum operation voltage or higher, and the SENSE pin voltage (V_SENSE) is the release voltage (+V_DET) or higher, the Nch transistor is turned off to output V_DD ("H") when the output is pulled up.

At this time, the input voltage to the comparator is \( \frac{(R_B + R_C) \cdot V_{SENSE}}{R_A + R_B + R_C} \).

(2) When V_SENSE decreases to the detection voltage (−V_DET) or lower (point A in Figure 38), the Nch transistor is turned on. And then V_SS ("L") is output from the OUT pin after the elapse of the detection delay time (t_RESET).

(3) Even if V_SENSE further decreases to the IC’s minimum operation voltage or lower, the output from the OUT pin is stable when V_DD is minimum operation voltage or higher.

(4) Even if V_SENSE increases, V_SS is output when V_SENSE is lower than +V_DET.

(5) When V_SENSE increases to +V_DET or higher (point B in Figure 38), the Nch transistor is turned off. And then V_DD is output from the OUT pin after the elapse of the release delay time (t_DELAY) when the output is pulled up.

![Figure 37 Operation of S-19110 Series G Type](image)

*1. Parasitic diode

**Remark** The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

![Figure 38 Timing Chart of S-19110 Series G Type](image)
1.8 S-19110 Series H type

(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage (+VDET) or higher, the Nch transistor is turned on to output VSS ("L"). At this time, the input voltage to the comparator is \( \frac{(R_B + R_C) \cdot V_{SENSE}}{R_A + R_B + R_C} \).

(2) When V_{SENSE} decreases to the detection voltage (−VDET) or lower (point A in Figure 40), the Nch transistor is turned off. And then VDD ("H") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}) when the output is pulled up.

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when VDD is minimum operation voltage or higher.

(4) Even if V_{SENSE} increases, VDD is output when V_{SENSE} is lower than +VDET.

(5) When V_{SENSE} increases to +VDET or higher (point B in Figure 40), the Nch transistor is turned on. And then VSS is output from the OUT pin after the elapse of the release delay time (t_{DELAY}).

![Figure 39 Operation of S-19110 Series H Type](image)

Remark
The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

![Figure 40 Timing Chart of S-19110 Series H Type](image)
2. SENSE pin

2.1 Error when detection voltage is set externally

The detection voltage for the S-19110 Series is 10.0 V max., however, in the SENSE detection product with $-V_{DET} = 10.0 \, V$, the detection voltage can be set externally by connecting a node that was resistance-divided by the resistor ($R_A$) and the resistor ($R_B$) to the SENSE pin as shown in Figure 41.

For conventional products without the SENSE pin, external resistor cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if external resistor is large, problems such as oscillation or larger error in the hysteresis width may occur.

In the S-19110 Series, $R_A$ and $R_B$ in Figure 41 are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance ($R_{SENSE}$) that will occur.

Although $R_{SENSE}$ in the S-19110 Series is large (26 MΩ min.) to make the error small, $R_A$ and $R_B$ should be selected such that the error is within the allowable limits.

2.2 Selection of $R_A$ and $R_B$

In Figure 41, the relation between the external setting detection voltage ($V_{DX}$) and the actual detection voltage ($-V_{DET}$) is ideally calculated by the equation below.

$$V_{DX} = -V_{DET} \times \left( 1 + \frac{R_A}{R_B} \right) \quad \cdots \, (1)$$

However, in reality there is an error in the current flowing through $R_{SENSE}$.

When considering this error, the relation between $V_{DX}$ and $-V_{DET}$ is calculated as follows.

$$V_{DX} = -V_{DET} \times \left( 1 + \frac{R_A}{R_B || R_{SENSE}} \right)$$

By using equations (1) and (2), the error is calculated as $-V_{DET} \times \frac{R_A}{R_{SENSE}}$.

The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100 \, [\%] = \frac{R_A || R_B}{R_{SENSE}} \times 100 \, [\%] \quad \cdots \, (3)$$

As seen in equation (3), the smaller the resistance values of $R_A$ and $R_B$ compared to $R_{SENSE}$, the smaller the error rate becomes.
Also, the relation between the external setting hysteresis width ($V_{HX}$) and the hysteresis width ($V_{HYS}$) is calculated by equation below. Error due to $R_{SENSE}$ also occurs to the relation in a similar way to the detection voltage.

$$V_{HX} = V_{HYS} \times \left(1 + \frac{R_A}{R_B}\right)$$ \quad \cdots (4)

![Detection Voltage External Setting Circuit](image)

**Caution**
1. When externally setting the detection voltage, perform the operation with $-V_{DET} = 10.0 \, \text{V}$ product. Contact our sales office for details.
2. If the current flowing through $R_B$ is set to $1 \, \mu\text{A}$ or less, the error may become larger.
3. If the parasitic resistance and parasitic inductance between $V_{DX}$ – point A and point A – VDD pin are larger, oscillation may occur. Perform thorough evaluation using the actual application.
4. If $R_A$ and $R_B$ are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.
3. Delay circuit

The delay circuit has a function that adjusts the detection delay time (t\textsubscript{RESET}) from when the power supply voltage (V\textsubscript{DD}) or SENSE pin voltage (V\textsubscript{SENSE}) reaches the detection voltage (-V\textsubscript{DET}) or lower to when the output from OUT pin inverts.

It also has a function that adjusts the release delay time (t\textsubscript{DELAY}) from when the power supply voltage (V\textsubscript{DD}) or SENSE pin voltage (V\textsubscript{SENSE}) reaches the release voltage (+V\textsubscript{DET}) to when the output from OUT pin inverts.

\( t_{\text{RESET}} \) is determined by the delay coefficient, the delay capacitor (C\textsubscript{N}) and the detection delay time when the CN pin is open (\( t_{\text{RESET0}} \)), and the \( t_{\text{DELAY}} \) is determined by the delay coefficient, the delay capacitor (C\textsubscript{P}) and the release delay time when the CP pin is open (\( t_{\text{DELAY0}} \)). They are calculated by the equations below.

\[
 t_{\text{RESET}} \ [\text{ms}] = \text{Delay coefficient} \times C_{\text{N}} \ [\text{nF}] + t_{\text{RESET0}} \ [\text{ms}] \\
 t_{\text{DELAY}} \ [\text{ms}] = \text{Delay coefficient} \times C_{\text{P}} \ [\text{nF}] + t_{\text{DELAY0}} \ [\text{ms}]
\]

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<th>Operation Temperature</th>
<th>Delay Coefficient</th>
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<tbody>
<tr>
<td></td>
<td>Min.</td>
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<tr>
<td>Ta = +125°C</td>
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<tr>
<td>Ta = +105°C</td>
<td>2.41</td>
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<tr>
<td>Ta = +25°C</td>
<td>2.41</td>
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<td>Ta = -40°C</td>
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Table 10

<table>
<thead>
<tr>
<th>Operation Temperature</th>
<th>Detection Delay Time when CN Pin is Open (t\textsubscript{RESET0})</th>
<th>Release Delay Time when CP Pin is Open (t\textsubscript{DELAY0})</th>
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<tbody>
<tr>
<td></td>
<td>Typ.</td>
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<tr>
<td>Ta = -40°C to +125°C</td>
<td>0.35 ms</td>
<td>0.35 ms</td>
</tr>
</tbody>
</table>

Caution

1. Mounted board layout should be made in such a way that no current flows into or flows from the CN pin or CP pin since the impedance of the CN pin and CP pin are high, otherwise correct delay time cannot be provided.

2. There is no limit for the capacitance of C\textsubscript{N} and C\textsubscript{P} as long as the leakage current of the capacitor can be ignored against the built-in constant current value (approximately 300 nA). The leakage current may cause error in delay time. When the leakage current is larger than the built-in constant current, no detect or release takes place.

3. The above equations will not guarantee successful operation. Determine the capacitance of C\textsubscript{N} and C\textsubscript{P} through thorough evaluation including temperature characteristics in the actual usage conditions.

When using an X8R equivalent capacitor, refer to the "2. Detection delay time (t\textsubscript{RESET} vs. Temperature (Ta))", "3. Detection delay time (t\textsubscript{RESET} vs. Power supply voltage (V\textsubscript{DD}))", "5. Release delay time (t\textsubscript{DELAY} vs. Temperature (Ta))" and "6. Release delay time (t\textsubscript{DELAY} vs. Power supply voltage (V\textsubscript{DD}))" in "Reference Data" for details.
Usage Precautions

1. Feed-through current during detection and release

In the S-19110 Series, the feed-through current flows at the time of detection and release. For this reason, if the input impedance is high, oscillation may occur due to voltage drop caused by the feed-through current. When using the S-19110 Series in configurations like those shown in Figure 42 and Figure 43, it is recommended that input impedance be set to 1 kΩ or less. Determine the impedance through thorough evaluation including temperature characteristics.

![Figure 42 VDD Detection Product](image1)
![Figure 43 SENSE Detection Product](image2)
2. Power on and shut down sequence

SENSE detection products monitor SENSE pin voltage \( V_{\text{SENSE}} \) while power is being supplied to the VDD pin. Apply power in the order, the VDD pin then the SENSE pin. In addition, when shutting down VDD pin, shut down the SENSE pin first, and shut down the VDD pin after the detection delay time \( t_{\text{RESET}} \) has elapsed.

![Figure 44](image)

3. Falling power (reference)

Figure 45 shows the relation between \( V_{\text{DD}} \) amplitude \( (V_{\text{P-P}}) \) and input voltage falling time \( (t_f) \) where the release status can be maintained when the VDD pin (VDD detection product) sharply drops to a voltage equal to or higher than the detection voltage \( -(V_{\text{DET}}) \) during release status.

![Figure 45](image)

Caution Figure 45 shows the input voltage conditions which can maintain the release status. If the voltage whose \( V_{\text{P-P}} \) and \( t_f \) are larger than these conditions is input to the VDD pin (VDD detection product), the OUT pin may change to a detection status.

![Figure 46](image)

*1. \( V_{\text{IH}} = 36.0 \text{ V} \)

*2. \( V_{\text{IL}} = -(V_{\text{DET}(S)} + 1.0 \text{ V} \)

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4. VDD pin, SENSE pin voltage glitch (reference)

4.1 Detection operation

Figure 47 and Figure 48 show the relation between pulse width and pulse voltage difference ($V_{OD}$) where the release status can be maintained when a pulse equal to or lower than the detection voltage ($-V_{DET}$) is input to the VDD pin (VDD detection product) or SENSE pin (SENSE detection product) during release status.

![Figure 47 VDD Detection Product](image)

![Figure 48 SENSE Detection Product](image)

Caution Figure 47 and Figure 48 show the pulse conditions which can maintain the release status. If the pulse whose pulse width and $V_{OD}$ are larger than these conditions is input to the VDD pin (VDD detection product) or SENSE pin (SENSE detection product), the OUT pin may change to a detection status.

*1. $V_{IH} = 16.0 \text{ V}$

*2. $V_{IL} = -V_{DET} - V_{OD}$
4.2 Release operation

Figure 50 and Figure 51 show the relation between pulse width and pulse voltage difference ($V_{OD}$) where the detection status can be maintained when a pulse equal to or higher than the release voltage ($+V_{DET}$) is input to the VDD pin (VDD detection product) or SENSE pin (SENSE detection product) during detection status.

Caution Figure 50 and Figure 51 show the pulse conditions which can maintain the detection status. If the pulse whose pulse width and $V_{OD}$ are larger than these conditions is input to the VDD pin (VDD detection product) or SENSE pin (SENSE detection product), the OUT pin may change to a release status.
5. Detection delay time accuracy (reference)

Figure 53 and Figure 54 show the relation between $V_{DD}$ amplitude ($V_{P-P}$) and input voltage falling time ($t_f$) where the arbitrarily set detection delay time accuracy can be maintained when the VDD pin (VDD detection product) sharply drops.

![Figure 53](image1.png) \[ C_N = 3.3 \text{ nF} \]  

![Figure 54](image2.png) \[ C_N = 100 \text{ nF} \]  

![Figure 55](image3.png) \[ V_{IH} = 36.0 \text{ V} \]

\[ V_{IL} = -V_{DET(S)} - 1.0 \text{ V (3.0 V min.)} \]

**Caution** Figure 53 and Figure 54 show the input voltage conditions which can maintain the detection delay time accuracy. If the voltage whose $V_{P-P}$ and $t_f$ are larger than these conditions is input to the VDD pin (VDD detection product), the desired detection delay time may not be achieved.
6. **V\text{DD}** drop during release delay time (reference)

Figure 56 and Figure 57 show the relation between pulse width (t\text{PW}) and **V\text{DD}** lower limit (V\text{DROP}) where a release signal can be output after the normal release delay time has elapsed when the **V\text{DD}** pin (VDD detection product) instantaneously drops to the detection voltage (−V\text{DET}) or lower and then increases to the release voltage (+V\text{DET}) or higher during release delay time.

![Figure 56](image1)

![Figure 57](image2)

Figure 56

Figure 57

Caution 1. Figure 56 and Figure 57 show the input voltage conditions when a release signal is output after the normal release delay time has elapsed. When this is within the inhibited area, release may erroneously be executed before the delay time completes.

2. When the **V\text{DD}** pin voltage is within the inhibited areas shown in Figure 56 and Figure 57 during release delay time, input 0 V to the **V\text{DD}** pin then restart the S-19110 Series.
## Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- Because the SENSE pin has a high impedance, malfunctions may occur due to noise. Be careful of wiring adjoining SENSE pin wiring in actual applications.

- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.
Characteristics (Typical Data)

1. Detection voltage (−V_{DET}), Release voltage (+V_{DET}) vs. Temperature (Ta)

1.1 VDD detection product

- {V_{DET(S)}} = 5.0 V, +{V_{DET(S)}} = 5.25 V
- {V_{DET(S)}} = 7.5 V, +{V_{DET(S)}} = 8.5 V
- {V_{DET(S)}} = 10.0 V, +{V_{DET(S)}} = 13.0 V

1.2 SENSE detection product

- {V_{DET(S)}} = 5.0 V, +{V_{DET(S)}} = 5.25 V, V_{DD} = 16.0 V
- {V_{DET(S)}} = 7.5 V, +{V_{DET(S)}} = 8.5 V, V_{DD} = 16.0 V
- {V_{DET(S)}} = 10.0 V, +{V_{DET(S)}} = 13.0 V, V_{DD} = 16.0 V
2. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Power supply voltage ($V_{DD}$)

2.1 SENSE detection product

![Graph 1: Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Power supply voltage ($V_{DD}$)]

- $V_{DET(S)} = 5.0 \, V$, $+V_{DET(S)} = 5.25 \, V$
- $V_{DET(S)} = 7.5 \, V$, $+V_{DET(S)} = 8.5 \, V$
- $V_{DET(S)} = 10.0 \, V$, $+V_{DET(S)} = 13.0 \, V$

3. Current consumption ($I_{SS}$) vs. Power supply voltage ($V_{DD}$)

3.1 VDD detection product

![Graph 2: Current consumption ($I_{SS}$) vs. Power supply voltage ($V_{DD}$)]

- $V_{DET(S)} = 5.0 \, V$, $+V_{DET(S)} = 5.25 \, V$, $V_{DD} = 0 \, V \rightarrow 36.0 \, V$
- $V_{DET(S)} = 7.5 \, V$, $+V_{DET(S)} = 8.5 \, V$, $V_{DD} = 0 \, V \rightarrow 36.0 \, V$
- $V_{DET(S)} = 10.0 \, V$, $+V_{DET(S)} = 13.0 \, V$, $V_{DD} = 0 \, V \rightarrow 36.0 \, V$
3.2 SENSE detection product

\[ V_{\text{DET(S)}} = 5.0 \, \text{V}, \quad V_{\text{DO}} = 0 \, \text{V} \rightarrow 36.0 \, \text{V}, \]

\[ V_{\text{SENSE}} = -V_{\text{DET}} - 0.1 \, \text{V} \text{ (during detection)} \]

\[ V_{\text{DET(S)}} = 7.5 \, \text{V}, \quad V_{\text{DO}} = 0 \, \text{V} \rightarrow 36.0 \, \text{V}, \]

\[ V_{\text{SENSE}} = -V_{\text{DET}} - 0.1 \, \text{V} \text{ (during detection)} \]

\[ V_{\text{DET(S)}} = 10.0 \, \text{V}, \quad V_{\text{DO}} = 0 \, \text{V} \rightarrow 36.0 \, \text{V}, \]

\[ V_{\text{SENSE}} = -V_{\text{DET}} - 0.1 \, \text{V} \text{ (during detection)} \]
4. Current consumption ($I_{SS}$) vs. Temperature ($T_a$)

4.1 VDD detection product

$V_{DET(S)} = 5.0 \, \text{V}$, $V_D = V_{DET} + 0.1 \, \text{V}$

$V_{DET(S)} = 7.5 \, \text{V}$, $V_D = V_{DET} + 0.1 \, \text{V}$

$V_{DET(S)} = 10.0 \, \text{V}$, $V_D = V_{DET} + 0.1 \, \text{V}$

4.2 SENSE detection product

$V_{DET(S)} = 5.0 \, \text{V}$, $V_D = V_{DET} + 0.1 \, \text{V}$

$V_{DET(S)} = 7.5 \, \text{V}$, $V_D = V_{DET} + 0.1 \, \text{V}$

$V_{DET(S)} = 10.0 \, \text{V}$, $V_D = V_{DET} + 0.1 \, \text{V}$
5. Current consumption during detection delay (I_{SS}) vs. Temperature (T_a)
5.1 VDD detection product
- V_{DET(S)} = 7.5 V, +V_{DET(S)} = 8.5 V,  
  V_{CN} = 0.2 V

5.2 SENSE detection product
- V_{DET(S)} = 7.5 V, +V_{DET(S)} = 8.5 V,  
  V_{DD} = 16.0 V, V_{CN} = 0.2 V

6. Current consumption during release delay (I_{SS}) vs. Temperature (T_a)
6.1 VDD detection product
- V_{DET(S)} = 7.5 V, +V_{DET(S)} = 8.5 V,  
  V_{CP} = 0.2 V

6.2 SENSE detection product
- V_{DET(S)} = 7.5 V, +V_{DET(S)} = 8.5 V,  
  V_{DD} = 16.0 V, V_{CP} = 0.2 V
7. Nch transistor output current (I_{OUT}) vs. V_{DS}

7.1 SENSE detection product

- V_{DET(S)} = 7.5 V, +V_{DET(S)} = 8.5 V, V_{SENSE} = 4.5 V, Ta = -40°C

8. Nch transistor output current (I_{OUT}) vs. Power supply voltage (V_{DD})

8.1 VDD detection product

- V_{DET} = 10.0 V, +V_{DET} = 13.0 V, V_{DS} = 0.05 V

8.2 SENSE detection product

- V_{DET(S)} = 7.5 V, +V_{DET(S)} = 8.5 V, V_{SENSE} = 4.5 V, V_{DS} = 0.05 V

Remark: V_{DS}: Drain-to-source voltage of the output transistor
9. Minimum operation voltage ($V_{OUT}$) vs. Power supply voltage ($V_{DD}$)

9.1 VDD detection product

\[ -V_{DET(S)} = 5.0 \text{ V}, \ +V_{DET(S)} = 5.25 \text{ V}, \]
\[ \text{Pull-up to } V_{DD}, \text{ Pull-up resistance: } 100 \text{ k}\Omega \]

\begin{figure}
\centering
\includegraphics[width=0.4\textwidth]{vout_vdd图表1.png}
\end{figure}

9.2 SENSE detection product

\[ -V_{DET(S)} = 5.0 \text{ V}, \ +V_{DET(S)} = 5.25 \text{ V}, \]
\[ V_{DD} = 3.0 \text{ V}, \]
\[ \text{Pull-up to } V_{DD}, \text{ Pull-up resistance: } 100 \text{ k}\Omega \]

\begin{figure}
\centering
\includegraphics[width=0.4\textwidth]{vout_vsense图表1.png}
\end{figure}
10. Dynamic response vs. Output pin capacitance (COUT) (CP pin, CN pin; open)

10.1 VDD detection product

**−V_{DET(S)} = 5.0 V, +V_{DET(S)} = 5.25 V, Ta = −40°C**

**−V_{DET(S)} = 5.0 V, +V_{DET(S)} = 5.25 V, Ta = +25°C**

**−V_{DET(S)} = 5.0 V, +V_{DET(S)} = 5.25 V, Ta = +105°C**

**−V_{DET(S)} = 5.0 V, +V_{DET(S)} = 5.25 V, Ta = +125°C**

---

**Input voltage**

\[ V_{IH}^{*1} \]

\[ V_{IL}^{*2} \]

**Output voltage**

\[ V_{DD1} \times 50\% \]

\[ V_{DD1} \times 50\% \]

---

*1. \[ V_{IH} = 36.0 \text{ V} \]

*2. \[ V_{IL} = 3.0 \text{ V} \]

---

**Figure 59  Test Condition of Response Time**

**Figure 60  Test Circuit of Response Time**

Caution  The above connection diagram and constants will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constants.
Reference Data

1. Detection delay time ($t_{\text{RESET}}$) vs. CN pin capacitance ($C_N$) (Without output pin capacitance)

   1.1 VDD detection product

   $-V_{\text{DET(S)}} = 5.0 \, \text{V}, \quad +V_{\text{DET(S)}} = 5.25 \, \text{V}$

   ![Graph showing $t_{\text{RESET}}$ vs. $C_N$ for different temperatures.]

   - $T_a = +125^\circ \text{C}$
   - $T_a = +105^\circ \text{C}$
   - $T_a = +25^\circ \text{C}$
   - $T_a = -40^\circ \text{C}$

2. Detection delay time ($t_{\text{RESET}}$) vs. Temperature ($T_a$)

   2.1 VDD detection product

   $-V_{\text{DET(S)}} = 5.0 \, \text{V}, \quad +V_{\text{DET(S)}} = 5.25 \, \text{V}$,

   $C_N = 3.3 \, \text{nF}$

   ![Graph showing $t_{\text{RESET}}$ vs. temperature.]

   ![Test Circuit of Detection Delay Time diagram.]

   - $V_{\text{IH}} \quad \mathbf{1 \mu S}$
   - $V_{\text{IL}}$ (input voltage)
   - $V_{\text{DD}}$ (output voltage)
   - $V_{\text{SS}}$

   - $V_{\text{DD}} = V_{\text{DET(S)}} + 1.0 \, \text{V}$
   - $V_{\text{IL}} = -V_{\text{DET(S)}} - 1.0 \, \text{V}$

   *1. $V_{\text{IH}} = -V_{\text{DET(S)}} + 1.0 \, \text{V}$
   *2. $V_{\text{IL}} = -V_{\text{DET(S)}} - 1.0 \, \text{V}$

Caution: The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.
3. Detection delay time \( (t_{\text{RESET}}) \) vs. Power supply voltage \( (V_{\text{DD}}) \)

3.1 SENSE detection product

\[-V_{\text{DET(S)}} = 5.0 \text{ V}, \quad +V_{\text{DET(S)}} = 5.25 \text{ V}, \]
\[C_N = 3.3 \text{ nF} \]

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{Ta} & \text{VDD [V]} & t_{\text{RESET}} [\text{ms}] \\
\hline
-25^\circ & 0.0 & 0.0 & 6.0 & 12.0 & 18.0 & 24.0 & 30.0 & 36.0 \\
+105^\circ & & & & & & & & \\
+125^\circ & & & & & & & & \\
+25^\circ & & & & & & & & \\
-40^\circ & & & & & & & & \\
\hline
\end{array}
\]

\[V_{\text{IH}} \rightarrow 1 \mu\text{s} \]

Input voltage

\[V_{\text{IL}} \rightarrow V_{\text{DD}} \]

Output voltage

\[V_{\ss} \rightarrow V_{\text{DD}} \times 50\% \]

\*1. \[V_{\text{IH}} = -V_{\text{DET(S)}} + 1.0 \text{ V} \]

\*2. \[V_{\text{IL}} = -V_{\text{DET(S)}} - 1.0 \text{ V} \]

Figure 63  Test Condition of Detection Delay Time

Figure 64  Test Circuit of Detection Delay Time

Caution  The above connection diagram and constants will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constants.
4. Release delay time (t_{DELAY}) vs. CP pin capacitance (C_p) (Without output pin capacitance)

4.1 VDD detection product

\[ -V_{DET(S)} = 5.0 \text{ V}, \quad +V_{DET(S)} = 5.25 \text{ V} \]

<table>
<thead>
<tr>
<th>C_p [nF]</th>
<th>0.01</th>
<th>0.1</th>
<th>1</th>
<th>10</th>
<th>100</th>
<th>1000</th>
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<tbody>
<tr>
<td>t_{DELAY} [ms]</td>
<td>1000</td>
<td>100</td>
<td>10</td>
<td>1</td>
<td>1</td>
<td>0.1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Ta [°C]</th>
<th>-40</th>
<th>-25</th>
<th>0</th>
<th>25</th>
<th>50</th>
<th>75</th>
<th>100</th>
<th>125</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{DELAY} [ms]</td>
<td>12.0</td>
<td>10.0</td>
<td>8.0</td>
<td>6.0</td>
<td>4.0</td>
<td>2.0</td>
<td>0.0</td>
<td>1 μs</td>
</tr>
</tbody>
</table>

5. Release delay time (t_{DELAY}) vs. Temperature (Ta)

5.1 VDD detection product

\[ -V_{DET(S)} = 5.0 \text{ V}, \quad +V_{DET(S)} = 5.25 \text{ V}, \quad C_p = 3.3 \text{ nF} \]

<table>
<thead>
<tr>
<th>Ta [°C]</th>
<th>-40</th>
<th>-25</th>
<th>0</th>
<th>25</th>
<th>50</th>
<th>75</th>
<th>100</th>
<th>125</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{DELAY} [ms]</td>
<td>12.0</td>
<td>10.0</td>
<td>8.0</td>
<td>6.0</td>
<td>4.0</td>
<td>2.0</td>
<td>0.0</td>
<td>1 μs</td>
</tr>
</tbody>
</table>

*1. \( V_{IH} = +V_{DET(S)} + 1.0 \text{ V} \)
*2. \( V_{IL} = +V_{DET(S)} - 1.0 \text{ V} \)

Figure 65 Test Condition of Release Delay Time

Figure 66 Test Circuit of Release Delay Time

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.
6. Release delay time ($t_{\text{DELAY}}$) vs. Power supply voltage ($V_{\text{DD}}$)

6.1 SENSE detection product

$$-V_{\text{DET(S)}} = 5.0 \text{ V}, +V_{\text{DET(S)}} = 5.25 \text{ V},$$
$$C_P = 3.3 \text{ nF}$$

- $V_{\text{ih}}$ = $+V_{\text{DET(S)}} + 1.0 \text{ V}$
- $V_{\text{il}}$ = $+V_{\text{DET(S)}} - 1.0 \text{ V}$

Figure 67 Test Condition of Release Delay Time

7. Load dump characteristics ($T_a = +25^\circ \text{C}$)

7.1 VDD detection, active "L" product

$$V_{\text{DD}} = 13.5 \text{ V} \leftrightarrow 45.0 \text{ V}$$

Caution  The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.
## Application Circuit Examples

1. **Microcomputer reset circuits**

   In microcomputers, when the power supply voltage is lower than the minimum operation voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the microcomputer may malfunction after that. Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.

   Using the S-19110 Series which has the low minimum operation voltage, the high-accuracy detection voltage and the hysteresis width, reset circuits can be easily constructed as seen in [Figure 70](#) and [Figure 71](#).

   ![Figure 70](#)  Example of Reset Circuit (VDD Detection Product)

   ![Figure 71](#)  Example of Reset Circuit (SENSE Detection Product)

   **Caution**  The above connection diagrams will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.
**Power Dissipation**

**SOT-23-6**

![Power Dissipation Graph](image)

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<th>Board</th>
<th>Power Dissipation ($P_d$)</th>
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<tr>
<td>A</td>
<td>0.63 W</td>
</tr>
<tr>
<td>B</td>
<td>0.81 W</td>
</tr>
<tr>
<td>C</td>
<td>–</td>
</tr>
<tr>
<td>D</td>
<td>–</td>
</tr>
<tr>
<td>E</td>
<td>–</td>
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</tbody>
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### SOT-23-3/3S/5/6 Test Board

#### Board A

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<th>Specification</th>
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<tbody>
<tr>
<td>Size [mm]</td>
<td>114.3 x 76.2 x t1.6</td>
</tr>
<tr>
<td>Material</td>
<td>FR-4</td>
</tr>
<tr>
<td>Number of copper foil layer</td>
<td>2</td>
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<td>Copper foil layer [mm]</td>
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<td>1</td>
<td>Land pattern and wiring for testing: t0.070</td>
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<tr>
<td>2</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>74.2 x 74.2 x t0.070</td>
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#### Board B

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<tr>
<td>Size [mm]</td>
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No. SOT23x-A-Board-SD-2.0

ABLIC Inc.
No. MP006-A-P-SD-2.1

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ABLIC Inc.
No. MP006-A-C-SD-3.1

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<td>UNIT</td>
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ABLIC Inc.
Enlarged drawing in the central part

No. MP006-A-R-SD-2.1

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ABLIC Inc.
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7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.

8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.

9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products’ failure or malfunction. The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer’s own responsibility.

10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.

11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.

12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.

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14. For more details on the information described herein or any other questions, please contact ABLIC Inc.’s sales representative.

15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.