

The S-19101xxxH Series, developed by using CMOS technology, is a voltage detector IC for automotive 105°C operation. The detection voltage is fixed internally with an accuracy of  $\pm 2.5\%$  ( $-V_{DET} = 2.4\text{ V}$ ). The release voltage is set to the same value as the detection voltage, since there is no hysteresis width. It operates with current consumption of 270 nA typ. The release signal can be delayed by setting a capacitor externally, and the delay time accuracy at  $T_a = +25^\circ\text{C}$  is  $\pm 15\%$ . The operation temperature range is  $T_a = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ . Two output forms Nch open-drain and CMOS output are available.

Compared with conventional CMOS voltage detectors, the S-19101xxxH Series has super-low current consumption and small packages.

**Caution** This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.

## ■ Features

- Detection voltage: 1.2 V to 4.6 V (0.1 V step)
- Detection voltage accuracy:  $\pm 2.5\%$  ( $2.4\text{ V} \leq -V_{DET} \leq 4.6\text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ )  
 $\pm(2.0\% + 12\text{ mV})$  ( $1.2\text{ V} \leq -V_{DET} < 2.4\text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ )
- Current consumption: 270 nA typ. ( $1.2\text{ V} \leq -V_{DET} < 2.3\text{ V}$ )
- Operation voltage range: 0.6 V to 10.0 V (CMOS output product)
- Delay time accuracy:  $\pm 15\%$  ( $C_D = 4.7\text{ nF}$ ,  $T_a = +25^\circ\text{C}$ )
- Output form: Nch open-drain output (active "L")  
CMOS output (active "L")
- Operation temperature range:  $T_a = -40^\circ\text{C}$  to  $+105^\circ\text{C}$
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified\*1

\*1. Contact our sales office for details.

## ■ Applications

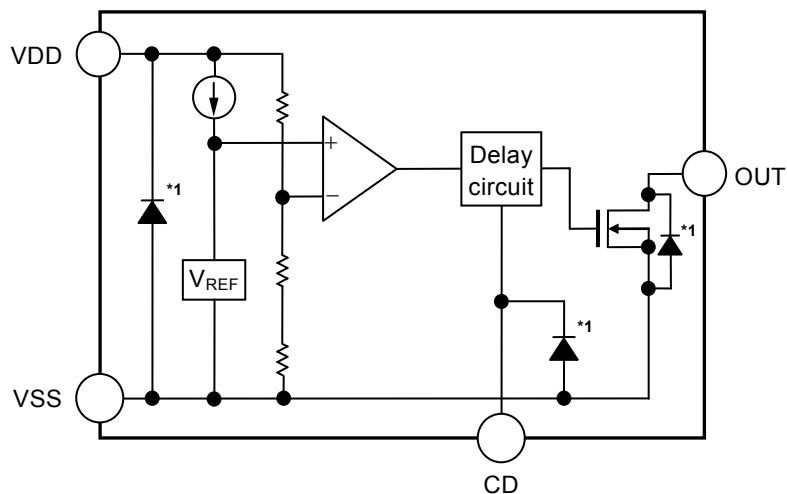
- For automotive use (car body, headlight, ITS, accessory, car navigation system, car audio system, etc.)

## ■ Packages

- SOT-23-5
- SC-82AB

■ **Block Diagrams**

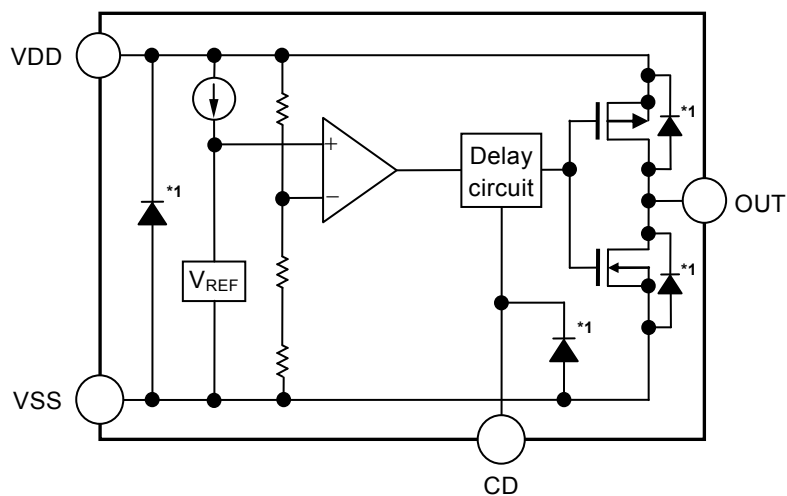
1. **Nch open-drain output product**



\*1. Parasitic diode

Figure 1

2. **CMOS output product**



\*1. Parasitic diode

Figure 2

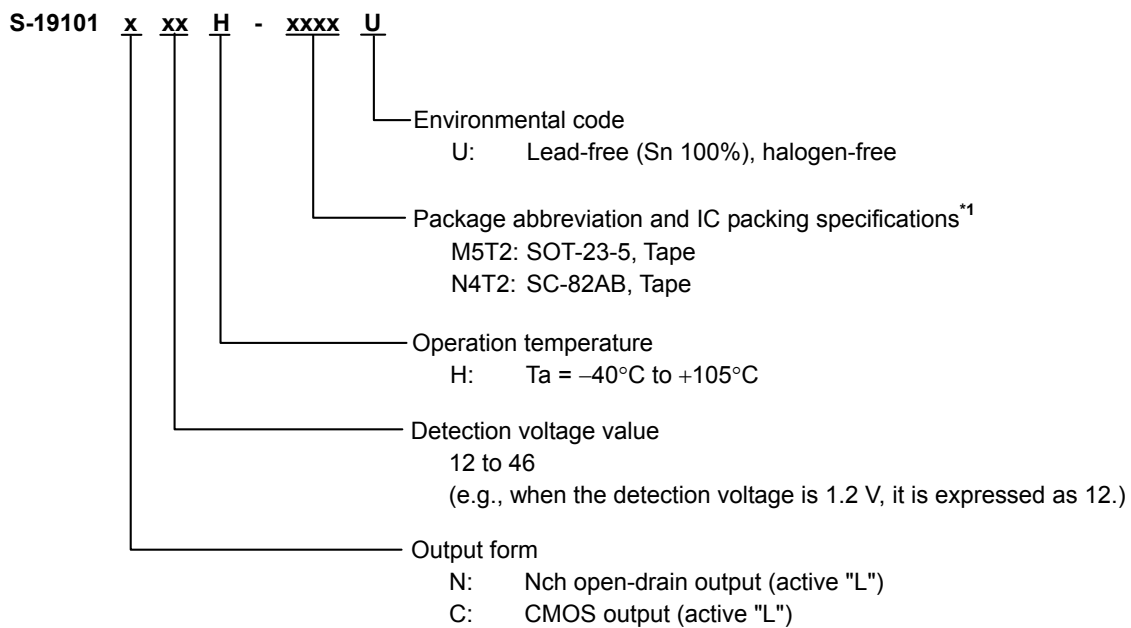
## ■ AEC-Q100 Qualified

This IC supports AEC-Q100 for the operation temperature grade 2.  
 Contact our sales office for details of AEC-Q100 reliability specification.

## ■ Product Name Structure

Users can select the output form, the detection voltage value and the package type for the S-19101xxxH Series. Refer to "1. Product name" regarding the contents of product name, "2. Packages" regarding the package drawings and "3. Product name list" regarding details of product name.

### 1. Product name



\*1. Refer to the tape drawing.

### 2. Packages

**Table 1 Package Drawing Codes**

Package Name	Dimension	Tape	Reel
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD
SC-82AB	NP004-A-P-SD	NP004-A-C-SD NP004-A-C-S1	NP004-A-R-SD

### 3. Product name list

#### 3.1 CMOS output product

**Table 2**

Detection Voltage	SOT-23-5	SC-82AB
2.5 V ± 2.5%	S-19101C25H-M5T2U	S-19101C25H-N4T2U
2.6 V ± 2.5%	S-19101C26H-M5T2U	S-19101C26H-N4T2U
2.7 V ± 2.5%	S-19101C27H-M5T2U	S-19101C27H-N4T2U
2.8 V ± 2.5%	S-19101C28H-M5T2U	S-19101C28H-N4T2U

**Remark** Please contact our sales office for products with specifications other than the above.

■ Pin Configurations

1. SOT-23-5

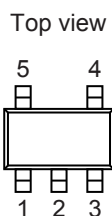


Figure 3

Table 3

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Input voltage pin
3	VSS	GND pin
4	NC <sup>*1</sup>	No connection
5	CD	Connection pin for delay capacitor

\*1. The NC pin is electrically open.  
 The NC pin can be connected to the VDD pin or the VSS pin.

2. SC-82AB

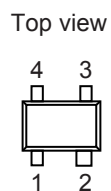


Figure 4

Table 4

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Input voltage pin
3	CD	Connection pin for delay capacitor
4	OUT	Voltage detection output pin

■ Absolute Maximum Ratings

Table 5

(Ta = -40°C to +105°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	$V_{DD} - V_{SS}$	12	V
CD pin input voltage	$V_{CD}$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Output voltage	$V_{OUT}$	Nch open-drain output product	$V_{SS} - 0.3$ to 12.0
		CMOS output product	$V_{SS} - 0.3$ to $V_{DD} + 0.3$
Output current	$I_{OUT}$	50	mA
Power dissipation	SOT-23-5	$600^{*1}$	mW
	SC-82AB	$350^{*1}$	mW
Operation ambient temperature	$T_{opr}$	-40 to +105	°C
Storage temperature	$T_{stg}$	-40 to +125	°C

\*1. When mounted on board

[Mounted board]

(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm

(2) Name: JEDEC STANDARD51-7

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

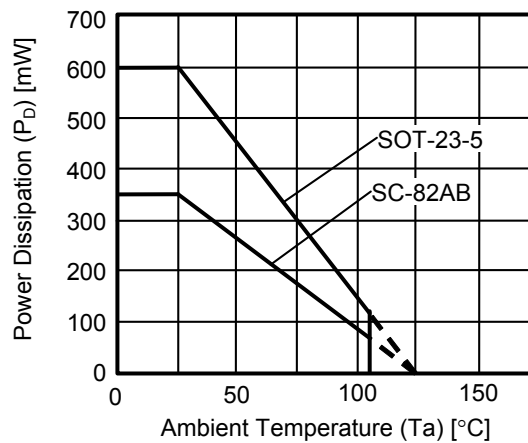


Figure 5 Power Dissipation of Package (When Mounted on Board)

■ **Electrical Characteristics**

1. **Nch open-drain output product**

**Table 6**

(Ta = -40°C to +105°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Detection voltage**1	$-V_{DET}$	$1.2\text{ V} \leq -V_{DET} < 2.4\text{ V}$	$-V_{DET(S)} \times 0.98 - 0.012$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.02 + 0.012$	V	1	
		$2.4\text{ V} \leq -V_{DET} \leq 4.6\text{ V}$	$-V_{DET(S)} \times 0.975$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025$	V	1	
Current consumption	$I_{SS}$	$V_{DD} = +V_{DET} + 0.6\text{ V}$	$1.2\text{ V} \leq -V_{DET} < 2.3\text{ V}$	–	0.27	1.10	$\mu\text{A}$	2
			$2.3\text{ V} \leq -V_{DET} < 3.6\text{ V}$	–	0.42	1.20	$\mu\text{A}$	2
			$3.6\text{ V} \leq -V_{DET} \leq 4.6\text{ V}$	–	0.39	1.20	$\mu\text{A}$	2
Operation voltage	$V_{DD}$	–	0.8	–	10.0	V	1	
Output current	$I_{OUT}$	Output transistor Nch $V_{DS}^{*2} = 0.5\text{ V}$	$V_{DD} = 0.7\text{ V}$ S-19101N12 to 14	0.14	0.40	–	mA	3
			$V_{DD} = 1.2\text{ V}$ S-19101N15 to 46	0.73	1.33	–	mA	3
			$V_{DD} = 2.4\text{ V}$ S-19101N27 to 46	1.17	2.39	–	mA	3
Leakage current	$I_{LEAK}$	Output transistor Nch $V_{DD} = 10.0\text{ V}, V_{OUT} = 10.0\text{ V}$	–	–	1.20	$\mu\text{A}$	3	
Delay time	$t_D$	$C_D = 4.7\text{ nF}$	12.0	26.0	57.0	ms	4	

\*1.  $-V_{DET}$ : Actual detection voltage value,  $-V_{DET(S)}$ : Set detection voltage value (The center value of the detection voltage range.)

\*2.  $V_{DS}$ : Drain-to-source voltage of the output transistor

2. CMOS output product

Table 7

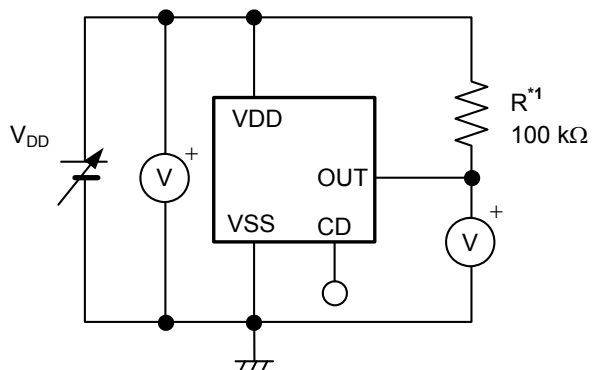
(Ta = -40°C to +105°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Detection voltage*1	$-V_{DET}$	$1.2\text{ V} \leq -V_{DET} < 2.4\text{ V}$	$-V_{DET(S)} \times 0.98 - 0.012$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.02 + 0.012$	V	1	
		$2.4\text{ V} \leq -V_{DET} \leq 4.6\text{ V}$	$-V_{DET(S)} \times 0.975$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025$	V	1	
Current consumption	$I_{SS}$	$V_{DD} = +V_{DET} + 0.6\text{ V}$	$1.2\text{ V} \leq -V_{DET} < 2.3\text{ V}$	-	0.27	1.70	$\mu\text{A}$	2
			$2.3\text{ V} \leq -V_{DET} < 3.6\text{ V}$	-	0.42	1.90	$\mu\text{A}$	2
			$3.6\text{ V} \leq -V_{DET} \leq 4.6\text{ V}$	-	0.39	1.90	$\mu\text{A}$	2
Operation voltage	$V_{DD}$	-	0.6	-	10.0	V	1	
Output current	$I_{OUT}$	Output transistor Nch $V_{DS}^{*2} = 0.5\text{ V}$	$V_{DD} = 0.7\text{ V}$ S-19101C12 to 14	0.14	0.40	-	mA	3
			$V_{DD} = 1.2\text{ V}$ S-19101C15 to 46	0.73	1.33	-	mA	3
			$V_{DD} = 2.4\text{ V}$ S-19101C27 to 46	1.17	2.39	-	mA	3
		Output transistor Pch $V_{DS}^{*2} = 0.5\text{ V}$	$V_{DD} = 4.8\text{ V}$ S-19101C12 to 39	1.42	2.60	-	mA	5
			$V_{DD} = 6.0\text{ V}$ S-19101C40 to 46	1.58	2.86	-	mA	5
Delay time	$t_D$	$C_D = 4.7\text{ nF}$	12.0	26.0	57.0	ms	4	

\*1.  $-V_{DET}$ : Actual detection voltage value,  $-V_{DET(S)}$ : Set detection voltage value (The center value of the detection voltage range in Table 2.)

\*2.  $V_{DS}$ : Drain-to-source voltage of the output transistor

■ Test Circuits



\*1. R is unnecessary for CMOS output product.

Figure 6 Test Circuit 1

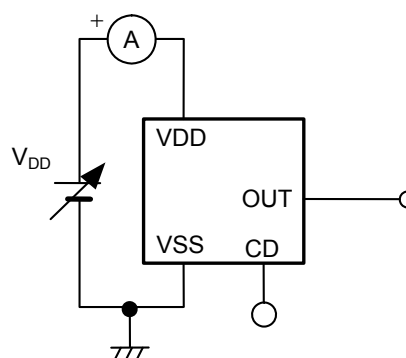


Figure 7 Test Circuit 2

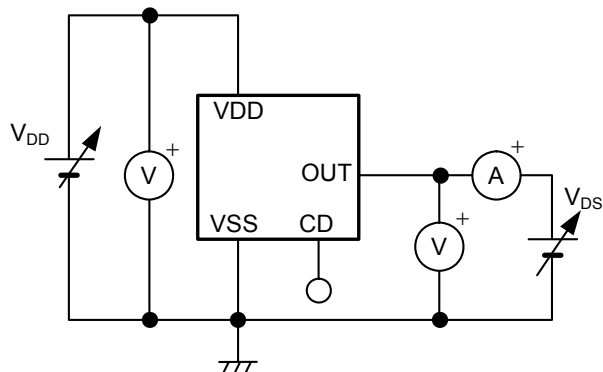
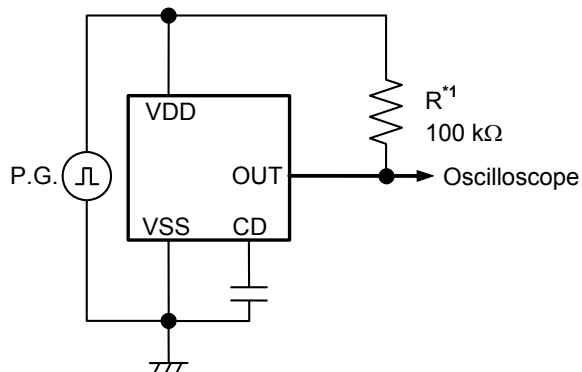


Figure 8 Test Circuit 3



\*1. R is unnecessary for CMOS output product.

Figure 9 Test Circuit 4

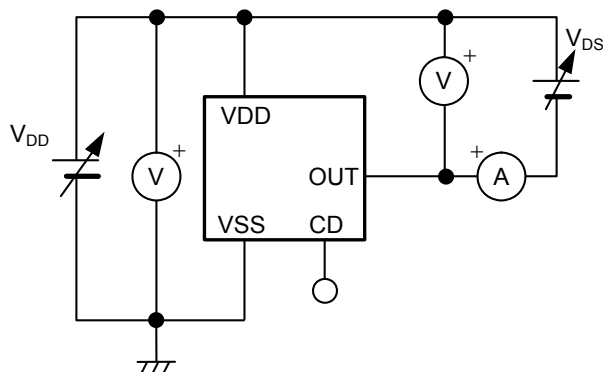
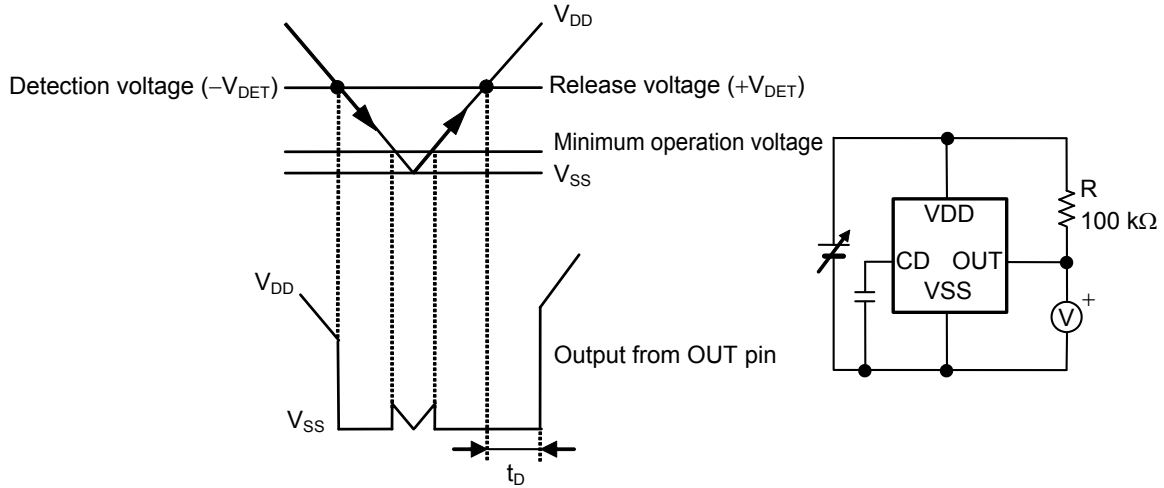


Figure 10 Test Circuit 5



■ Timing Charts

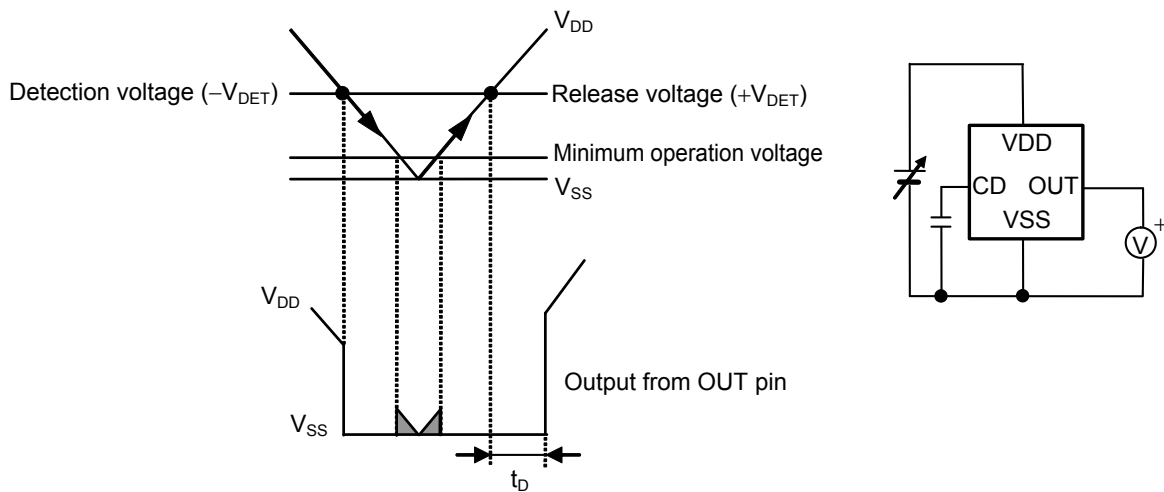
1. Nch open-drain output product



**Remark** The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 11

2. CMOS output product



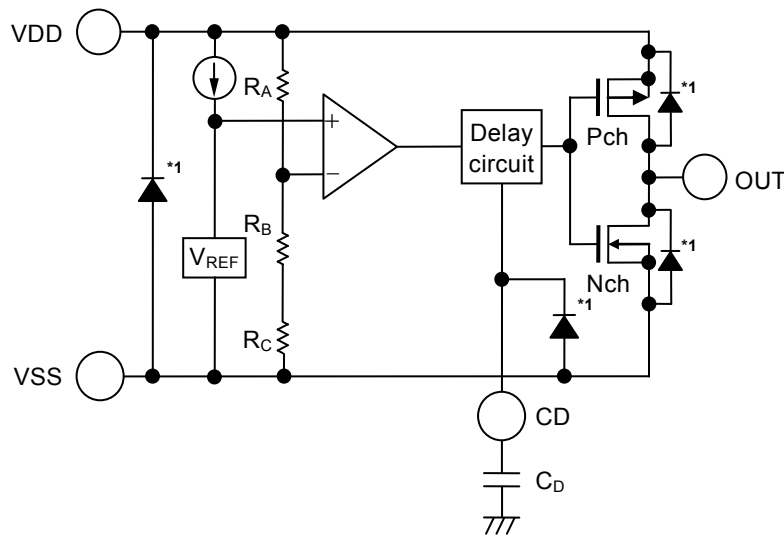
**Remark** When  $V_{DD}$  is the minimum operation voltage or less, the output voltage from the OUT pin is indefinite in the shaded area.  
 The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 12

■ **Operation**

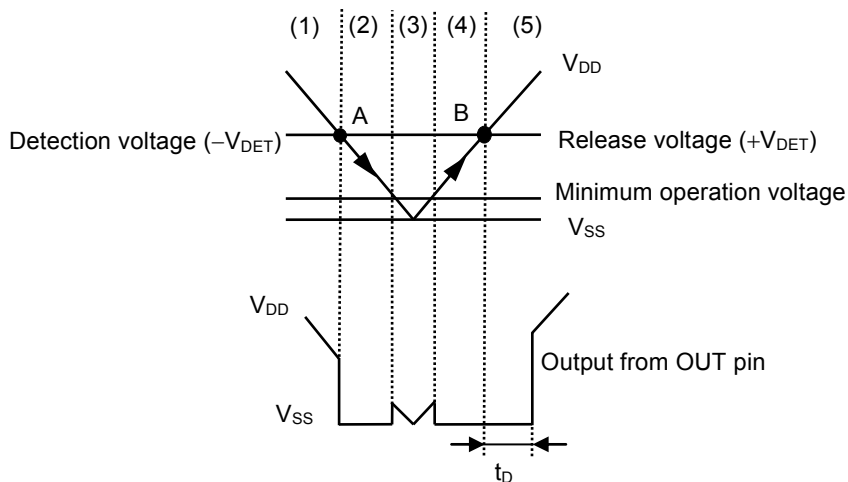
**1. Basic operation: CMOS output (active "L") product**

- (1) When the power supply voltage ( $V_{DD}$ ) is the release voltage ( $+V_{DET}$ ) or more, the Nch transistor is OFF and the Pch transistor is ON to output  $V_{DD}$  ("H"). At this time, as shown in **Figure 13**, the comparator input voltage is  $\frac{(R_B + R_C) \cdot V_{DD}}{R_A + R_B + R_C}$ .
- (2) When  $V_{DD}$  decreases to  $-V_{DET}$  or less (point A in **Figure 14**), the Nch transistor is ON and the Pch transistor is OFF so that  $V_{SS}$  is output.
- (3) The output is indefinite by decreasing  $V_{DD}$  to the IC's minimum operation voltage or less. If the output is pulled up, it will be  $V_{DD}$ .
- (4)  $V_{SS}$  is output by increasing  $V_{DD}$  to the minimum operation voltage or more. Although  $V_{DD}$  is less than  $+V_{DET}$ , the output is  $V_{SS}$ .
- (5) When increasing  $V_{DD}$  to  $+V_{DET}$  or more (point B in **Figure 14**), the Nch transistor is OFF and the Pch transistor is ON so that  $V_{DD}$  is output. At this time,  $V_{DD}$  is output from the OUT pin after the passage of the delay time ( $t_D$ ).



\*1. Parasitic diode

**Figure 13 Operation 1**



**Remark** The release voltage is set to the same value as the detection voltage, since there no hysteresis width.

**Figure 14 Operation 2**

**2. Delay circuit**

The delay circuit delays the output signal to the OUT pin from the time at which the power supply voltage ( $V_{DD}$ ) exceeds the release voltage ( $+V_{DET}$ ) when the power supply voltage ( $V_{DD}$ ) is turned on. The output signal is not delayed when  $V_{DD}$  decreases to the detection voltage ( $-V_{DET}$ ) or less (refer to "Figure 14 Operation 2").

The delay time ( $t_D$ ) is determined by the time constant of the built-in constant current (approx. 100 nA) and the attached delay capacitor ( $C_D$ ), or the delay time ( $t_{D0}$ ) when the CD pin is open, and calculated from the following equation. When the  $C_D$  value is sufficiently large, the  $t_{D0}$  value can be disregarded.

$$t_D [\text{ms}] = \text{Delay coefficient} \times C_D [\text{nF}] + t_{D0} [\text{ms}]$$

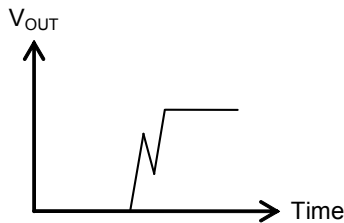
**Table 8 Delay Coefficient**

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +105°C	2.58	3.70	5.40
Ta = +25°C	4.70	5.47	6.24
Ta = -40°C	5.64	8.40	12.01

**Table 9 Delay Time**

Operation Temperature	Delay Time ( $t_{D0}$ )		
	Min.	Typ.	Max.
Ta = -40°C to +105°C	0.01 ms	0.10 ms	0.80 ms

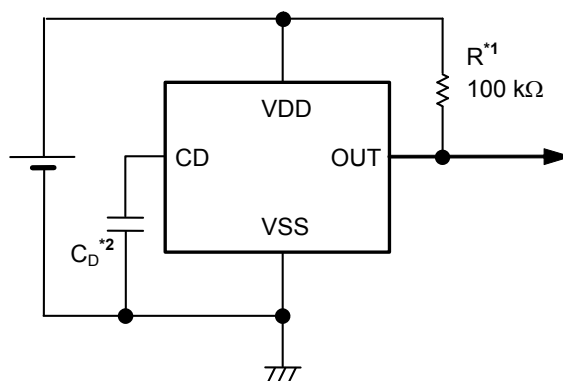
- Caution 1.** When the CD pin is open, a double pulse shown in Figure 15 may appear at release. To avoid the double pulse, attach 100 pF or more capacitor to the CD pin. Do not apply voltage to the CD pin from the exterior.



**Figure 15**

2. Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.
3. There is no limit for the capacitance of  $C_D$  as long as the leakage current of the capacitor can be ignored against the built-in constant current value. Leakage current causes deviation in delay time. When the leakage current is larger than the built-in constant current, no release takes place.

■ Standard Circuit



- \*1. R is unnecessary for CMOS output products.
- \*2. The delay capacitor (C<sub>D</sub>) should be connected directly to the CD pin and the VSS pin.

Figure 16

**Caution** The above connection diagram and constant will not guarantee successful operation.  
Perform thorough evaluation using the actual application to set the constant.

## ■ Explanation of Terms

### 1. Detection voltage ( $-V_{DET}$ )

The detection voltage is a voltage at which the output in **Figure 19** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ( $-V_{DET}$  min.) and the maximum ( $-V_{DET}$  max.) is called the detection voltage range (refer to **Figure 17**).

Example: In the S-19101C20H, the detection voltage is either one in the range of  $1.948\text{ V} \leq -V_{DET} \leq 2.052\text{ V}$ . This means, at the operation temperature  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ , some S-19101C20H have  $-V_{DET} = 1.948\text{ V}$  and some have  $-V_{DET} = 2.052\text{ V}$ .

### 2. Release voltage ( $+V_{DET}$ )

The release voltage is a voltage at which the output in **Figure 19** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltages between the specified minimum ( $+V_{DET}$  min.) and the maximum ( $+V_{DET}$  max.) is called the release voltage range (refer to **Figure 18**). The release voltage ( $+V_{DET}$ ) is the same value as the actual detection voltage ( $-V_{DET}$ ) of a product.

Example: In the S-19101C20H, the release voltage is either one in the range of  $1.948\text{ V} \leq +V_{DET} \leq 2.052\text{ V}$ . This means, at the operation temperature  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ , some S-19101C20H have  $+V_{DET} = 1.948\text{ V}$  and some have  $+V_{DET} = 2.052\text{ V}$ .

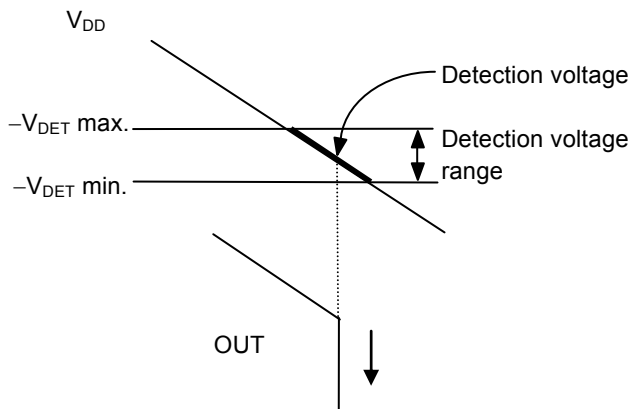


Figure 17 Detection Voltage

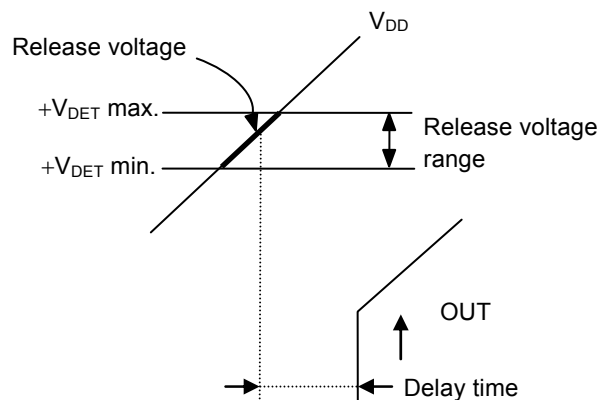
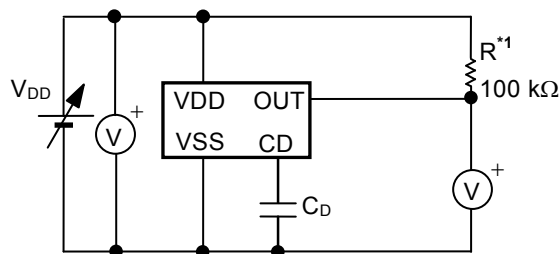


Figure 18 Release Voltage



\*1. R is unnecessary for CMOS output product.

Figure 19 Test Circuit of Detection Voltage and Release Voltage

**3. Delay time ( $t_D$ )**

The delay time in the S-19101xxxH Series is a period from the input voltage to the VDD pin exceeding the release voltage ( $+V_{DET}$ ) until the output from the OUT pin inverts. The delay time changes according to the delay capacitor ( $C_D$ ).

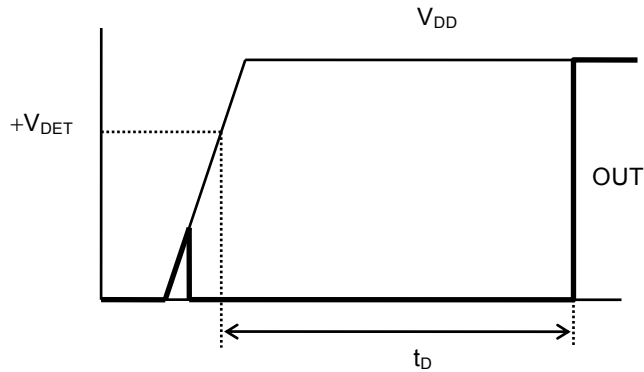


Figure 20 Delay Time

**4. Feed-through current**

Feed-through current is a current that flows instantaneously at the time of detection and release of a voltage detector. The feed-through current is large in CMOS output product, small in Nch open-drain output product.

**5. Oscillation**

In applications where a resistor is connected to the voltage detector input (Figure 21), taking a CMOS output (active "L") product for example, the feed-through current which is generated when the output goes from "L" to "H" (release) causes a voltage drop equal to [feed-through current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ( $-V_{DET}$ ) as a result, the output voltage goes to low level. In this state, the feed-through current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The feed-through current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

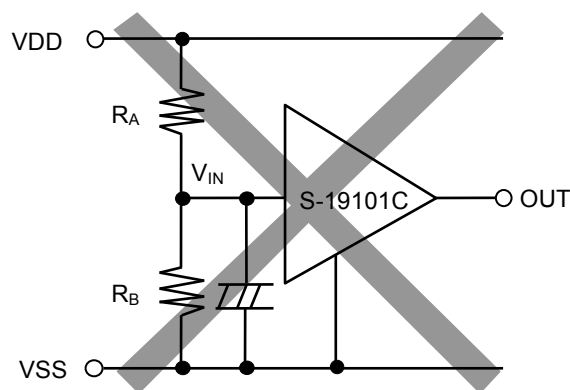


Figure 21 Example for Bad Implementation Due to Detection Voltage Change

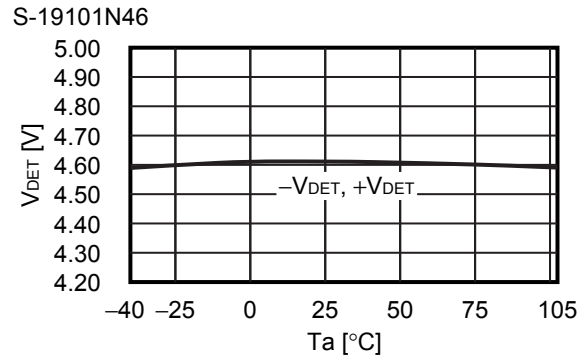
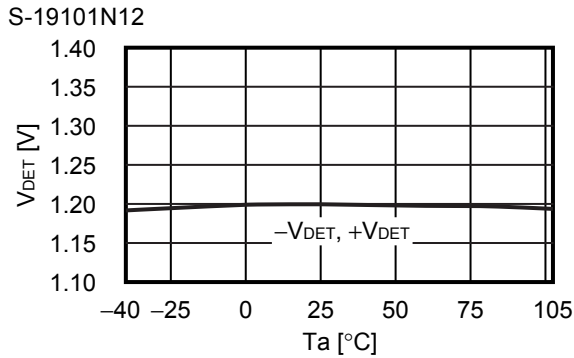
**Caution** The release voltage is set to the same value as the detection voltage, since there is no hysteresis width in the S-19101xxxH Series. Therefore, the output goes from "H" to "L" if the power supply voltage ( $V_{DD}$ ) reaches the detection voltage. The voltage which once became to "L" goes from "L" to "H" again. This repeating process may induce oscillation as well. Perform thorough evaluation using the actual application.

## ■ Precautions

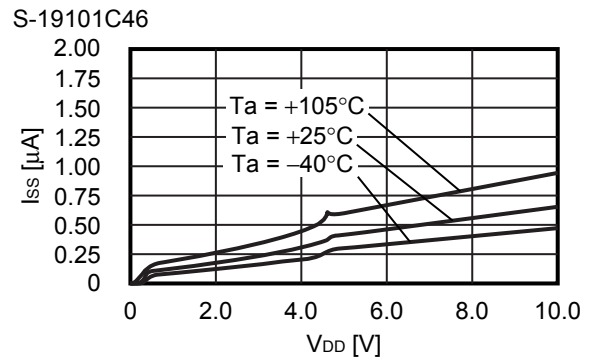
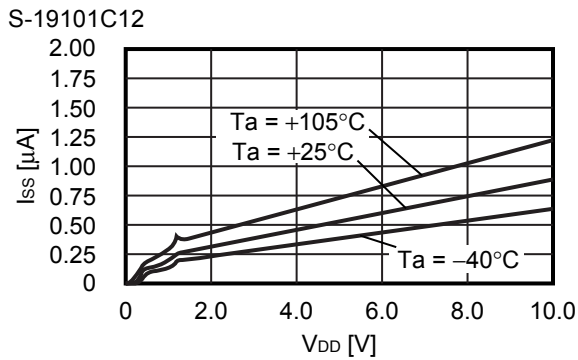
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output product, the feed-through current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the feed-through current during releasing.
- In CMOS output product, oscillation may occur when a pull-down resistor is used, and falling speed of the power supply voltage ( $V_{DD}$ ) is slow near the detection voltage.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ **Characteristics (Typical Data)**

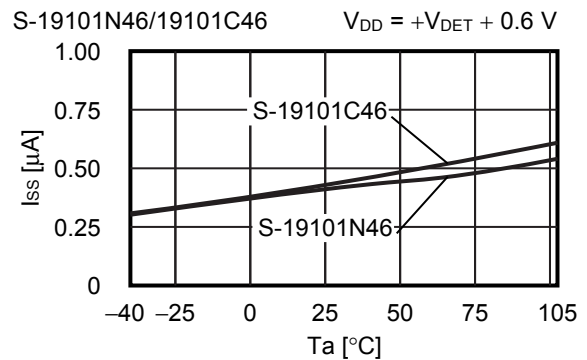
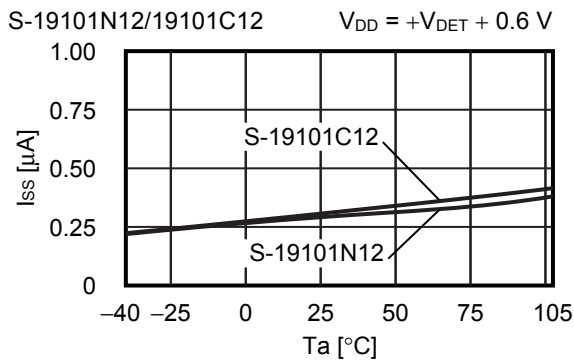
**1. Detection voltage ( $V_{DET}$ ) vs. Temperature ( $T_a$ )**



**2. Current consumption ( $I_{SS}$ ) vs. Input voltage ( $V_{DD}$ )**

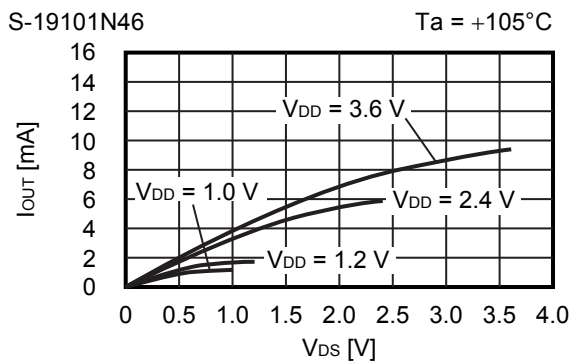
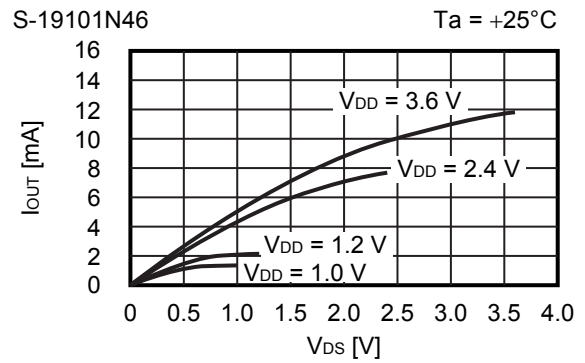
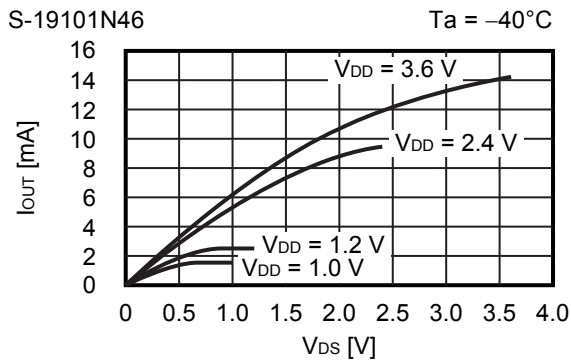


**3. Current consumption ( $I_{SS}$ ) vs. Temperature ( $T_a$ )**

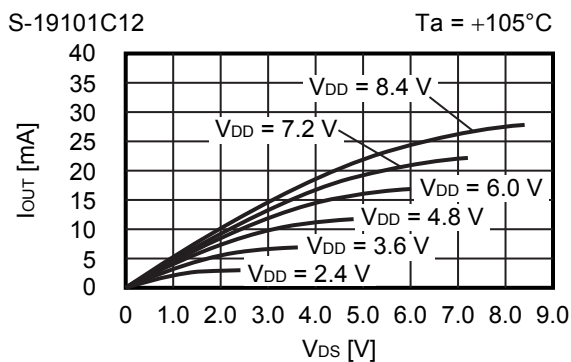
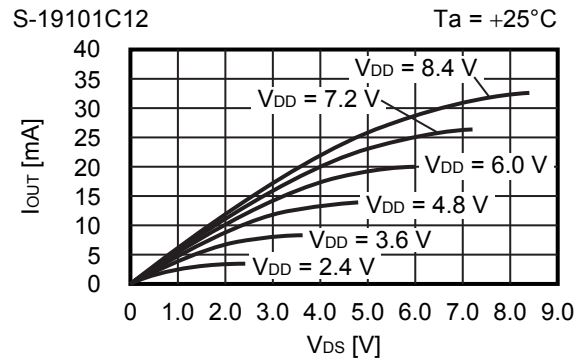
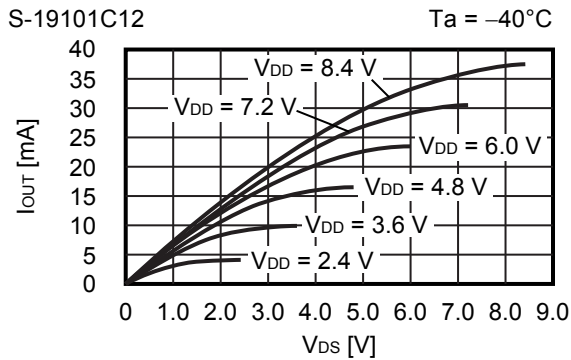




**4. Nch transistor output current ( $I_{OUT}$ ) vs.  $V_{DS}$**

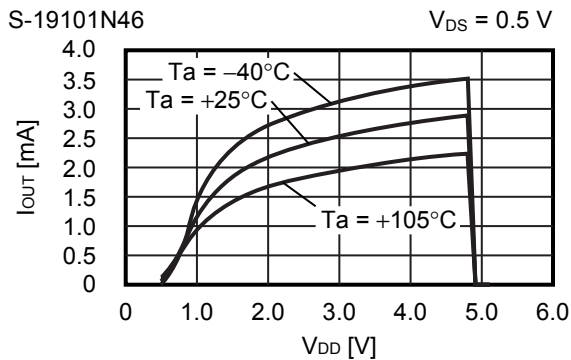


**5. Pch transistor output current ( $I_{OUT}$ ) vs.  $V_{DS}$**

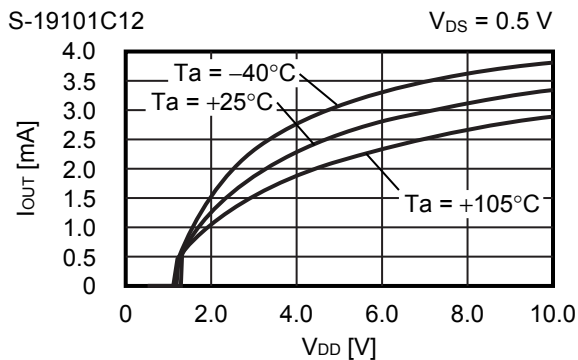


**Remark**  $V_{DS}$ : Drain-to-source voltage of the output transistor

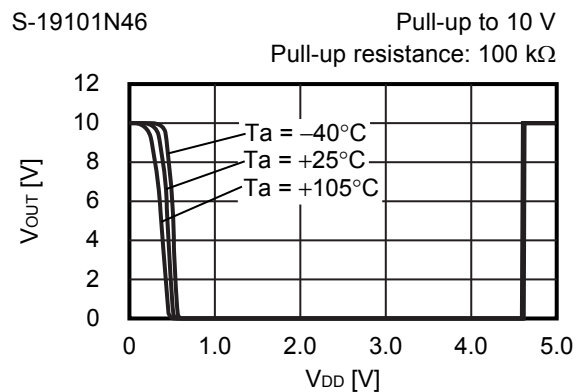
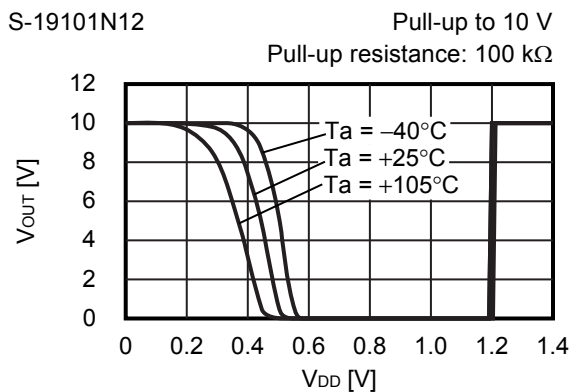
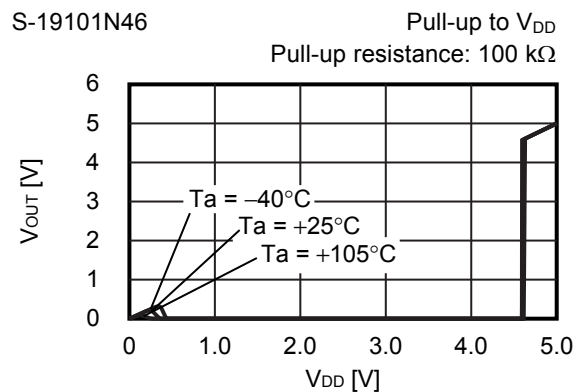
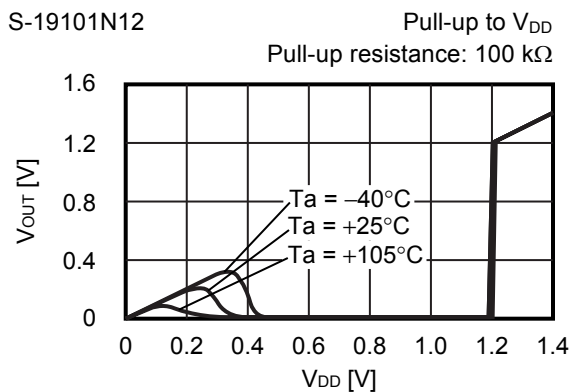
**6. Nch transistor output current ( $I_{OUT}$ ) vs. Input voltage ( $V_{DD}$ )**



**7. Pch transistor output current ( $I_{OUT}$ ) vs. Input voltage ( $V_{DD}$ )**



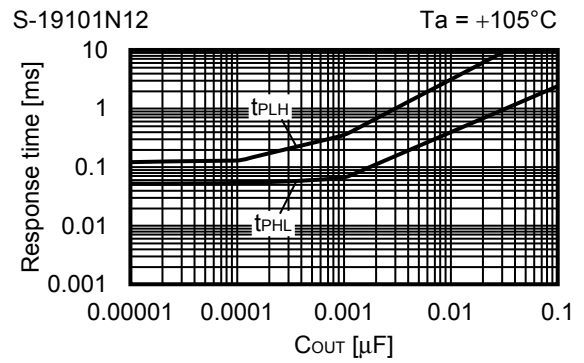
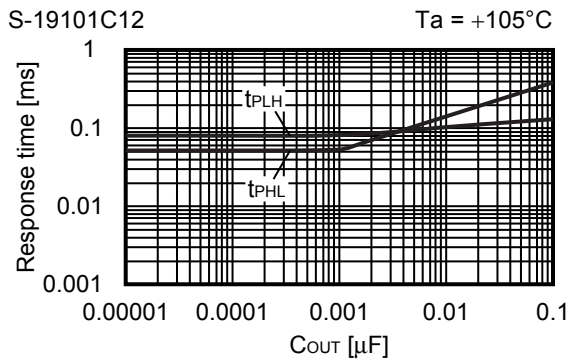
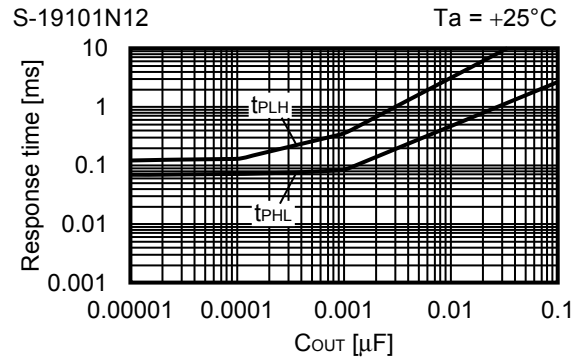
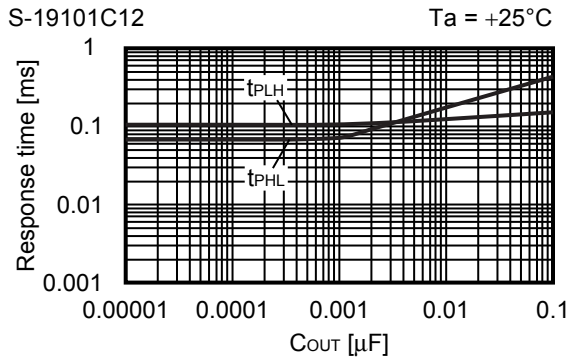
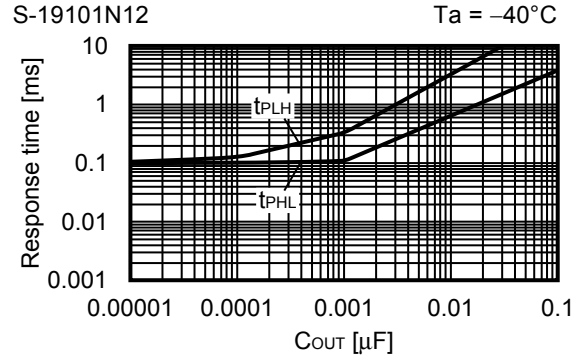
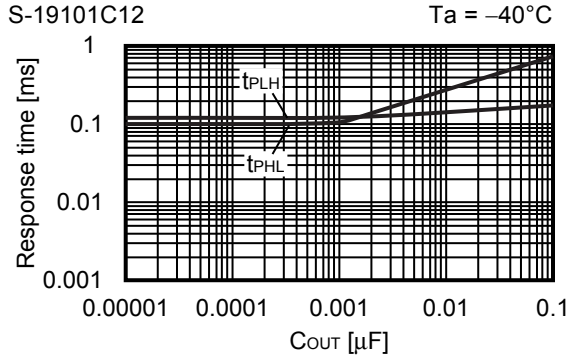
**8. Minimum operation voltage ( $V_{OUT}$ ) vs. Input voltage ( $V_{DD}$ )**



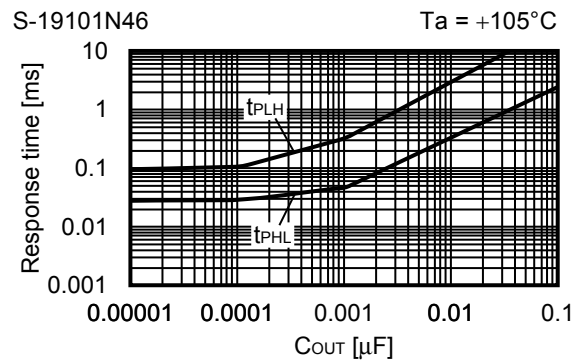
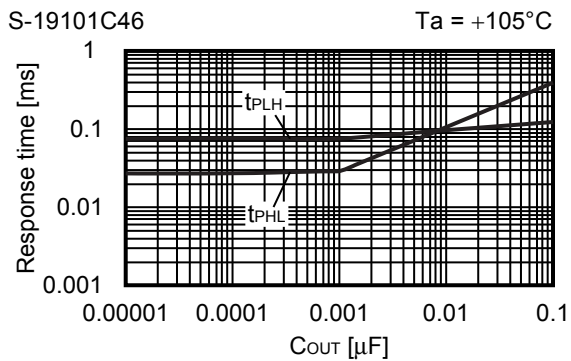
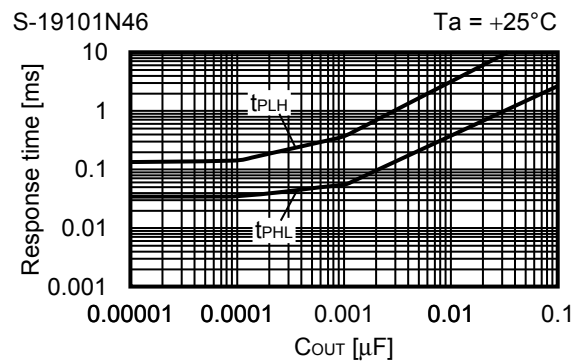
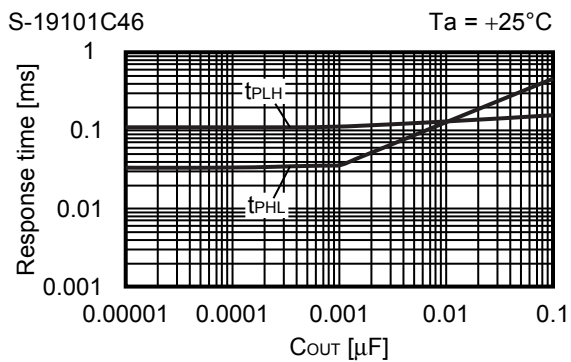
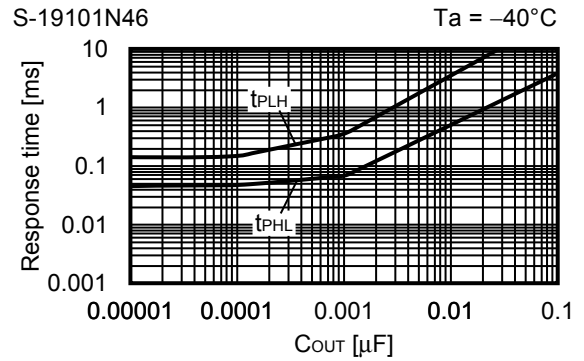
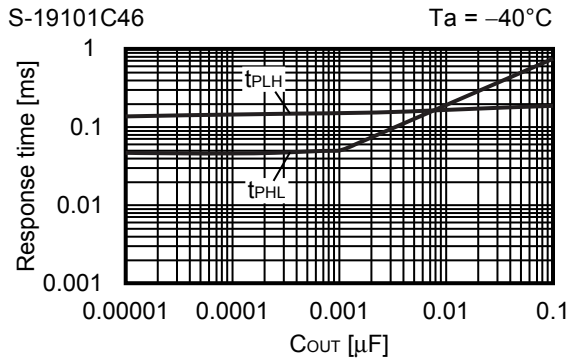
**Remark**  $V_{DS}$ : Drain-to-source voltage of the output transistor

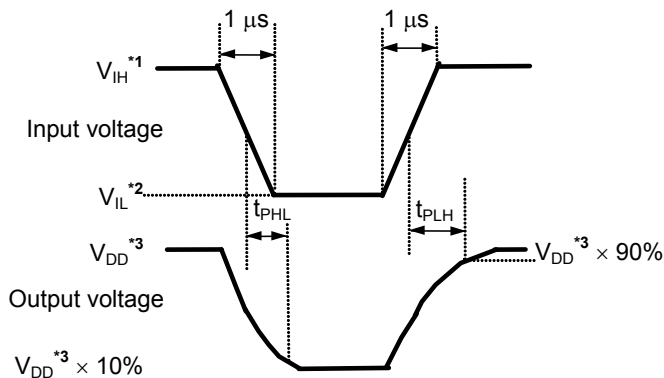
**9. Dynamic response characteristics vs. Output pin capacitance (C<sub>OUT</sub>) (CD pin; open)**

**9.1 -V<sub>DET</sub> = 1.2 V**



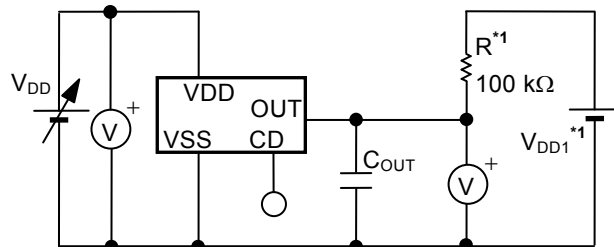
**9.2  $-V_{DET} = 4.6 V$**





- \*1.  $V_{IH} = 10\text{ V}$
- \*2.  $V_{IL} = 0.8\text{ V}$
- \*3. CMOS output product:  $V_{DD}$   
 Nch open-drain product:  $V_{DD1}$

Figure 22 Test Condition of Response Time

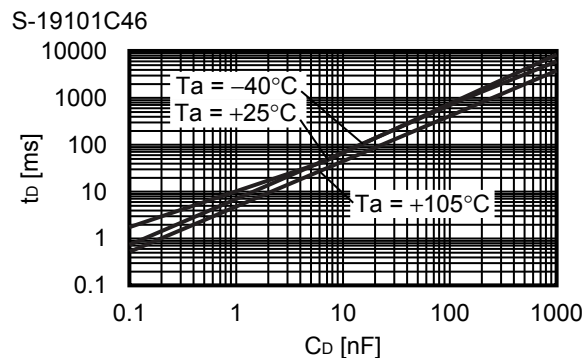
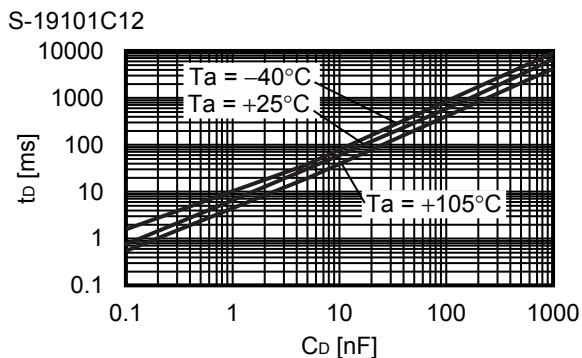


- \*1. R and  $V_{DD1}$  are unnecessary for CMOS output product.

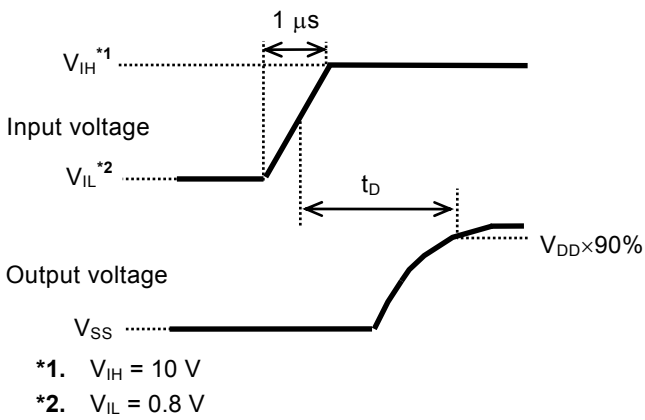
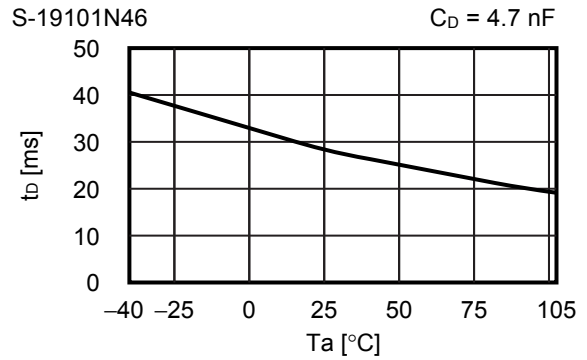
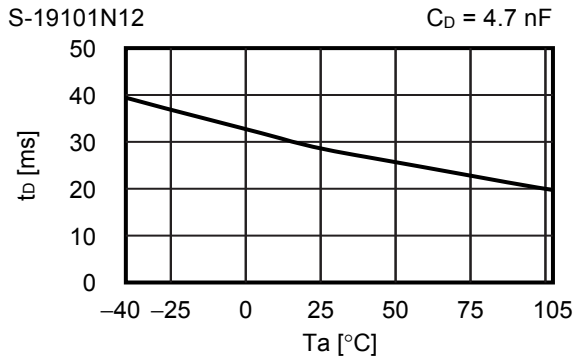
Figure 23 Test Circuit of Response Time

- Caution**
1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
  2. When the CD pin is open, a double pulse may appear at release. To avoid the double pulse, attach 100 pF or more capacitor to the CD pin. Response time when detecting ( $t_{PHL}$ ) is not affected by CD pin capacitance. Besides, response time when releasing ( $t_{PLH}$ ) can be set the delay time by attaching the CD pin. Refer to "10. Delay time ( $t_D$ ) vs. CD pin capacitance ( $C_D$ ) (without output pin capacitance) for details.

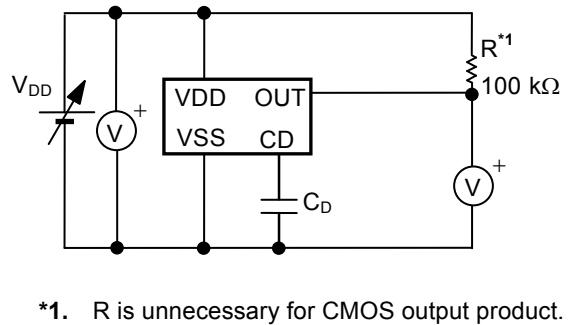
**10. Delay time ( $t_D$ ) vs. CD pin capacitance ( $C_D$ ) (without output pin capacitance)**



**11. Delay time ( $t_D$ ) vs. Temperature ( $T_a$ )**



**Figure 24 Test Condition of Delay Time**

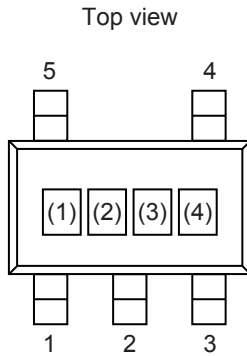


**Figure 25 Test Circuit of Delay Time**

**Caution** The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

## ■ Marking Specifications

### 1. SOT-23-5



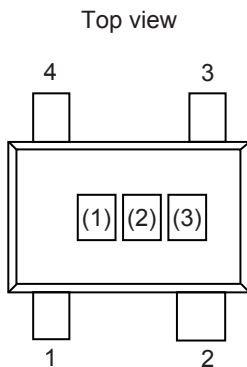
(1) to (3): Product code (Refer to **Product name vs. Product code**)  
 (4): Lot number

#### Product name vs. Product code

##### 1.1 CMOS output product

Product Name	Product Code		
	(1)	(2)	(3)
S-19101C25H-M5T2U	3	Q	A
S-19101C26H-M5T2U	3	Q	B
S-19101C27H-M5T2U	3	Q	C
S-19101C28H-M5T2U	3	Q	K

### 2. SC-82AB



(1) to (3): Product code (Refer to **Product name vs. Product code**)

#### Product name vs. Product code

##### 2.1 CMOS output product

Product Name	Product Code		
	(1)	(2)	(3)
S-19101C25H-N4T2U	3	Q	A
S-19101C26H-N4T2U	3	Q	B
S-19101C27H-N4T2U	3	Q	C
S-19101C28H-N4T2U	3	Q	K



No. MP005-A-P-SD-1.3

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	





Feed direction →

No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
<b>ABLIC Inc.</b>			



No. NP004-A-P-SD-2.0

TITLE	SC82AB-A-PKG Dimensions
No.	NP004-A-P-SD-2.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



No. NP004-A-C-SD-3.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-SD-3.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



→  
Feed direction

No. NP004-A-C-S1-2.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-S1-2.0
ANGLE	
UNIT	mm

**ABLIC Inc.**



Enlarged drawing in the central part



No. NP004-A-R-SD-1.1

TITLE	SC82AB-A-Reel		
No.	NP004-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
<b>ABLIC Inc.</b>			

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2.2-2018.06