S-19989 Series

AUTOMOTIVE, 125°C OPERATION, 36 V INPUT, START-STOP STEP-UP SWITCHING REGULATOR CONTROLLER

www.ablic.com

Rev.1.3_00

This IC is a step-up switching regulator controller developed using high withstand voltage CMOS process technologies.
It is suitable for automotive start-stop systems and emergency battery backup systems due to its wide input operating range of 3.0 V to 36 V and the capacity to extend the input voltage below the operating input voltage range after startup.
This IC enters a low current consumption sleep mode when the output voltages are equal to or higher than the sleep voltage, and it starts switching operation when the output voltage drops below the wake-up voltage.
This IC contributes to system space saving as it adopted suitable packages for high-density mounting like small-sized HSNT-8(2030), can operate at very high switching frequencies, and the peripheral parts can be made compact.
An overcurrent protection circuit protects the IC and the coil from excessive load current, and a thermal shutdown circuit prevents damage from heat generation.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.

■ Features

- Input voltage: 3.0 V to 36.0 V
- Low voltage operation after startup
- Wake-up voltage triggers auto startup
- Control system: Current mode
- Output regulation voltage: 6.80 V, 8.50 V
- Output regulation voltage accuracy: ±2.0%
- Oscillation frequency: 2.2 MHz typ., 400 kHz typ.
- Overcurrent protection function: Pulse-by-pulse method
- Thermal shutdown function: 170°C typ. (detection temperature)
- Short-circuit protection function: Hiccup control
- Under voltage lockout function (UVLO): 2.75 V typ. (detection voltage)
- Input and output capacitors: Ceramic capacitor compatible
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified*1

■ Applications

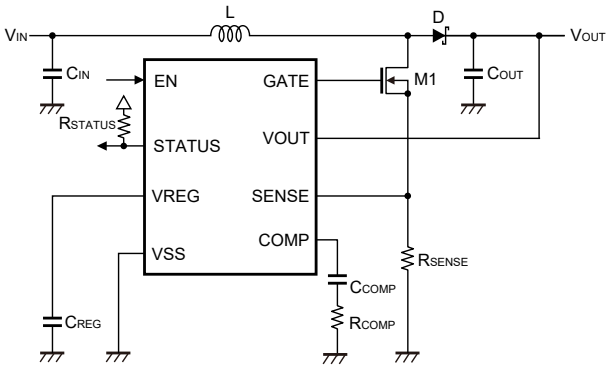
- Automotive and industrial step-up
- Automotive start-stop systems
- Emergency battery backup systems
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

■ Packages

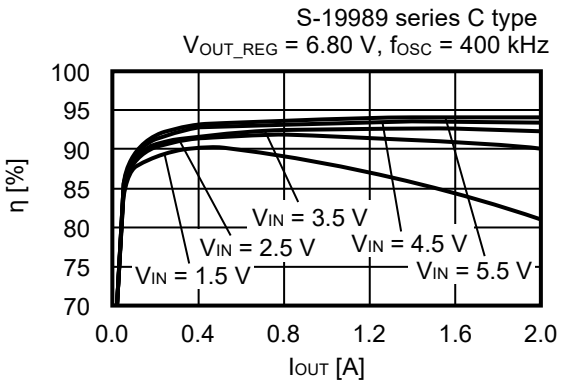
- HTMSOP-8
  (4.0 mm × 2.9 mm × t0.8 mm max.)
- HSNT-8(2030)
  (3.0 mm × 2.0 mm × t0.5 mm max.)

***1.** Contact our sales representatives for details.

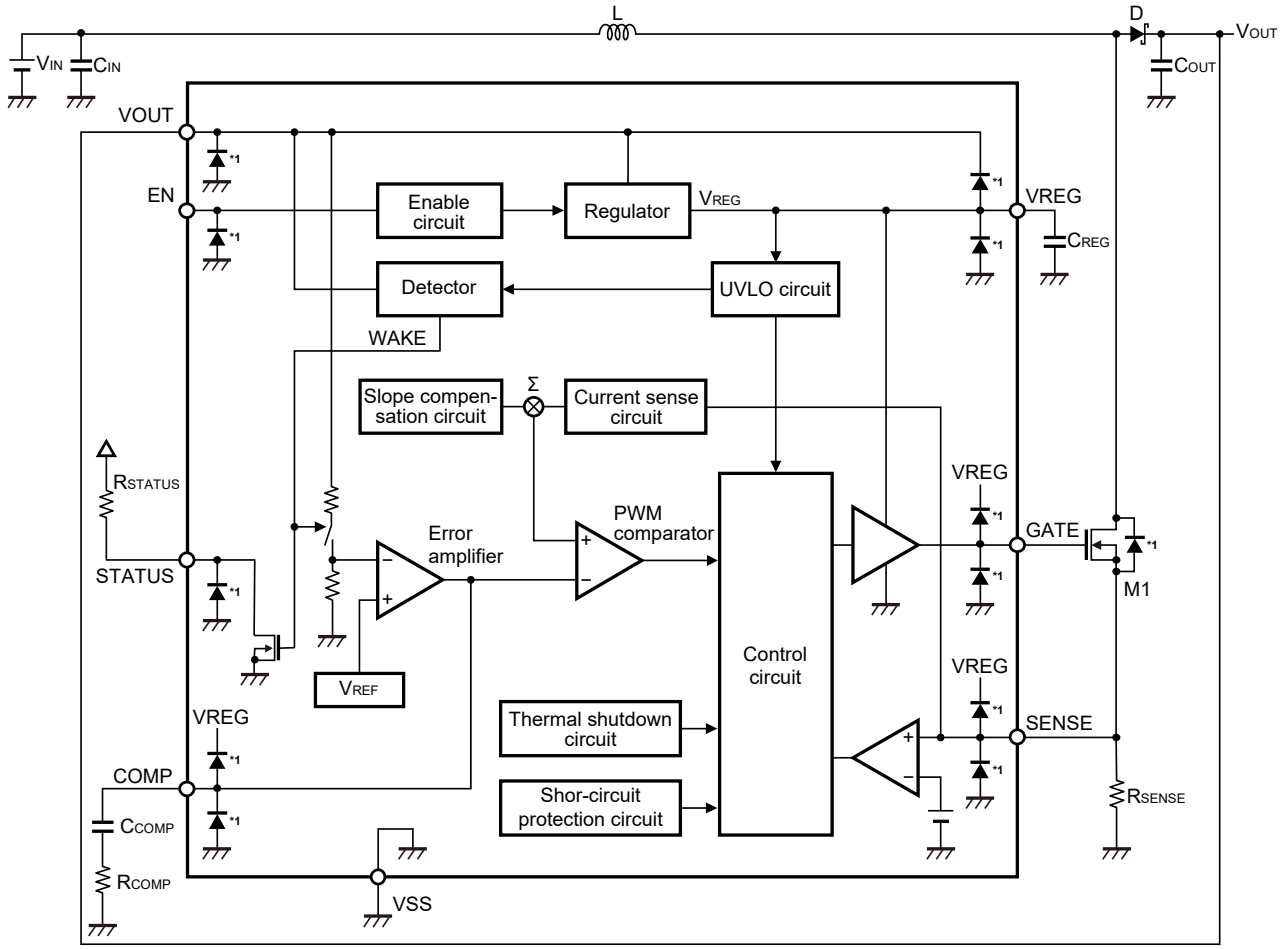
■ Typical Application Circuit



■ Efficiency



■ Block Diagram



***1.** Parasitic diode

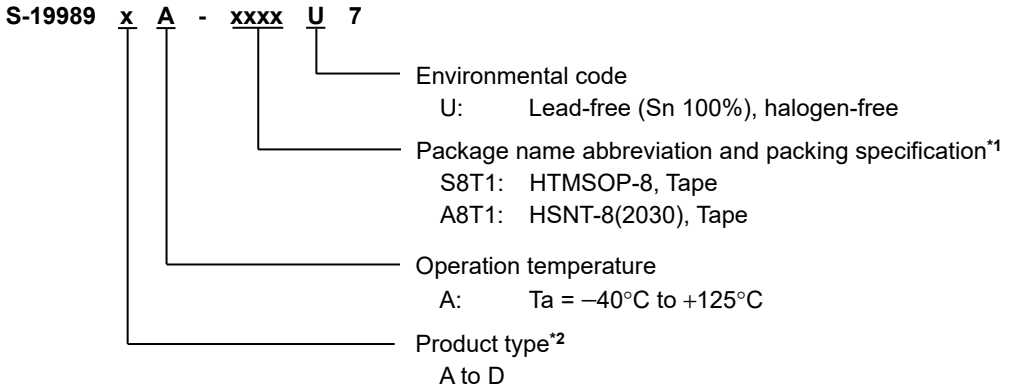
Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** Refer to "**2. Function list of product types**".

2. Function list of product types

Table 1

Product Type	Oscillation Frequency	Short-circuit Protection Function	Output Regulation Voltage (V_{OUT_REG})	Wake-up Voltage (V_{WAKEUP})	Sleep Voltage (V_{SLEEP})
A	2.2 MHz	Hiccup control	6.80 V	7.30 V	7.70 V
B	2.2 MHz	Hiccup control	8.50 V	9.11 V	9.62 V
C	400 kHz	Hiccup control	6.80 V	7.30 V	7.70 V
D	400 kHz	Hiccup control	8.50 V	9.11 V	9.62 V

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land	Stencil Opening
HTMSOP-8	FP008-A-P-SD	FP008-A-C-SD	FP008-A-R-SD	FP008-A-L-SD	–
HSNT-8(2030)	PP008-A-P-SD	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD	PP008-A-L-S1

■ Pin Configurations

1. HTMSOP-8

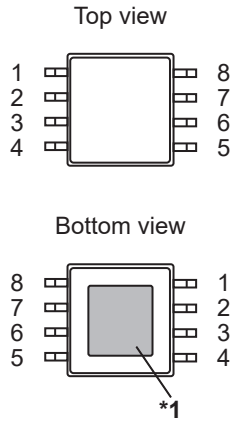


Figure 2

Table 3

Pin No.	Symbol	Description
1	EN	Enable pin
2	COMP	Error amplifier circuit output pin
3	STATUS	STATUS pin
4	VOUT	Power supply pin, Output voltage monitor pin
5	VREG*2	Internal power supply pin
6	GATE	Gate drive output pin
7	VSS	GND pin
8	SENSE	Current detection input pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.
***2.** The VREG pin cannot supply load current outside.

2. HSNT-8(2030)

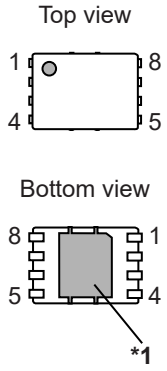


Figure 3

Table 4

Pin No.	Symbol	Description
1	EN	Enable pin
2	COMP	Error amplifier circuit output pin
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4	VOUT	Power supply pin, Output voltage monitor pin
5	VREG*2	Internal power supply pin
6	GATE	Gate drive output pin
7	VSS	GND pin
8	SENSE	Current detection input pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.
***2.** The VREG pin cannot supply load current outside.

■ Absolute Maximum Ratings

Table 5

(Unless otherwise specified: Ta = +25°C, V_{SS} = 0 V)

Item	Symbol	Absolute Maximum Ratings	Unit
VOUT pin voltage	V_{OUT}	V_{SS} – 0.3 to V_{SS} + 45	V
EN pin voltage	V_{EN}	V_{SS} – 0.3 to V_{SS} + 45	V
STATUS pin voltage	V_{STATUS}	V_{SS} – 0.3 to V_{REG} + 0.3 ≤ V_{SS} + 6.0	V
VREG pin voltage	V_{REG}	V_{SS} – 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 6.0	V
GATE pin voltage	V_{GATE}	V_{SS} – 0.3 to V_{REG} + 0.3 ≤ V_{SS} + 6.0	V
COMP pin voltage	V_{COMP}	V_{SS} – 0.3 to V_{REG} + 0.3 ≤ V_{SS} + 6.0	V
SENSE pin voltage	V_{SENSE}	V_{SS} – 0.3 to V_{REG} + 0.3 ≤ V_{SS} + 6.0	V
Junction temperature	T_j	−40 to +150	°C
Operation ambient temperature	T_{opr}	−40 to +125	°C
Storage temperature	T_{stg}	−40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	HTMSOP-8	Board A	–	159	–	°C/W
			Board B	–	113	–	°C/W
			Board C	–	39	–	°C/W
			Board D	–	40	–	°C/W
			Board E	–	30	–	°C/W
		HSNT-8(2030)	Board A	–	181	–	°C/W
			Board B	–	135	–	°C/W
			Board C	–	40	–	°C/W
			Board D	–	42	–	°C/W
			Board E	–	32	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 7

(A / C type: $V_{OUT} = V_{WAKEUP} - 0.9$ V, B / D type: $V_{OUT} = V_{WAKEUP} - 1.21$ V, $T_j = -40$°C to +150°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Operating input voltage	V_{OUT}	–		3.0	–	36.0	V
Current consumption during shutdown	I_{SSS}	V_{OUT} = 12 V, V_{EN} = 0 V		–	0.1	5.0	μA
Current consumption during switching off	I_{SS}	$V_{OUT} = V_{WAKEUP} \times 0.95$, V_{EN} = 12 V, when switching operation is off		–	70	120	μA
Current consumption during sleep mode	I_{SLEEP}	$V_{OUT} = V_{EN}$ = 12 V		–	60	120	μA
UVLO detection voltage	V_{UVLO-}	VREG pin voltage		2.55	2.75	2.95	V
UVLO release voltage	V_{UVLO+}	VREG pin voltage		2.65	2.85	3.05	V
Output regulation voltage	V_{OUT_REG}	A / C type		6.66	6.80	6.94	V
		B / D type		8.33	8.50	8.67	V
Wake-up voltage	V_{WAKEUP}	V_{OUT} falling	A / C type	6.89	7.30	7.71	V
			B / D type	8.64	9.11	9.58	V
Sleep voltage	V_{SLEEP}	V_{OUT} rising	A / C type	7.27	7.70	8.13	V
			B / D type	9.13	9.62	10.11	V
Error amplifier transconductance	gm	–		–	220	–	μS
Oscillation frequency	f_{OSC}	A / B type		1.98	2.2	2.42	MHz
		C / D type		360	400	440	kHz
Minimum ON time	t_{ON_MIN}	–		–	45	–	ns
Maximum duty ratio	MaxDuty	A / B type		82	88	94	%
		C / D type		91	95	99	%
GATE pin ON-resistance	R_{ONH}	Output is "H", I_{GATE} = 50 mA		–	1.5	3.0	Ω
	R_{ONL}	Output is "L", I_{GATE} = –50 mA		–	1.0	2.0	Ω
Overcurrent protection detection voltage	V_{LIM}	–		0.128	0.14	0.152	V
VREG pin output voltage	V_{REG}	–		–	5.0	–	V
STATUS pin pull-down capability	V_{STA}	I_{STATUS} = 1 mA		20	60	200	mV
STATUS pin fall delay time	t_{STA_DLY}	R_{STATUS} = 100 kΩ		0.5	2.5	12.5	μs
Thermal shutdown detection temperature	T_{SD}	Junction temperature		–	170	–	°C
Thermal shutdown release temperature	T_{SR}	Junction temperature		–	150	–	°C
High level input voltage	V_{SH}	EN pin		2.0	–	–	V
Low level input voltage	V_{SL}	EN pin		–	–	0.8	V
High level input current	I_{SH}	EN pin, V_{EN} = 2.0 V		–	–	1	μA
Low level input current	I_{SL}	EN pin, V_{EN} = 0 V		–0.5	–	0.5	μA

■ Operation

1. Overview of operation

This IC monitors the output voltage (V_{OUT}), and if it reaches the wake-up voltage (V_{WAKEUP}) or higher, it operates in sleep mode.
When the V_{OUT} drops below V_{WAKEUP}, a step-up operation is triggered to maintain the output regulation voltage (V_{OUT_REG}).
After the V_{OUT} stops falling and starts to rise, a step-up operation stops when the V_{OUT} exceeds V_{OUT_REG}. In addition, the sleep mode is resumed when the V_{OUT} exceeds the sleep voltage (V_{SLEEP}). Refer to **Figure 4**.
The VOUT pin powers the IC, monitors the voltage and provides feedback. A feedback resistor is integrated into the IC. In sleep mode, the current consumption is reduced by blocking the current of the feedback resistor.
This IC adopts current mode control. GATE pin duty ratio is determined by comparing the current feedback signal, which is the current flowing through the SENSE resistor plus slope compensation, with the output signal of the error amplifier circuit. The configured negative feedback loop regulates the error amplifier output signal to a voltage at which the internal reference voltage (V_{REF}) equals the feedback voltage from the VOUT pin. This maintains the constant output voltage.

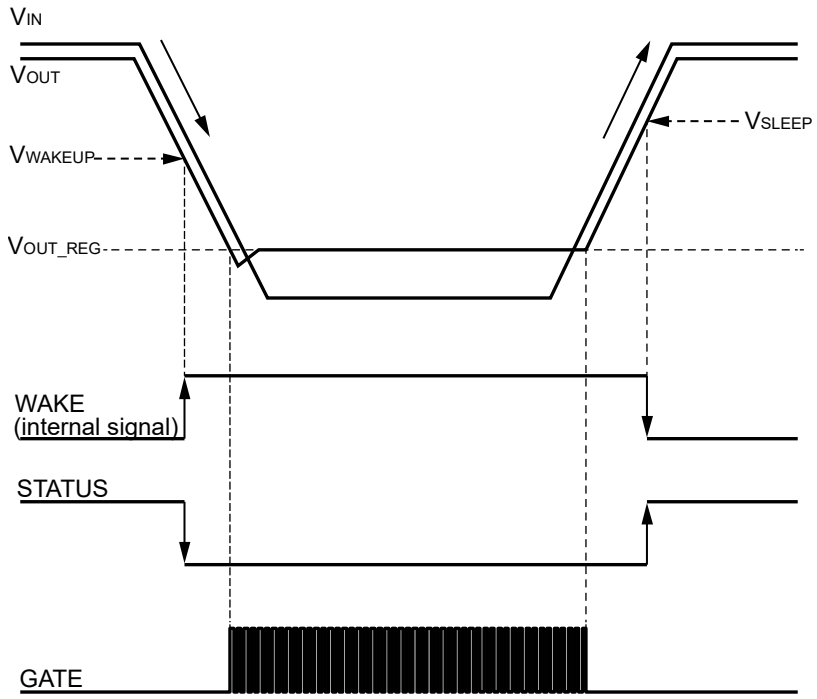
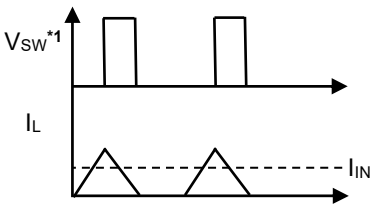


Figure 4

2. Inductor current operating mode

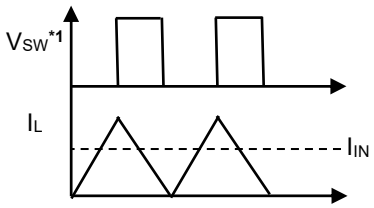
In converters that use diodes as rectifier elements, the inductor current (I_L) shifts between Discontinuous Current Mode (DCM) and Continuous Current Mode (CCM), depending on the load current (I_{OUT}).
The I_{OUT} when the inductor current is exactly zero during the switching cycle is the boundary mode between the discontinuous and continuous current modes. The I_{OUT} at this time is shown below. For details, refer to **Figure 5** to **Figure 7**.

$$I_{OUT} = \frac{V_{IN}^2}{2 \times L \times V_{OUT}}\left(1 - \frac{V_{IN}}{V_{OUT}}\right)T$$



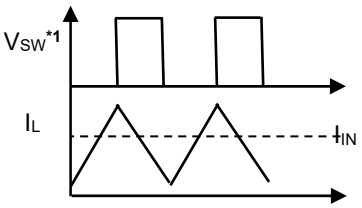
Discontinuous current mode

Figure 5



Boundary mode

Figure 6



Continuous Current Mode

Figure 7

***1.** V_{SW} is the voltage at the point (switching node) where the step-up switching regulator circuit, FET, and diode are connected, which is a square wave.

The duty cycle (D_{dcm}) in discontinuous current mode operation is shown in the equation below. D_{dcm} varies significantly with load changes.

$$D_{dcm} = \frac{\sqrt{2 \times L \times I_{OUT} \times (V_{OUT} + V_F - V_{IN}) \times f_{OSC}}}{V_{IN}}$$

And the duty cycle (D_{ccm}) in continuous current mode operation is shown in the equation below. The input and output voltages determine D_{ccm}.

$$D_{ccm} = 1 - \frac{V_{IN}}{V_{OUT} + V_F}$$

Remark	L:	Inductor [H]
	I_{OUT}:	Load current [A]
	V_{IN}:	Input voltage [V]
	V_{OUT}:	Output voltage [V]
	V_F:	Diode forward voltage [V]
	f_{OSC}:	Oscillation frequency [Hz]
	T:	Period [s]

3. Minimum ON time

When the external FET M1 in **Figure 1** on "■ **Block Diagram",** is turned on, this IC starts switching at high-speed generating high-frequency spike noise in the inductor current detection resistor (R_{SENSE}). Normally, a slope voltage proportional to the inductor current value is input to the SENSE pin, and the IC's internal latch circuit is reset to the desired voltage value. If there is any spike noise, the occurrence of the noise will reset the latch incorrectly. To prevent such malfunctions, a blank time is set so that a reset is not triggered even if M1 is turned on. This blank time is defined as the minimum ON time (t_{ON_MIN}).

4. PWM / PFM switching control

This IC automatically switches between pulse width modulation method (PWM) and pulse frequency modulation method (PFM) according to the load current. PFM control is selected when under light load, and the pulse will skip according to the load current. Pulse skips will occur when the following conditions are met.

$$D_{dcm} < t_{ON\_MIN} \times f_{OSC}$$

Pulse skipping reduces self-current consumption and improves efficiency at light loads.

5. Under voltage lockout function (UVLO)

This IC has a built-in UVLO circuit to prevent the IC from malfunctioning due to a transient status at power-on or a momentary drop in the supply voltage. When UVLO status is detected, the GATE pin is pulled down. For this reason, switching operation will stop.
Note that the other internal circuits operate normally, and the status is different from the disabled status.
Also, there is a hysteresis width for avoiding malfunctions due to generation of noise etc. in the input voltage.

6. EN pin

This pin starts and stops switching operation. When the EN pin is set to "L", the operation of all internal circuits is stopped, reducing current consumption. When not using the EN pin, connect it to the VOUT pin. Since the EN pin is neither pulled down nor pulled up internally, do not use it in the floating status. The structure of the EN pin is shown in **Figure 8**, and the clamp circuit is internally connected.

Table 8

EN Pin	Internal Circuit	GATE
"H"	Enable (normal operation)	Switching operation
"L"	Disable (standby)	Pulled down to V_{SS}

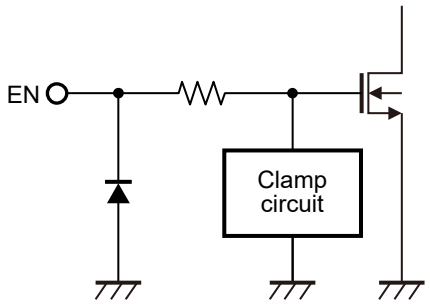


Figure 8

7. Thermal shutdown function

This IC has a built-in thermal shutdown circuit to limit overheating. When the junction temperature increases to 170°C typ., the thermal shutdown circuit becomes the detection status, and the switching operation is stopped. When the junction temperature decreases to 150°C typ., the thermal shutdown circuit becomes the release status, and the switching operation is restarted.

If the thermal shutdown circuit becomes the detection status due to self-heating, the switching operation is stopped and output voltage (V_{OUT}) decreases. For this reason, the self-heating is limited and the temperature of the IC decreases. The thermal shutdown circuit becomes release status when the temperature of the IC decreases, and the switching operation is restarted, thus the self-heating is generated again. Repeating this procedure makes the waveform of V_{OUT} into a pulse-like form. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously. Switching operation stopping and starting can be stopped by either setting the EN pin to "L", lowering the output current (I_{OUT}) to reduce internal power consumption, or decreasing the ambient temperature.

Table 9

Thermal Shutdown Circuit	GATE
Release: 150°C typ.*1	Switching operation
Detection: 170°C typ.*1	Pulled down to V_{SS}

***1.** Junction temperature

8. Overcurrent protection function

The overcurrent protection circuit provides FET overcurrent protection using the voltage generated by the R_{SENSE} connected in series with the N-channel power MOS FET to prevent thermal destruction of the IC due to an overload, magnetic saturation in the inductor, etc.

When overcurrent flows through the N-channel power MOS FET and the potential difference between the SENSE pin and GND exceeds the overcurrent protection detection voltage (V_{LIM}) (0.14 V typ.), the N-channel power MOS FET is turned off. It is turned back on when the next switching cycle starts. If the potential difference between the SENSE pin and GND remains above V_{LIM}, the N-channel power MOS FET is turned off again, and this sequence of operations is repeated.

However, when the current flowing through the N-channel power MOS FET decreases and the potential difference between the SENSE pin and GND drops below V_{LIM}, the IC returns to normal operation.

If the slope of the inductor current is large, the delay time of the overcurrent protection circuit may cause an apparent increase in the potential difference between the SENSE pin and GND. This tends to occur when an inductor with low inductance is used or when V_{IN} is large.

9. Short-circuit protection function

This IC has a built-in short-circuit protection function for Hiccup control.
The hiccup control is a method for periodically carrying out automatic recovery when the IC detects overcurrent and stops the switching operation.

9. 1 When overload status is released

<1> Overcurrent detection
<2> Detection of $V_{OUT} < 62.5\% \times V_{OUT\_REG}$ typ.
<3> 0.3 ms elapse
<4> Switching operation stop (for 21 ms typ.) (short-circuit protection detection status)
<5> Overload status release
<6> The IC restarts.
In this case, it is unnecessary to input an external reset signal for restart.

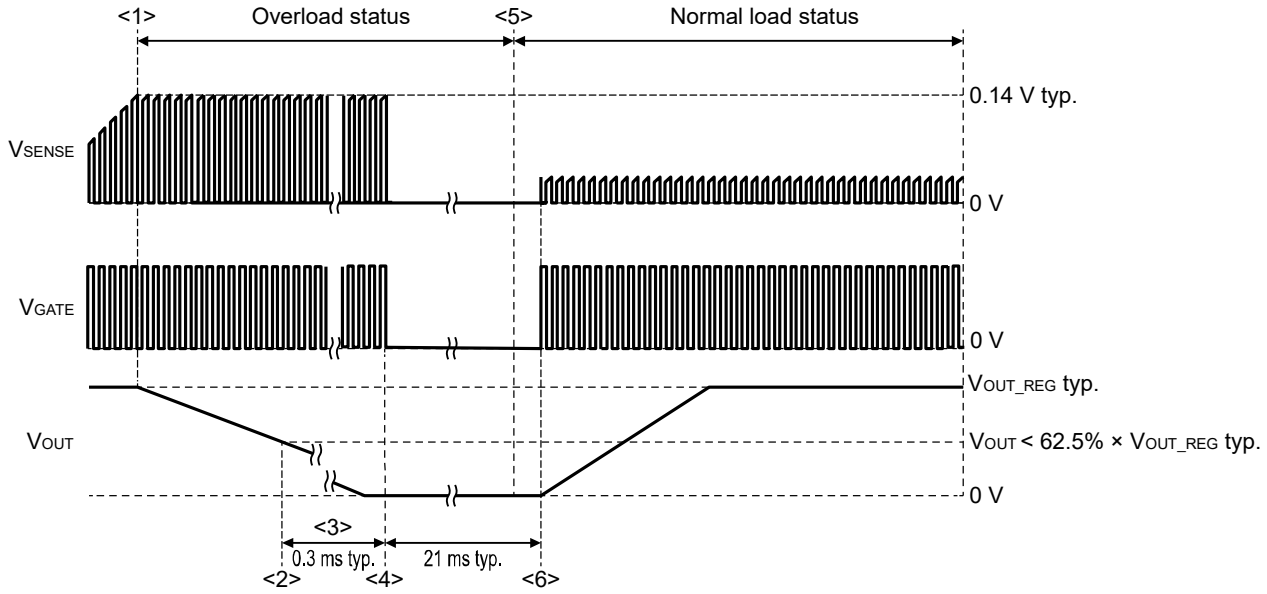


Figure 9

9. 2 When overload status continues

<1> Overcurrent detection
<2> Detection of V_{OUT} < 62.5% × V_{OUT_REG} typ.
<3> 0.3 ms elapse
<4> Switching operation stop (for 21 ms typ.) (short-circuit protection detection status)
<5> The status repeat < 3 > and < 4 > when overload status continues after the IC restarts.

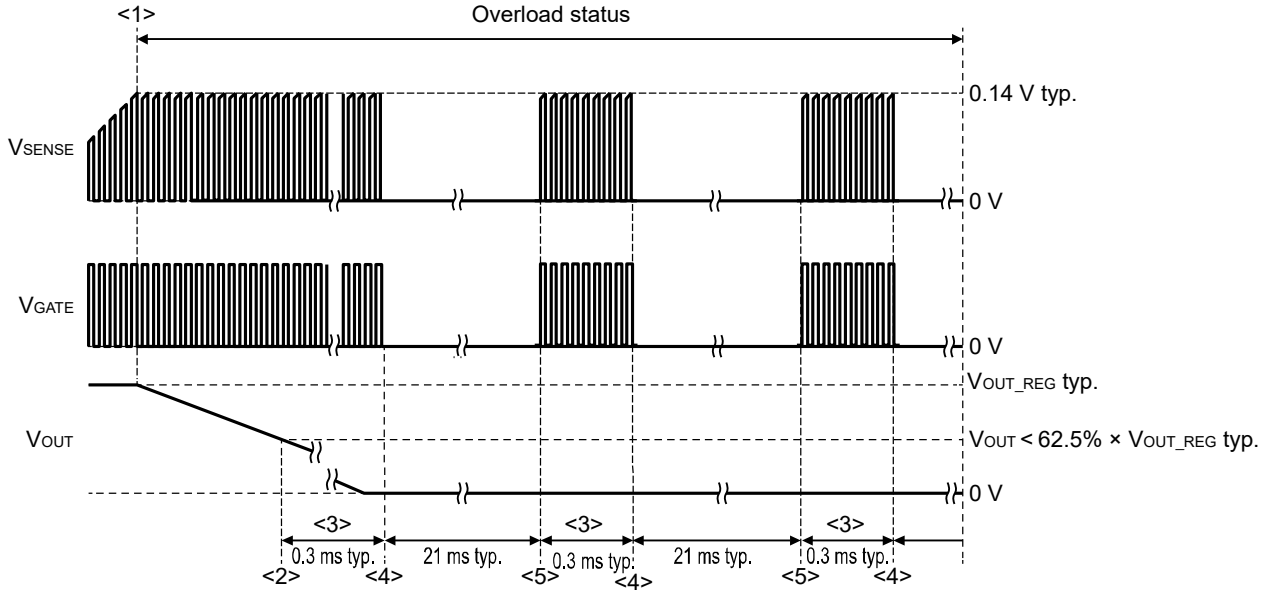


Figure 10

10. Internal power supply (V_{REG})

Some of the circuits in the IC operate using the VREG pin voltage (V_{REG}) as the power supply. To stabilize this internal power supply, a ceramic capacitor with 1 μF needs to be connected between the VREG pin and the VSS pin. To achieve low impedance, this capacitor should be placed as close to the IC as possible. Additionally, note that any external parts other than C_{REG} or any load must not connect to the VREG pin.

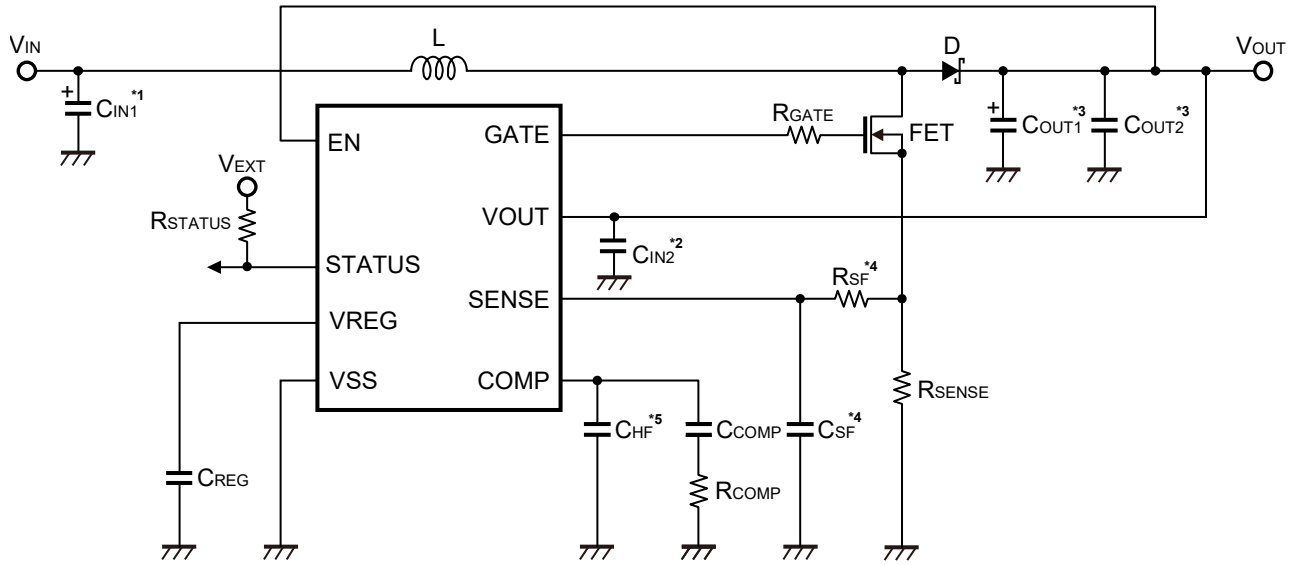
11. STATUS pin

The STATUS pin can output the step-up operation status in this IC by connecting it to a pull-up resistor. When the VOUT pin voltage of this IC is higher than sleep voltage, the Nch MOS FET of the STATUS pin turns off and outputs "H". When the VOUT pin voltage is falls below the wake-up voltage, the Nch MOS FET of the STATUS pin turns on, the STATUS pin is pulled down, and "L" is output. It is also pulled down and outputs "L" when the EN pin is "L" level, UVLO is detected, thermal shutdown is detected.
The STATUS pin is pulled up to external voltage (V_{EXT}) by an external resistor, but make sure that the applied voltage does not exceed absolute maximum ratings. If the STATUS pin output is not to be used, set it to open or connect it to GND.

Table 10

Status		STATUS Pin Output
During operation ($V_{EN} \geq V_{SH}$)	$V_{OUT} \geq V_{SLEEP}$	"H" (High-Z)
	$V_{OUT} \leq V_{WAKEUP}$	"L"
During shutdown operation	$V_{EN} < V_{SL}$	"L"
During UVLO detection	$V_{OUT} < V_{UVLO-}$	"L"
During thermal shutdown detection	$T_j > T_{SD}$	"L"

■ Typical Circuits



***1.** C_{IN1} is a capacitor for stabilizing the input. If operation is unstable, add a capacitor in parallel.
***2.** C_{IN2} is a bypass capacitor for stabilizing the IC operation. Connect it to the area nearest the VOUT pin.
***3.** C_{OUT1} and C_{OUT2} are capacitors for stabilizing the output. If operation is unstable, add a capacitor in parallel.
***4.** R_{SF} and C_{SF} are RC filters to prevent FET switching noise from propagating to the SENSE pin.
***5.** C_{HF} is a high-frequency noise blocking capacitor to prevent malfunctions caused by switching noise.

Figure 11

■ External Parts Selection

Figure 11 shows a typical circuit based on our evaluation. **Table 11** shows its operating conditions and **Table 12** shows its external component constants.
The output voltage (V_{OUT}) during boost operation is set as the output regulation voltage (V_{OUT_REG}) inside the IC, which allows you to set 6.80 V or 8.50 V optionally.
Since this IC supplies the power supply voltage from the converter's output voltage (V_{OUT}) to the IC, even if the input voltage (V_{IN}) becomes lower than the VREG pin output voltage (V_{REG}), V_{REG} is maintained at 5 V, and the FET ON resistance can be reduced.
At a frequency of 2.2 MHz, the FET losses will increase, and the FET may be damaged. Measure FET surface temperature during standard circuit operation to ensure that there is a margin for the maximum junction temperature rating.

Table 11 Design Example

Design parameter	Value
Input voltage (V_{IN})	6 V
Output voltage (V_{OUT})	6.80 V or 8.50 V (Set in the IC)
Load current (I_{LOAD})	2 A
Oscillation frequency (f_{OSC})	2.2 MHz

Table 12 Constants for External Components

Symbol	Value	Quantity	Part Number	Manufacturer
L	0.47 μH	1	SPM5030VT-R47M-D	TDK Corporation
FET	–	1	IPC50N04S5L-5R5	Infineon Technologies
D	–	1	PMEG045V100EPD	Nexperia B.V.
C_{IN1}	33 μF	2	GYC1H330MCQ1GS	NICHICON CORPORATION
C_{IN2}	0.1 μF	1	CGA4J2X8R1H104K	TDK Corporation
C_{OUT1}	100 μF	3	GYC1H101MCQ1GS	NICHICON CORPORATION
C_{OUT2}	10 μF	1	CGA5L1X7R1H106K	TDK Corporation
R_{GATE}	10 Ω	1	MCR3 series (1608)	ROHM CO., LTD.
R_{SENSE}	4 mΩ	1	TLR2BPDTD4L00F75	KOA CORPORATION
R_{SF}	22 Ω	1	MCR3 series (1608)	ROHM CO., LTD.
R_{STATUS}	100 kΩ	1	MCR3 series (1608)	ROHM CO., LTD.
C_{SF}	10 nF	1	CGA3E2X8R1H103K	TDK Corporation
C_{REG}	1 μF	1	CGA5L3X8R1H105K	TDK Corporation
R_{COMP}	12 kΩ	1	MCR3 series (1608)	ROHM CO., LTD.
C_{COMP}	4.7 nF	1	CGA3E2X8R1H472K	TDK Corporation
C_{HF}	220 pF	1	CGA3E2NP01H221J	TDK Corporation

Caution The connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

■ Board Layout Guidelines

Note the following cautions when determining the board layout for this IC.

- Place C_{IN} (C10) as close to the VOUT pin and the VSS pin as possible. Prioritize the layout of C_{IN}.
- Place C_{REG} (C11) as close to the VREG pin and the VSS pin as possible.
- Make the switching loop composed of C_{OUT} (C13 to C19) → D → FET → R_{SENSE} → C_{OUT} (C13 to C19) as small as possible. This measure effectively reduces inductive high-frequency noise.
- The switching node (SW) wiring area (Dashed line area in "**Figure 12 Reference Board Pattern**") should be as small as possible to reduce high-frequency radiation noise.
- Place R_{SENSE} close to the FET source.

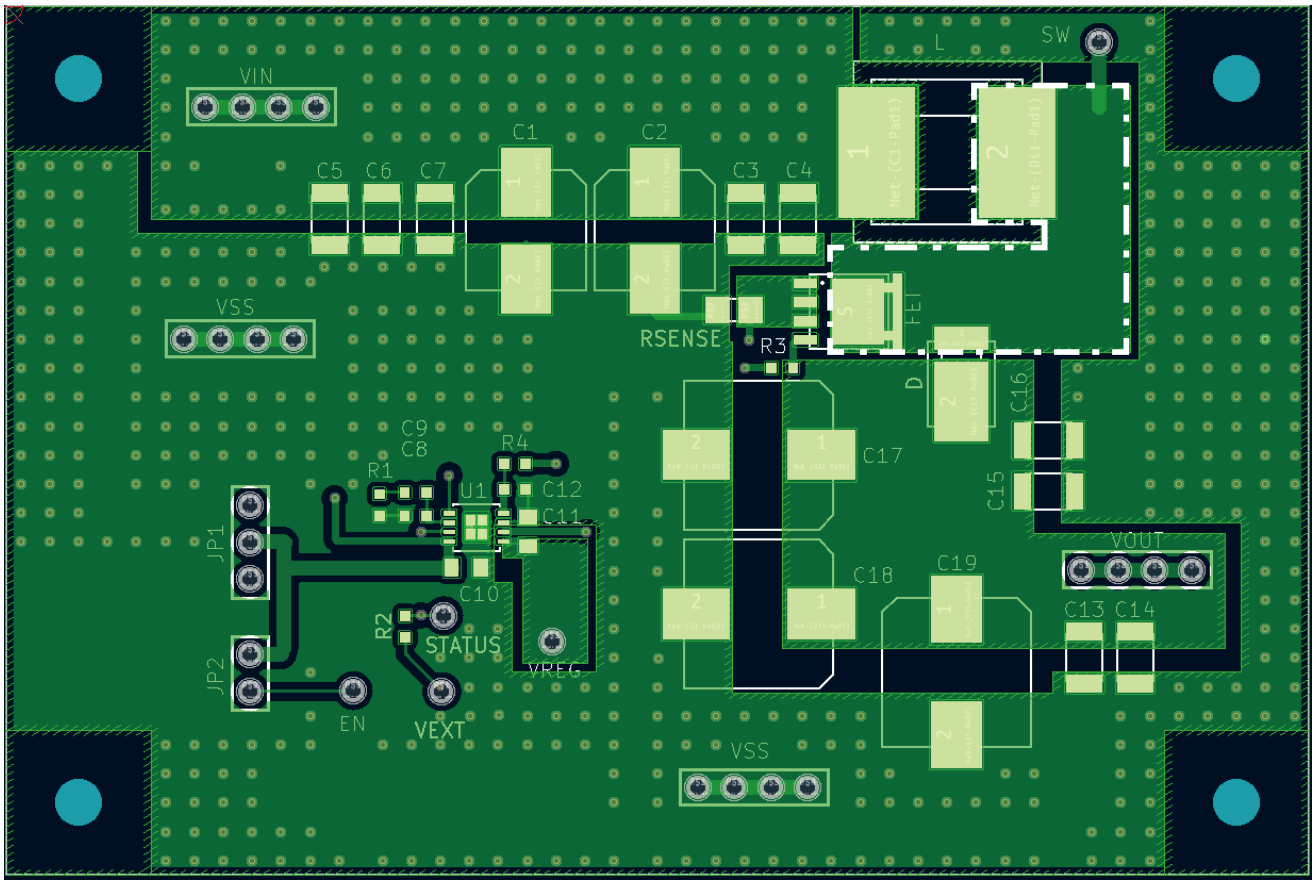


Figure 12 Reference Board Pattern

Caution The above pattern diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to determine the pattern.

■ Related Source

Refer to the following application note for external parts selection and board layout for this IC.

S-19989/19999 Series EXTERNAL PARTS SELECTION Application Note

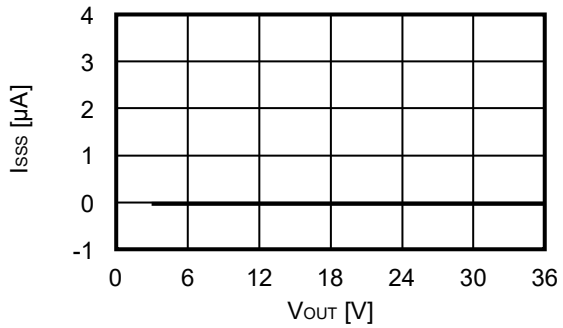
■ Precautions

- Mount external capacitors and inductors as close as possible to the IC, and make single GND.
- Characteristic ripple voltage and spike noise occur in the IC containing switching regulators. Moreover rush current flows at the time of a power supply injection. Because these largely depend on the inductor, the capacitor and impedance of power supply to be used, fully check them using an actually mounted model.
- The 0.1 μF capacitor (C_{IN2} in **Figure 11**) connected between the VOUT pin and the VSS pin of the IC is a bypass capacitor. It stabilizes the power supply in the IC, and thus effectively works for stable switching regulator operation. Allocate the bypass capacitor as close to the IC as possible, prioritized over other parts.
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- The power dissipation of the IC greatly varies depending on the size and material of the board to be connected. Perform sufficient evaluation using an actual application before designing.
- ABLIC Inc. assumes no responsibility for the way in which this IC is used on products created using this IC or for the specifications of that product, nor does ABLIC Inc. assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Japan or in other countries.

■ Characteristics (Typical Data)

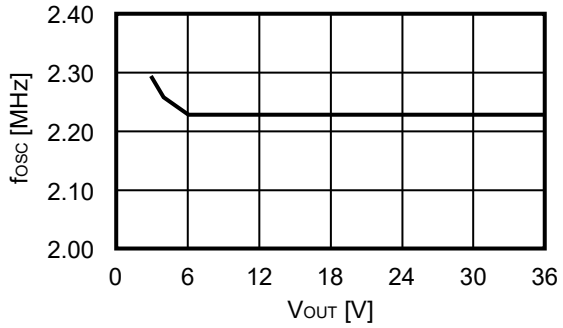
1. Example of major power supply dependence characteristics (Ta = +25°C)

1. 1 Current consumption during shutdown (I_{SSS}) vs. Output voltage (V_{OUT})

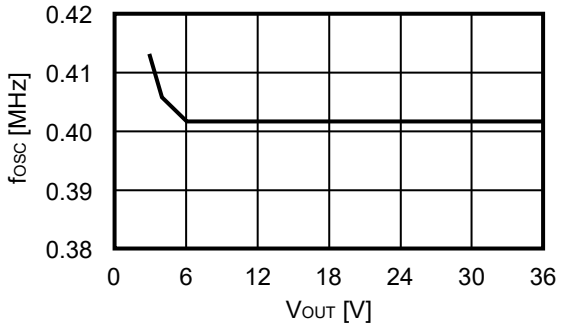


1. 2 Oscillation frequency (f_{OSC}) vs. Output voltage (V_{OUT})

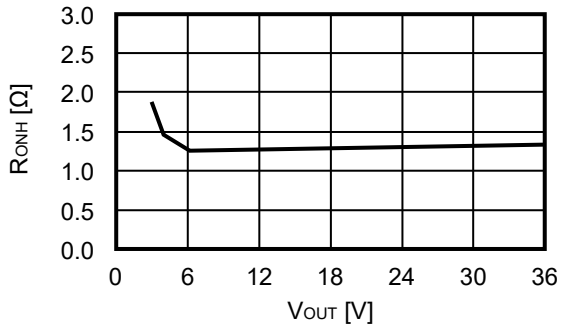
1. 2. 1 S-19989 Series A / B type



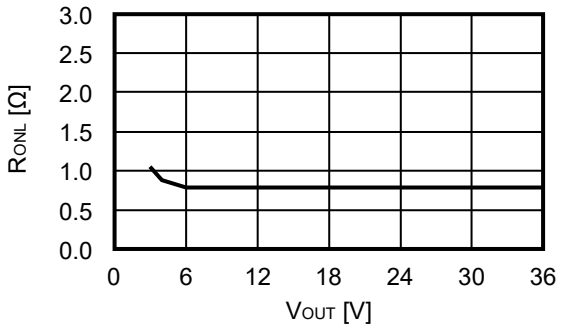
1. 2. 2 S-19989 Series C / D type



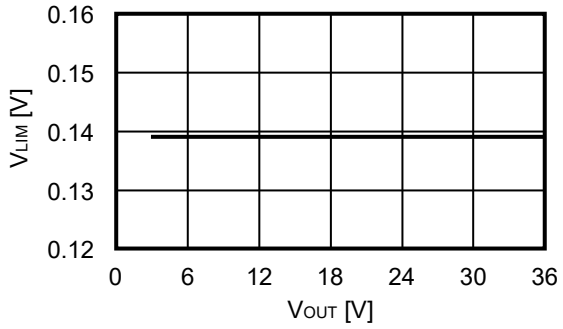
1. 3 GATE pin ON-resistance (R_{ONH}) vs. Output voltage (V_{OUT})



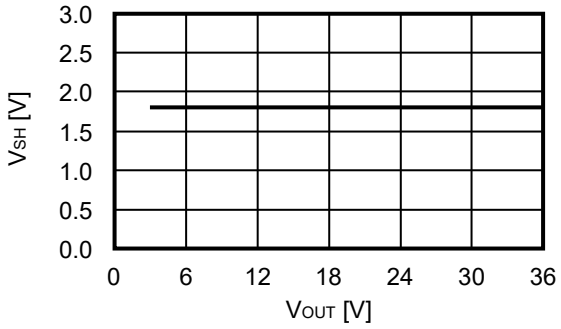
1. 4 GATE pin ON-resistance (R_{ONL}) vs. Output voltage (V_{OUT})



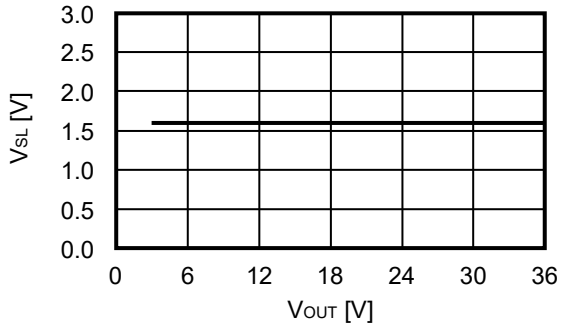
1. 5 Overcurrent protection detection voltage (V_{LIM}) vs. Output voltage (V_{OUT})



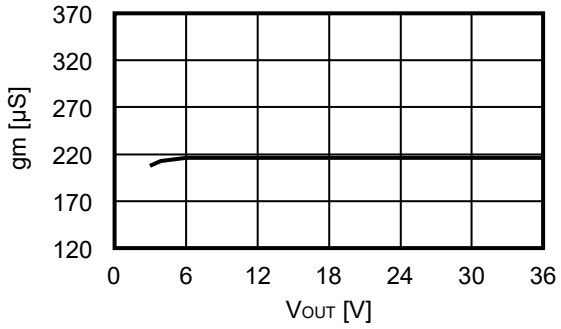
1. 6 High level input voltage (V_{SH}) vs. Output voltage (V_{OUT})



1. 7 Low level input voltage (V_{SL}) vs. Output voltage (V_{OUT})



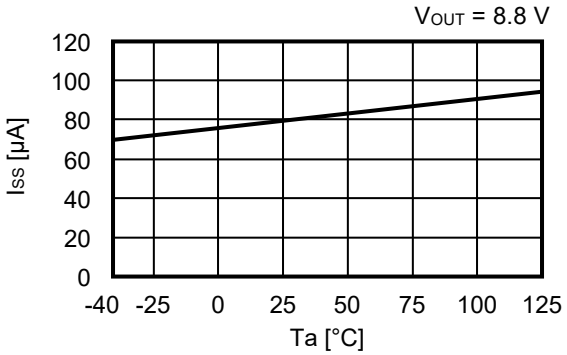
1. 8 Error amplifier transconductance (gm) vs. Output voltage (V_{OUT})



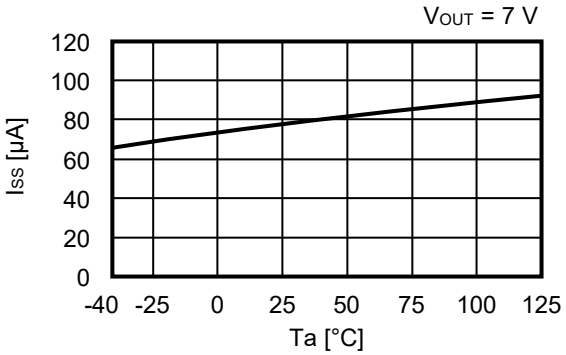
2. Example of major temperature characteristics (Ta = –40°C to +125°C)

2. 1 Current consumption during switching off (I_{SS}) vs. Temperature (Ta)

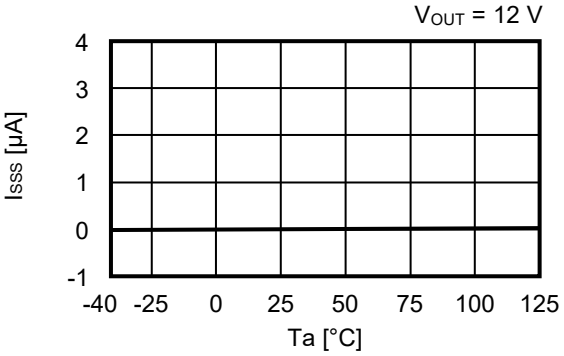
2. 1. 1 S-19989 Series A / B type



2. 1. 2 S-19989 Series C / D type

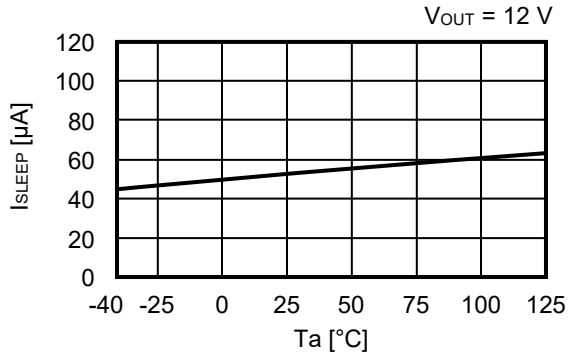


2. 2 Current consumption during shutdown (I_{SSS}) vs. Temperature (Ta)

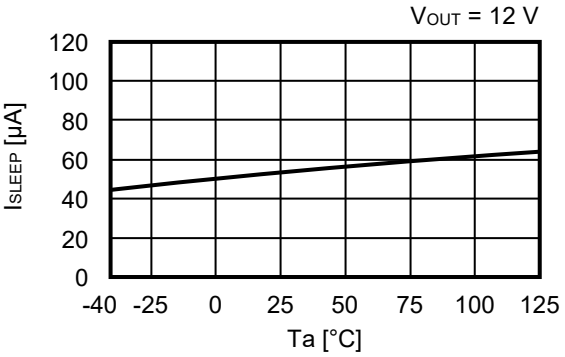


2. 3 Current consumption during sleep mode (I_{SLEEP}) – Temperature (Ta)

2. 3. 1 S-19989 Series A / B type

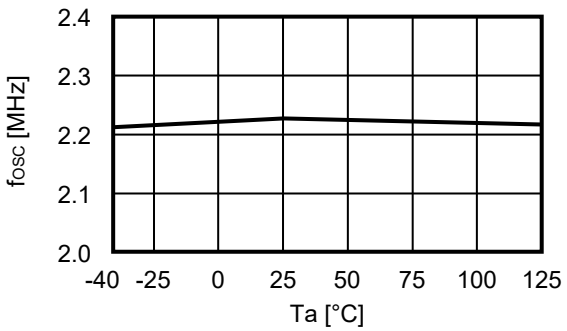


2. 3. 2 S-19989 Series C / D type

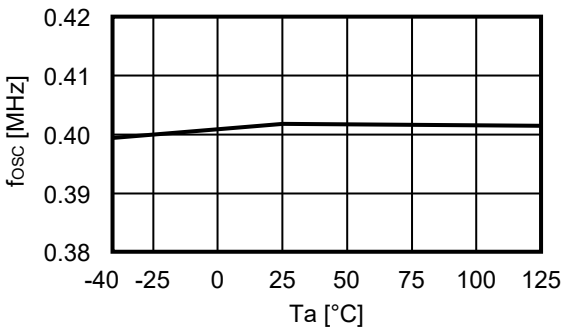


2. 4 Oscillation frequency (f_{OSC}) vs. Temperature (Ta)

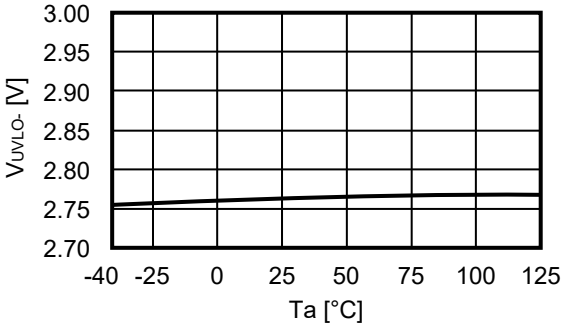
2. 4. 1 S-19989 Series A / B type



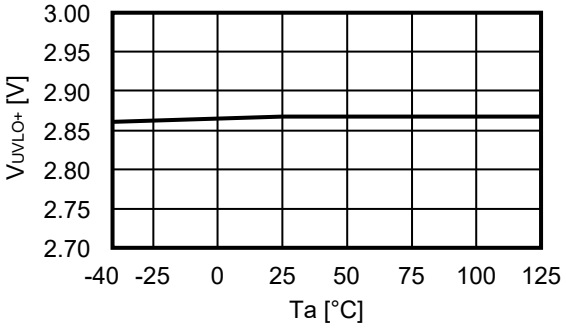
2. 4. 2 S-19989 Series C / D type



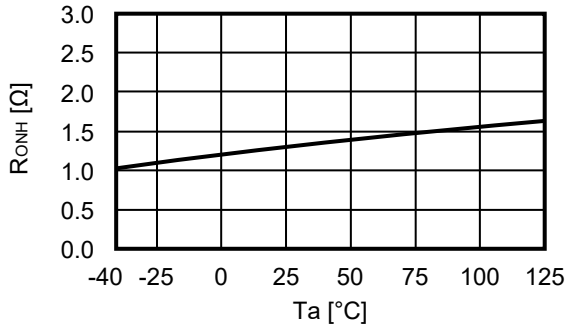
2. 5 UVLO detection voltage (V_{UVLO-}) vs. Temperature (Ta)



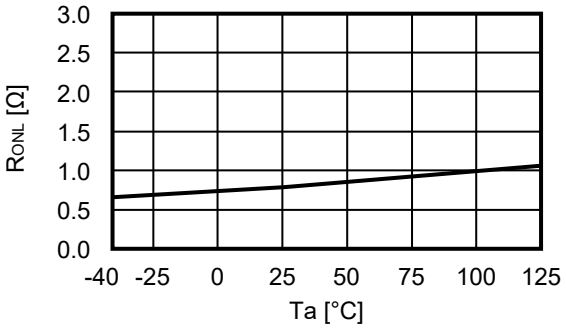
2. 6 UVLO release voltage (V_{UVLO+}) vs. Temperature (Ta)



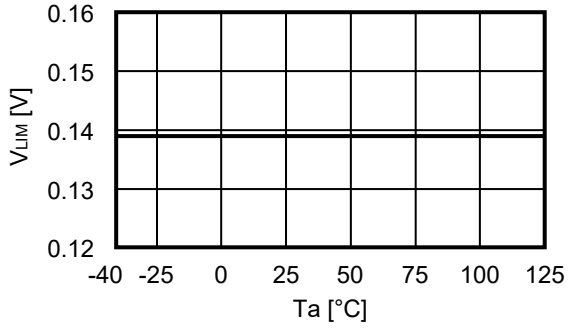
2. 7 GATE pin ON-resistance (R_{ONH}) vs. Temperature (Ta)



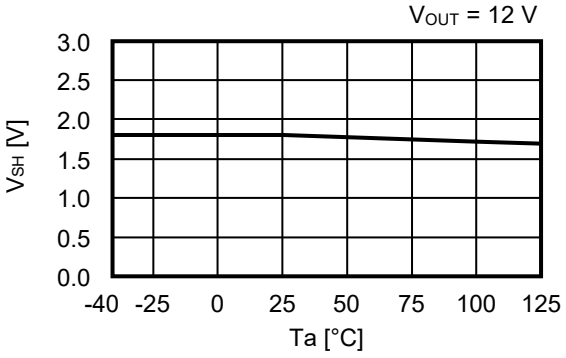
2. 8 GATE pin ON-resistance (R_{ONL}) vs. Temperature (Ta)



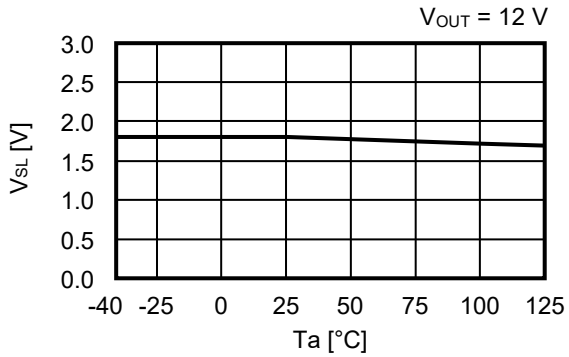
2. 9 Overcurrent protection detection voltage (V_{LIM}) vs. Temperature (Ta)



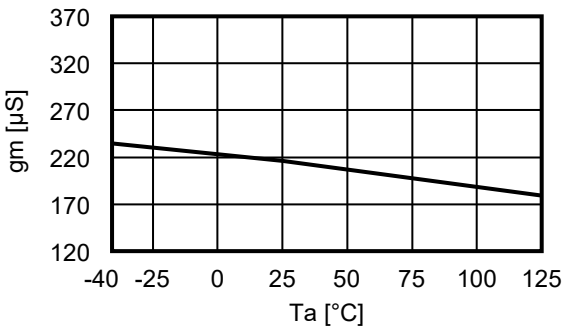
2. 10 High level input voltage (V_{SH}) vs. Temperature (Ta)



2. 11 Low level input voltage (V_{SL}) vs. Temperature (Ta)

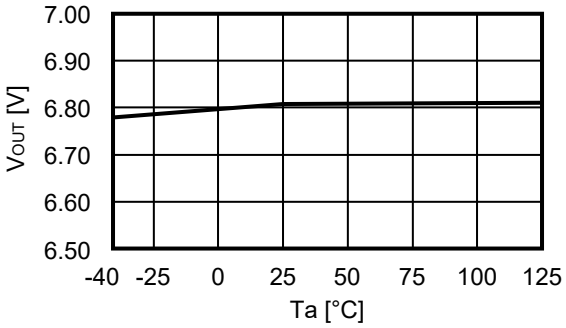


2. 12 Error amplifier transconductance (gm) vs. Temperature (Ta)

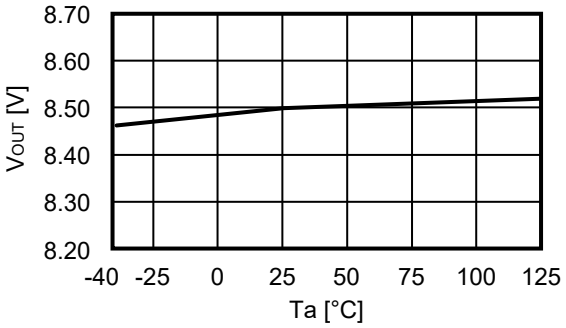


2. 13 Output voltage (V_{OUT}) – Temperature (Ta)

2. 13. 1 S-19989 Series A / C type

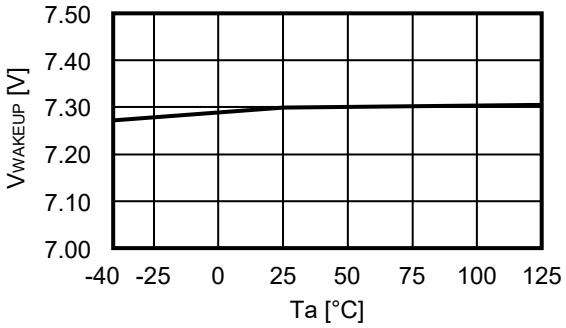


2. 13. 2 S-19989 Series B / D type

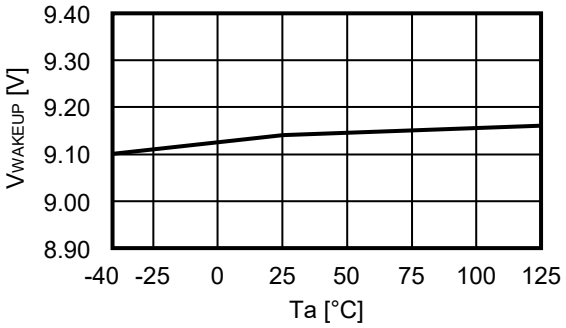


2. 14 Wake-up voltage (V_{WAKEUP}) – Temperature (Ta)

2. 14. 1 S-19989 Series A / C type

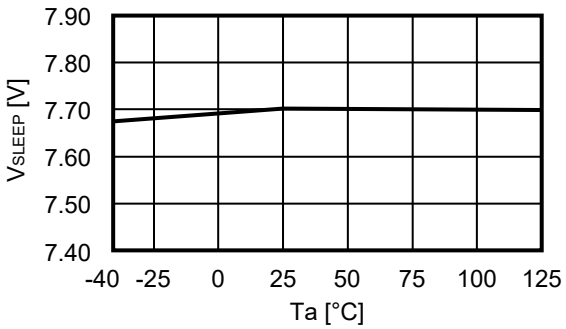


2. 14. 2 S-19989 Series B / D type

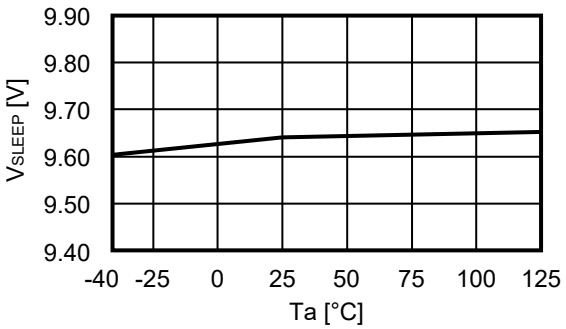


2. 15 Sleep voltage (V_{SLEEP}) – Temperature (Ta)

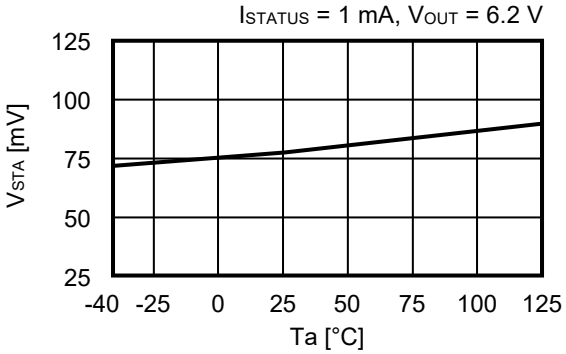
2. 15. 1 S-19989 Series A / C type



2. 15. 2 S-19989 Series B / D type

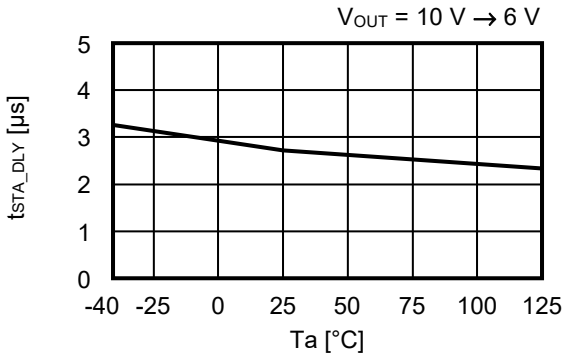


2. 16 STATUS pin pull-down capability (V_{STA}) – Temperature (Ta)

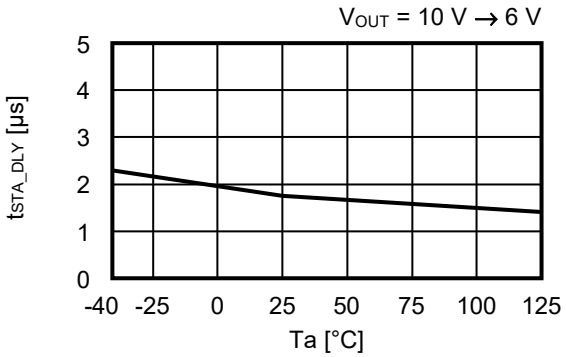


2. 17 STATUS pin fall delay time (t_{STA_DLY}) – Temperature (Ta)

2. 17. 1 S-19989 Series A / C type

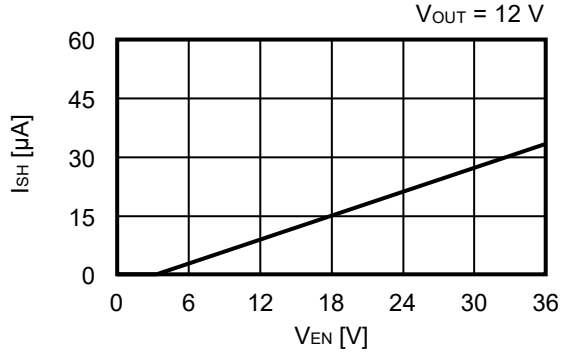


2. 17. 2 S-19989 Series B / D type



3. EN pin characteristics (Ta = +25°C)

3. 1 High level input current (I_{SH}) vs. EN pin voltage (V_{EN})



4. Transient response characteristics

The external parts shown in **Table 13** are used in "**4. Transient response characteristics**".

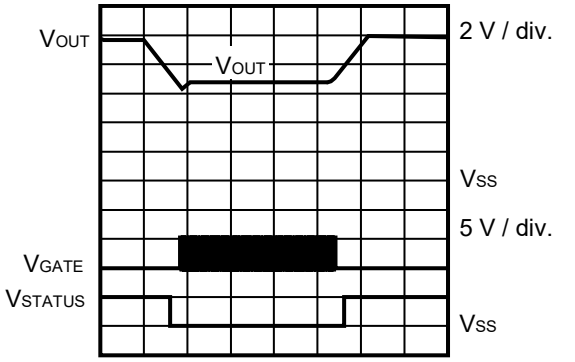
Table 13

Symbol	Value	Part Number	Manufacturer
L	A / B type: 0.47 µH	SPM5030VT-R47M-D	TDK Corporation
	C / D type: 1.5 µH	SPM12565VT-1R5M-D	TDK Corporation
FET	–	IPC50N04S5L-5R5	Infineon Technologies
D	–	PMEG045V100EPD	Nexperia B.V.
C_{IN1}	33 µF	GYC1H330MCQ1GS	NICHICON CORPORATION
C_{IN2}	0.1 µF	CGA4J2X8R1H104K	TDK Corporation
C_{OUT1}	100 µF	GYC1H101MCQ1GS	NICHICON CORPORATION
C_{OUT2}	10 µF	CGA5L1X7R1C106K	TDK Corporation

4. 1 Start-stop operation (Ta = +25°C)

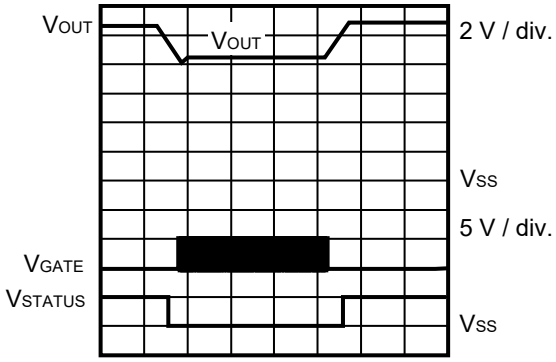
4. 1. 1 S-19989 Series A type

V_{IN} = V_{EN} = 10 V → 5 V → 10 V, I_{OUT} = 1500 mA



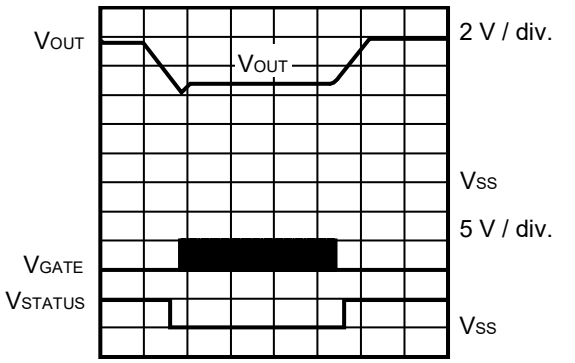
4. 1. 2 S-19989 Series B type

V_{IN} = V_{EN} = 11 V → 6 V → 11 V, I_{OUT} = 1500 mA



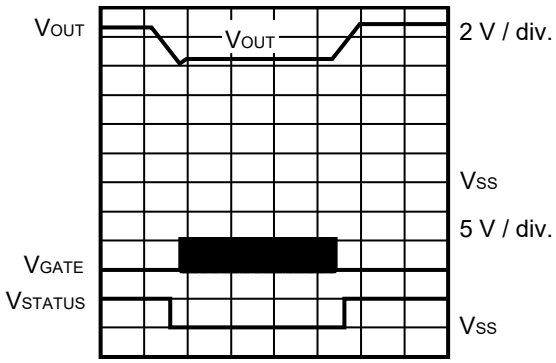
4. 1. 3 S-19989 Series C type

V_{IN} = V_{EN} = 10 V → 5 V → 10 V, I_{OUT} = 1500 mA



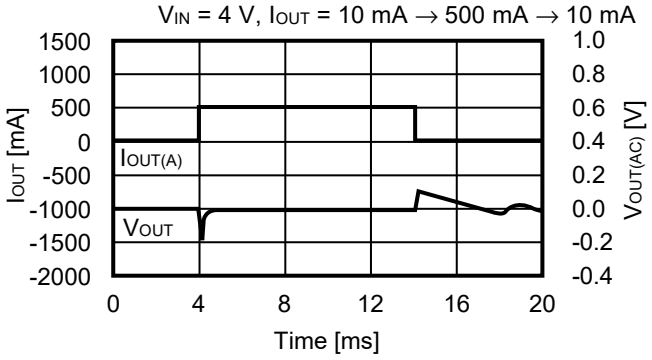
4. 1. 4 S-19989 Series D type

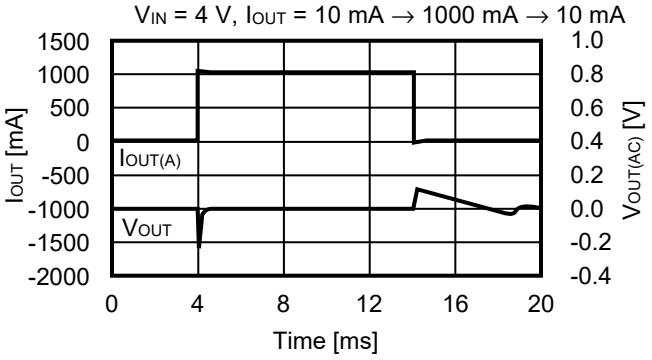
V_{IN} = V_{EN} = 11 V → 6 V → 11 V, I_{OUT} = 1500 mA



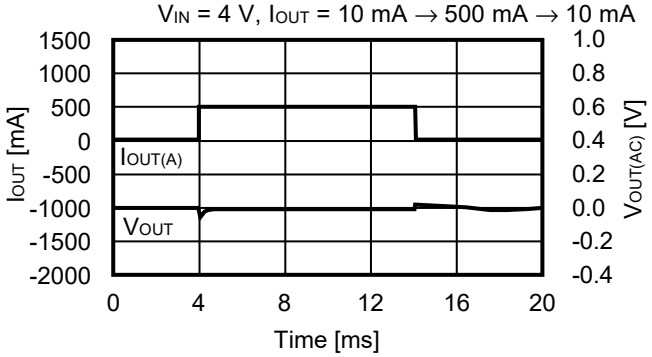
4. 2 Load transient response (Ta = +25°C)

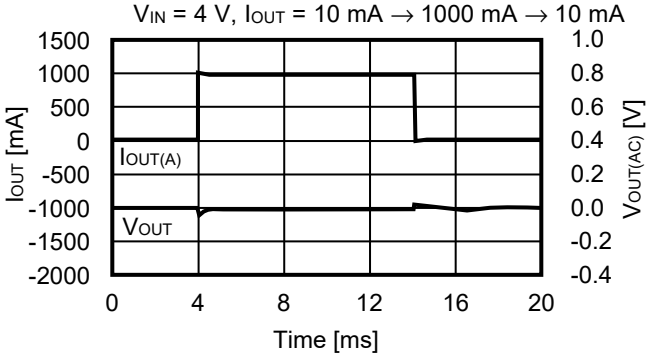
4. 2. 1 S-19989 Series A type



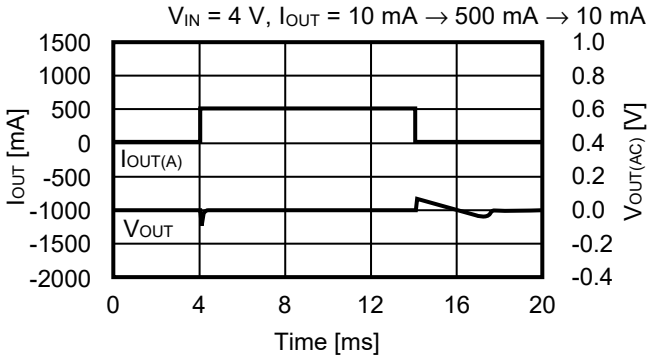


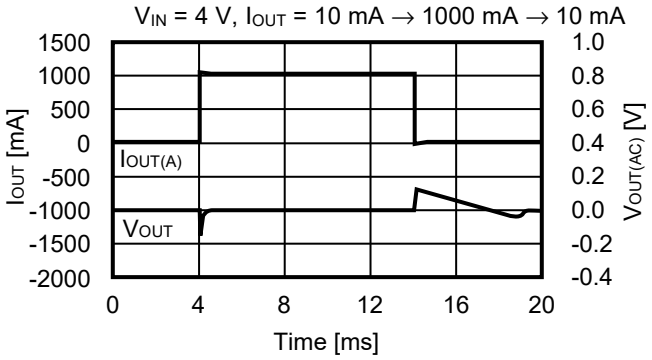
4. 2. 2 S-19989 Series B type



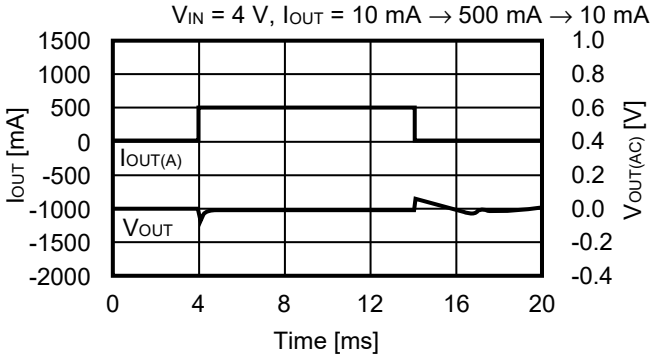


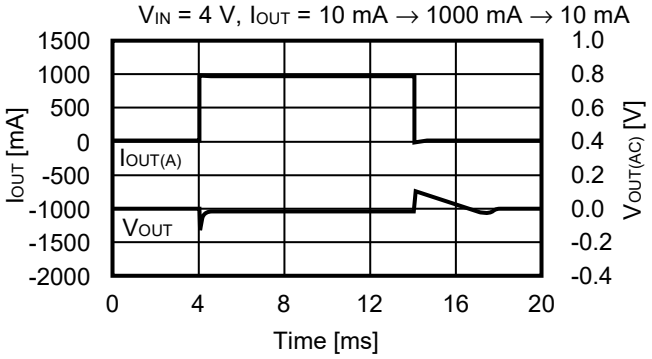
4. 2. 3 S-19989 Series C type





4. 2. 4 S-19989 Series D type





■ Reference Data

The external parts shown in **Table 14** are used in "■ **Reference Data**".

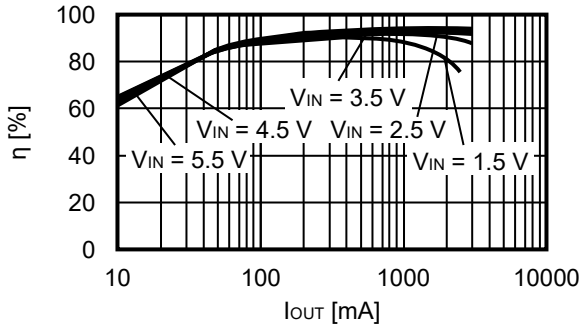
Table 14

Condition	Symbol	Value	Quantity	Part Number	Manufacturer
<1>	L	1.5 μH	1	SPM12565VT-1R5M-D	TDK Corporation
	FET	–	1	IPC50N04S5L-5R5	Infineon Technologies
	D	–	1	PMEG045V100EPD	Nexperia B.V.
	C_{IN}	0.1 μF	1	CGA4J2X8R1H104K	TDK Corporation
		33 μF	2	GYC1H330MCQ1GS	NICHICON CORPORATION
	C_{OUT}	10 μF	2	CGA5L1X7R1C106K	TDK Corporation
		100 μF	3	GYC1H101MCQ1GS	NICHICON CORPORATION
<2>	L	0.47 μH	1	SPM5030VT-R47M-D	TDK Corporation
	FET	–	1	IPC50N04S5L-5R5	Infineon Technologies
	D	–	1	PMEG045V100EPD	Nexperia B.V.
	C_{IN}	0.1 μF	1	CGA4J2X8R1H104K	TDK Corporation
		33 μF	2	GYC1H330MCQ1GS	NICHICON CORPORATION
	C_{OUT}	10 μF	2	CGA5L1X7R1C106K	TDK Corporation
		100 μF	3	GYC1H101MCQ1GS	NICHICON CORPORATION

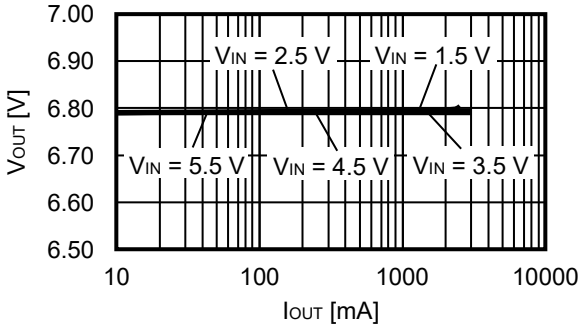
1. V_{OUT_REG} = 6.80 V (External parts: Condition <1>)

1. 1 S-19989 Series C type

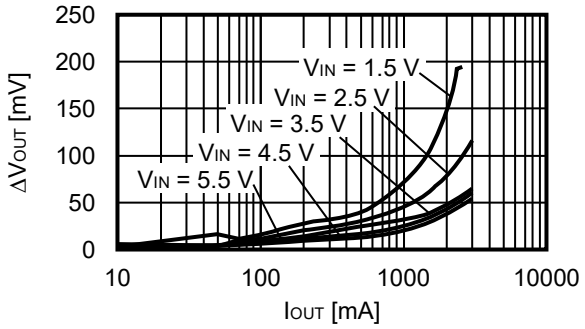
1. 1. 1 Efficiency (η) vs. Output current (I_{OUT})



1. 1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})



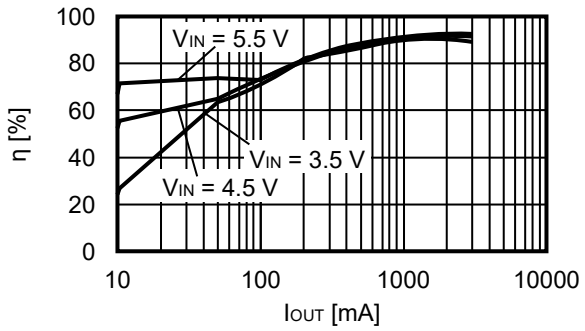
1. 1. 3 Ripple voltage (ΔV_{OUT}) vs. Output current (I_{OUT})



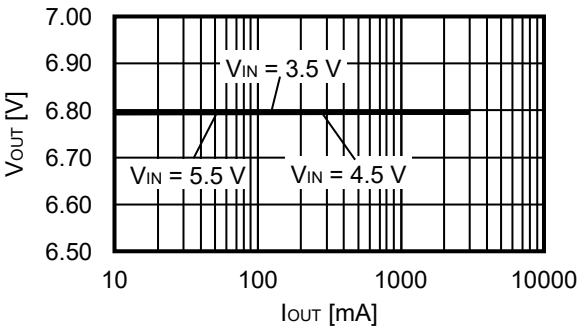
2. V_{OUT_REG} = 6.80 V (External parts: Condition <2>)

2. 1 S-19989 Series A type

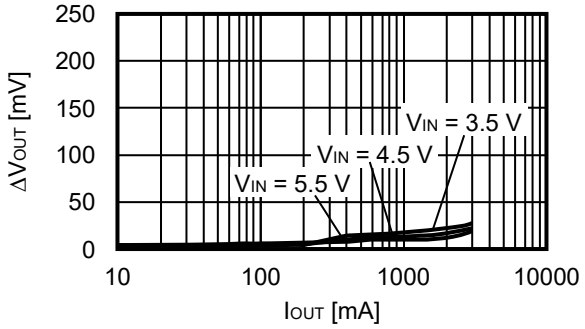
2. 1. 1 Efficiency (η) vs. Output current (I_{OUT})



2. 1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})



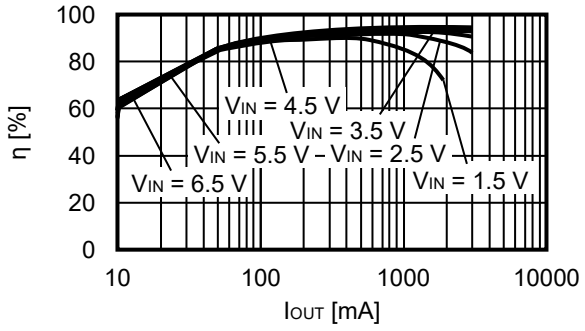
2. 1. 3 Ripple voltage (ΔV_{OUT}) vs. Output current (I_{OUT})



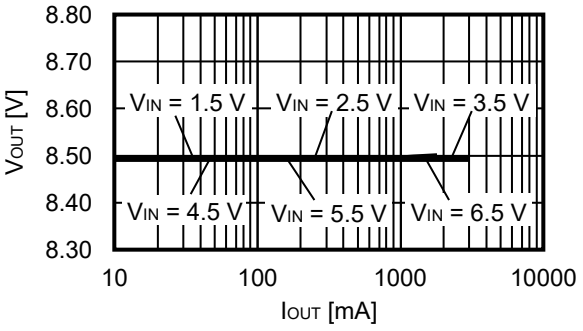
3. V_{OUT_REG} = 8.50 V (External parts: Condition <1>)

3. 1 S-19989 Series D type

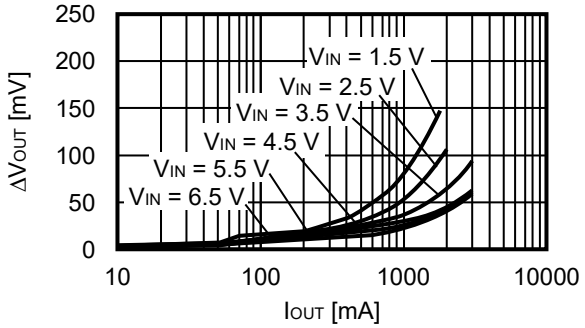
3. 1. 1 Efficiency (η) vs. Output current (I_{OUT})



3. 1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})



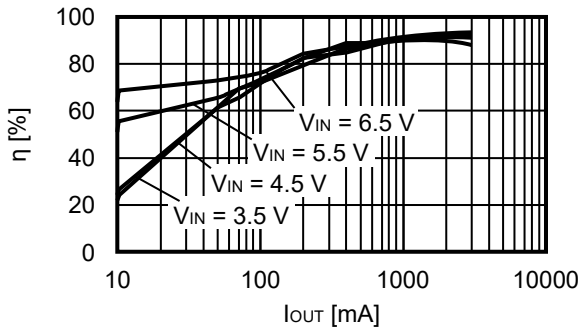
3. 1. 3 Ripple voltage (ΔV_{OUT}) vs. Output current (I_{OUT})



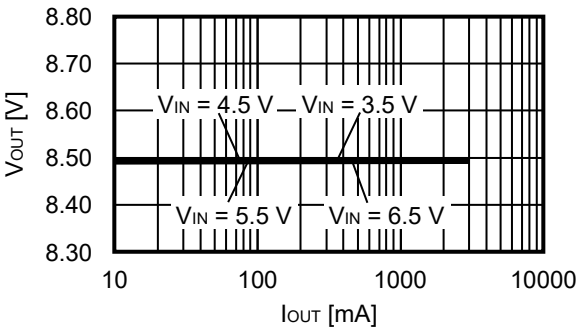
4. V_{OUT_REG} = 8.50 V (External parts: Condition <2>)

4. 1 S-19989 Series B type

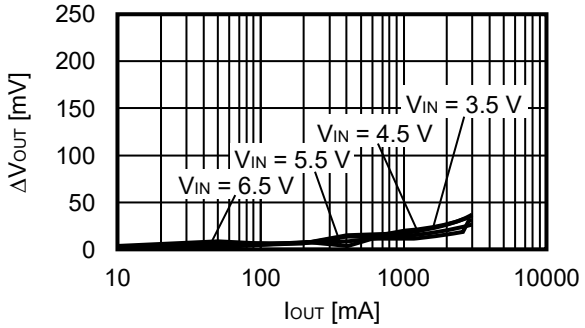
4. 1. 1 Efficiency (η) vs. Output current (I_{OUT})



4. 1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})

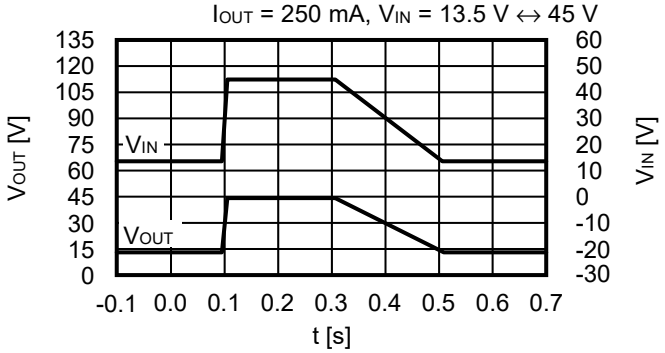


4. 1. 3 Ripple voltage (ΔV_{OUT}) vs. Output current (I_{OUT})



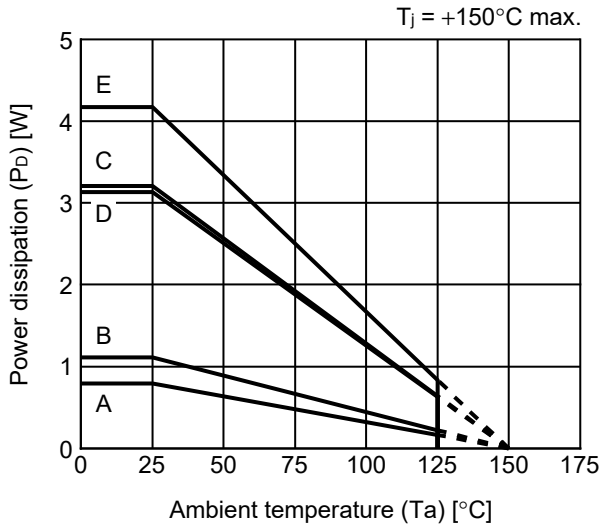
5. Load dump characteristics (Ta = +25°C)

5. 1 V_{OUT_REG} = 6.80 V



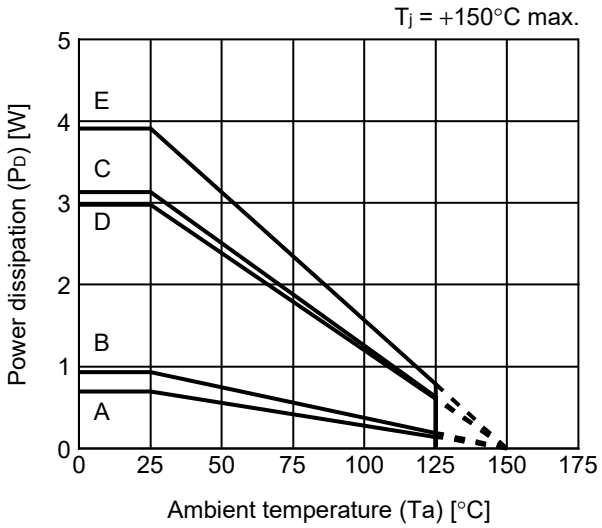
■ Power Dissipation

HTMSOP-8



Board	Power Dissipation (P_D)
A	0.79 W
B	1.11 W
C	3.21 W
D	3.13 W
E	4.17 W

HSNT-8(2030)

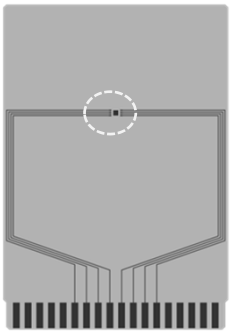


Board	Power Dissipation (P_D)
A	0.69 W
B	0.93 W
C	3.13 W
D	2.98 W
E	3.91 W

HTMSOP-8 Test Board

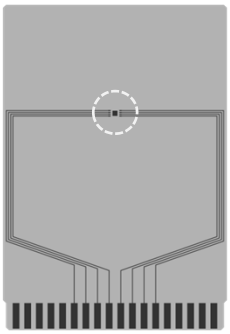
IC Mount Area

(1) Board A



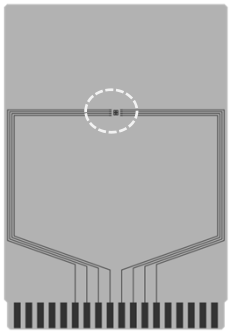
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

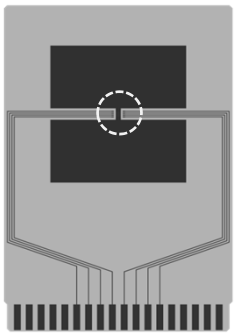
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HTMSOP8-A-Board-SD-1.0

HTMSOP-8 Test Board

IC Mount Area

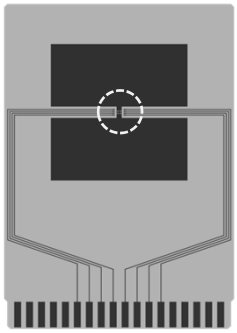
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



enlarged view

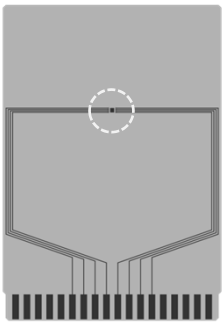
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HTMSOP8-A-Board-SD-1.0

HSNT-8(2030) Test Board

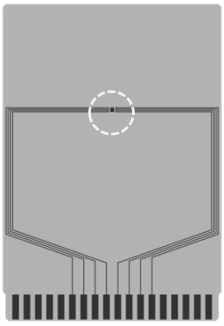
IC Mount Area

(1) Board A



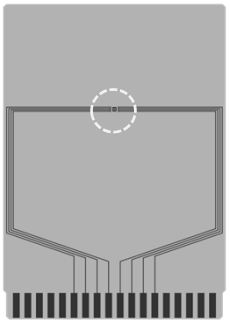
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

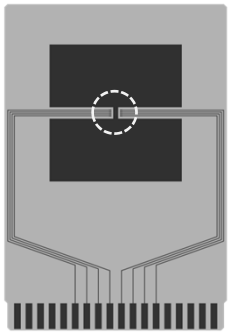
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-A-Board-SD-2.0

HSNT-8(2030) Test Board

IC Mount Area

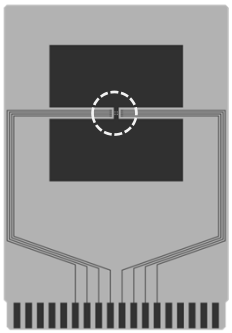
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

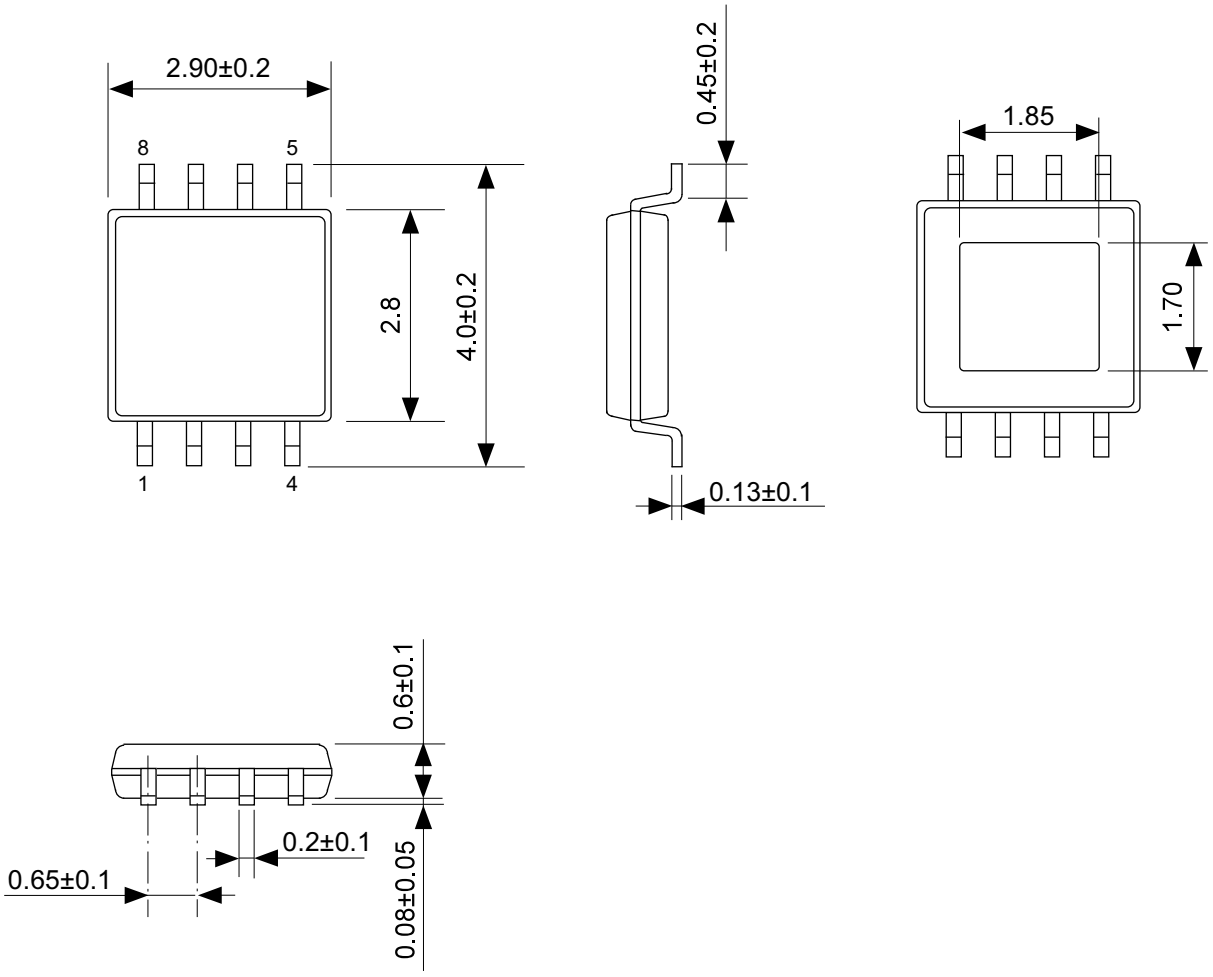
(5) Board E



enlarged view

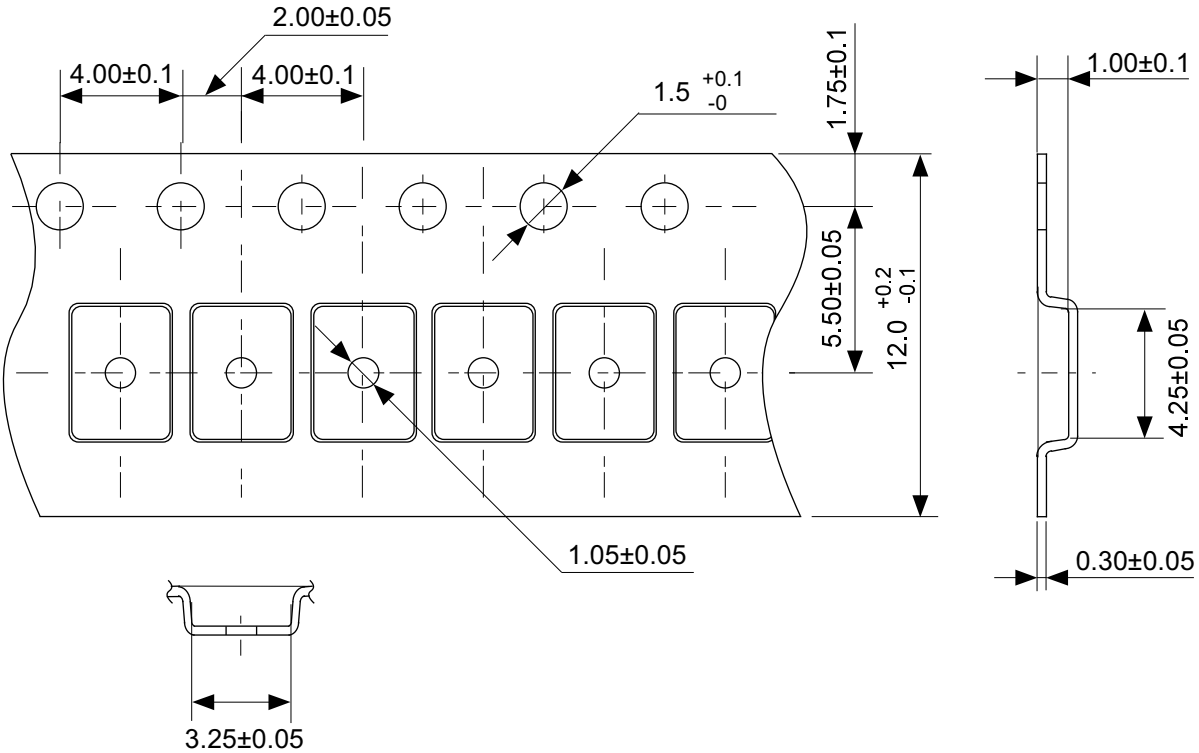
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

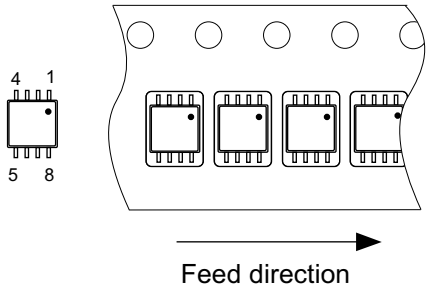
No. HSNT8-A-Board-SD-2.0



No. FP008-A-P-SD-2.0

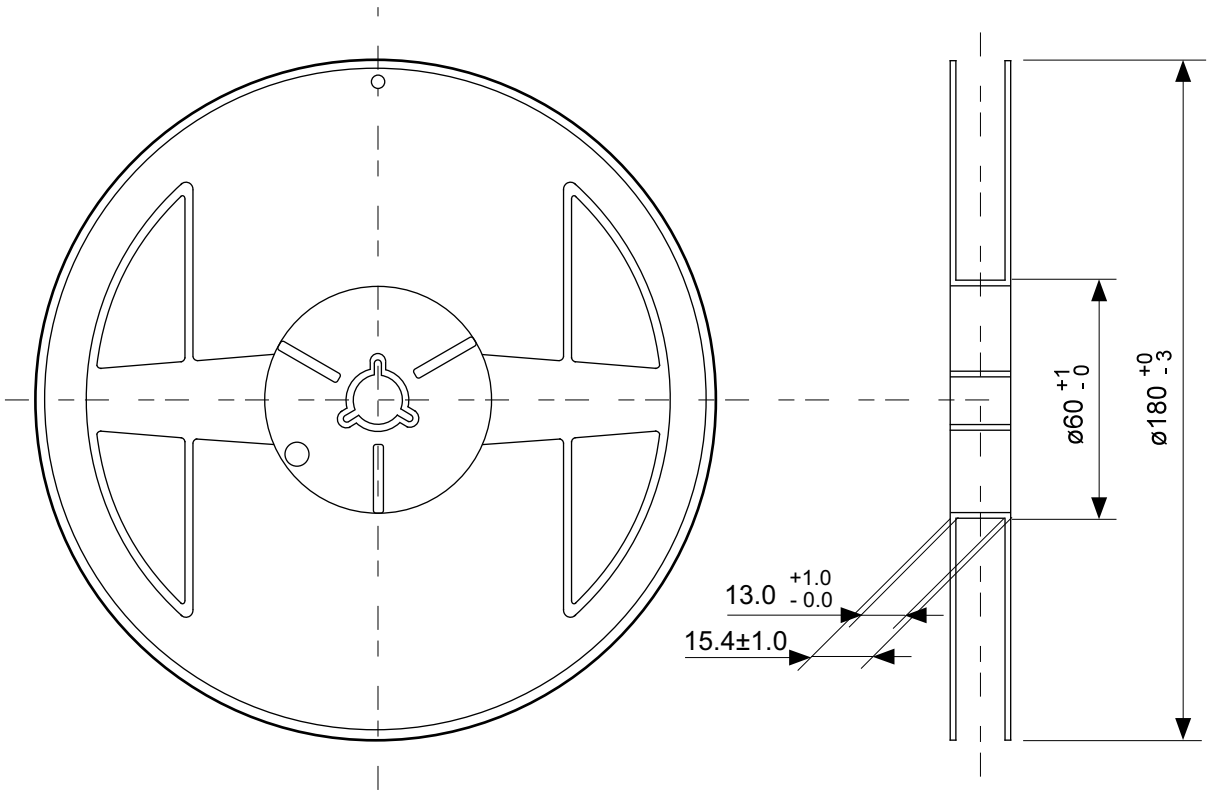
TITLE	HTMSOP8-A-PKG Dimensions
No.	FP008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



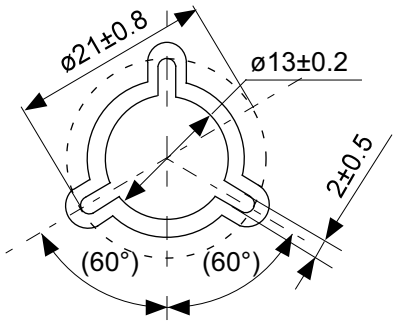


No. FP008-A-C-SD-1.0

TITLE	HTMSOP8-A-Carrier Tape
No.	FP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

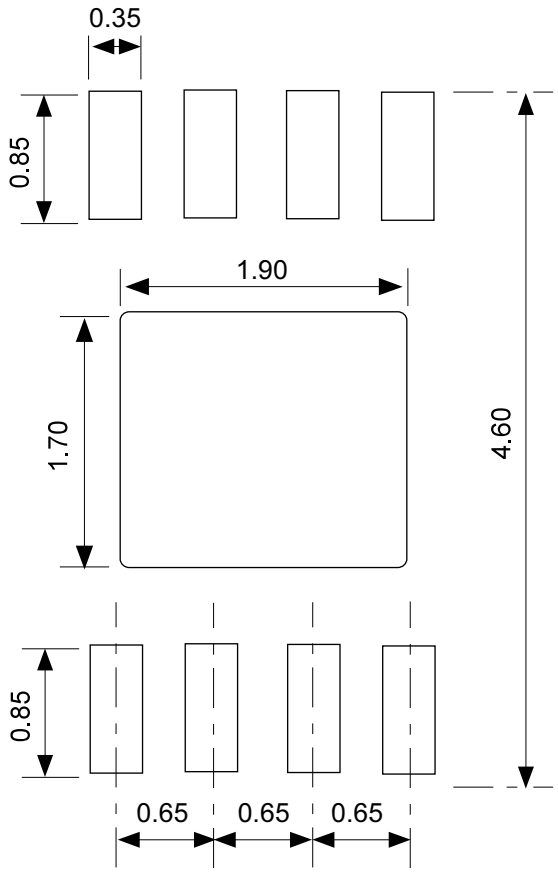


Enlarged drawing in the central part



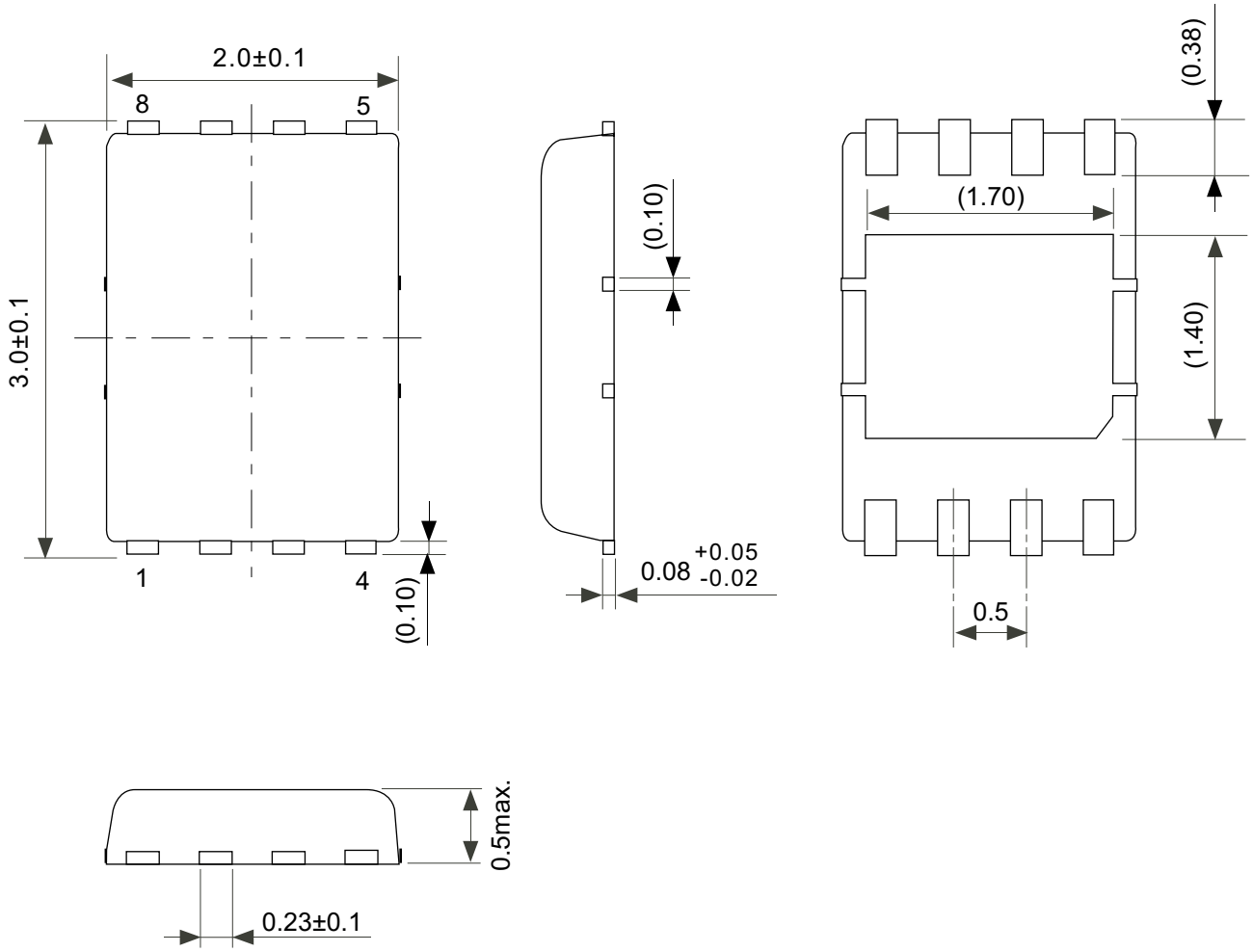
No. FP008-A-R-SD-2.0

TITLE	HTMSOP8-A-Reel		
No.	FP008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



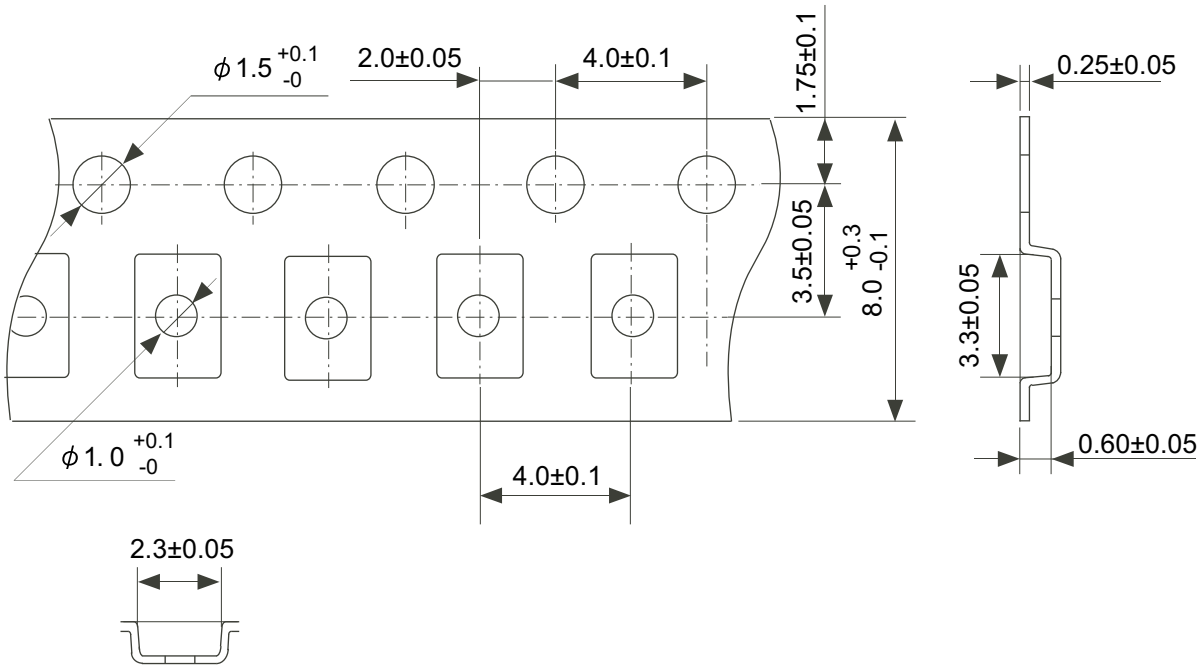
No. FP008-A-L-SD-2.0

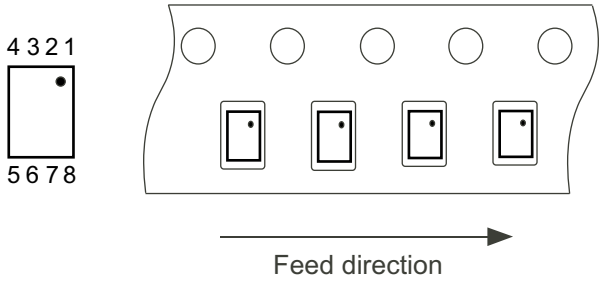
TITLE	HTMSOP8-A -Land Recommendation
No.	FP008-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. PP008-A-P-SD-3.0

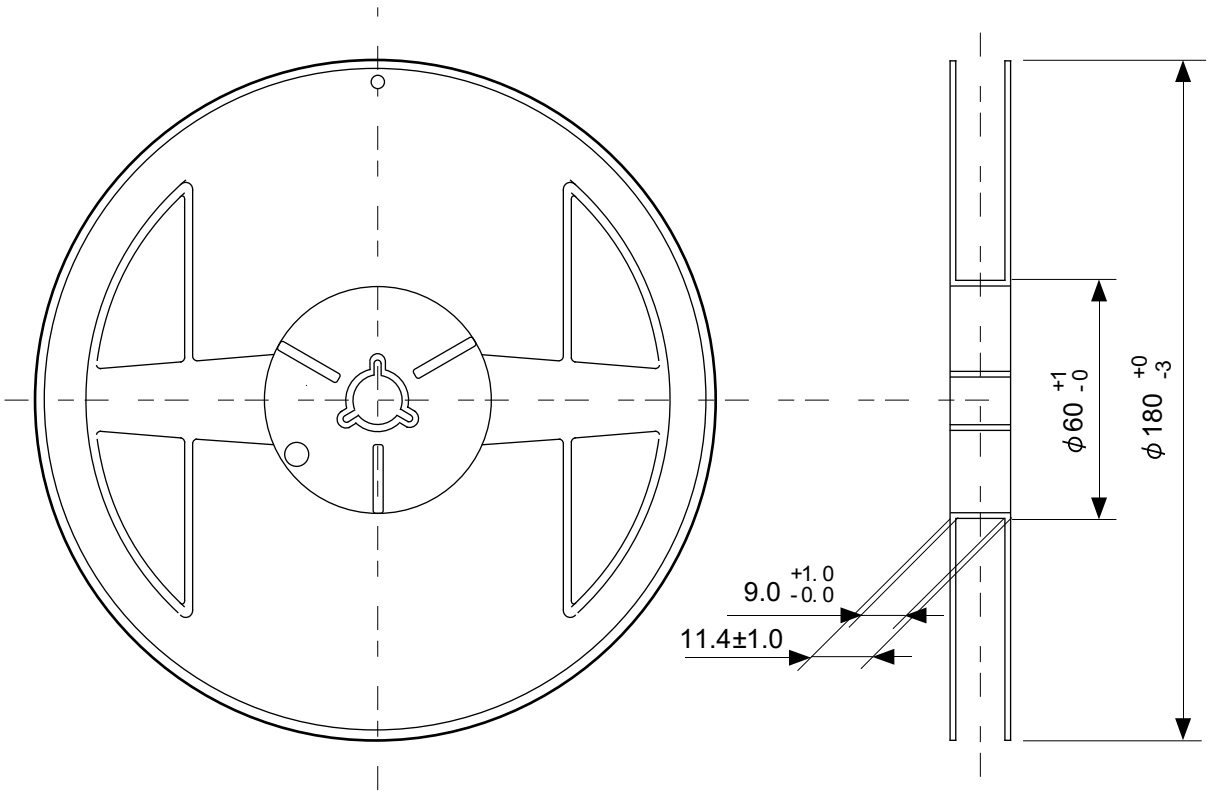
TITLE	HSNT-8-A-PKG Dimensions
No.	PP008-A-P-SD-3.0
ANGLE	
UNIT	mm
ABLIC Inc.	



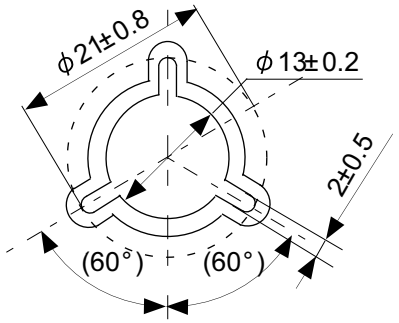


No. PP008-A-C-SD-1.0

TITLE	HSNT-8-A-Carrier Tape
No.	PP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

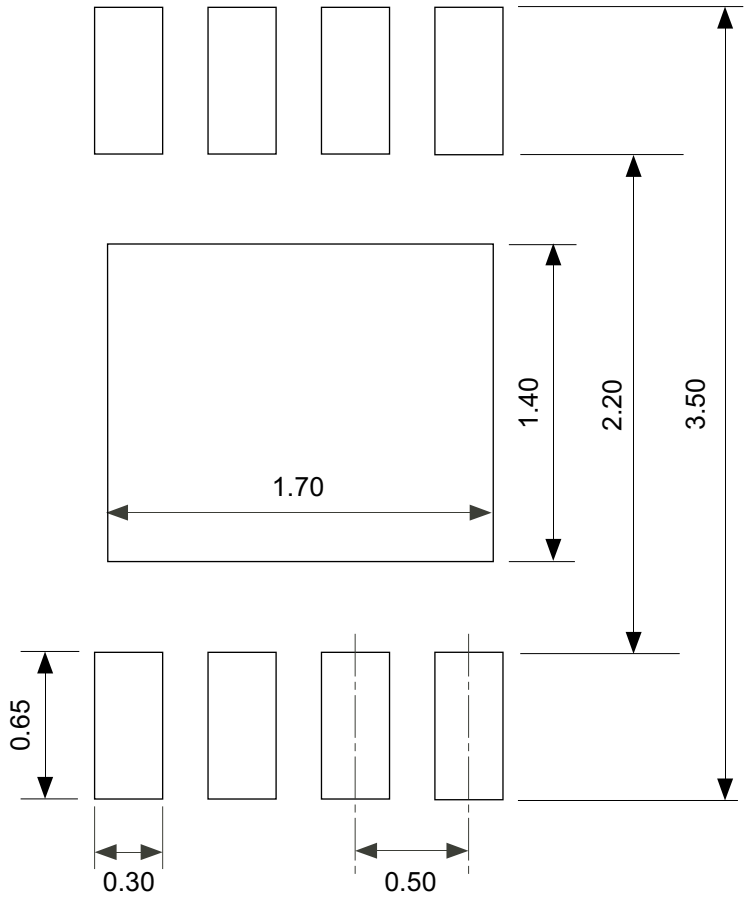


Enlarged drawing in the central part



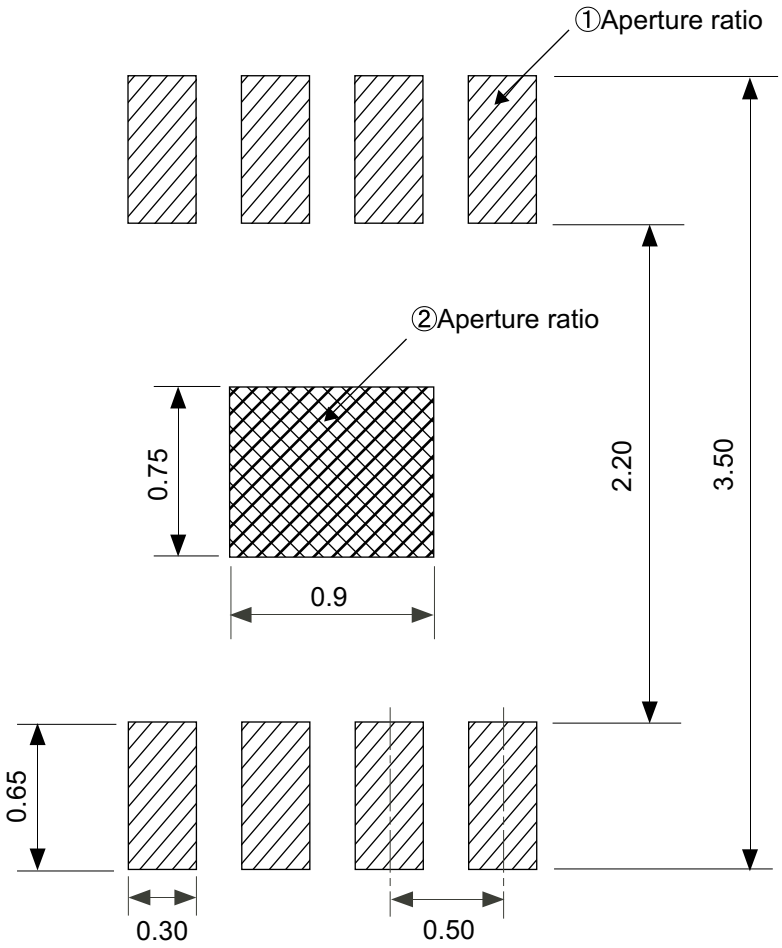
No. PP008-A-R-SD-2.0

TITLE	HSNT-8-A-Reel		
No.	PP008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
	ABLIC Inc.		



No. PP008-A-L-SD-2.0

TITLE	HSNT-8-A -Land Recommendation
No.	PP008-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is approximately 30%.
③ Mask thickness: t0.12 mm
④ Reflow atmosphere: Nitrogen atmosphere is recommended.
(Oxygen concentration: 1000ppm or less)

注意 ①リード実装部のマスク開口率 : 100%
②放熱板実装のマスク開口率 ：約30%
③マスク厚み : t 0.12 mm
④リフロー雰囲気 : 窒素雰囲気(酸素濃度1000ppm以下)推奨

No. PP008-A-L-S1-2.0

TITLE	HSNT-8-A-Stencil Opening
No.	PP008-A-L-S1-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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