S-19954/19955 Series

AUTOMOTIVE, 125°C OPERATION, 5.5 V INPUT, 1 A, POWER GOOD, SYNCHRONOUS STEP-DOWN SWITCHING REGULATOR

www.ablic.com

Rev.1.3_00

This IC is a secondary step-down switching regulator developed using CMOS process technologies with a built-in Power Good function.
PWM control (S-19954 Series) or PWM / PFM switching control (S-19955 Series) can be selected as an option.
S-19954 Series, which features PWM control, can be used without interfering with AM radio bands.
Since the S-19955 Series, which features PWM / PFM switching control, operates with PWM control under heavy load and automatically switches to PFM control under light load. It achieves high-efficiency operation in accordance with the device's status.
This IC is implemented as a small package and can comprise an application circuit with an inductor and two capacitors at the minimum configuration. Since the switching frequency is as high as 2.25 MHz, and the peripheral parts can be made compact, the IC is suitable for space-saving uses.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.

■ Features

- Input voltage: 2.7 V to 5.5 V
- Output voltage: 0.8 V to 3.3 V
- Output current: 1 A
- VOUT pin detection voltage accuracy: ±1.5% (T_j = –40°C to +125°C)
- Efficiency: 95%
- Oscillation frequency: 2.25 MHz typ.
- Overcurrent protection function: 1.75 A typ. (pulse-by-pulse method)
- Thermal shutdown function: 170°C typ. (detection temperature)
- Short-circuit protection function: Hiccup control, Latch control
- 100% duty cycle operation
- Output discharge function: "Available " / "Unavailable " is selectable.
- Power Good function: Nch open-drain output
- Soft-start function: 0.35 ms typ.
- Under voltage lockout function (UVLO): 2.43 V typ. (detection voltage)
- Input and output capacitors: Ceramic capacitor compatible
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*1

*1. Contact our sales representatives for details.

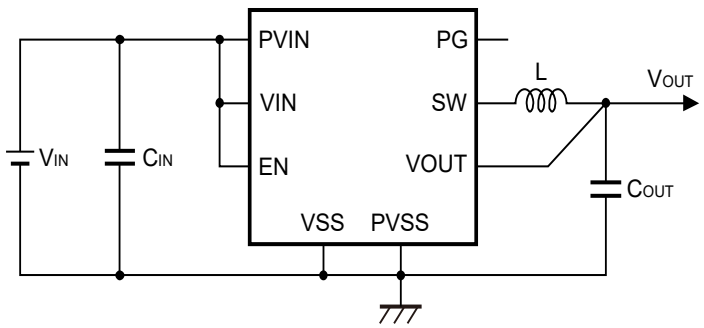
■ Applications

- Secondary power supply for automotive equipment
- Camera module
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)
- Constant-voltage power supply for electrical application for vehicle interior

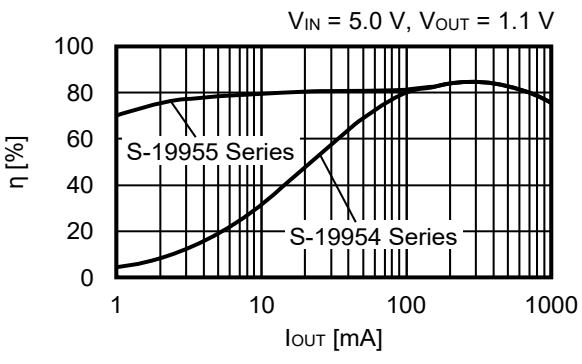
■ Packages

- HTMSOP-8 (2.9 mm × 4.0 mm × t0.8 mm max.)
- HSNT-8(1616)B (1.6 mm × 1.6 mm × t0.41 mm max.)

■ Typical Application Circuit

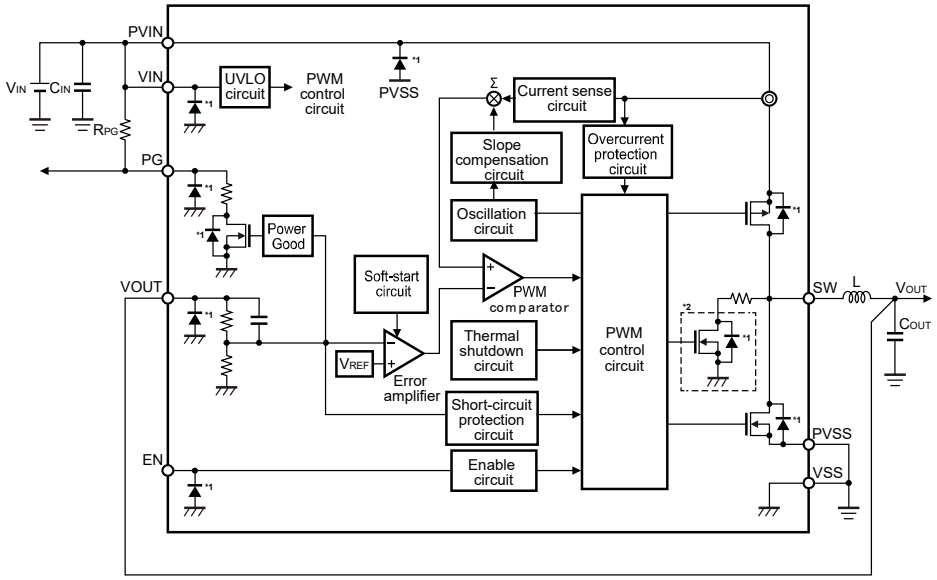


■ Efficiency



■ Block Diagrams

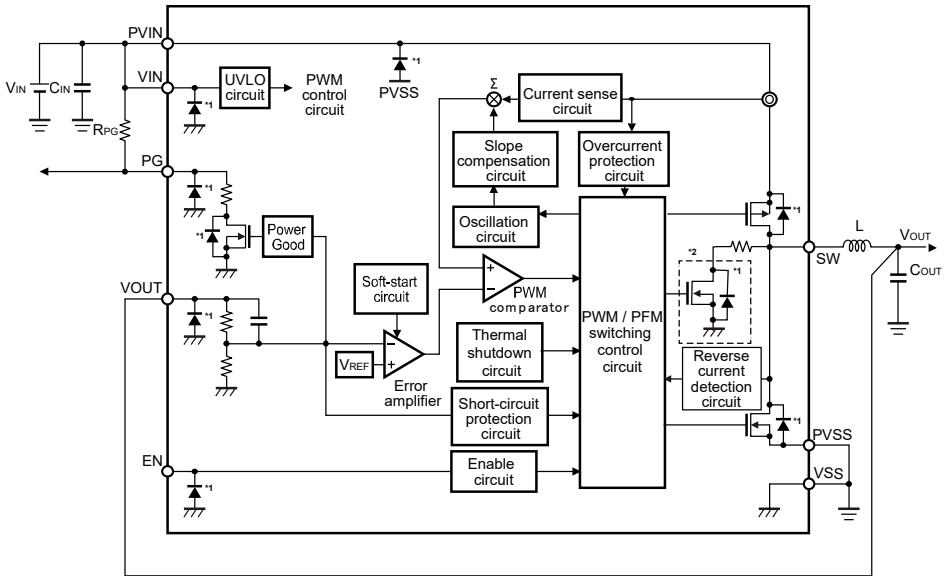
1. S-19954 Series (PWM control)



***1.** Parasitic diode
***2.** Discharge switch

Figure 1

2. S-19955 Series (PWM / PFM switching control)



***1.** Parasitic diode
***2.** Discharge switch

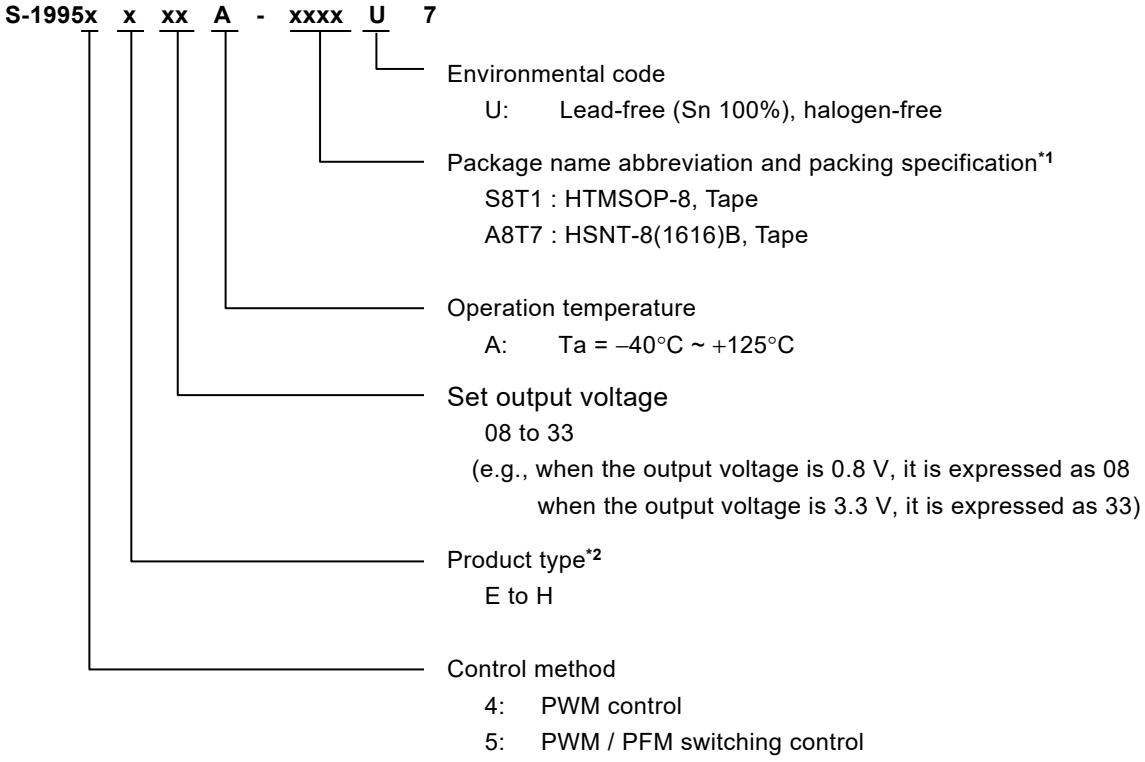
Figure 2

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** Refer to "**2. Function list of product types**".

2. Function list of product types

Table 1

Product Type	Oscillation Frequency	Output Discharge Function*1	Short-circuit Protection Function
E	2.25 MHz	Available	Hiccup control
F	2.25 MHz	Available	Latch control
G	2.25 MHz	Unavailable	Hiccup control
H	2.25 MHz	Unavailable	Latch control

***1.** Refer to "**12. Output Discharge Function**" in "**■ Operation**"

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
HTMSOP-8	FP008-A-P-SD	FP008-A-C-SD	FP008-A-R-SD	FP008-A-L-SD
HSNT-8(1616)B	PY008-B-P-SD	PY008-B-C-SD	PY008-B-R-SD	PY008-B-L-SD

■ Pin Configurations

1. HTMSOP-8

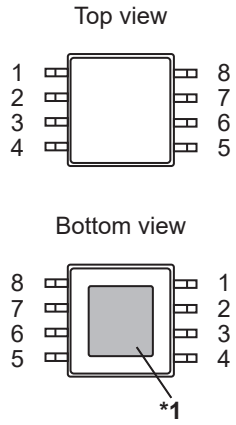


Figure 3

Table 3

Pin No.	Symbol	Description
1	PVSS*2	Power GND pin
2	SW	External inductor connection pin
3	VSS*2	GND pin
4	VOUT	Output voltage monitor pin
5	PG*3	Power Good output pin (Nch open-drain output)
6	EN*4	Enable pin (active "H")
7	VIN*5	Power supply pin (analog)
8	PVIN*5	Power supply pin (power)

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.
***2.** Connect the PVSS and VSS pins to the board, and set electric potential GND.
***3.** If the PG pin is unused, open it or connect to GND.
If the PG pin is used, pull it up with a resistor.
***4.** Do not float the EN pin.
Pull it up to the VIN pin or connect to GND.
***5.** Connect the VIN and PVIN pins on the board.

2. HSNT-8(1616)B

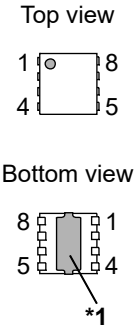


Figure 4

Table 4

Pin No.	Symbol	Description
1	PVSS*2	Power GND pin
2	SW	External inductor connection pin
3	VSS*2	GND pin
4	VOUT	Output voltage monitor pin
5	PG*3	Power Good output pin (Nch open-drain output)
6	EN*4	Enable pin (active "H")
7	VIN*5	Power supply pin (analog)
8	PVIN*5	Power supply pin (power)

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.
***2.** Connect the PVSS and VSS pins to the board, and set electric potential GND.
***3.** If the PG pin is unused, open it or connect to GND.
If the PG pin is used, pull it up with a resistor.
***4.** Do not float the EN pin.
Pull it up to the VIN pin or connect to GND.
***5.** Connect the VIN and PVIN pins on the board.

■ Absolute Maximum Ratings

Table 5

(Unless otherwise specified: Ta = +25°C, V_{SS} = V_{PVSS} = 0 V, V_{IN} = V_{PVIN})

Item	Symbol	Absolute Maximum Ratings	Unit
VIN pin voltage	V_{IN}	V_{SS} – 0.3 to V_{SS} + 6.5	V
EN pin voltage	V_{EN}	V_{SS} – 0.3 to V_{SS} + 6.5	V
PG pin voltage	V_{PG}	V_{SS} – 0.3 to V_{SS} + 6.5	V
PVIN pin voltage	V_{PVIN}	V_{SS} – 0.3 to V_{SS} + 6.5	V
VOUT pin voltage	V_{OUT}	V_{SS} – 0.3 to V_{SS} + 6.5	V
SW pin voltage	V_{SW}	V_{SS} – 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 6.5	V
		V_{SS} – 2 to V_{IN} + 2 ≤ V_{SS} + 6.5 (< 20 ns)	
Junction temperature	T_j	–40 to +150	°C
Operation ambient temperature	T_{opr}	–40 to +125	°C
Storage temperature	T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	HTMSOP-8	Board A	–	159	–	°C/W
			Board B	–	113	–	°C/W
			Board C	–	39	–	°C/W
			Board D	–	40	–	°C/W
			Board E	–	30	–	°C/W
		HSNT-8(1616)B	Board A	–	214	–	°C/W
			Board B	–	172	–	°C/W
			Board C	–	52	–	°C/W
			Board D	–	55	–	°C/W
			Board E	–	43	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Recommended Operation Conditions

Table 7

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output current	I_{OUT}	–	–	–	1	A
Effective output capacitance value	C_{OUT}	–	5	10	20	μF
Effective inductance value	L	–	1.05	2.2	3.0	μH

Remark Refer to **Table 12** in "■ **External Parts Selection**" for details on recommended values.

■ Electrical Characteristics

Table 8

(V_{IN} = V_{PVIN} = 5.0 V*1, T_j = −40°C to +125°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Operating input voltage	V_{IN}	V_{IN} = V_{PVIN}		2.7	−	5.5	V
Current consumption during shutdown	I_{SSS}	V_{IN} = V_{PVIN} = 5.5 V*1, V_{EN} = V_{SW} = 0 V		−	0.1	18	μA
Current consumption during switching off	I_{SS}	S-19954 Series	$V_{OUT} \leq V_{OUT(S)} \times 0.95$, Power supply current*1, V_{EN} = 5.0 V	−	0.33	−	mA
		S-19955 Series	$V_{OUT} \geq V_{OUT(S)} \times 1.05$, Power supply current*1, V_{EN} = 5.0 V	−	38	80	μA
UVLO detection voltage	V_{UVLO-}	V_{IN} = V_{PVIN}*1, falling		2.3	2.43	2.55	V
UVLO release voltage	V_{UVLO+}	V_{IN} = V_{PVIN}*1, rising		2.4	2.53	2.65	V
Maximum duty ratio	MaxDuty	−		100	−	−	%
Soft-start time	t_{SS}	Time after V_{EN} = V_{SL} → V_{SH} is applied until V_{OUT} = 0 V → $V_{OUT(S)}$ × 90% is reached		0.18	0.35	0.65	ms
High side power MOS FET on-resistance	R_{HFET}	HTMSOP-8, I_{SW} = 100 mA		−	0.17	0.275	Ω
		HSNT-8(1616)B, I_{SW} = 100 mA		−	0.155	0.25	Ω
Low side power MOS FET on-resistance	R_{LFET}	HTMSOP-8, I_{SW} = −100 mA		−	0.13	0.245	Ω
		HSNT-8(1616)B, I_{SW} = −100 mA		−	0.12	0.22	Ω
Limit current	I_{LIM}	High side power MOS FET peak current value		1.4	1.75	2.2	A
High level input voltage	V_{SH}	EN pin, V_{IN} = 2.7 V to 5.5 V		2.0	−	−	V
Low level input voltage	V_{SL}	EN pin, V_{IN} = 2.7 V to 5.5 V		−	−	0.8	V
High level input current	I_{SH}	EN pin, V_{IN} = V_{PVIN} = 5.5 V*1, V_{EN} = V_{IN}		0.3	1.3	5	μA
Low level input current	I_{SL}	EN pin, V_{IN} = V_{PVIN} = 5.5 V*1, V_{EN} = 0 V		−0.1	−	0.1	μA
Output voltage*2	$V_{OUT(E)}$	During PWM operation, I_{OUT} = 1 mA		$V_{OUT(S)}$ × 0.985	$V_{OUT(S)}$	$V_{OUT(S)}$ × 1.015	V
PWM operation oscillation frequency	f_{OSC}	−		2.025	2.25	2.475	MHz
SW pin leakage current "H"	I_{SWH}	V_{IN} = V_{PVIN} = 5.5 V*1, V_{SW} = 0 V, High side power MOS FET OFF, Low side power MOS FET OFF		−16	−	−	μA
SW pin leakage current "L"	I_{SWL}	V_{IN} = V_{PVIN} = 5.5 V*1, V_{SW} = 5.5 V, High side power MOS FET OFF, Low side power MOS FET OFF, discharge switch OFF		−	−	16	μA
SW pin discharge switch resistance value	R_{DCHG}	Discharge switch ON, V_{IN} = V_{PVIN} = 5.5 V*1		−	95	200	Ω
Power Good detection threshold*3	TH_{PG_UR}	$V_{OUT(E)}$ ratio, VOUT falling		−	110	−	%
	TH_{PG_LR}	$V_{OUT(E)}$ ratio, VOUT rising		−	90	−	%
Power Good release threshold*3	TH_{PG_UF}	$V_{OUT(E)}$ ratio, VOUT rising		−	114	−	%
	TH_{PG_LF}	$V_{OUT(E)}$ ratio, VOUT falling		−	86	−	%
PG pin low level voltage	V_{PG}	V_{IN} = V_{PVIN} = 5.5 V*1, I_{PG} = 2 mA		−	−	0.4	V
PG pin leakage current	I_{PG}	−		−	−	1	μA
Thermal shutdown detection temperature	T_{SD}	Junction temperature		−	170	−	°C
Thermal shutdown release temperature	T_{SR}	Junction temperature		−	145	−	°C

***1.** Short the VIN and PVIN pins on the board.

***2.** $V_{OUT(S)}$: Set output voltage
$V_{OUT(E)}$: Actual output voltage

***3.** When the soft start function is working, the Power Good function is disabled, and the PG pin is pulled down regardless of V_{OUT}. When the soft start function operation ends, the Power Good function is enabled.

■ Operation

1. Overview of operation

This IC adopts the current mode control. By comparing the current feedback signal which has slope compensation added to the current flows through the high side power MOS FET with the output signal of error amplifier, the duty ratio of the SW pin is determined. Using the negative feedback loop configured, the error amplifier output signal is maintained at the value that internal reference voltage V_{REF} and the feedback voltage from the VOUT pin will be equalized.

2. PWM control (S-19954 Series)

The S-19954 Series operates with the pulse width modulation method (PWM) regardless of the extent of load current and allows the switching frequency to stabilize.

3. PWM / PFM switching control (S-19955 Series)

The S-19955 Series automatically switches between PWM and pulse frequency modulation method (PFM) according to the load current. PFM control is selected when under light load, and the pulse will skip according to the load current. This reduces self-current consumption and improves efficiency when under light load.
In addition, our distinctive PWM / PFM switching control technology enables constant voltage output without generating excessive ripple voltage in V_{OUT} during PFM control. For PFM control, the output current value to be switched is set to I_{OUT} = 120 mA typ.

4. 100% duty cycle operation

The high side power MOS FET allows for 100% duty cycle operation. Even when the input voltage (V_{IN}) is lowered up to the output voltage ($V_{OUT(E)}$), the high side power MOS FET is kept on and current can be supplied to the load. The output voltage at this time is the input voltage from which the voltage drop due to the DC resistance of the inductor and the on-resistance of the high side power MOS FET are subtracted.
If set output voltage ($V_{OUT(S)}$) is high and V_{IN} is low, the short-circuit protection function may operate.

5. Under voltage lockout function (UVLO)

This IC has a built-in UVLO circuit to prevent the IC from malfunctioning due to a transient status at power-on or a momentary drop in the supply voltage. When UVLO status is detected, the high side power MOS FET and the low side power MOS FET will turn off and switching operation will stop. The soft-start function is reset if UVLO status is detected once and is restarted by releasing the UVLO status.
Note that the internal circuits operate when UVLO status is detected, and the status is different from the disabled status. Also, there is a hysteresis width of approximately 0.1 V typ. for detection and release voltages to avoid malfunctions due to generation of noise, etc. in the input voltage.

6. EN pin

This pin controls IC operation or stop. When the EN pin is set to "L", the operation of all internal circuits, including the high side power MOS FET, is stopped, reducing current consumption. If the output discharging function is available, the discharging switch connected to the SW pin works.
When not using the EN pin, connect it to the VIN pin. If the EN pin is open, it is pulled down to "L" level depending on the built-in current source.

Table 9

EN Pin	Internal Circuit
"H"	Enable (normal operation)
"L"	Disable (power off)

7. Thermal shutdown function

This IC has a built-in thermal shutdown circuit to limit overheating. When the junction temperature increases to 170°C typ., the thermal shutdown circuit becomes the detection status, and the switching operation is stopped. When the junction temperature decreases to 145°C typ., the thermal shutdown circuit becomes the release status, and the switching operation is restarted. The detection temperature and release temperature have a hysteresis width of 25°C typ.

If the thermal shutdown circuit becomes the detection status due to self-heating, the switching operation is stopped and output voltage (V_{OUT}) decreases. For this reason, the self-heating is limited and the temperature of the IC decreases. The thermal shutdown circuit becomes release status when the temperature of the IC decreases, and the switching operation is restarted, thus the self-heating is generated again. Repeating this procedure makes the waveform of V_{OUT} into a pulse-like form. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously. Consider usage conditions carefully. Switching operation stop and restart can be suppressed by either setting the EN pin to "L", lowering the output current (I_{OUT}) to reduce internal power consumption, or decreasing the ambient temperature.

Since the thermal shutdown circuit is in detection state and the internal circuits are working, it is different from disable status.

If the junction temperature is not equal to or lower than the release temperature when the IC starts, switching operation stops until the junction temperature becomes equal to or lower than the release temperature.

Table 10

Thermal Shutdown Circuit	V_{OUT}	Output Discharge Switch
Release: 145°C typ.*1	Constant value*2	OFF
Detection: 170°C typ.*1	Pulled down to V_{SS}*3	ON

***1.** Junction temperature

***2.** A constant value is output due to regulating operation based on the internal resistance.

***3.** V_{OUT} is pulled down to V_{SS} due to the VOUT pin resistance and a load.

Caution If the heat dissipation of the application is not good, self-heating cannot be restricted immediately, and the IC may be destroyed. The actual application should be evaluated carefully to verify that there is no problem.

8. Overcurrent protection function

This IC has a built-in overcurrent protection circuit to prevent IC destruction due to overload or magnetic saturation of an inductor. The overcurrent protection circuit performs pulse-by-pulse overcurrent protection that monitors the current of the high-side power MOS FET for each cycle of switching operation.

When a current reaching or exceeding the limit current (I_{LIM}) flows through the high side power MOS FET, the high side power MOS FET is turned off. When the next switching cycle starts, the high side power MOS FET is turned on. If the current value continues to remain at I_{LIM} or higher, the high side power MOS FET is turned off again, repeating this series of operation.

Meanwhile, when the current, which flows through the high side power MOS FET, falls to I_{LIM} or lower, this IC will return to the normal operation.

When the slope of inductor current is large, I_{LIM} may appear to increase due to the delay time of overcurrent protection circuit. This phenomenon tends to occur when low-inductance inductor is used or when the voltage difference between V_{IN} and V_{OUT} is large.

9. Frequency foldback function

The frequency foldback function reduces the oscillation frequency in proportion to V_{OUT} when VOUT pin voltage is $V_{OUT(E)} \times 0.8$ V typ. or lower. Refer to "**10. Short-circuit protection function**" for details.

The frequency foldback function in this IC sets to invalid when the soft-start function is operating. If the VOUT pin voltage is equal to or greater than $V_{OUT(E)} \times 0.84$ V typ., the IC works at the PWM operation oscillation frequency (f_{OSC}). If the output current increases when there is a little difference between the input and output voltages, a voltage drop occurs due to ON resistance of the high-side power MOS FET, and the VOUT pin voltage may be equal to or less than the frequency foldback detection threshold.

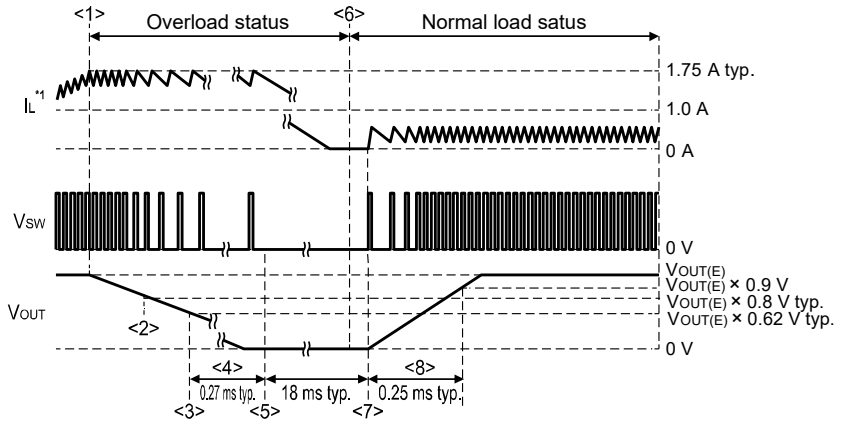
10. Short-circuit protection function

10. 1 Hiccup control

E, G type of this IC has a built-in short-circuit protection function for Hiccup control.
The hiccup control is a method for periodically carrying out automatic recovery when the IC detects overcurrent and stops the switching operation.

10. 1. 1 When overload status is released

<1> Overcurrent detection
<2> After detection of the VOUT pin voltage (V_{OUT}) < $V_{OUT(E)} \times 0.8$ V typ., frequency foldback function becomes valid.
<3> Detection of $V_{OUT} < V_{OUT(E)} \times 0.62$ V typ.
<4> 0.27 ms elapse
<5> Switching operation stop (for 18 ms typ.) (short-circuit protection detection status)
<6> Overload status release
<7> The IC restarts, soft-start function starts.
In this case, it is unnecessary to input an external reset signal for restart.
<8> V_{OUT} reaches $V_{OUT(E)} \times 0.9$ V typ. after 0.25 ms typ. elapses.

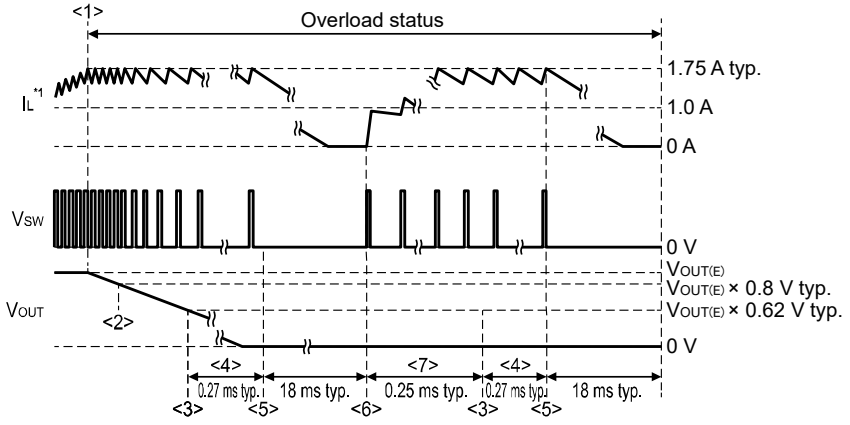


***1.** Inductor current

Figure 5

10. 1. 2 When overload status continues

<1> Overcurrent detection
<2> After detection of $V_{OUT} < V_{OUT(E)} \times 0.8$ V typ, frequency foldback function becomes valid.
<3> Detection of $V_{OUT} < V_{OUT(E)} \times 0.62$ V typ.
<4> 0.27 ms elapse
<5> Switching operation stop (for 18 ms typ.) (short-circuit protection detection status)
<6> The IC restarts, soft-start function starts.
<7> The status returns to <3> when overload status continues after 0.25 ms typ. elapses.



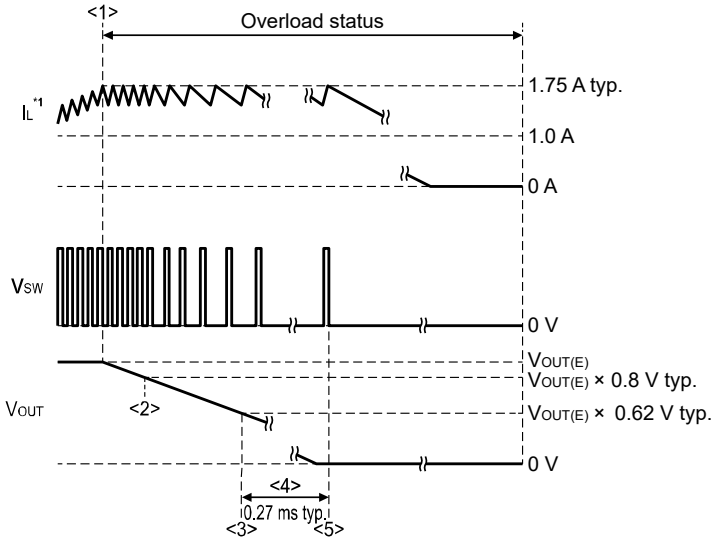
***1.** Inductor current

Figure 6

10. 2 Latch control

F, H type of this IC has a built-in short-circuit protection function for Latch control.
The latch control is a method for maintaining the Latch status when the IC detects overcurrent and stops the switching operation.

<1> Overcurrent detection
<2> After detection of $V_{OUT} < V_{OUT(E)} \times 0.8$ V typ., frequency foldback function becomes valid.
<3> Detection of $V_{OUT} < V_{OUT(E)} \times 0.62$ V typ.
<4> 0.27 ms elapse
<5> Switching operation stop (short-circuit protection detection status)



***1.** Inductor current

Figure 7

In addition, Latch status is reset under the following conditions.

- At UVLO detection
- When the EN pin changes from "H" to "L".

11. Pre-bias compatible soft-start function

This IC has a built-in pre-bias compatible soft-start circuit.
If the pre-bias compatible soft-start circuit starts when electrical charge remains in the output voltage (V_{OUT}) because of power supply restart, etc., or when V_{OUT} is biased beforehand (pre-bias status), switching operation is stopped until the internal soft-start voltage exceeds the feedback voltage from VOUT pin, and then V_{OUT} is maintained. If the soft-start voltage exceeds the feedback voltage from VOUT pin, switching operation will restart and V_{OUT} will rise to the output voltage setting value ($V_{OUT(S)}$). This allows $V_{OUT(S)}$ to be reached without lowering the pre-biased V_{OUT}.
In soft-start circuits which are not pre-bias compatible, a large current flows as a result of the discharge of the residual electric charge in C_{OUT} through the low side power MOS FET when switching operation starts, which could cause damage to the IC, however in a pre-bias compatible soft-start circuit, the IC is protected from the large current when switching operation starts, and it makes power supply design for the application circuit simpler.

In this IC, V_{OUT} reaches $V_{OUT(S)}$ gradually due to the soft-start circuit.
In the following cases, rush current and V_{OUT} overshoot are reduced.

- When the EN pin changes from "L" to "H".
- When UVLO operation is released*1.
- When thermal shutdown is released*1.
- When recovering from Short-circuit protection detection status*1.

***1.** In this case, the soft-start wait time is eliminated.

The soft-start circuit starts operating after "H" is input to the EN pin and the soft-start wait time (t_{SSW}) = 0.08 ms typ. elapses. The time after V_{OUT} starts rising until $V_{OUT(S)} \times 90\%$ is reached is set internally to 0.25 ms typ.

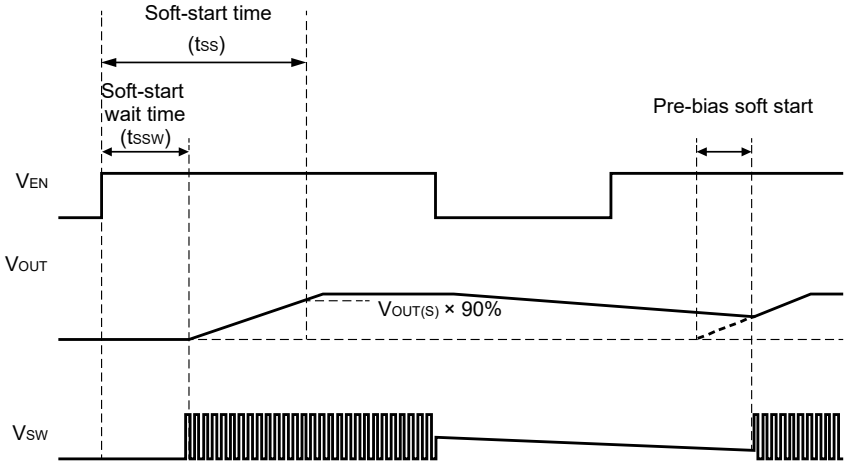


Figure 8

12. Output discharge function

The ICs of type E and F have an output discharging function to discharge output capacitor C_{OUT}.
When the EN pin = "L", the 95 Ω typ. output discharging switch connected to the SW pin turns on and discharges C_{OUT}.

13. Power Good function

This IC has the Power Good function for Nch open drain output to monitor output voltage (V_{OUT}).
If V_{OUT} is within the Power Good detection threshold, the Nch transistor at the PG pin turns off and outputs "H". If V_{OUT} deviates from the Power Good release threshold, the Nch transistor at the PG pin turns on, the PG pin is pulled down, and outputs "L".
Also, the PG pin is pulled down and "L" is output in the following cases.

- The EN pin is at "L" level
- UVLO is detected
- Thermal shutdown is detected
- Soft start operates

If "L" is output, it is pulled down with 70 Ω typ., and when it is pulled up with a power supply, the pull-up resistance is about 3 kΩ to 100 kΩ. The detection threshold and the release threshold have a hysteresis width of 4% typ. The Power Good response time has a 10 μs typ. response delay time for both detection and release.
The PG pin is pulled up with an external resistor, but the application voltage must not exceed the absolute maximum rating. If Power Good output is not used, connect it to open or GND.
Sequence operations can be performed by connecting the PG pin to the EN pin of other S-19952/19953 Series, S-19954/19955 Series.

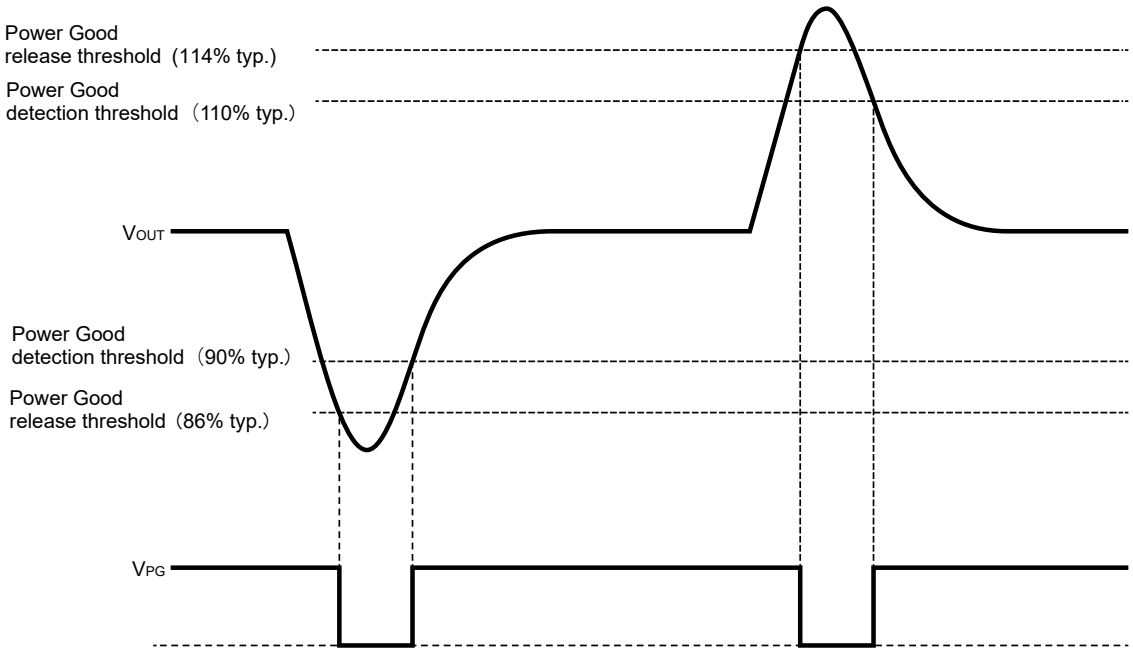
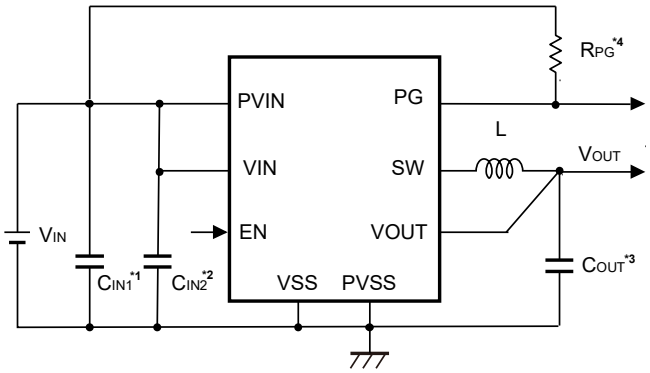


Figure 9

Table 11

Status		Power Good output
During operation ($V_{EN} \geq V_{SH}$)	$V_{OUT} \geq V_{OUT(E)} \times TH_{PG\_UF}$ (114% typ.), V_{OUT} rising	"L"
	$V_{OUT} \leq V_{OUT(E)} \times TH_{PG\_UR}$(110% typ.), V_{OUT} falling	"H" (High-Z)
	$V_{OUT} \geq V_{OUT(E)} \times TH_{PG\_LR}$ (90% typ.), V_{OUT} rising	"H" (High-Z)
	$V_{OUT} \leq V_{OUT(E)} \times TH_{PG\_LF}$ (86% typ.), V_{OUT} falling	"L"
During shutdown operation	$V_{EN} < V_{SL}$	"L"
During UVLO detection.	$V_{IN} < V_{UVLO-}$	"L"
During thermal shutdown detection	$T_{SD} < T_j$	"L"
During soft start operation		"L"

■ Typical Circuit



***1.** C_{IN1} is a capacitor for stabilizing the input. If C_{IN2} is not used, connect C_{IN1} as close to the IC as possible.

***2.** C_{IN2} is a capacitor for stabilizing the input. If the operation is unstable, connect the decoupling capacitor C_{IN2} close to the IC and connect C_{IN1} in parallel with C_{IN2}.

***3.** C_{OUT} is a capacitor for stabilizing the output.

***4.** R_{PG} is a Power Good pull-up resistor. If the PG pin is unused, connect it to open or GND.

Figure 10

Caution The above connection diagram will not guarantee successful operation. Perform thorough evaluation using an actual application to set the constants.

■ External Parts Selection

The recommended values for each external part are shown in **Table 12**, and the recommended parts are shown in **Table 13** to **Table 16**.
When selecting an input capacitor (C_{IN1}, C_{IN2}) and output capacitor (C_{OUT}), take into consideration the temperature range and DC current superposition characteristics to be used.
When selecting an inductor (L), take into consideration the temperature range, DC current superposition characteristics and the rated current value of the inductor to be used.

Table 12

Input voltage range	V_{OUT}	C_{IN1}	C_{IN2}	C_{OUT}	L
2.7 V to 5.5 V	0.8 V to 1.2 V	10 µF	0.1 µF	10 µF	1.5 µH
	0.8 V to 3.3 V	10 µF	0.1 µF	10 µF	2.2 µH
2.7 V to 3.6 V	0.8 V to 1.8 V	10 µF	0.1 µF	10 µF	1.5 µH

Table 13 Recommended Capacitors (C_{IN1}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	CGA4J1X7S1C106K125AC	10 µF	16 V	2.0 mm × 1.25 mm × 1.25 mm
TDK Corporation	CGA4J3X7S1A106K125AB	10 µF	10 V	2.0 mm × 1.25 mm × 1.25 mm
Murata Manufacturing Co., Ltd.	GCM21BC71C106KE36#	10 µF	16 V	2.0 mm × 1.25 mm × 1.25 mm

Table 14 Recommended Capacitors (C_{IN2}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	CGA2B1X7R1C104K050BC	0.1 µF	16 V	1.0 mm × 0.5 mm × 0.5 mm

Table 15 Recommended Capacitors (C_{OUT}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	CGA4J1X7S1C106K125AC	10 µF	16 V	2.0 mm × 1.25 mm × 1.25 mm
TDK Corporation	CGA4J3X7S1A106K125AB	10 µF	10 V	2.0 mm × 1.25 mm × 1.25 mm
Murata Manufacturing Co., Ltd.	GCM21BC71C106KE36#	10 µF	16 V	2.0 mm × 1.25 mm × 1.25 mm
TDK Corporation	CGA3E1X7T0J106M080AC	10 µF	6.3 V	1.6 mm × 0.8 mm × 0.8 mm
Murata Manufacturing Co., Ltd.	GCM188D70J106ME36#	10 µF	6.3 V	1.6 mm × 0.8 mm × 0.8 mm

Table 16 Recommended Inductors (L) List

Manufacturer	Part Number	Inductance	Temperature Range	Dimensions (L × W × H)
TDK Corporation	TFM201610ALMA1R5MTAA	1.5 µH	−55°C to 150°C	2.0 mm × 1.6 mm × 1.0 mm
TDK Corporation	TFM252012ALMA1R5MTAA	1.5 µH	−55°C to 150°C	2.5 mm × 2.0 mm × 1.2 mm
Murata Manufacturing Co., Ltd.	DFE2MCAH1R5MJ0#	1.5 µH	−40°C to 150°C	2.5 mm × 2.0 mm × 1.2 mm
TDK Corporation	TFM252012ALMA2R2MTAA	2.2 µH	−55°C to 150°C	2.5 mm × 2.0 mm × 1.2 mm
TDK Corporation	TFM201610ALMA2R2MTAA	2.2 µH	−55°C to 150°C	2.0 mm × 1.6 mm × 1.0 mm

1. Input capacitor (C_{IN1}, C_{IN2})

C_{IN1} is a capacitor for stabilizing the input. It has an effect to suppress the ripple voltage and switching noise to be generated in the power supply line. Ceramic capacitor with 10 μF or higher is recommended. Connecting a decoupling capacitor C_{IN2} close to the IC and connecting C_{IN1} in parallel with C_{IN2} is effective in stabilizing operation. If C_{IN2} is not used, connect C_{IN1} close to the IC. When selecting a capacitor, take into consideration the temperature range and DC current superposition characteristics.

2. Output capacitor (C_{OUT})

C_{OUT} is used to smooth output voltage. The ripple voltage (V_{RIPPLE}) to be generated in V_{OUT} is inversely proportional to C_{OUT}. When selecting a capacitor whose ESR is sufficiently small, V_{RIPPLE} during current continuous mode is calculated by the following expression. When selecting a capacitor, take into consideration the temperature range and DC current superposition characteristics.

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \times f_{OSC} \times C_{OUT}}$$

In addition, since C_{OUT} contributes to the stability of feedback loop, a ceramic capacitor with 10 μF or higher is recommended. When selecting a capacitor whose capacitance is extremely large, the overcurrent protection function may start the operation and cause a start-up failure.

3. Inductor (L)

To suppress the intrinsic subharmonic oscillation in current mode control, the optimal L value needs to be selected. Considering the slope compensation in the IC, select an inductor from the range of 1.5 μH to 2.2 μH depending on input voltage range and V_{OUT}. When selecting a capacitor, take into consideration DC current superposition characteristics, and operating temperature range, including self rising in temperature.

When selecting L, note the rated current. If a current exceeding the rated current flows through the inductor, magnetic saturation may occur, and there may be risks which substantially lower efficiency and damage the IC as a result of large current.
The ripple current (ΔI_L) and peak current (I_{PK}) flow through the inductor during current continuous mode are calculated by the following expressions respectively. ΔI_L is generally set to approximately 30% of the maximum output current. Make sure I_{PK} will not exceed the rated current of inductor.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{OSC} \times L \times V_{IN}}$$

$$I_{PK} = I_{OUT} + \frac{\Delta I_L}{2}$$

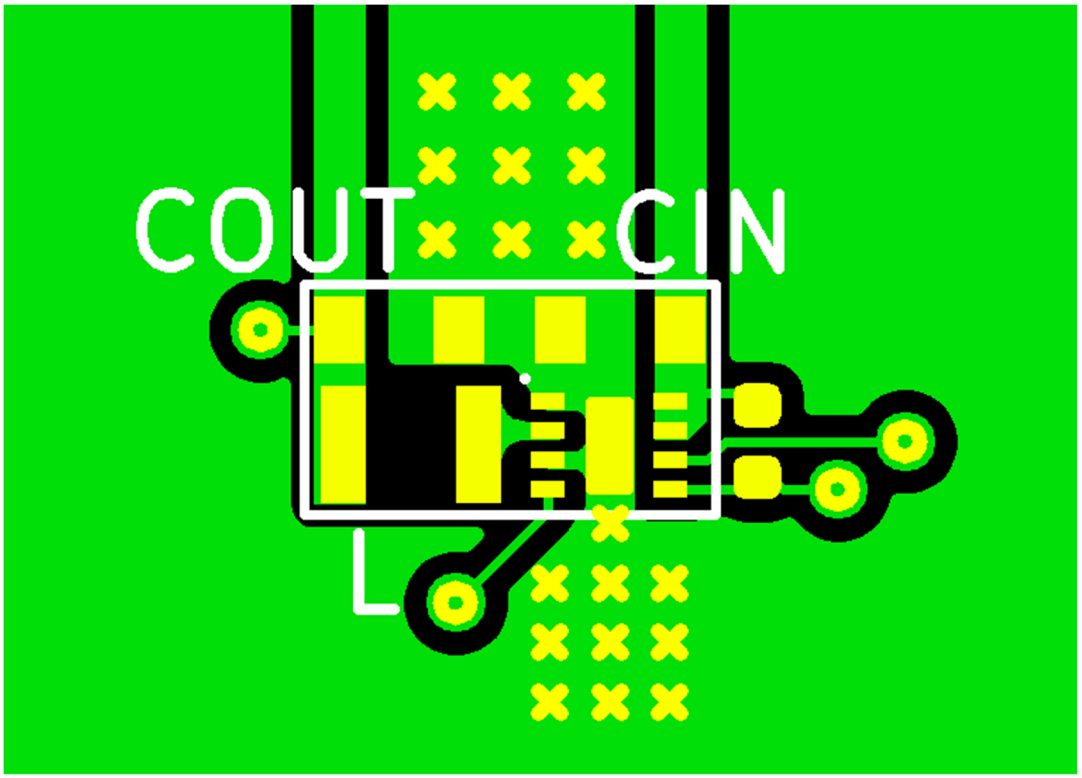
To maintain the rated current of an inductor even in cases V_{OUT} shorts to V_{SS} or other fault conditions occur, the inductor with the rated current, the maximum value of limit current (I_{LIM}) or higher, needs to be selected.

Caution Switching regulators generally oscillate depending on selection of external parts.
The characteristics of external parts, including temperature characteristics, should be evaluated carefully in actual applications to verify that they do not oscillate.

■ Board Layout Guidelines

Note the following cautions when determining the board layout for this IC.

- Place C_{IN} as close to the VIN pin and the VSS pin as possible. Prioritize the layout of C_{IN}.
- Mount C_{IN} on the same surface layer as the IC. If they are connected through thermal vias, the impedance of the thermal vias may influence the operation, resulting in unstable condition.
- Connecting a decoupling capacitor C_{IN2} close to the IC and connecting C_{IN1} in parallel with C_{IN2} is effective in stabilizing operation. If C_{IN2} is not used, connect C_{IN1} close to the IC.
- Do not place the VOUT pin close to noise sources such as the wiring of SW pin to avoid unstable operations. The VOUT pin wire may be surrounded by a GND pattern.
- Connect PVSS and VSS pins with a GND pattern on the surface layer.
- Make the GND pattern as wide as possible.
- Place thermal vias in the GND pattern to ensure sufficient heat dissipation.
- Large current flows through the SW pin. Make the wiring area of the pattern to be connected to the SW pin small to minimize parasitic capacitance and emission noise.
- Make a short loop wiring of the SW pin → L → C_{OUT} → PVSS and VSS pins. This is effective to reduce emission noise.
- Do not wire the SW pin pattern under the IC.
- As much as possible, do not draw a pattern directly under the inductor (L), including the surface layer and the back layer.



Total size 5.5 mm × 3.1 mm = 17.05 mm^2

Figure 11 Reference Board Pattern

Caution **The above pattern diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to determine the pattern.**

Remark Power Good pull-up resistor (R_{PG}) is optional.

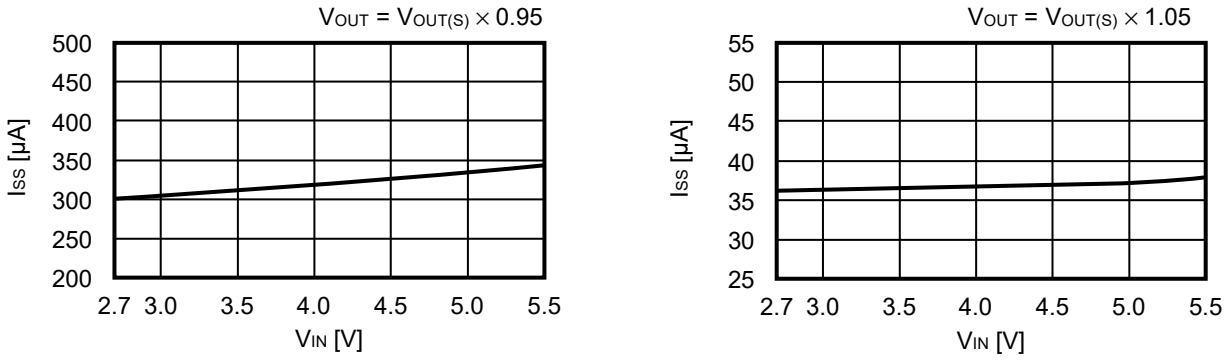
■ Precautions

- Mount external capacitors and inductors as close as possible to the IC, and make single GND.
- Characteristic ripple voltage and spike noise occur in the IC containing switching regulators. Moreover rush current flows at the time of a power supply injection. Because these largely depend on the inductor, the capacitor and impedance of power supply to be used, fully check them using an actually mounted model.
- C_{IN} connected between the PVIN (VIN) pin and the PVSS (VSS) pin is a bypass capacitor (refer to "**■ Typical Circuit**"). It stabilizes the power supply in the IC, and thus effectively works for stable switching regulator operation. Allocate the bypass capacitor as close to the IC as possible, prioritized over other parts.
- Connecting a decoupling capacitor C_{IN2} close to the IC and connecting C_{IN1} in parallel with C_{IN2} is effective in stabilizing operation. If C_{IN2} is not used, connect C_{IN1} close to the IC.
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- The power dissipation of the IC greatly varies depending on the size and material of the board to be connected. Perform sufficient evaluation using an actual application before designing.
- ABLIC Inc. assumes no responsibility for the way in which this IC is used on products created using this IC or for the specifications of that product, nor does ABLIC Inc. assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Japan or in other countries.

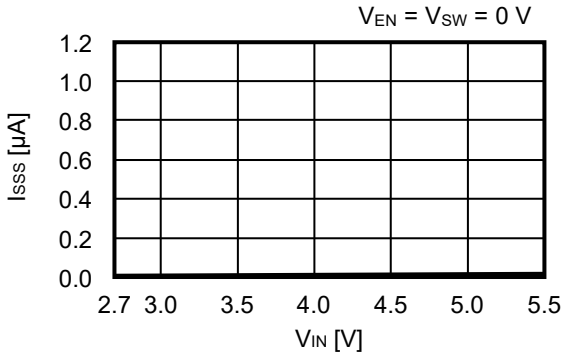
■ Characteristics (Typical Data)

1. Example of major power supply dependence characteristics (Ta = +25°C)

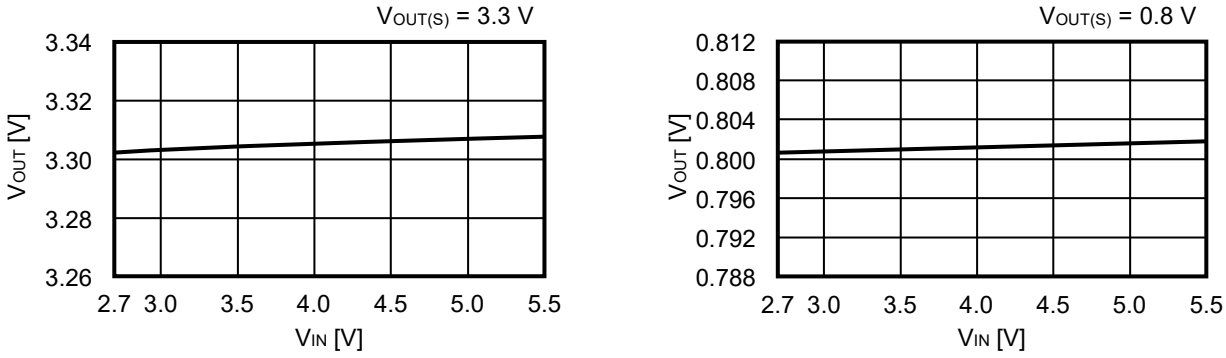
1. 1 Current consumption during switching off (I_{SS}) vs. Input voltage (V_{IN})



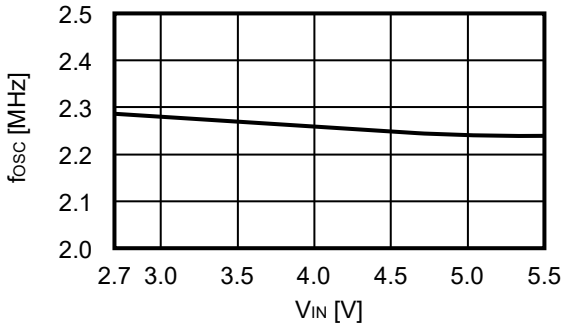
1. 2 Current consumption during shutdown (I_{SSS}) vs. Input voltage (V_{IN})



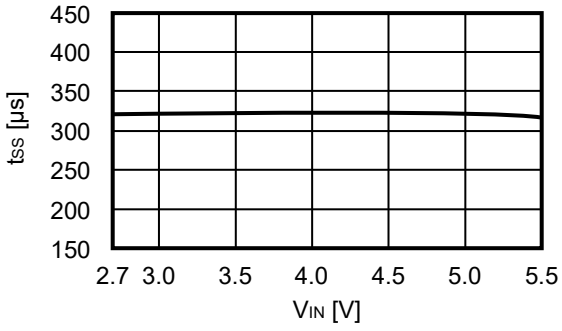
1. 3 VOUT detection voltage (V_{OUT}) vs. Input voltage (V_{IN})



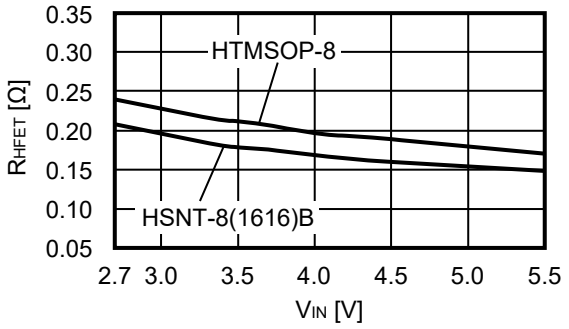
1. 4 Oscillation frequency (f_{OSC}) vs. Input voltage (V_{IN})



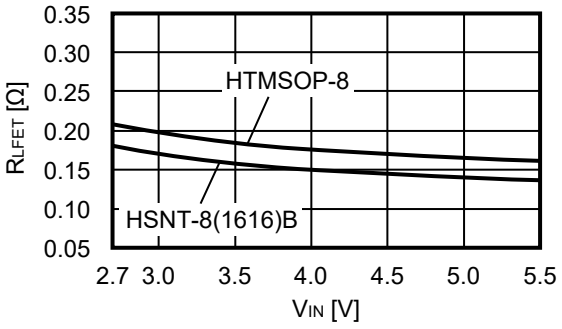
1. 5 Soft-start time (t_{SS}) vs. Input voltage (V_{IN})



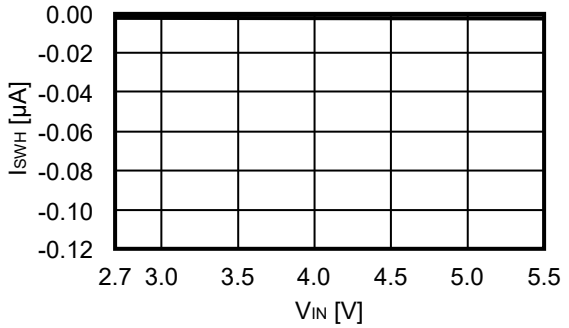
1. 6 High side power MOS FET on-resistance (R_{HFET}) vs. Input voltage (V_{IN})



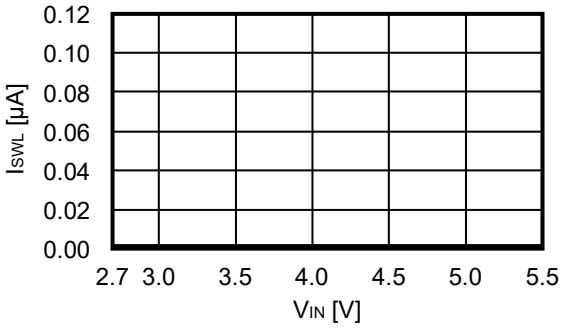
1. 7 Low side power MOS FET on-resistance (R_{LFET}) vs. Input voltage (V_{IN})



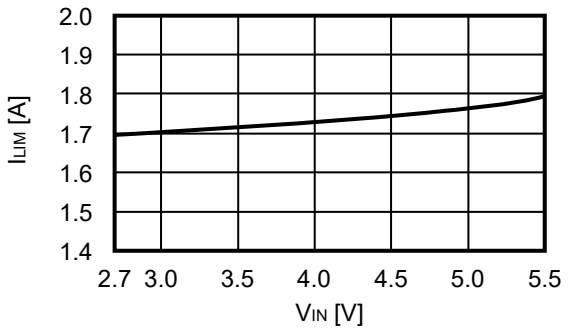
1. 8 SW pin leakage current "H" (I_{SWH}) vs. Input voltage (V_{IN})



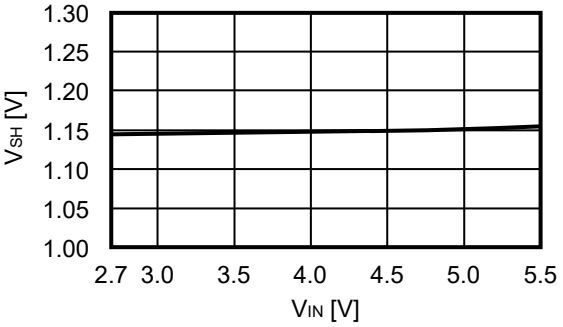
1. 9 SW pin leakage current "L" (I_{SWL}) vs. Input voltage (V_{IN})



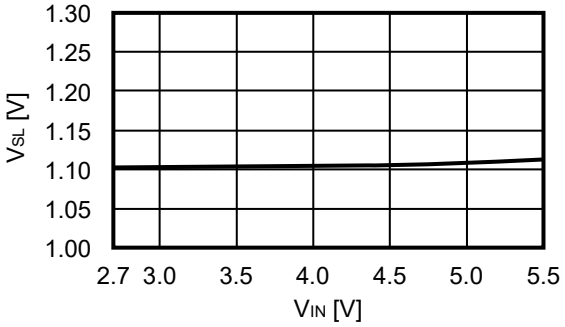
1. 10 Limit current (I_{LIM}) vs. Input voltage (V_{IN})



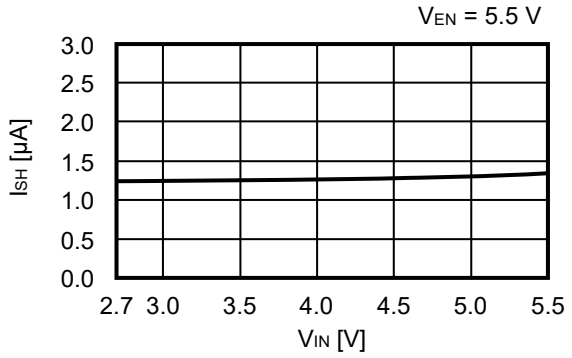
1. 11 High level input voltage (V_{SH}) vs. Input voltage (V_{IN})



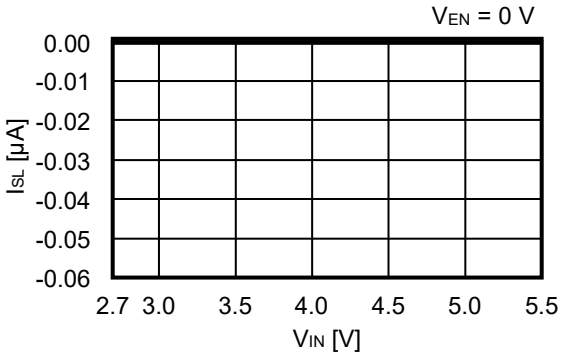
1. 12 Low level input voltage (V_{SL}) vs. Input voltage (V_{IN})



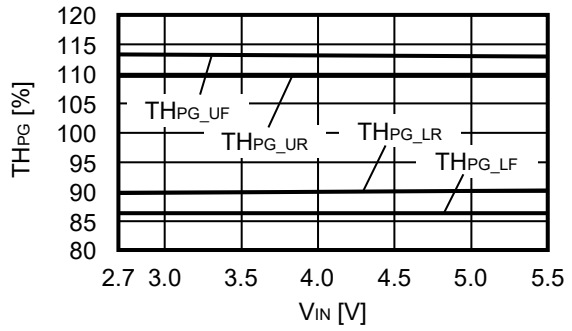
1. 13 High level input current (I_{SH}) vs Input voltage (V_{IN})



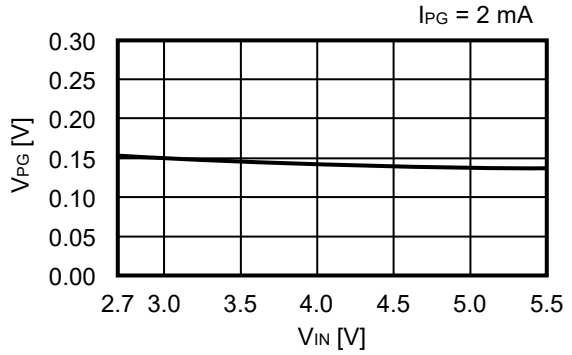
1. 14 Low level input current (I_{SL}) vs Input voltage (V_{IN})



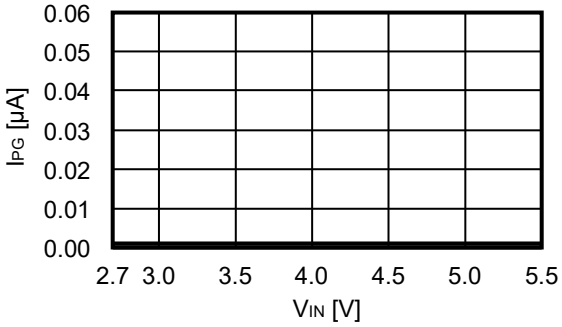
1. 15 Power Good threshold (TH_{PG}) vs Input voltage (V_{IN})



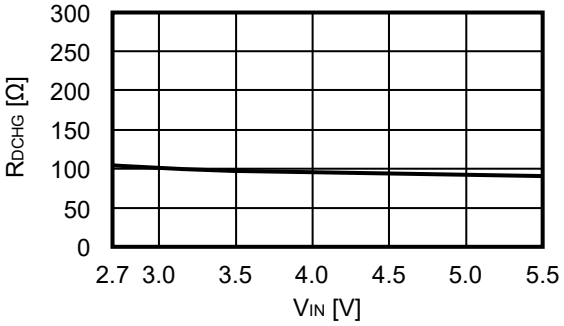
1. 16 PG pin low level voltage (V_{PG}) vs Input voltage (V_{IN})



1. 17 PG pin leakage current (I_{PG}) vs Input voltage (V_{IN})

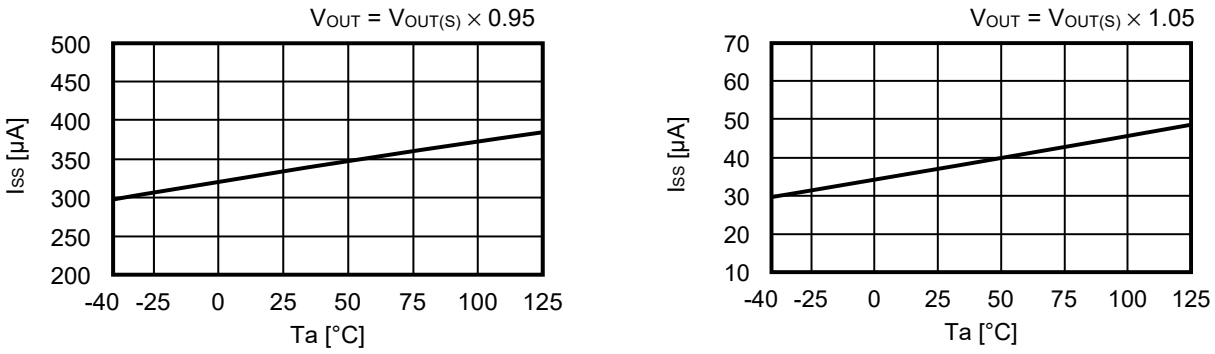


1. 18 SW pin discharge switch resistance value (R_{DCHG}) vs Input voltage (V_{IN})

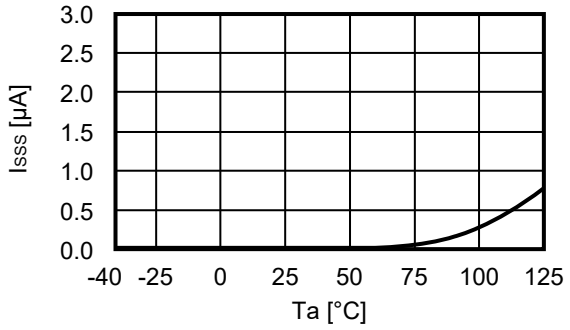


2. Example of major temperature characteristics (Ta = –40°C to +125°C, V_{IN} = 5.0 V)

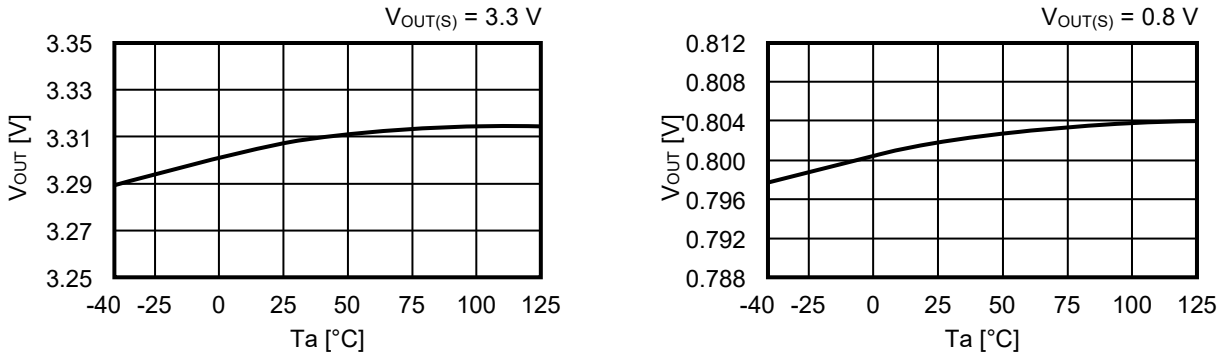
2. 1 Current consumption during switching off (I_{SS}) vs. Temperature (Ta)



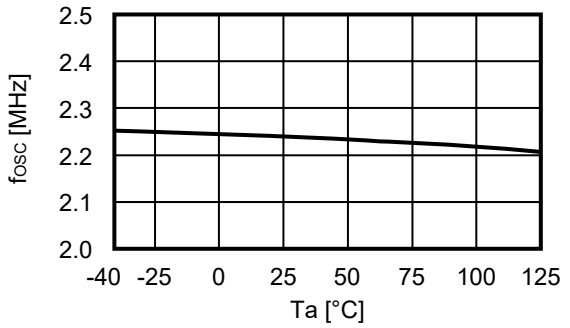
2. 2 Current consumption during shutdown (I_{SSS}) vs. Temperature (Ta)



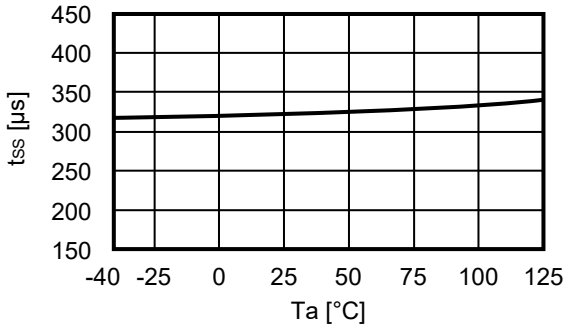
2. 3 VOUT detection voltage (V_{OUT}) vs. Temperature (Ta)



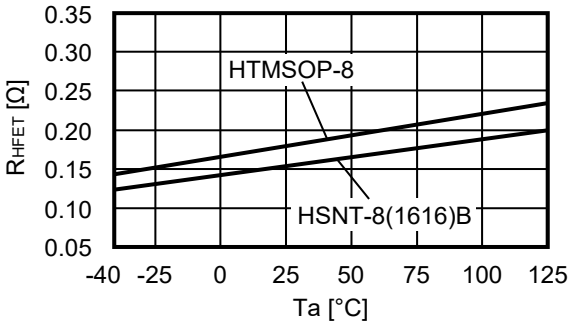
2. 4 Oscillation frequency (f_{OSC}) vs. Temperature (Ta)



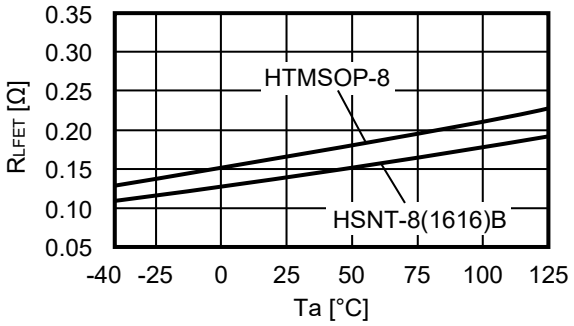
2. 5 Soft-start time (t_{SS}) vs. Temperature (Ta)



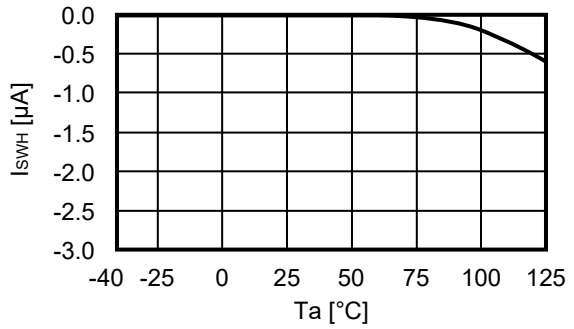
2. 6 High side power MOS FET on-resistance (R_{HFET}) vs. Temperature (Ta)



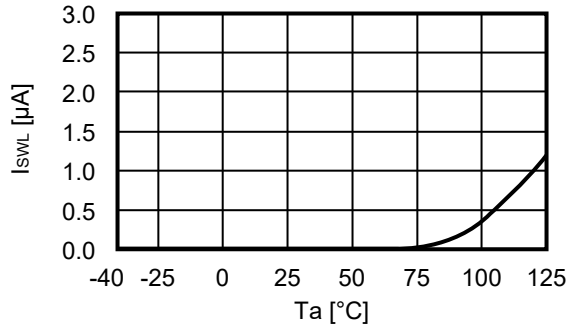
2. 7 Low side power MOS FET on-resistance (R_{LFET}) vs. Temperature (Ta)



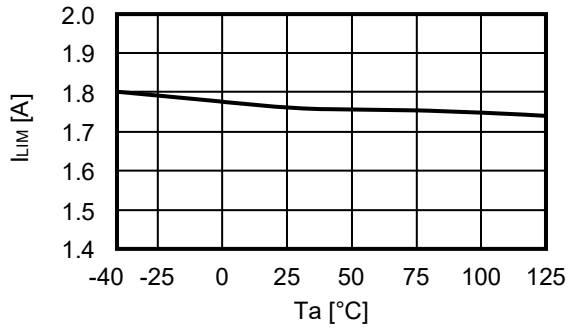
2. 8 High side power MOS FET leakage current (I_{SWH}) vs. Temperature (Ta)



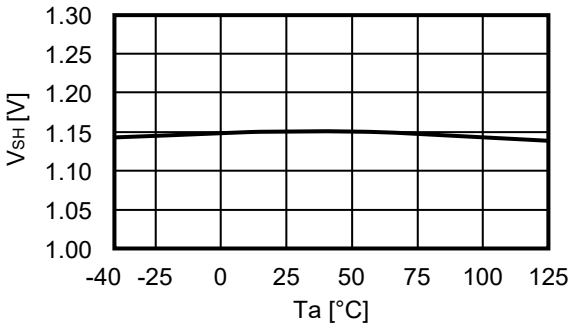
2. 9 Low side power MOS FET leakage current (I_{SWL}) vs. Temperature (Ta)



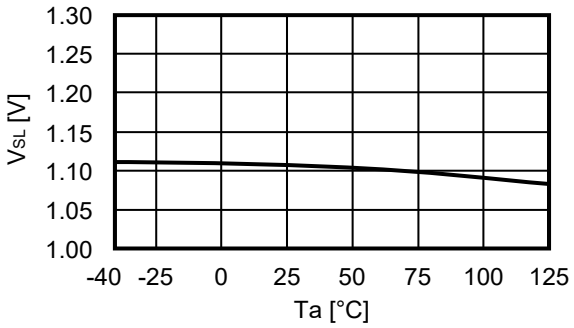
2. 10 Limit current (I_{LIM}) vs. Temperature (Ta)



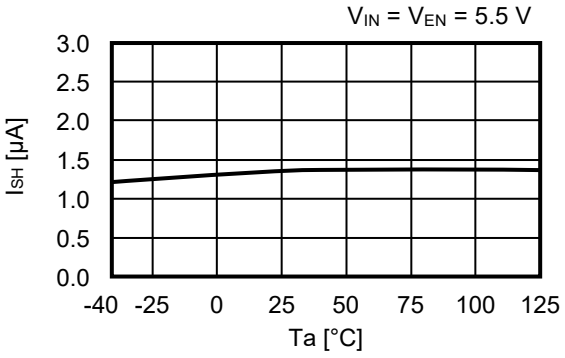
2. 11 High level input voltage (V_{SH}) vs. Temperature (Ta)



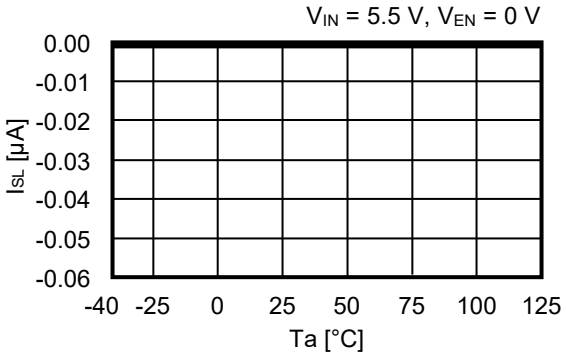
2. 12 Low level input voltage (V_{SL}) vs. Temperature (Ta)



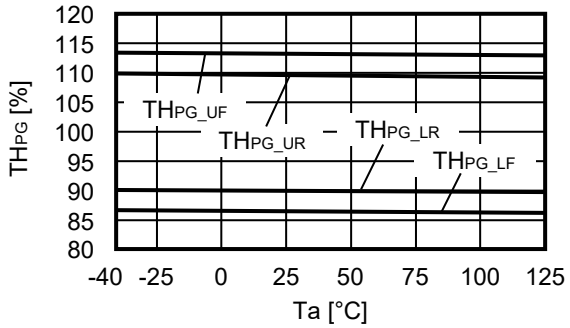
2. 13 High level input current (I_{SH}) vs. Temperature (Ta)



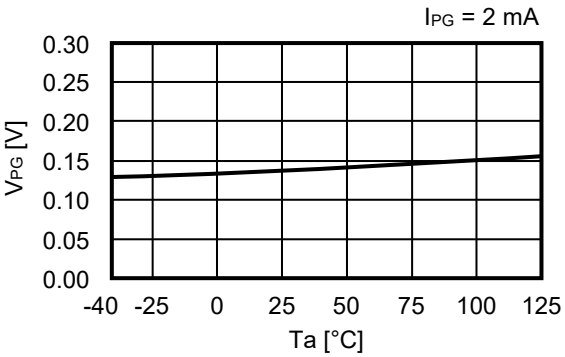
2. 14 Low level input voltage (I_{SL}) vs. Temperature (Ta)



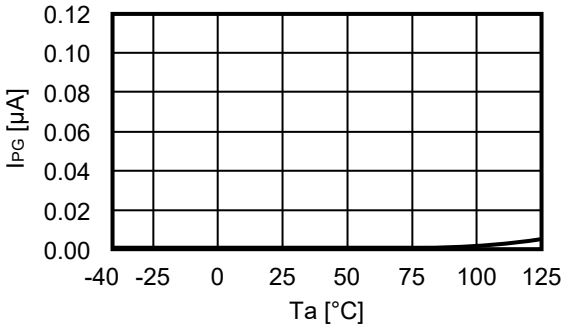
2. 15 Power Good threshold (TH_{PG}) vs. Temperature (Ta)



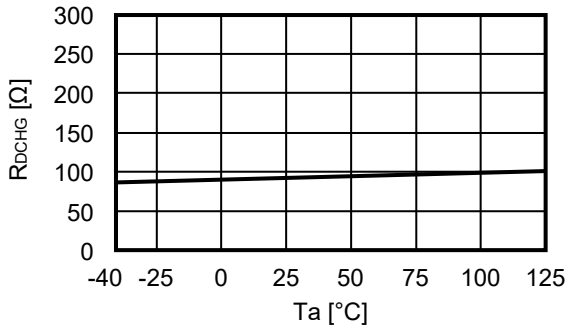
2. 16 PG pin low level voltage (V_{PG}) vs. Temperature (Ta)



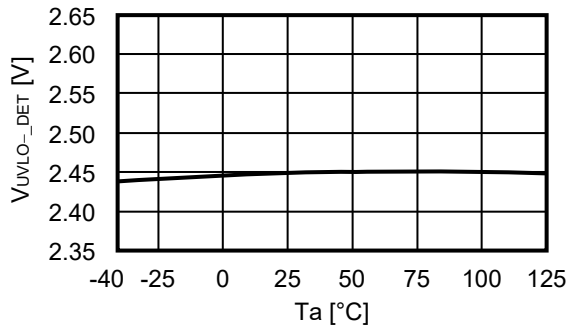
2. 17 PG pin leakage current (I_{PG}) vs. Temperature (Ta)



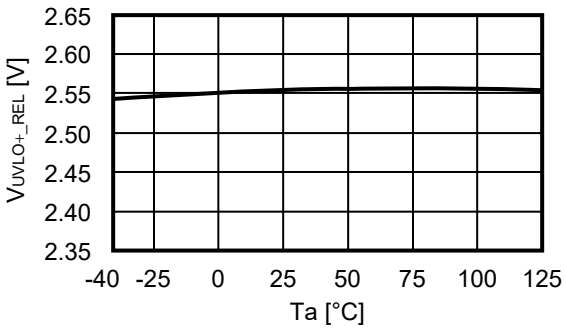
2. 18 SW pin discharge switch resistance value (R_{DCHG}) vs. Temperature (Ta)



2. 19 UVLO detection voltage (V_{UVLO-}) vs. Temperature (Ta)



2. 20 UVLO release voltage (V_{UVLO+}) vs. Temperature (Ta)



3. Transient response characteristics (Ta = +25°C)

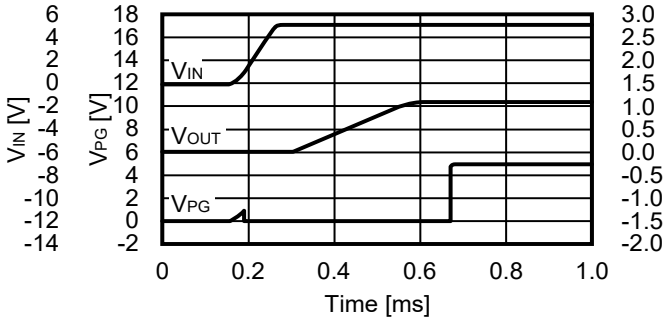
The external parts shown in **Table 17** are used in "**3. Transient response characteristics**".

Table 17

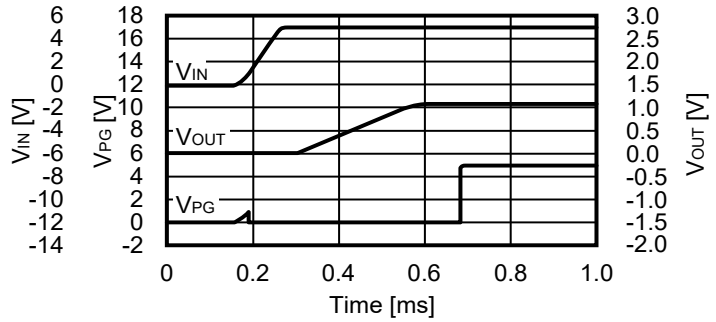
Element Name	Constant	Manufacturer	Part Number
Inductor	1.5 µH	TDK Corporation	TFM201610ALMA1R5MTAA
Input capacitor	10 µF	TDK Corporation	CGA4J1X7S1C106K125AC
Output capacitor	10 µF	TDK Corporation	CGA4J1X7S1C106K125AC
Power Good pull-up resistor	33 kΩ	–	–

3. 1 Power-on ($V_{OUT(S)}$ = 1.1 V, V_{IN} = V_{EN} = 0 V → 5 V, Ta = +25°C, R_{PG} = 33 kΩ (Connect to V_{IN}))

3. 1. 1 I_{OUT} = 1 mA

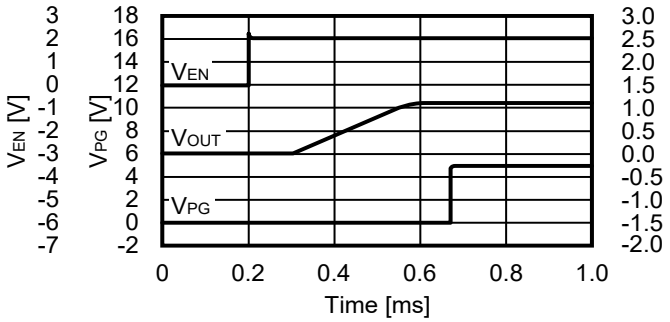


3. 1. 2 I_{OUT} = 1 A

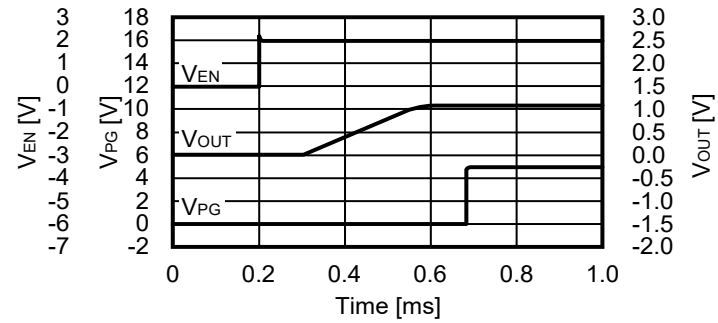


3. 2 Transient response characteristics of EN pin
($V_{OUT(S)}$ = 1.1 V, V_{IN} = 5 V, V_{EN} = 0 V → 2 V, Ta = +25°C, R_{PG} = 33 kΩ (Connect to V_{IN}))

3. 2. 1 I_{OUT} = 1 mA



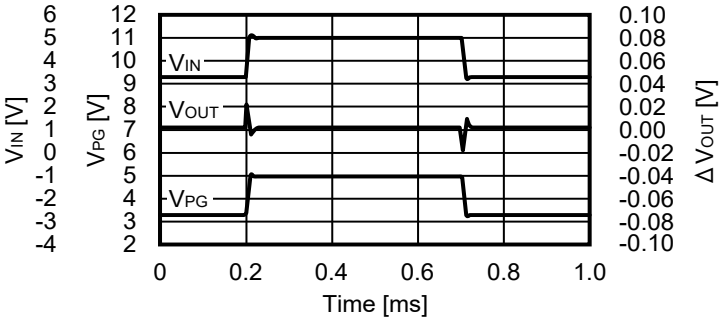
3. 2. 2 I_{OUT} = 1 A



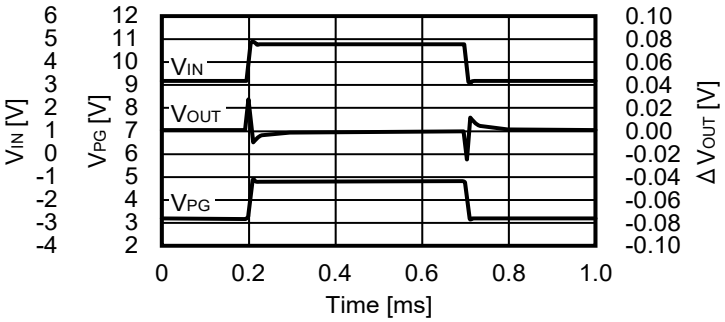
3. 3 Line transient response

($V_{OUT(S)}$ = 1.1 V, V_{IN} = 3.3 V → 5 V → 3.3 V, Ta = +25°C, R_{PG} = 33 kΩ (Connect to V_{IN}))

3. 3. 1 I_{OUT} = 1 mA



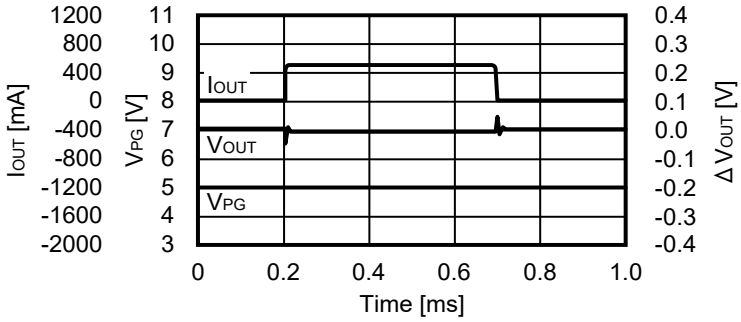
3. 3. 2 I_{OUT} = 1 A



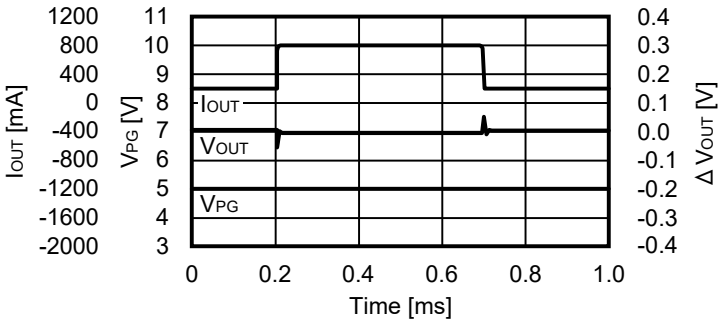
3. 4 Load transient response

($V_{OUT(S)}$ = 1.1 V, V_{IN} = 5 V, Ta = +25°C, R_{PG} = 33 kΩ (Connect to V_{IN}))

3. 4. 1 I_{OUT} = 10 mA → 500 mA → 10 mA

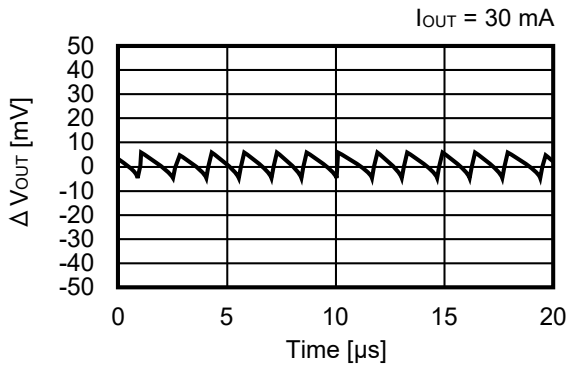


3. 4. 2 I_{OUT} = 200 mA → 800 mA → 200 mA

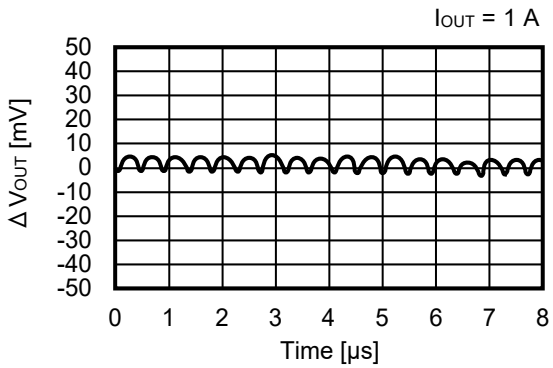


3. 5 Output ripple voltage ($V_{OUT(S)}$ = 1.1 V, V_{IN} = 5 V, Ta = +25°C)

3. 5. 1 S-19955 Series



3. 5. 2 S-19954/19955 Series



■ Reference Data

The external parts shown in **Table 18** are used in "■ **Reference Data**".

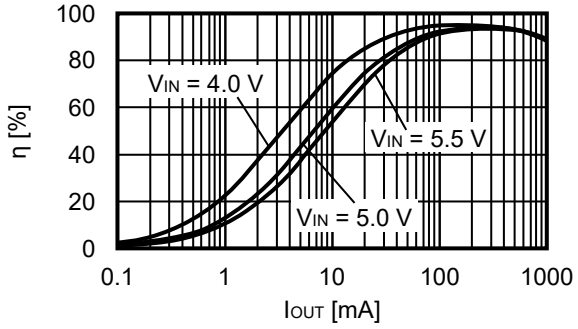
Table 18

Condition	Inductor (L)	Input Capacitor (C_{IN})	Output Capacitor (C_{OUT})
<1>	TFM201610ALMA2R2MTAA (2.2 μH) TDK Corporation	CGA4J1X7S1C106K125AC (10 μF) TDK Corporation	CGA4J3X7S1A106K125AB (10 μF) TDK Corporation
<2>	TFM201610ALMA1R5MTAA (1.5 μH) TDK Corporation	CGA4J1X7S1C106K125AC (10 μF) TDK Corporation	CGA4J3X7S1A106K125AB (10 μF) TDK Corporation

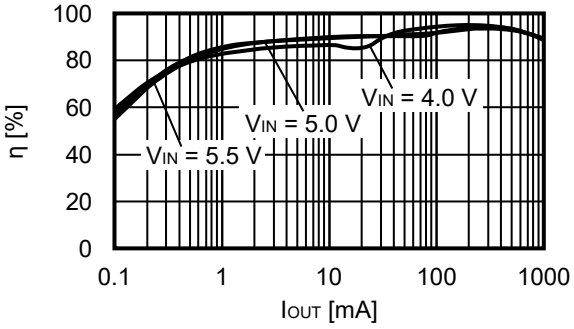
1. V_{OUT} = 3.3 V (External parts: Condition <1>)

1. 1 Efficiency (η) vs. Output current (I_{OUT})

1. 1. 1 S-19954 Series

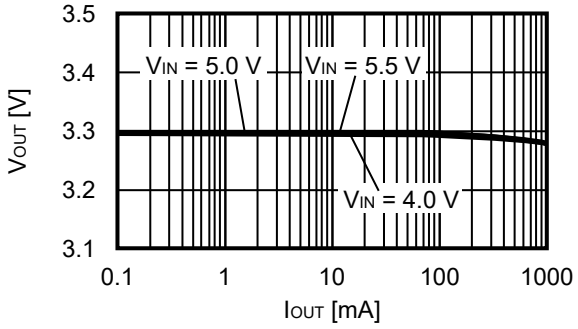


1. 1. 2 S-19955 Series

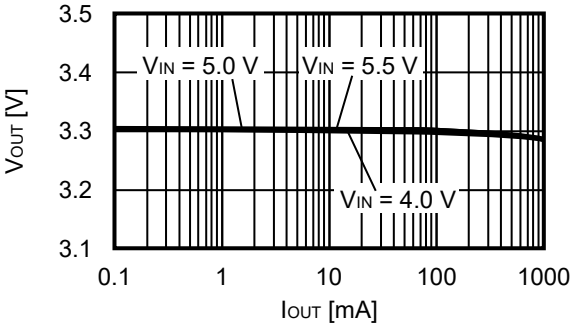


1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})

1. 2. 1 S-19954 Series

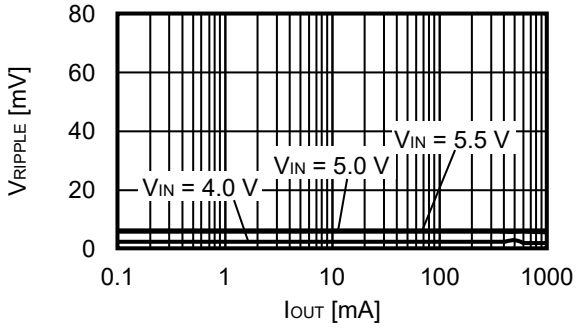


1. 2. 2 S-19955 Series

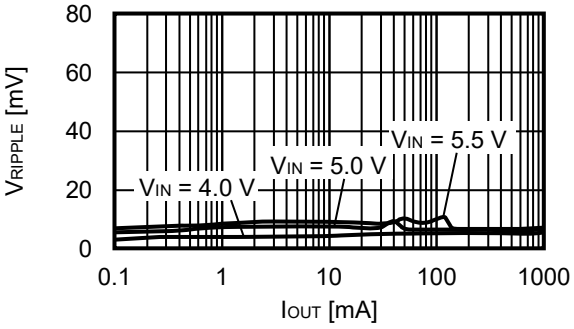


1. 3 Ripple voltage (V_{RIPPLE}) vs. Output current (I_{OUT})

1. 3. 1 S-19954 Series



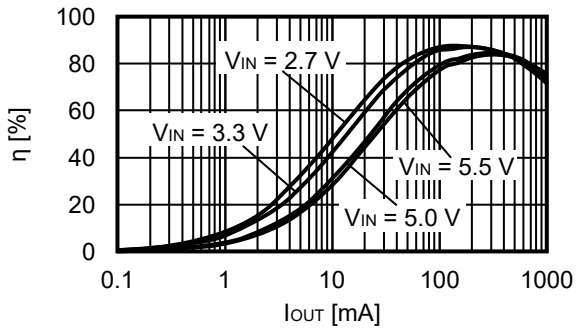
1. 3. 2 S-19955 Series



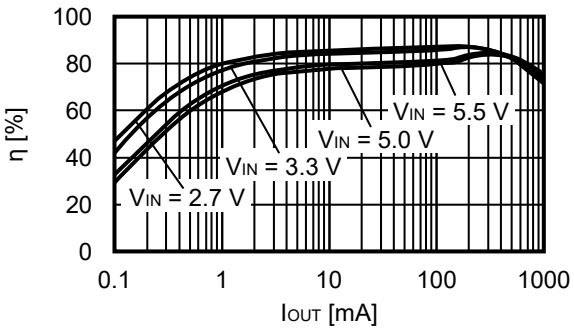
2. V_{OUT} = 1.1 V (External parts: Condition <2>)

2. 1 Efficiency (η) vs. Output current (I_{OUT})

2. 1. 1 S-19954 Series

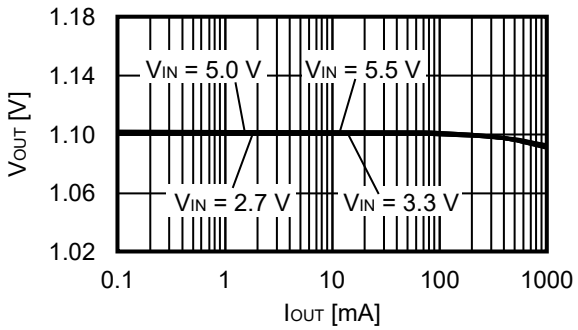


2. 1. 2 S-19955 Series

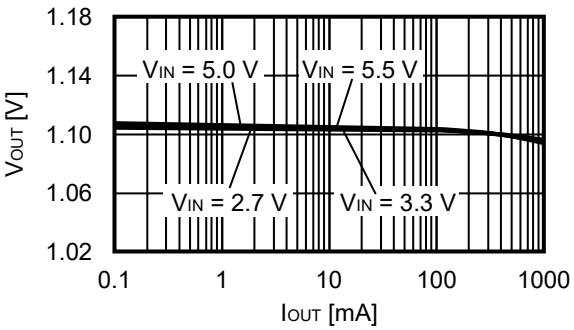


2. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})

2. 2. 1 S-19954 Series

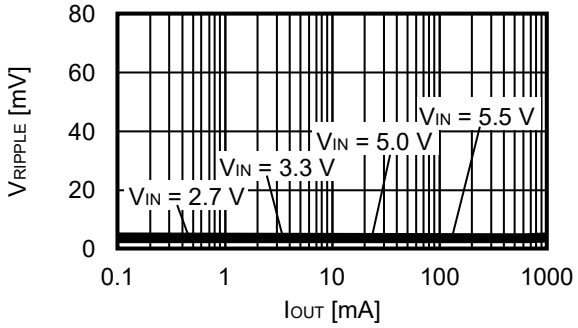


2. 2. 2 S-19955 Series

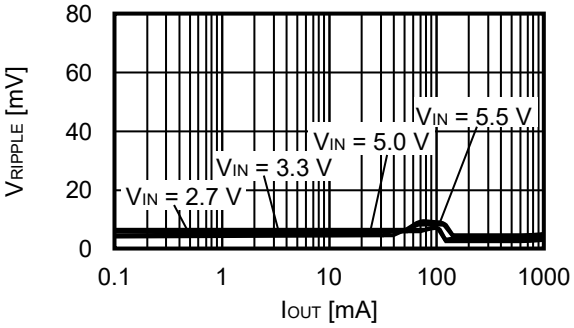


2. 3 Ripple voltage (V_{RIPPLE}) vs. Output current (I_{OUT})

2. 3. 1 S-19954 Series

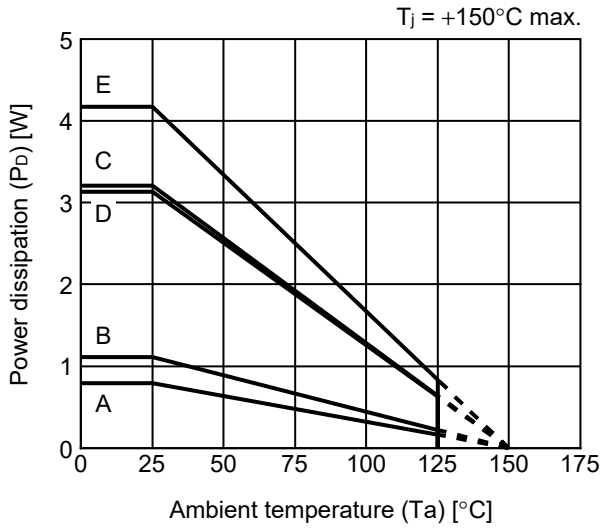


2. 3. 2 S-19955 Series



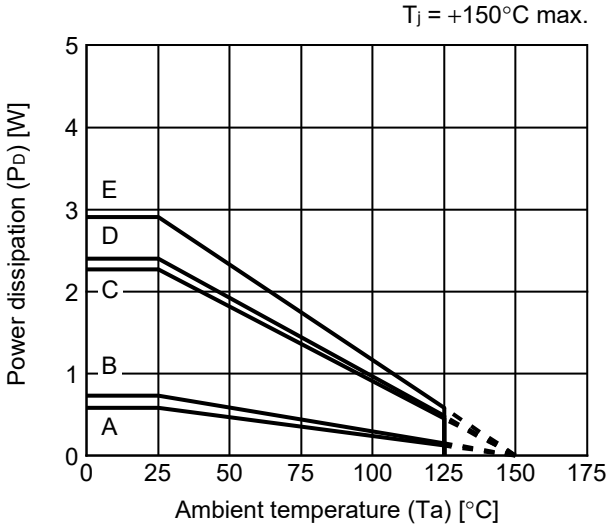
■ Power Dissipation

HTMSOP-8



Board	Power Dissipation (P_D)
A	0.79 W
B	1.11 W
C	3.21 W
D	3.13 W
E	4.17 W

HSNT-8(1616)B

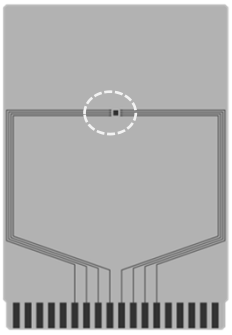


Board	Power Dissipation (P_D)
A	0.58 W
B	0.73 W
C	2.40 W
D	2.27 W
E	2.91 W

HTMSOP-8 Test Board

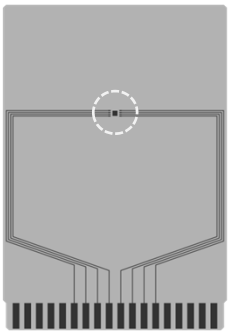
IC Mount Area

(1) Board A



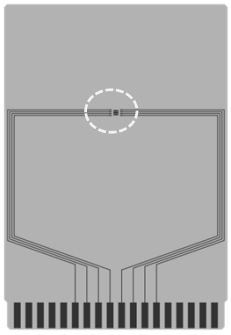
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

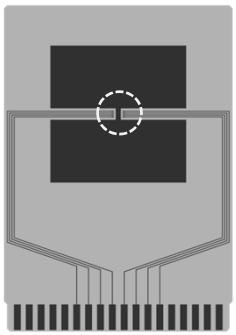
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HTMSOP8-A-Board-SD-1.0

HTMSOP-8 Test Board

IC Mount Area

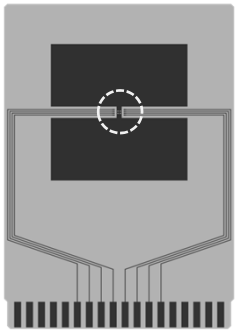
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



enlarged view

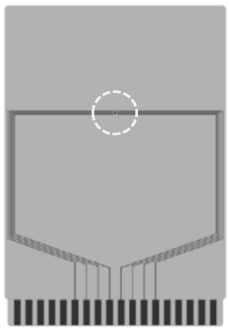
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HTMSOP8-A-Board-SD-1.0

HSNT-8(1616)B Test Board

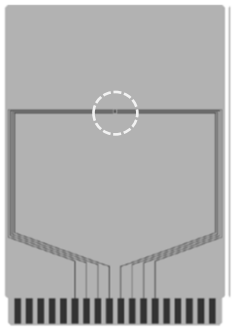
IC Mount Are

(1) Board A



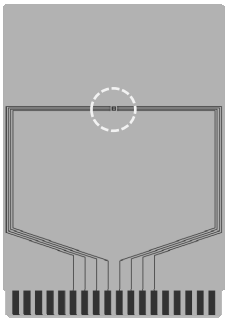
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

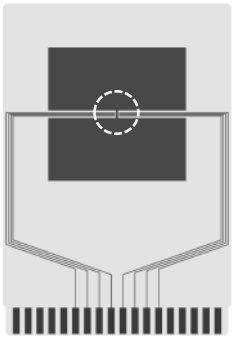
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-C-Board-SD-1.0

HSNT-8(1616)B Test Board

IC Mount Are

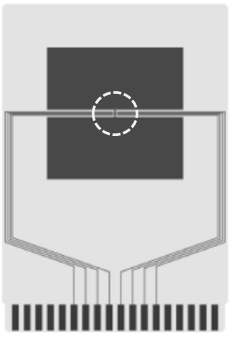
(4) Board D



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

enlarged view

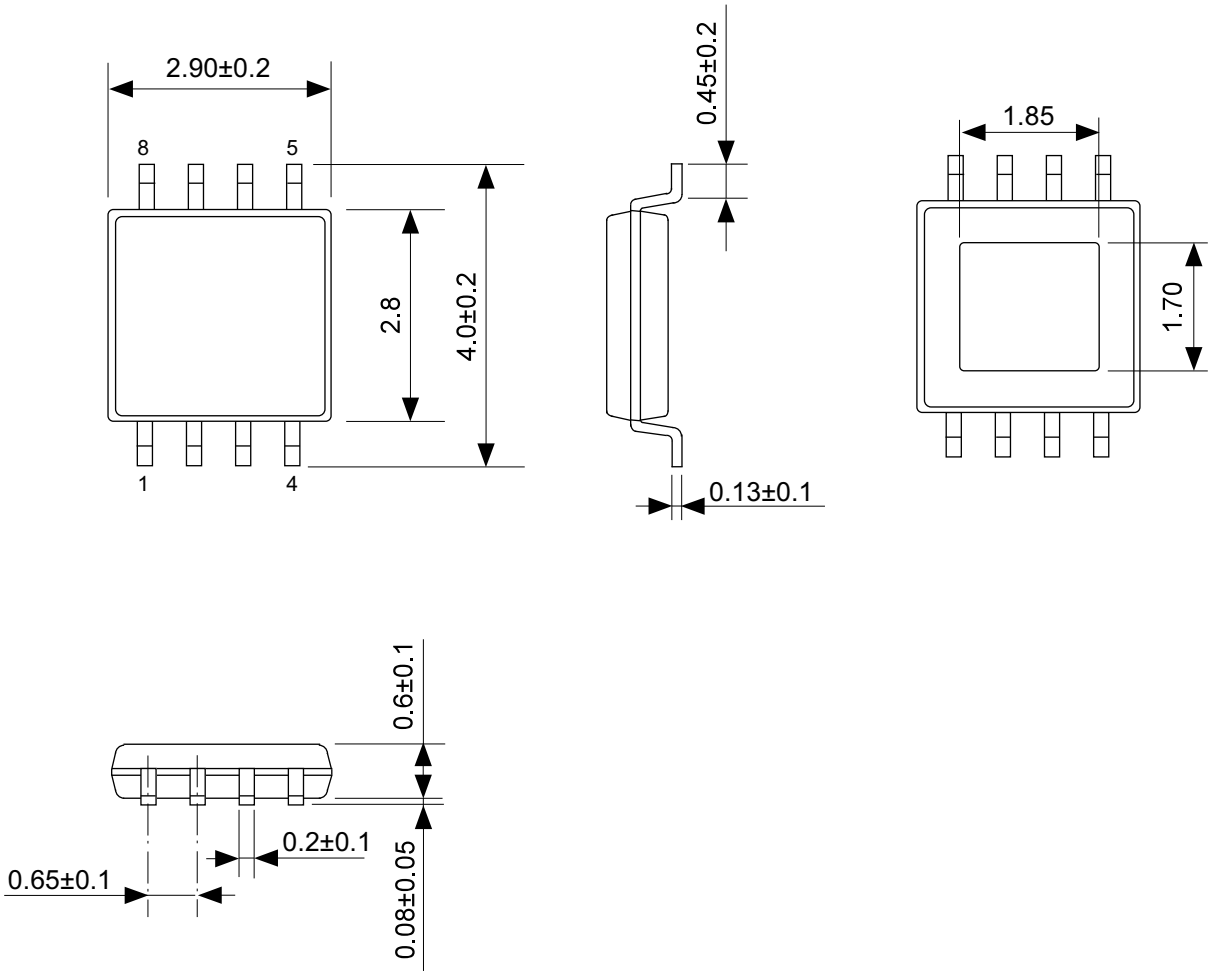
(5) Board E



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

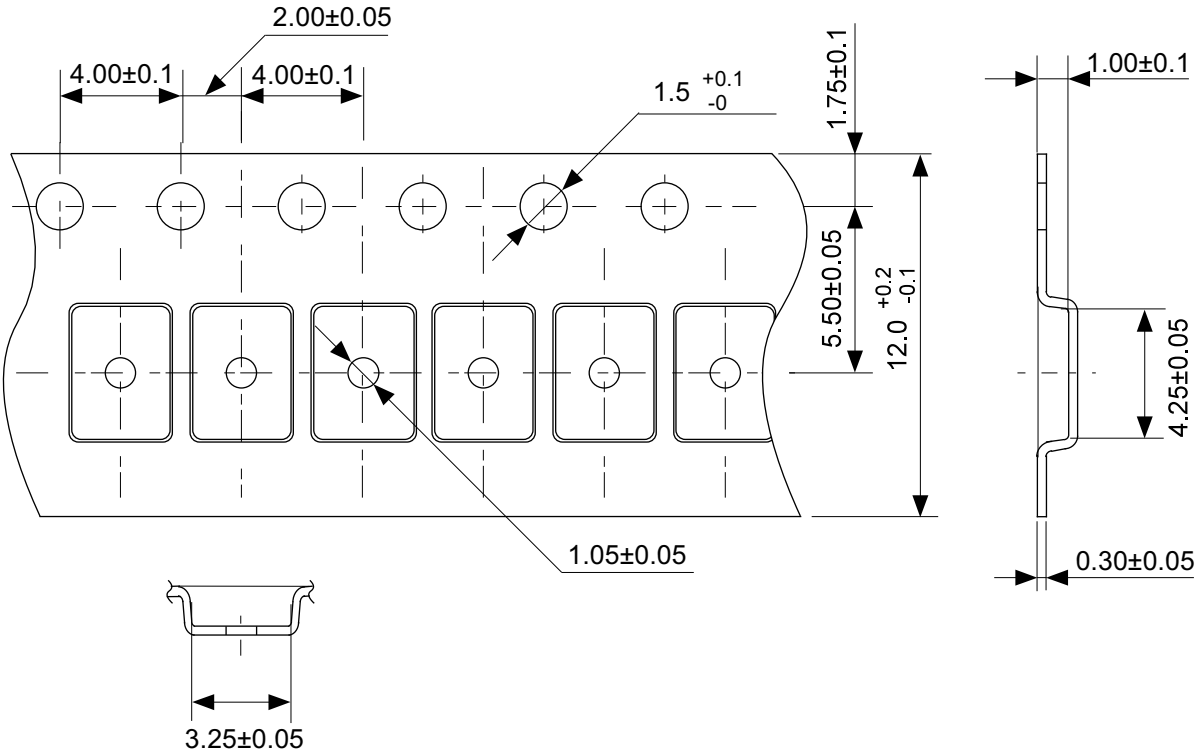
enlarged view

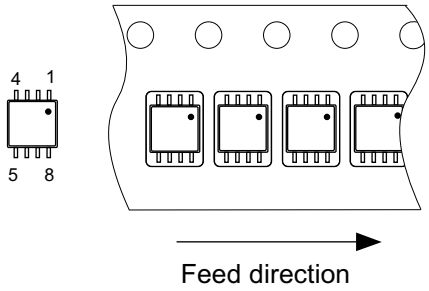
No. HSNT8-C-Board-SD-1.0



No. FP008-A-P-SD-2.0

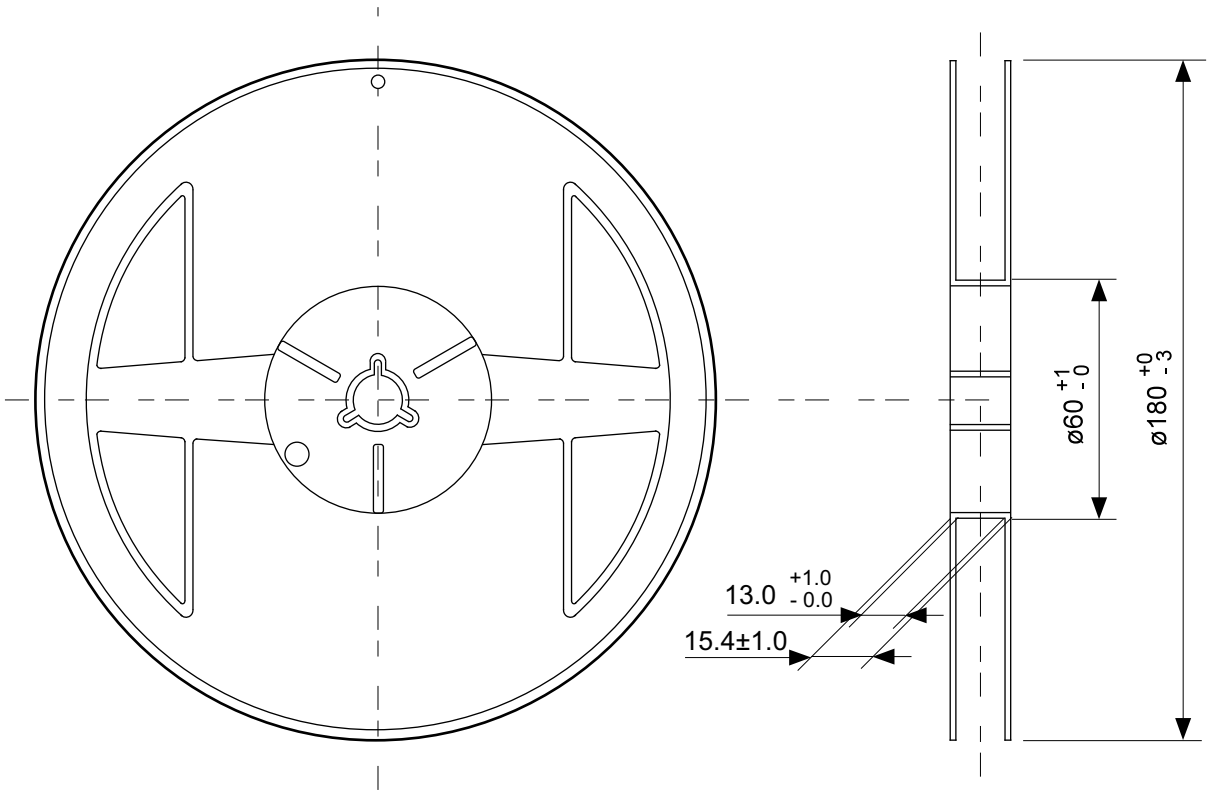
TITLE	HTMSOP8-A-PKG Dimensions
No.	FP008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



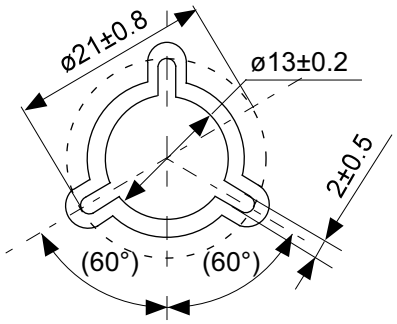


No. FP008-A-C-SD-1.0

TITLE	HTMSOP8-A-Carrier Tape
No.	FP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

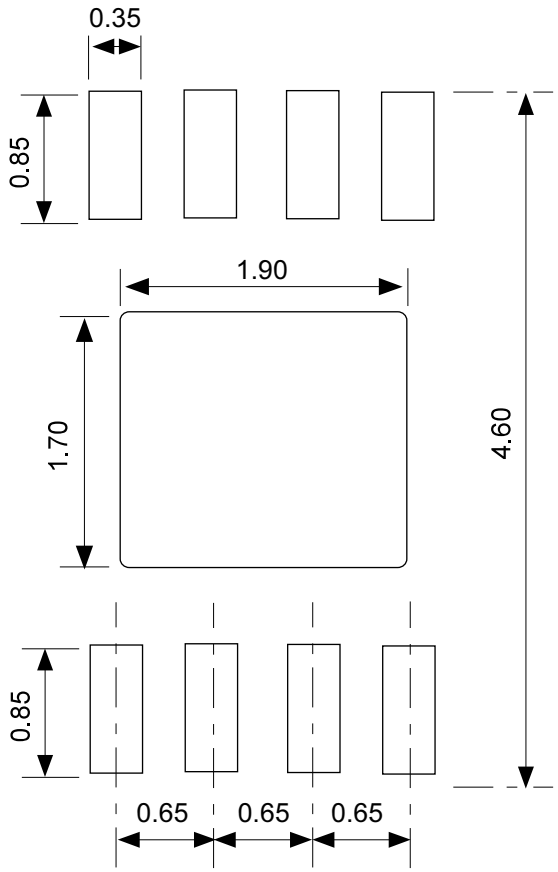


Enlarged drawing in the central part



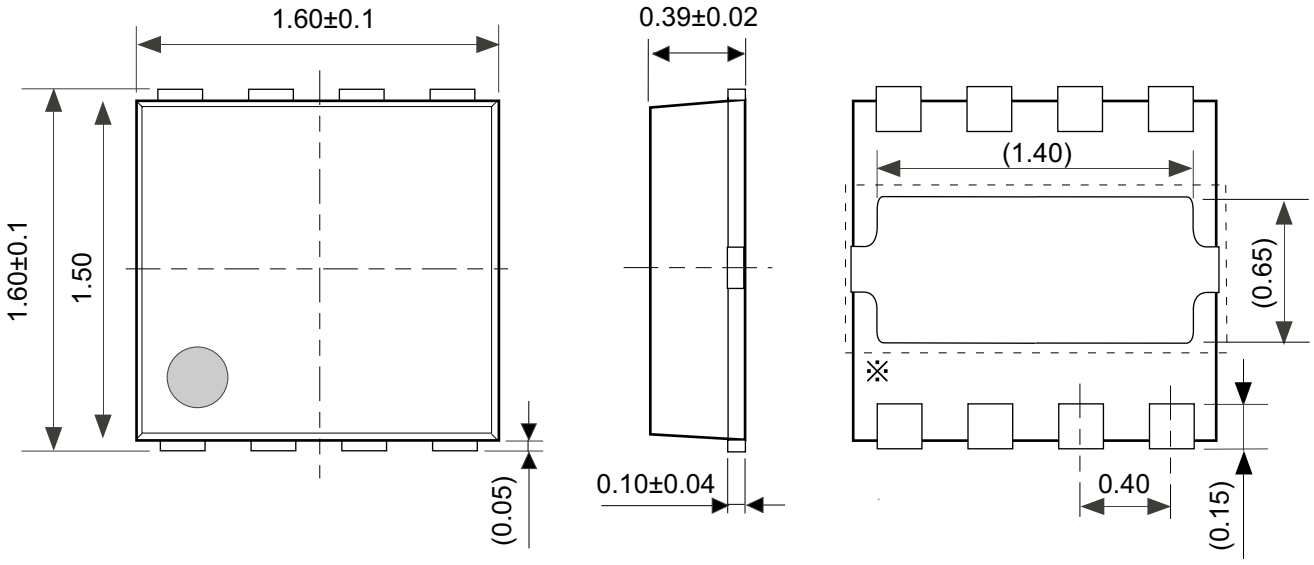
No. FP008-A-R-SD-2.0

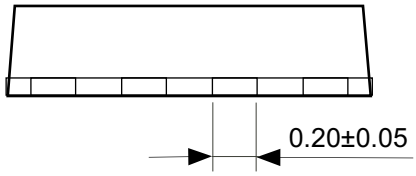
TITLE	HTMSOP8-A-Reel		
No.	FP008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



No. FP008-A-L-SD-2.0

TITLE	HTMSOP8-A -Land Recommendation
No.	FP008-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

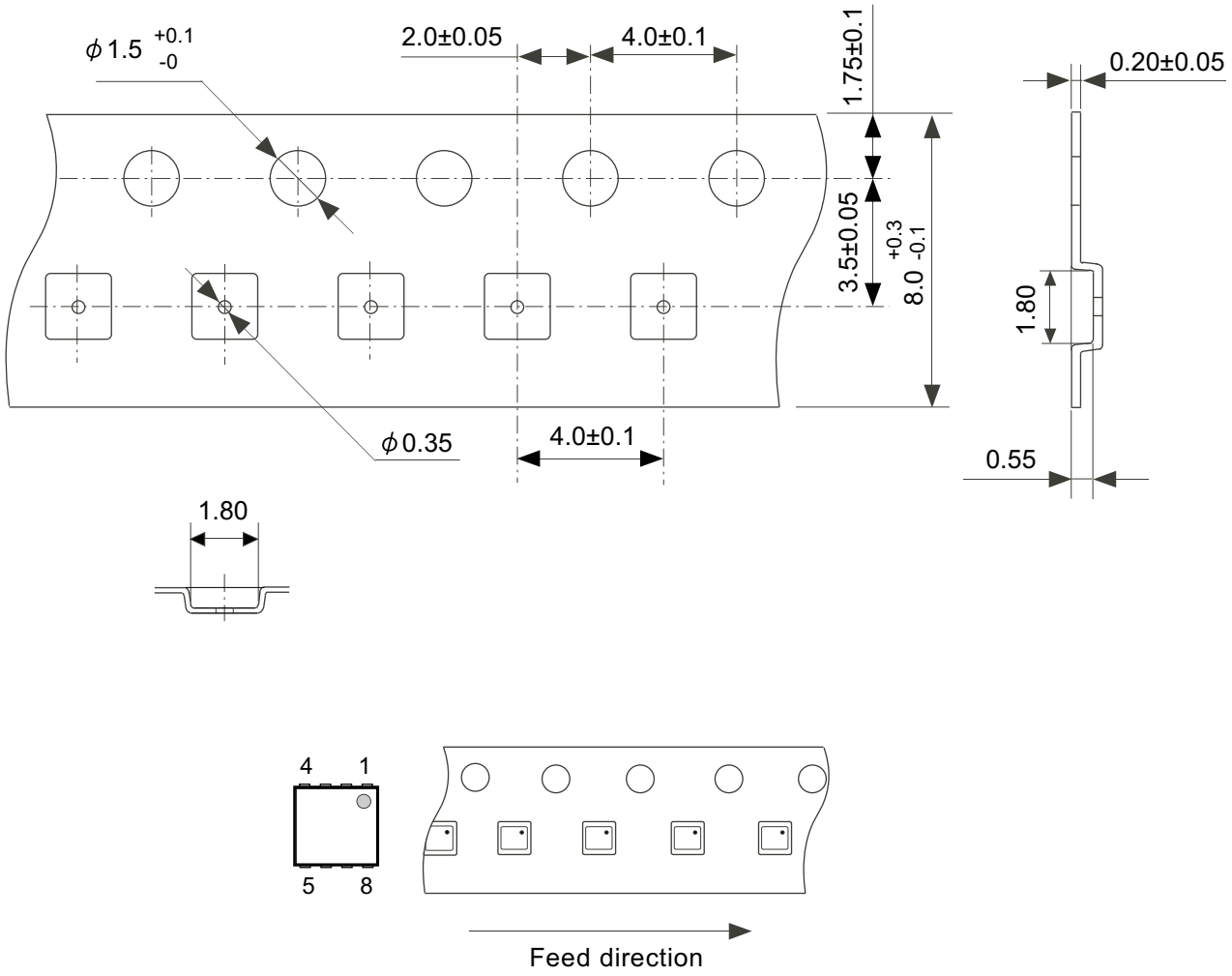




※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

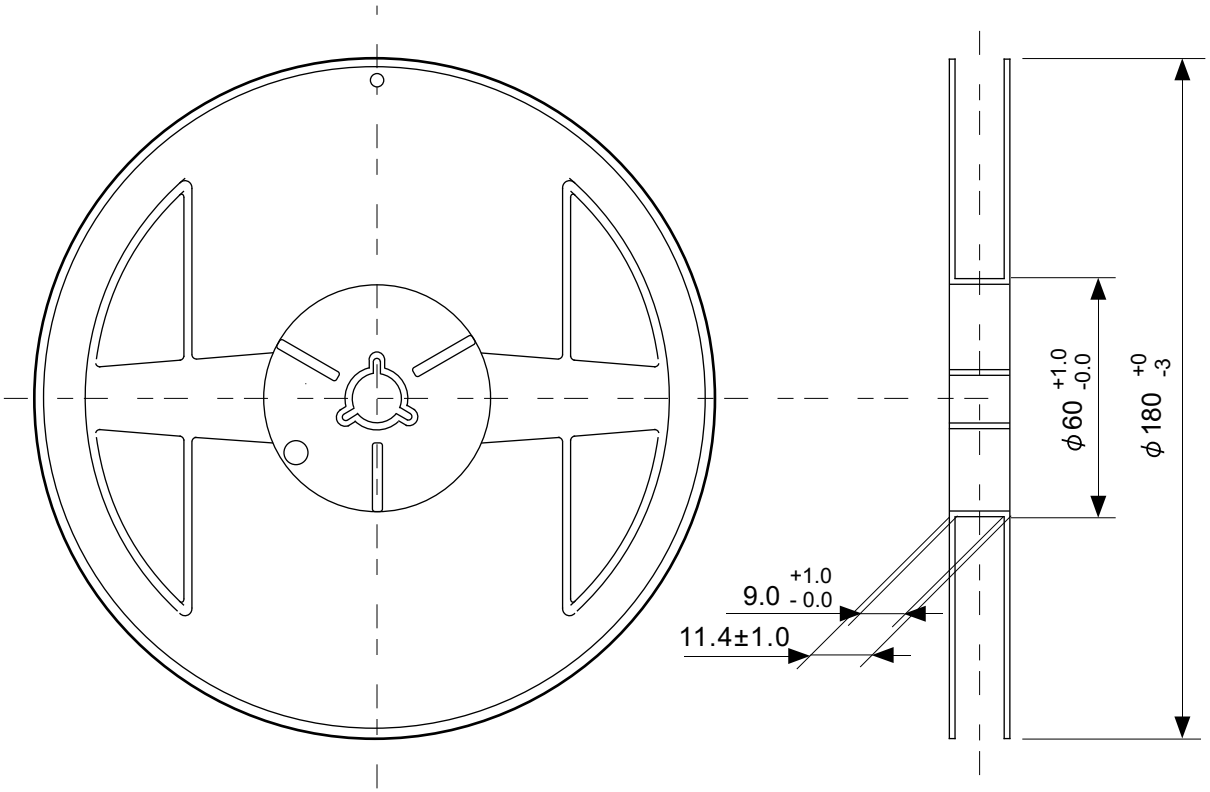
No. PY008-B-P-SD-1.0

TITLE	HSNT-8-C-PKG Dimensions
No.	PY008-B-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

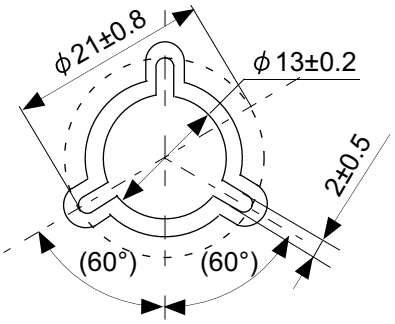


No. PY008-B-C-SD-1.0

TITLE	HSNT-8-C-Carrier Tape
No.	PY008-B-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



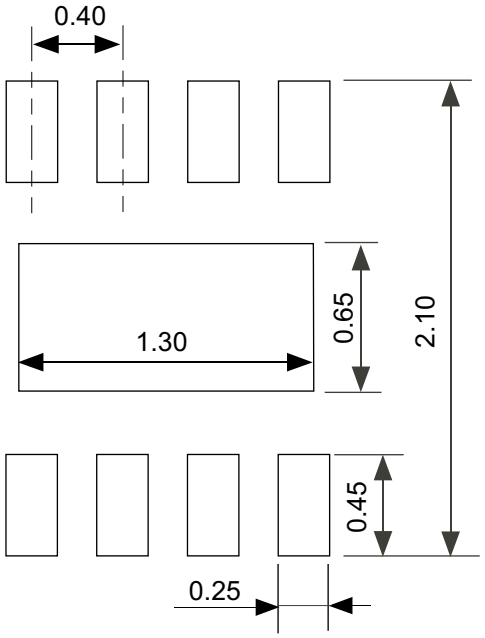
Enlarged drawing in the central part



No. PY008-B-R-SD-1.0

TITLE	HSNT-8-C-Reel		
No.	PY008-B-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

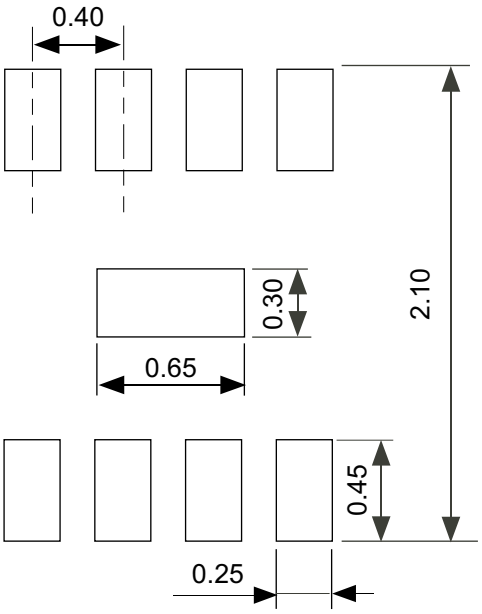
Land Pattern



Cauion It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意 放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Metal Mask Pattern



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is 20%.
③ Mask thickness: t0.10 mm

注意 ①リード実装部のマスク開口率は100%です。
②放熱板実装のマスク開口率は20%です。
③マスク厚み：t0.10 mm

No. PY008-B-L-SD-1.0

TITLE	HSNT-8-C -Land Recommendation
No.	PY008-B-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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2.4-2019.07