S-19560B Series

AUTOMOTIVE, 125°C OPERATION, 16 V INPUT, 3 CHANNEL OUTPUT, COMPACT PMIC FOR CAMERA MODULES

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Rev.1.0_00

This IC is a power management IC for automotive devices and is composed of a 2 channel step-down switching regulator (step-down DC-DC converter) and a 1 channel voltage regulator (LDO regulator).
It has a high maximum operating voltage of 16 V and maintains a high accuracy of ±2.0% for each output voltage. step-down DC-DC converter operates via PWM control thereby achieving both high efficiency and low ripple voltage. It also has a built-in spread spectrum clock generation circuit capable of reducing conductive noise and emission noise.
Each output has a built-in overcurrent protection circuit to protect the IC and coil from excessive load current and a built-in thermal shutdown circuit to prevent damage from heat generation. The startup sequence for each output is fixed within the IC, so there is no need for control via an external signal, and each output voltage can be automatically and safely supplied by simply providing power.
The use of compact HSNT-8(2030) package allows high-density mounting and contributes to device downsizing.

ABLIC Inc. offers a "thermal simulation service" which supports the thermal design in conditions when our power management ICs are in use by customers.
Our thermal simulation service will contribute to reducing the risk in the thermal design at customers' development stage.
ABLIC Inc. also offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
Contact our sales representatives for details.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.

■ Features

Step-down **DC-DC converter block (Ch1, Ch2)**
- Output voltage (Ch1): 3.3 V to 5.0 V
- Output voltage (Ch2): 0.9 V to 3.0 V
- Output current (Ch1): 600 mA
- Output current (Ch2): 700 mA
- Oscillation frequency: 2.2 MHz typ.
- Spread spectrum clock generation function: F_{SSS} = +6% typ. (Diffusion rate)
- Overcurrent protection function: 1.2 A typ. (Pulse-by-pulse method)
- Short-circuit protection function: Hiccup control
- Phase Shift Function: Shift the oscillation phase of Ch1 and Ch2 by 180°

LDO regulator block (Ch3)
- Output voltage: 0.9 V to 3.3 V
- Output current: 300 mA
- Ripple rejection: 50 dB typ. ($V_{OUT3(S)}$ = 1.8 V, f = 100 kHz)

Overall
- Iutput voltage: 4 V to 16 V
- Output voltage accuracy (Ch1, Ch2, Ch3): ±2.0% (T_j = -40°C to +150°C)
- Operation temperature range: Ta = -40°C to +125°C
- Under voltage lockout function (UVLO) : 3.35 V typ. (detection voltage)
- Thermal shutdown function: 170°C typ. (detection temperature)
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 in process*1

*1. Contact our sales representatives for details.

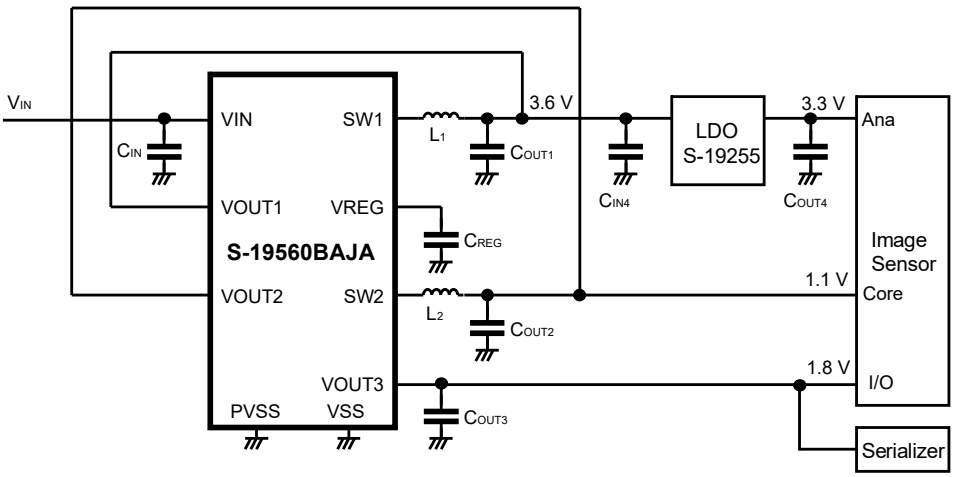
■ Applications

- Camera module for automotive
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

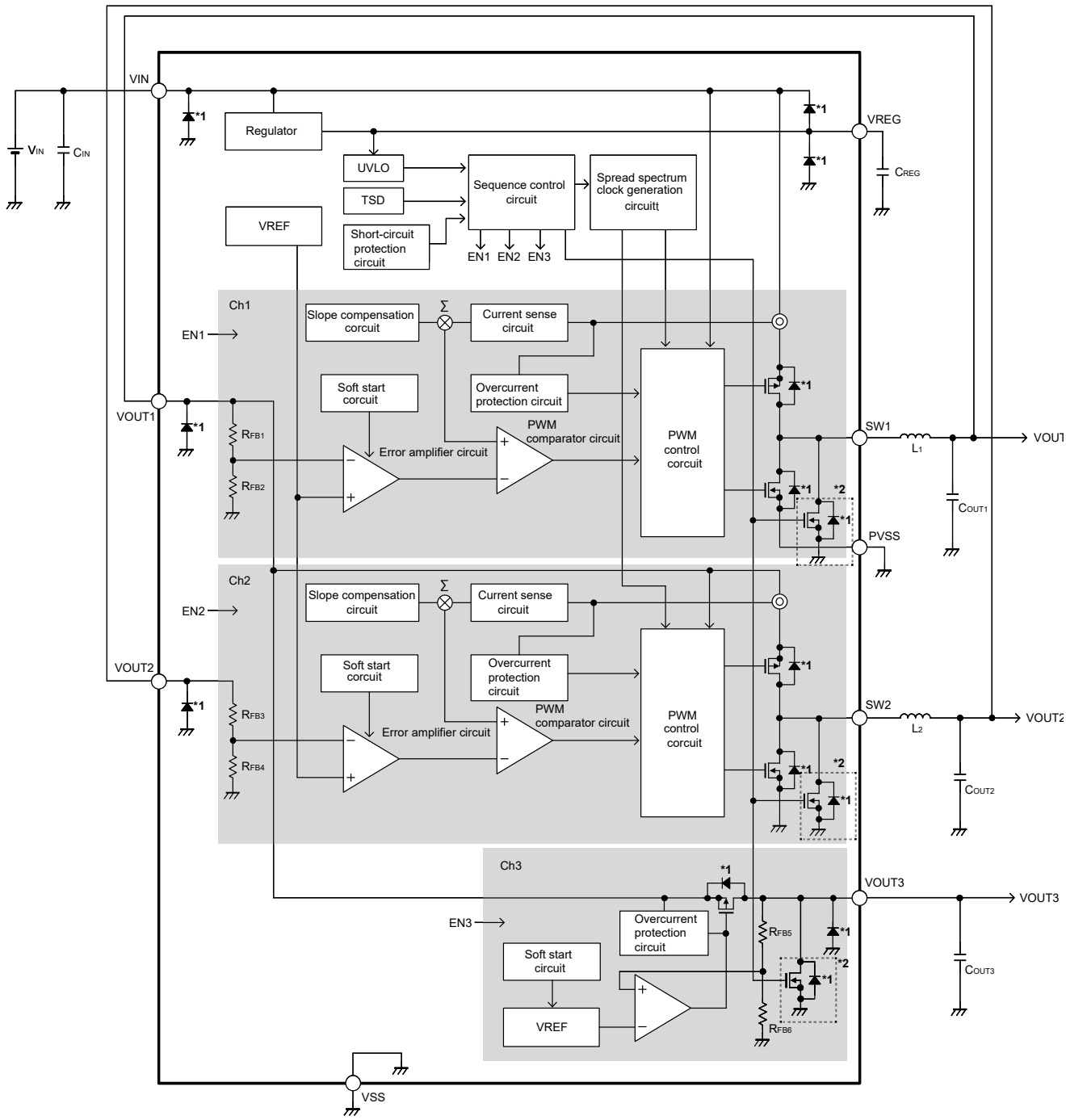
■ Package

- HSNT-8(2030) (3.0 mm × 2.0 mm × t0.5 mm max.)

■ Application Circuit



■ Block Diagram



***1.** Parasitic diode

***2.** Discharge Switch

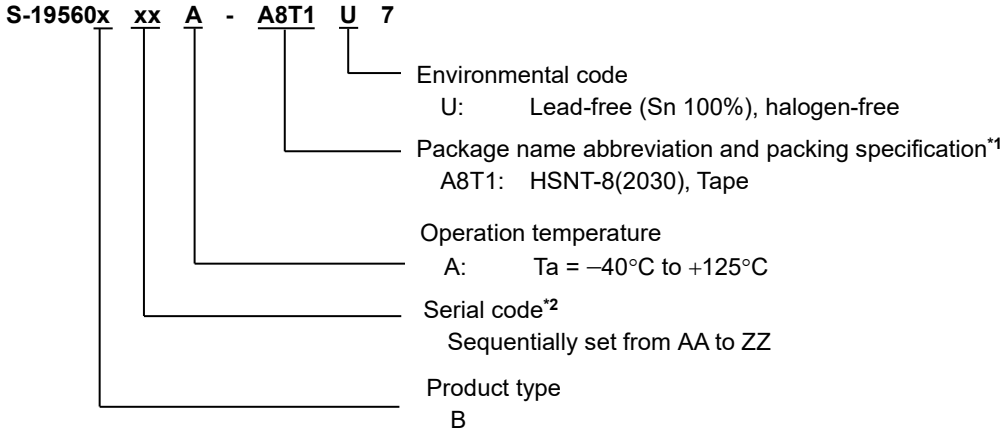
Figure 1

■ AEC-Q100 in Process

Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1**. Refer to the tape drawing.
***2**. Includes each setting for VOUT1 pin set output voltage, VOUT2 pin set output voltage, VOUT3 pin set output voltage, spread spectrum, discharge shunt, startup sequence, soft-start time, and interval time.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land	Stencil Opening
HSNT-8(2030)	PP008-A-P-SD	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD	PP008-A-L-S1

3. Output voltage configurable range

Table 2

Output Voltage*1	Configurable Range	Condition
$V_{OUT1(S)}$	3.3 V to 5.0 V	$V_{OUT1(S)} \leq V_{IN}$ - 1.0 V
$V_{OUT2(S)}$	0.9 V to 3.0 V	$V_{OUT2(S)} \leq V_{OUT1(s)}$ - 0.7 V
$V_{OUT3(S)}$	0.9 V to 3.3 V	$V_{OUT3(S)} \leq V_{OUT1(s)}$ - 0.3 V

***1.** $V_{OUT1(S)}$, $V_{OUT2(S)}$, $V_{OUT3(S)}$: Set output voltage

■ Pin Configurations

1. HSNT-8(2030)

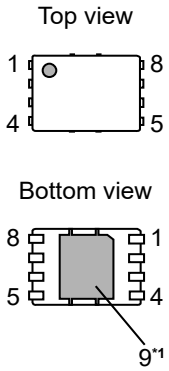


Figure 2

Table 3

Pin No.	Symbol	Description
1	VOUT2	Feedback pin for Ch2
2	VOUT1	Feedback pin for Ch1, Power supply pin for Ch2, Power supply pin for Ch3
3	SW2	External inductor connection pin for Ch2
4	VSS*2	GND pin
5	SW1	External inductor connection pin for Ch1
6	VIN	Power supply pin
7	VREG*3	Internal power supply pin
8	VOUT3	Ch3 voltage output pin
9	PVSS*2	GND pin

***1.** The heat sink of backside at shadowed area is the PVSS pin. Make sure to connect it to the board to set the electric potential GND.
The PVSS pin is a Ch1 (DC-DC converter) GND. Refer to **Figure 1**.
***2.** The PVSS pin and VSS pin should be connected on the board to have the same electrical potential.
***3.** The VREG pin cannot supply load current outside.

■ Absolute Maximum Ratings

Table 4

(Unless otherwise specified: Ta = +25°C, V_{SS} = PV_{SS} = 0 V)

Item	Symbol	Absolute Maximum Ratings	Unit
VIN pin voltage	V_{IN}	V_{SS} - 0.3 to V_{SS} + 18	V
VOUT1 pin voltage	V_{OUT1}	V_{SS} - 0.3 to V_{SS} + 6.5	V
VOUT2 pin voltage	V_{OUT2}	V_{SS} - 0.3 to V_{SS} + 6.5	V
VOUT3 pin voltage	V_{OUT3}	V_{SS} - 0.3 to V_{OUT1} + 0.3 ≤ V_{SS} + 6.5	V
VREG pin voltage	V_{REG}	V_{SS} - 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 6.5	V
SW1 pin voltage	V_{SW1}	V_{SS} - 2 to V_{IN} + 2 ≤ V_{SS} + 18 (< 20 ns)	V
		V_{SS} - 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 18	
SW2 pin voltage	V_{SW2}	V_{SS} - 2 to V_{OUT1} + 2 ≤ V_{SS} + 6.5 (< 20 ns)	V
		V_{SS} - 0.3 to V_{OUT1} + 0.3 ≤ V_{SS} + 6.5	
Junction temperature	T_j	−40 to +150	°C
Operation ambient temperature	T_{opr}	−40 to +125	°C
Storage temperature	T_{stg}	−40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	HSNT-8(2030)	Board A	-	181	-	°C/W
			Board B	-	135	-	°C/W
			Board C	-	40	-	°C/W
			Board D	-	42	-	°C/W
			Board E	-	32	-	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board"** for details.

■ Electrical Characteristics

Table 6 (1 / 2)

(V_{IN} = 6 V, T_j = -40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Ch1 (Step-down **DC-DC converter)**						
Output voltage*1	$V_{OUT1(E)}$	I_{OUT1} = 0 mA	$V_{OUT1(S)}$ × 0.98	$V_{OUT1(S)}$	$V_{OUT1(S)}$ × 1.02	V
Oscillation frequency	f_{OSC1}	-	1.98	2.20	2.42	MHz
Oscillation frequency modulation rate	F_{SSS1}	-	-	+6	-	%
Maximum duty ratio	MaxDuty1	-	100	-	-	%
High side power MOS FET on-resistance	R_{HEFT1}	I_{SW1} = 50 mA	-	0.55	1.00	Ω
Low side Power MOS FET on-resistance	R_{LEFT1}	I_{SW1} = -50 mA	-	0.35	0.60	Ω
Limit current	I_{LIM1}	-	0.9	1.2	1.5	A
Soft-start time*2	t_{SS1}	Time until $V_{OUT1(S)}$ reaches 90% after it starts rising	$t_{SS1(S)}$ × 0.6	$t_{SS1(S)}$	$t_{SS1(S)}$ × 1.4	ms
Discharge shunt function	R_{DCHG1}	V_{IN} = 3.0 V, SW1 = 0.1 V	-	100	200	Ω
Ch2 (Step-down **DC-DC converter)**						
Output voltage*1	$V_{OUT2(E)}$	I_{OUT2} = 0 mA	$V_{OUT2(S)}$ × 0.98	$V_{OUT2(S)}$	$V_{OUT2(S)}$ × 1.02	V
Oscillation frequency	f_{OSC2}	-	1.98	2.20	2.42	MHz
Oscillation frequency modulation rate	F_{SSS2}	-	-	+6	-	%
Maximum duty ratio	MaxDuty2	-	100	-	-	%
High side power MOS FET on-resistance	R_{HEFT2}	I_{SW2} = 50 mA, V_{OUT1} = 4 V	-	0.30	0.50	Ω
Low side Power MOS FET on-resistance	R_{LEFT2}	I_{SW2} = -50 mA	-	0.25	0.45	Ω
Limit current	I_{LIM2}	-	1.0	1.2	1.5	A
Soft-start time*2	t_{SS2}	Time until $V_{OUT2(S)}$ reaches 90% after it starts rising	$t_{SS2(S)}$ × 0.6	$t_{SS2(S)}$	$t_{SS2(S)}$ × 1.45	ms
Discharge shunt function	R_{DCHG2}	V_{IN} = 3.0 V, SW2 = 0.1 V	-	100	200	Ω
Ch3 (LDO regulator)						
Output voltage*1	$V_{OUT3(E)}$	V_{OUT1} = $V_{OUT1(S)}$ × 0.95, I_{OUT3} = 30 mA	$V_{OUT3(S)}$ × 0.98	$V_{OUT3(S)}$	$V_{OUT3(S)}$ × 1.02	V
Output current*3	I_{OUT3}	V_{OUT1} = $V_{OUT1(S)}$	300*4	-	-	mA
Limit current	I_{LIM3}	V_{OUT1} = $V_{OUT1(S)}$, V_{OUT3} = $V_{OUT3(S)}$ × 0.9	-	650	-	mA
Load regulation	ΔV_{OUT3}	V_{OUT1} = $V_{OUT1(S)}$ × 0.95, 1 mA ≤ I_{OUT3} ≤ 200 mA, Ta = +25°C	-	15	40	mV
Ripple rejection	|RR|	V_{OUT1} = 4.0 V, f = 100 kHz, ΔV_{rip} = 0.5 Vp-p, I_{OUT3} = 30 mA; $V_{OUT3(S)}$ = 1.8 V	-	50	-	dB
		V_{OUT1} = 4.0 V, f = 1.0 kHz, ΔV_{rip} = 0.5 Vp-p, I_{OUT3} = 30 mA; $V_{OUT3(S)}$ = 1.8 V	-	66	-	dB
Soft-start time*5	t_{SS3}	V_{OUT1} = $V_{OUT1(S)}$ × 0.95, I_{OUT3} = 1 mA, C_{OUT3} = 2.2 µF	0.07	0.13	0.19	ms
Discharge shunt function	R_{DCHG3}	V_{IN} = 3.0 V, V_{OUT3} = 0.1 V	-	100	200	Ω

***1.** $V_{OUT1(S)}$, $V_{OUT2(S)}$, $V_{OUT3(S)}$: Set output voltage value
$V_{OUT1(E)}$, $V_{OUT2(E)}$, $V_{OUT3(E)}$: Actual output voltage value

***2.** Refer to **Table 8, Figure 3, Figure 4** and **Figure 5.**

***3.** The output current at which the output voltage becomes 95% of $V_{OUT3(E)}$ after gradually increasing output current.

***4.** Due to limitation of the power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation when the output current is large. This specification is guaranteed by design.
Refer to **"12. Thermal design" in "■ Operation ".**

***5.** The time it takes for V_{OUT3} to reach 90% from the set value of 25% during start-up. Refer to **Figure 3, Figure 4** and **Figure 5.**

Table 6 (2 / 2)

(V_{IN} = 6 V, T_j = -40°C to +150°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Overall							
Operating input voltage	V_{IN}	-		4.0	-	16	V
Current consumption during UVLO detection	I_{UVLO}	V_{IN} = 3 V, During UVLO detection		-	45	90	µA
VIN pin current consumption swiching off	I_{SS}	V_{OUT1} = $V_{OUT1(S)}$ × 1.1 V_{OUT2} = $V_{OUT2(S)}$ × 1.1		-	330	590	µA
VOUT1 pin current consumption during swiching off	I_{VOUT1}	V_{OUT1} = $V_{OUT1(S)}$ × 1.1 V_{OUT2} = $V_{OUT2(S)}$ × 1.1		-	300	450	µA
VOUT2 pin current consumption during swiching off	I_{VOUT2}	V_{OUT1} = $V_{OUT1(S)}$ × 1.1 V_{OUT2} = $V_{OUT2(S)}$ × 1.1	1.89 V < $V_{OUT2(S)}$	-	1.2	1.8	µA
			1.59 V < $V_{OUT2(S)}$ ≤ 1.89 V	-	0.6	0.9	
			$V_{OUT2(S)}$ ≤ 1.59 V	-	0.5	0.8	
UVLO detection voltage	V_{UVLO-}	VREG pin voltage		3.1	3.35	3.6	V
UVLO release voltage	V_{UVLO+}	VREG pin voltage		3.2	3.45	3.7	V
Thermal shutdown detection temperature	T_{SD}	Junction temperature		-	170	-	°C
Thermal shutdown release temperature	T_{SR}	Junction temperature		-	150	-	°C

Remark $V_{OUT1(S)}$, $V_{OUT2(S)}$, $V_{OUT3(S)}$: Set output voltage

■ Operation

1. Power supply connection for each channel (Ch)

This IC is a power management IC composed of an 18 V withstand voltage step-down DC-DC converter (Ch1), a 6.5 V withstand voltage step-down DC-DC converter (Ch2), and a single LDO regulator (Ch3).
The VOUT1 pin serves as the feedback pins and the power supply input pins for other Ch*1.

***1.** VOUT1 pin: Ch1 feedback pin and power supply pin for Ch2 and Ch3
VOUT2 pin: Ch2 feedback pin

2. Startup sequence

After V_{IN} is applied, if the voltage of the VREG pin, which is the internal power supply, rises to equal or above the UVLO release voltage, the IC will enter the enable status, and the startup sequence will begin. Because the VREG pin output current capacity is limited to 30 mA typ., a certain amount of time will be required until C_{REG} charging is complete after V_{IN} is applied.
There are three types of startup sequences, with different startup orders for each Ch. Refer to "**2. 1 Sequence operation outline**".
The soft-start time for Ch1 and Ch2 can also be selected from 3 types of times. This is locked to 1 type when shipped from the factory, so the product will startup in the specified sequence by just supplying power. This feature enables users to avoid time-consuming programming tasks.

Each output pin has a frequency foldback function (VOUT1 pin, VOUT2 pin) and short-circuit protection function (VOUT1 pin, VOUT2 pin, VOUT3 pin) as functions to protect against abnormal drops in output voltage, however all of these functions are disabled during the normal startup sequence. For details, refer to **Figure 3**, **Figure 4** and **Figure 5.**

2. 1 Sequence operation outline

Table 7 Startup sequence

Setting	Startup Order
SEQ1	Ch1 → Ch2 → Ch3
SEQ2	Ch1 → Ch2, Ch3
SEQ3	Ch1 → Ch3 → Ch2

2. 2 Soft-start time

Each channel of Ch1 to Ch3 has a built-in soft-start circuit. The soft-start time for Ch1 and Ch2 can be selected from 3 types of times. The soft start times for Ch1 and Ch2 will be the same setting and cannot be set to different values for each.
The soft-start time for Ch3 is locked to 130 µs typ. Refer to **Table 8**.

2. 3 Interval time

The time in a startup sequence between the previous Ch soft start completing and the next Ch soft start beginning is called the interval time. Interval time is shown in the timing charts in **Figure 3**, **Figure 4** and **Figure 5.**

t_{INT1}: The time until the next Ch soft-start begins after the Ch1 or Ch2 soft-start completes
t_{INT2}: The time until the Ch2 starts the soft-start after the Ch3 soft-start completes (This only applies for SEQ3)

Soft-start time and interval time can be set using the combinations shown in **Table 8.**

Table 8

No.	Soft-start Time		Interval Time	
	Ch1, Ch2*1 [t_{SS1}, t_{SS2}]	Ch3 [t_{SS3}]	t_{INT1}	t_{INT2} (SEQ3)
1	320 µs typ.	130 µs typ.	290 µs typ.	20 µs typ.
2	640 µs typ.	130 µs typ.	560 µs typ.	20 µs typ.
3	1280 µs typ.	130 µs typ.	1100 µs typ.	20 µs typ.

*1. Ch1 and Ch2 will be set to the same times.

3. Termination sequence

This IC enters the standby status by detecting UVLO status. When switching to the standby status, Ch1 and Ch2 switching will stop and V_{OUT3} output will stop simultaneously. Refer to "**8. Under voltage lockout function (UVLO)**" in "**■ Operation**".

3. 1 Discharge shunt function

A discharge shunt circuit is available for this IC to discharge the output capacitance. Select a product option with the discharge shunt function enabled since the enable/disable shunt function is fixed when shipped from the factory.
The discharge shunt circuit is located on each pin of the SW1 pin, SW2 pin, and VOUT3 pin and can discharge the output capacitance. As a result, the V_{SS} level will be the electrical potential of the SW1 pin, SW2 pin, VOUT1 pin, VOUT2 pin and VOUT3 pin (The VOUT1 pin and VOUT2 pin are connected to the SW1 pin and SW2 pin via an external inductor).

Discharge shunt function operation conditions
(1) UVLO detected status
(2) Overheat protection detected status
(3) Hiccup protected status

For products that do not have a built-in discharge shunt circuit, the V_{SS} level is set by the built-in resistance dividers between the VOUT1, VOUT2 and VOUT3 pins and the VSS pin. The resistance divider values are approximately several hundred kΩ to several MΩ.

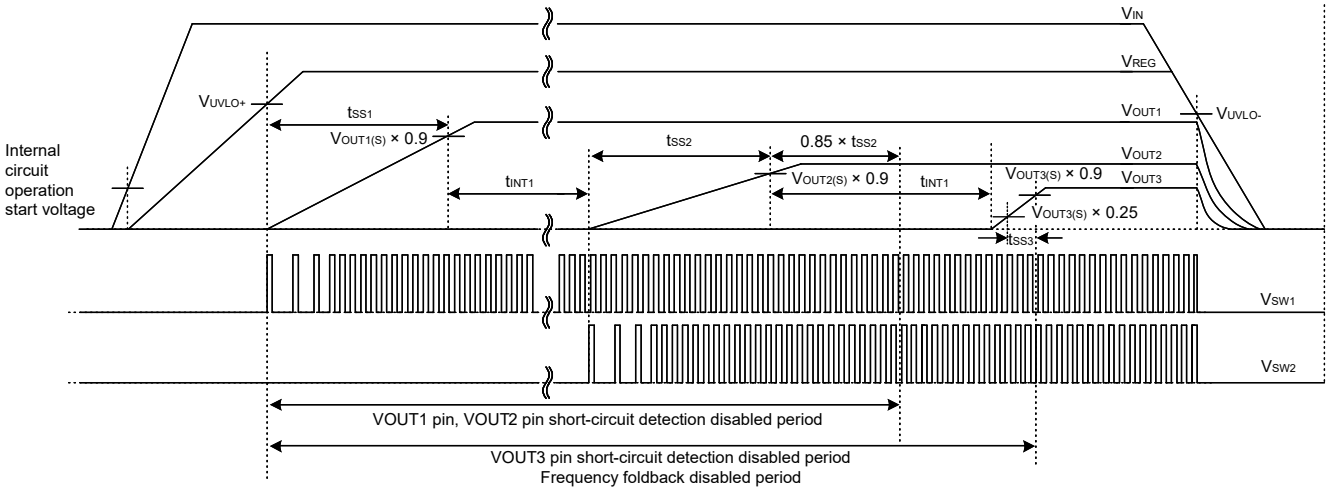


Figure 3 Timing Chart SEQ1

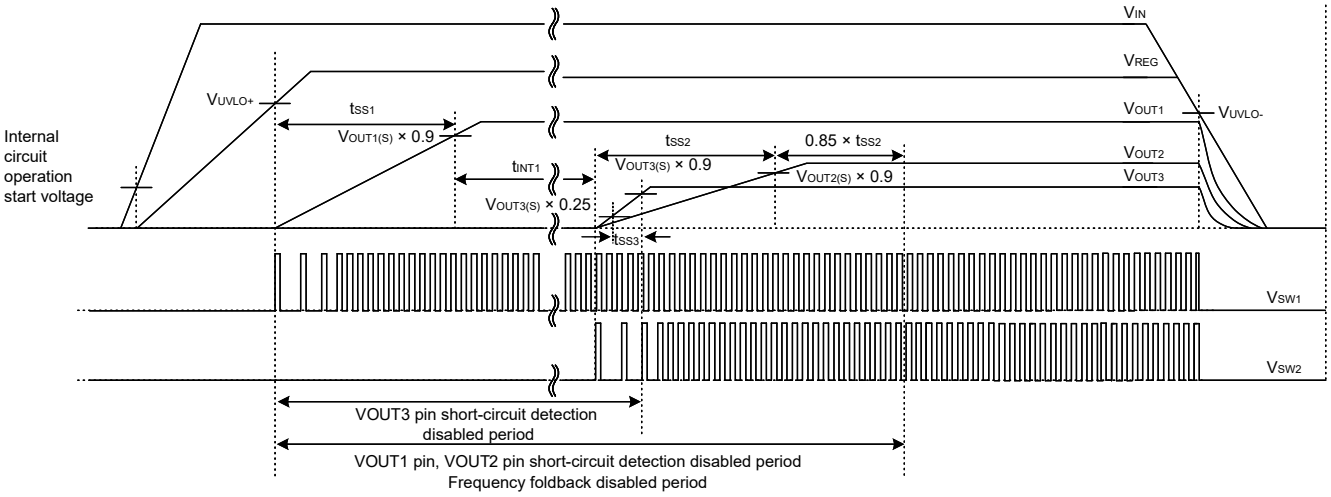


Figure 4 Timing Chart SEQ2

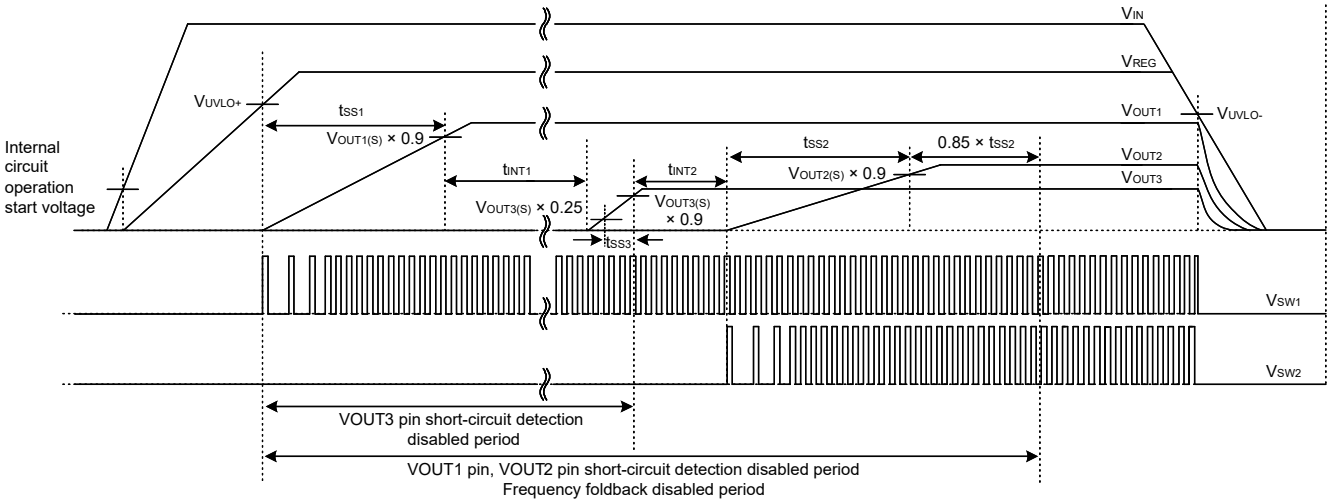


Figure 5 Timing Chart SEQ3

4. Step-down DC-DC converter channels (Ch1, Ch2)

This IC adopts the current mode control. The SW1 pin and SW2 pin duty cycle are determined by comparing the error amplifier output signal to a current feedback signal with slope compensation added to the current which flows to the high side power MOS FET. Due to the configured negative feedback loop, the error amplifier output signal is maintained at a value where the internal reference voltage, the VOUT1 pin voltage, and the feedback voltage from the VOUT2 pin are equal.

4. 1 PWM Control

This IC operates with the pulse width modulation method (PWM) regardless of the extent of load current and allows the switching frequency to stabilize.

4. 2 100% duty cycle operation

The high side power MOS FET allows for 100% duty cycle operation. Even when the input voltage is lowered up to the output voltage setting value, the high side power MOS FET is kept on and current can be supplied to the load. The output voltage at this time is the input voltage from which the voltage drop due to the DC resistance of the inductor and the on-resistance of the high side power MOS FET are subtracted.

4. 3 Spread spectrum clock generation function

This IC has a built-in spread spectrum clock generation circuit to reduce conductive noise and emission noise. The spread spectrum clock generation circuit spreads the operating frequency range across a wide bandwidth during PWM operation to suppress noise peaks for specific frequency ranges. This IC uses the oscillation frequency (f_{OSC1}, f_{OSC2}) *1 as a lower limit and turns the frequency to a triangular wave shape using an oscillation frequency modulation rate (F_{SSS1}, F_{SSS2}) *2 = +6% typ. range. The modulation period is 320 / f_{OSC1}, f_{OSC2} sec typ.

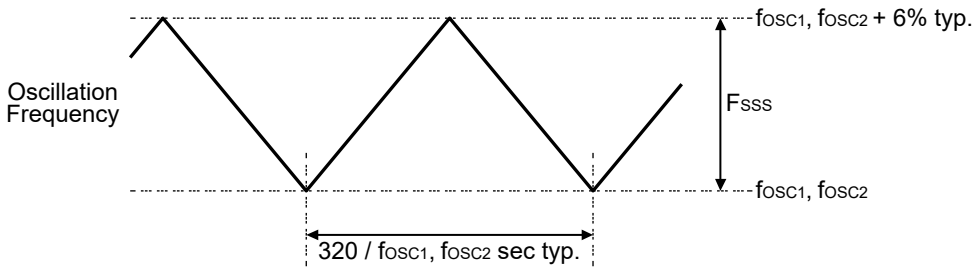


Figure 6

***1.** f_{OSC1}, f_{OSC2}: Ch1 or Ch2 oscillation frequency

***2.** F_{SSS1}, F_{SSS2}: Ch1 or Ch2 oscillation frequency modulation rate

4. 4 Overcurrent protection function

The overcurrent protection circuit monitors the current that flows through the high side power MOS FET and limits current to prevent thermal destruction of the IC due to an overload, magnetic saturation in the inductor, etc.
When a current exceeding the limit current (I_{LIM1}, I_{LIM2}) *1 flows through the high side power MOS FET, the high side power MOS FET is turned off. When the next switching cycle starts, the high side power MOS FET is turned on. If the current value continues to remain at I_{LIM1}, I_{LIM2} or higher, the high side power MOS FET is turned off again, repeating this series of operation.
Meanwhile, when the current, which flows through the high side power MOS FET, falls to I_{LIM1}, I_{LIM2} or lower, this IC will return to the normal operation.
When the slope of inductor current is large, I_{LIM1}, I_{LIM2} may appear to increase due to the delay time of overcurrent protection circuit. This tends to occur when an inductor with low inductance is used or when the voltage difference between input and output is large. When the peak current (I_{L_max}) shown in "**4. Inductors (L_1 and L_2)**" in "**■ External Parts Selection**" reaches I_{LIM1}, I_{LIM2}, overcurrent will be detected.

***1.** I_{LIM1}, I_{LIM2}: Ch1 or Ch2 Limit current

4. 5 Frequency foldback function

The frequency foldback function maintains the proportional relationship between the ratio of the VOUT1 pin voltage or the VOUT2 pin voltage to the setting value and the oscillation frequency (f_{osc1}, f_{osc2}) when the VOUT1 pin voltage or VOUT2 pin voltage is equal to or less than the 83% typ. of the setting value. If both the VOUT1 pin voltage and VOUT2 pin voltage are equal to or less than 83% typ. of the setting value, there will be a proportional relationship between the pin with the lower ratio to the setting value and the oscillation frequency.
Ch1 and Ch2 share an oscillation circuit, so Ch1 and Ch2 will be the same frequency even during frequency foldback.

Table 9 Examples of $V_{OUT1(E)}$, $V_{OUT2(E)}$ and f_{OSC}

$V_{OUT1(E)}$ / $V_{OUT1(S)}$	$V_{OUT2(E)}$ / $V_{OUT2(S)}$	f_{osc1}, f_{osc2}
100%	100%	2.20 MHz typ.
80%	100%	1.76 MHz typ.
50%	70%	1.10 MHz typ.

Remark $V_{OUT1(S)}$, $V_{OUT2(S)}$: Set output voltage
$V_{OUT1(E)}$, $V_{OUT2(E)}$: Actual output voltage

This IC's frequency foldback function is set to disabled during the normal startup sequence. Refer to **Figure 3, Figure 4** and **Figure 5**.

5. LDO regulator channel (Ch3)

5. 1 Overview

The Ch3 power supply is provided by the VOUT1 pin.
For the maximum output current of the VOUT3 pin (Ch3), refer to "**6. Allowable load current for each output**" in "**■ Operation**".

5. 2 Overcurrent protection circuit

This IC's Ch3 has a built-in overcurrent protection circuit to limit the overcurrent of the output transistor.
If the VOUT3 pin enters the overcurrent status, the load current will be limited to a constant value in order to protect the output transistor. As a result, the VOUT3 pin voltage will drop. The output current is limited to a constant value due to the overcurrent protection circuit activation.

Output current limit (I_{LIM3}) = 650 mA typ.

This IC restarts regulating when the output transistor is released from the overcurrent status.
If the overcurrent status continues and the VOUT3 pin voltage drops to 65% typ. of the setting value, the short-circuit protection circuit will detect short-circuit status.
Refer to "**7. Short-circuit protection function**" in "**■ Operation**" for short-circuit prevention circuit operation.

Caution This overcurrent protection circuit does not work as for thermal protection. For example, if the VOUT3 pin voltage does not drop to the value at which the short-circuit protection functions when the overcurrent protection circuit functions, significant heat loss will occur on this IC, so exercise caution.

6. Allowable load current for each output

The maximum output current for each Ch is as follow.

I_{OUT1} (Ch1): 600 mA
I_{OUT2} (Ch2): 700 mA
I_{OUT3} (Ch3): 300 mA

Note that the I_{OUT1} is also added to later stage Ch output current. The following shows how each channel's load currents (I_{LOAD1}, I_{LOAD2}, I_{LOAD3}) are assigned. Set the load current (I_{LOAD1}, I_{LOAD2}, I_{LOAD3}) so that the output current (I_{OUT1}, I_{OUT2}, I_{OUT3}) does not exceed the maximum output current.

The Ch3 power supply pin is connected to the VOUT1 pin.

$$I_{OUT3} = I_{LOAD3}$$
$$I_{OUT2} = I_{LOAD2}$$

$$I_{IN1} = \frac{V_{OUT2}}{V_{OUT1}} \times I_{LOAD2} \times \frac{1}{\eta_2} + I_{LOAD3}$$

$$I_{OUT1} = I_{IN1} + I_{LOAD1}$$
$$= \frac{V_{OUT2}}{V_{OUT1}} \times I_{LOAD2} \times \frac{1}{\eta_2} + I_{LOAD1} + I_{LOAD3}$$

Remark η_2: Ch2 conversion efficiency. For the Ch2 conversion efficiency, refer to "**4 V_{OUT2} = 1.1 V**" through "**6. V_{OUT2} = 3.0 V**" in "**■ Reference Data** ".

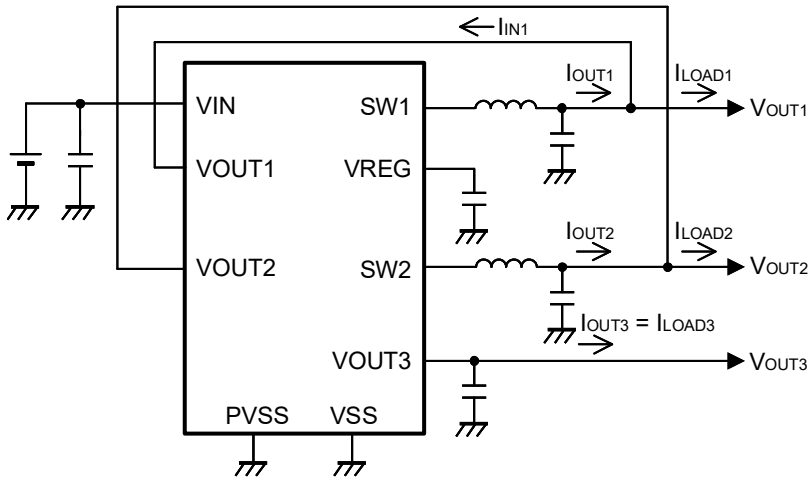


Figure 7

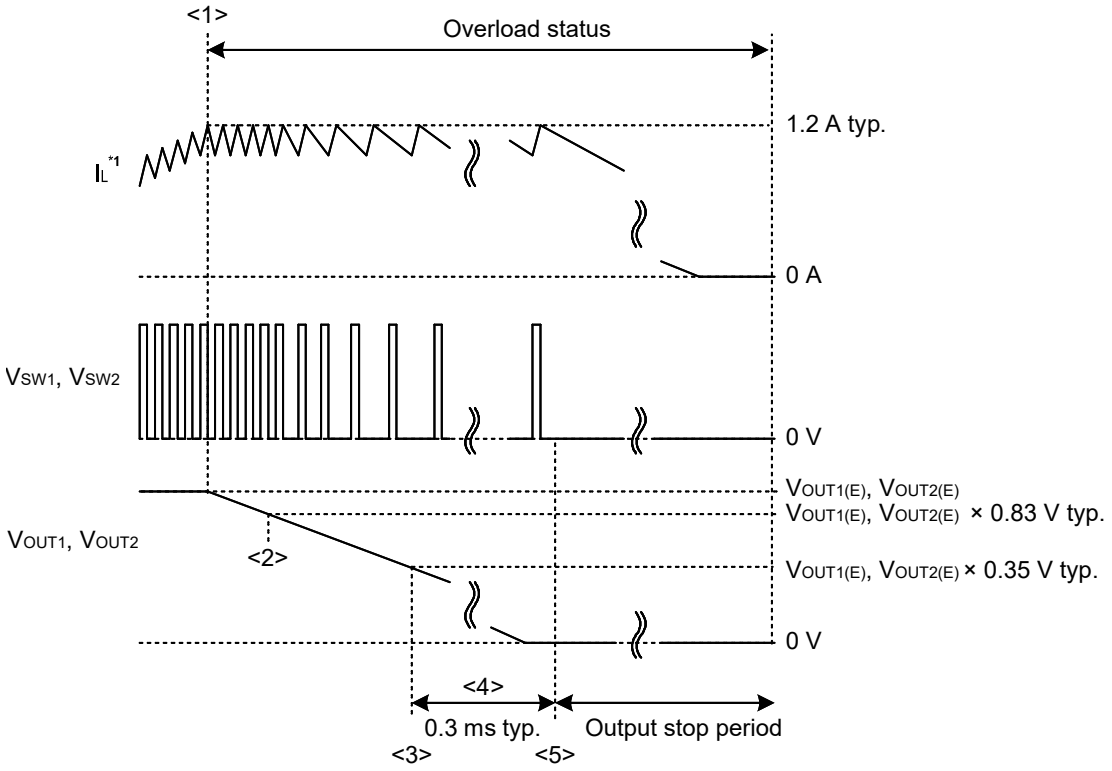
7. Short-circuit protection function

7. 1 Short-circuit detection operation

This IC has a built-in short-circuit protection function for hiccup control. The hiccup control is a method for periodically carrying out automatic recovery when the IC detects overcurrent and stops the switching operation. If a specific amount of time elapses after a short-circuit is detected at any one of the VOUT1, VOUT2, or VOUT3, the hiccup control will trigger, and all output will stop.

7. 1. 1 Ch1, Ch2

<1> Overcurrent detection
<2> After detection of the VOUT1 pin voltage, VOUT2 pin voltage (V_{OUT1}, V_{OUT2}) < $V_{OUT1(E)}$, $V_{OUT2(E)}$ × 0.83 V typ., frequency foldback function becomes valid.
<3> Detection of V_{OUT1}, V_{OUT2} < $V_{OUT1(E)}$, $V_{OUT2(E)}$ × 0.35 V typ.
<4> 0.3 ms elapse
<5> Switching operation stop



***1.** Inductor current

Figure 8

7. 1. 2 Ch3

<1> Overcurrent detection
<2> Detection of V_{OUT3} < $V_{OUT3(E)}$ × 0.65 V typ.
<3> 0.3 ms elapse
<4> Output stop

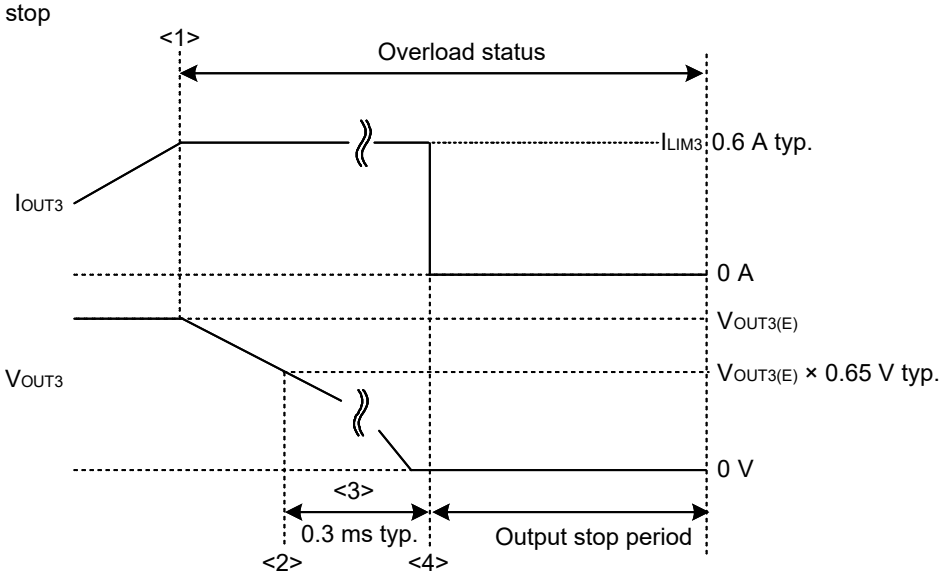


Figure 9

7. 2 Short-circuit detection voltage

The conditions for switching to short-circuit detection function operation are as follows.

- Ch1, Ch2: VOUT1 pin voltage = $V_{OUT1(S)}$ × 0.35, VOUT2 pin voltage = $V_{OUT2(S)}$ × 0.35
- Ch3: VOUT3 pin voltage = $V_{OUT3(S)}$ × 0.65

A short-circuit will be detected if any of the VOUT pin voltages drop to the voltages listed above.
If the VOUT1 pin, which is the power supply for Ch3, is short-circuited, the VOUT3 pin voltage will also drop. As a result, Ch3 may detect a short-circuit on the VOUT1 pin, depending on the voltage settings.

7. 3 Automatic recovery operation

Once the output stop time of 21 ms typ. has elapsed, automatic recovery will be attempted based on the startup sequence. If a short-circuit is detected again during this automatic recovery attempt, all output will again be stopped. The short-circuit detection function is disabled for a set amount of time during the startup sequence; however startup will begin with the frequency foldback function in the enable status. Refer to "**2. Startup sequence**" and "**7. 4 Short-circuit detection, recovery sequence**" in "**■ Operation**".

7. 4 Short-circuit detection, recovery sequence

7. 4. 1 SEQ1: V_{OUT1} short-circuit

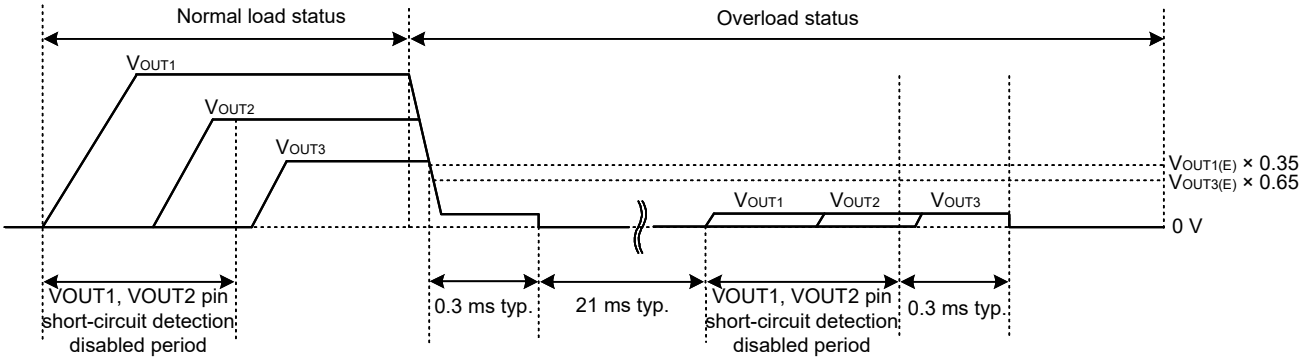


Figure 10 V_{OUT1} Enters Overload Status → Overload Status Continues

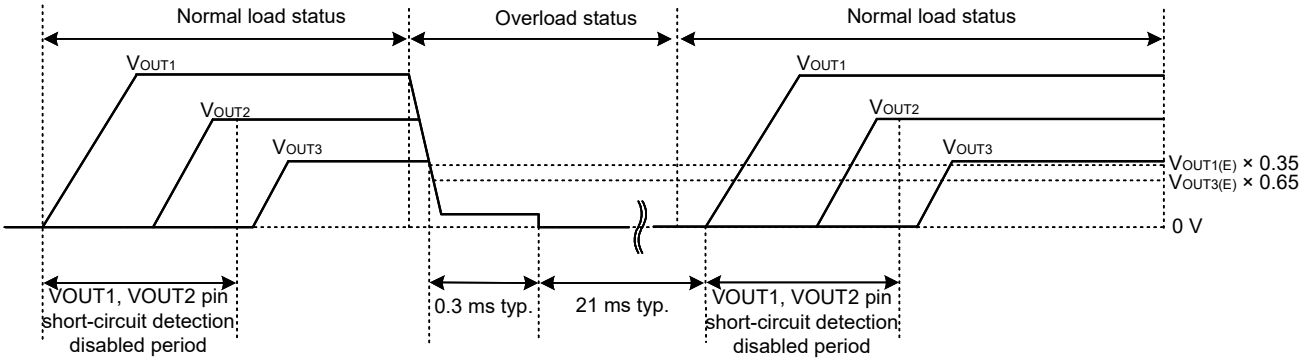


Figure 11 V_{OUT1} Enters Overload Status → Overload Status Is Released

7. 4. 2 SEQ1: V_{OUT2} short-circuit

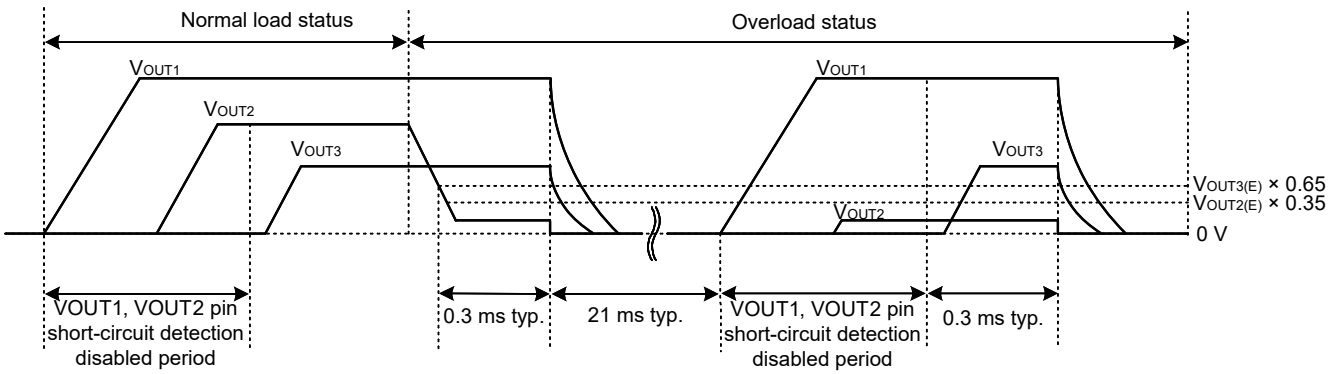


Figure 12 V_{OUT2} Enters Overload Status → Overload Status Continues

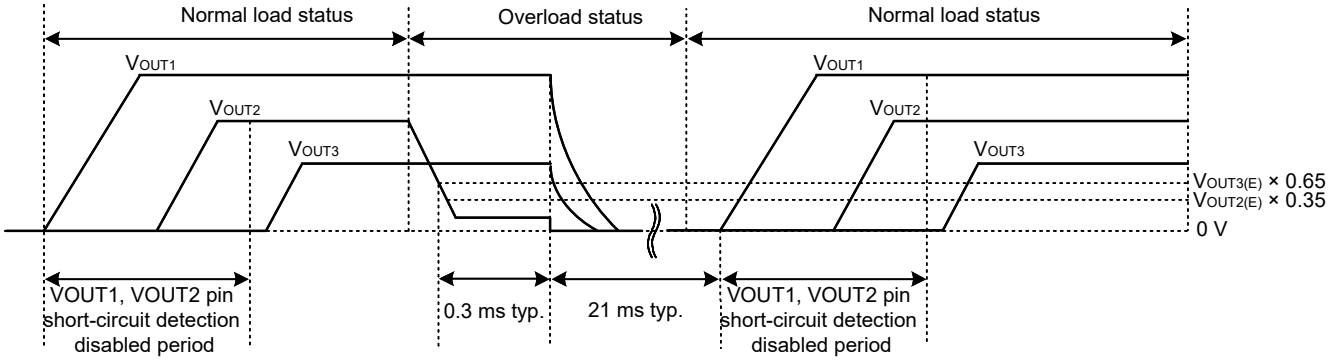


Figure 13 V_{OUT2} Enters Overload Status → Overload Status Is Released

7. 4. 3 SEQ1: V_{OUT3} short-circuit

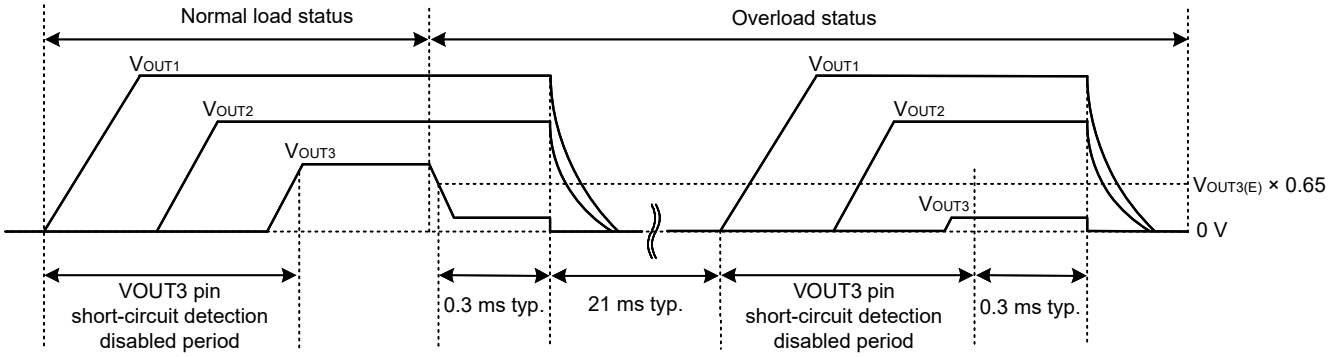


Figure 14 V_{OUT3} Enters Overload Status → Overload Status Continues

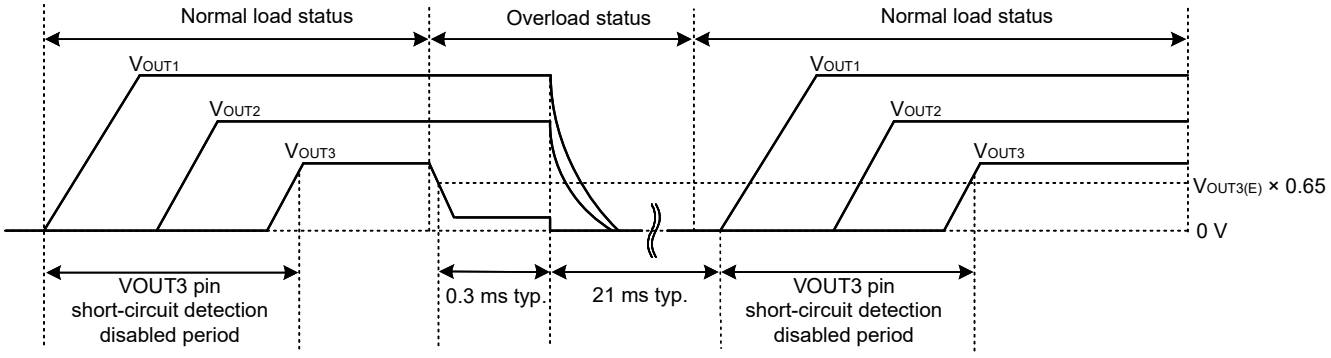


Figure 15 V_{OUT3} Enters Overload Status → Overload Status Is Released

7. 4. 4 SEQ3: V_{out1} short-circuit

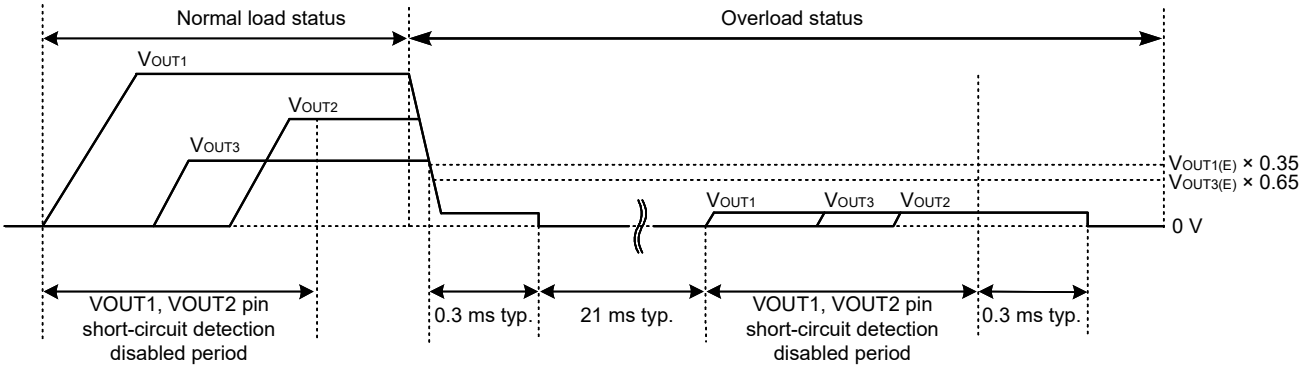


Figure 16 V_{OUT1} Enters Overload Status → Overload Status Continues

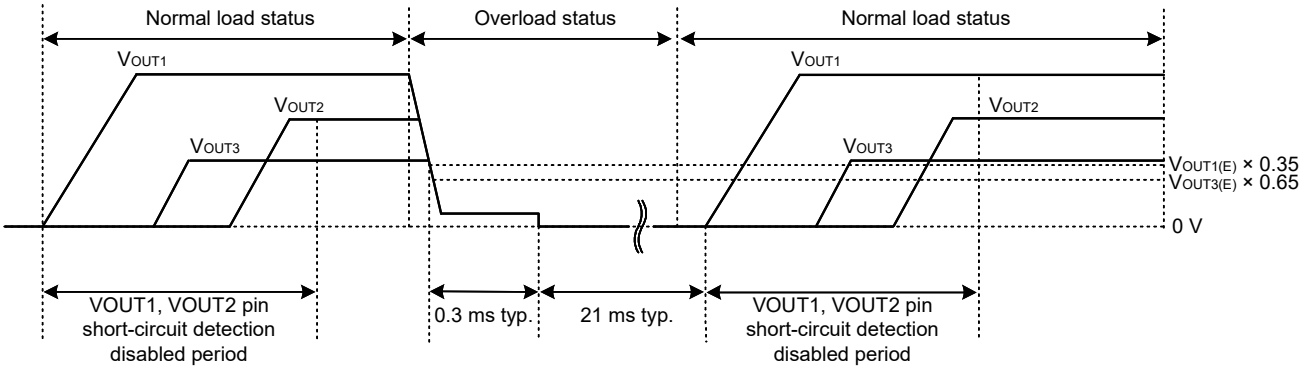


Figure 17 V_{OUT1} Eenters Overload Status → Overload Status Is Released

7. 4. 5 SEQ3: V_{OUT2} short-circuit

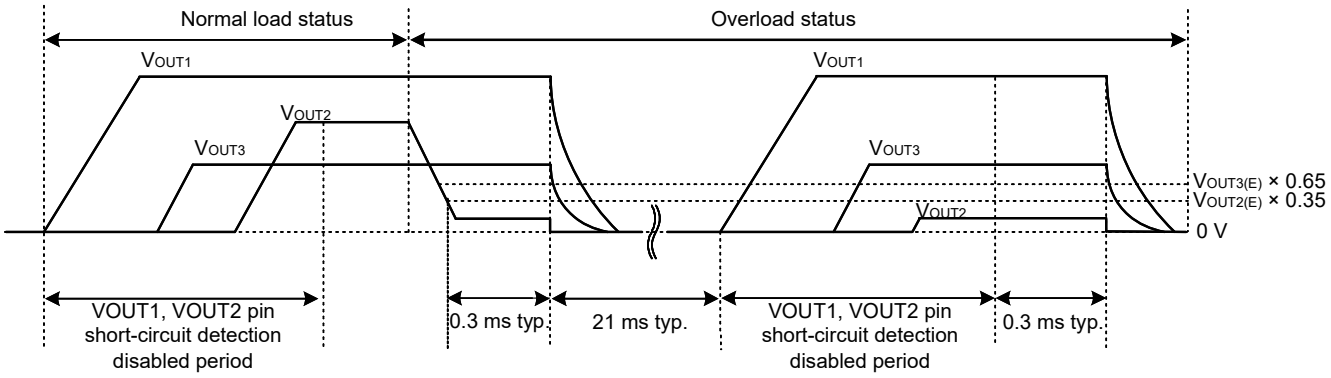


Figure 18 V_{OUT2} Enters Overload Status → Overload Status Continues

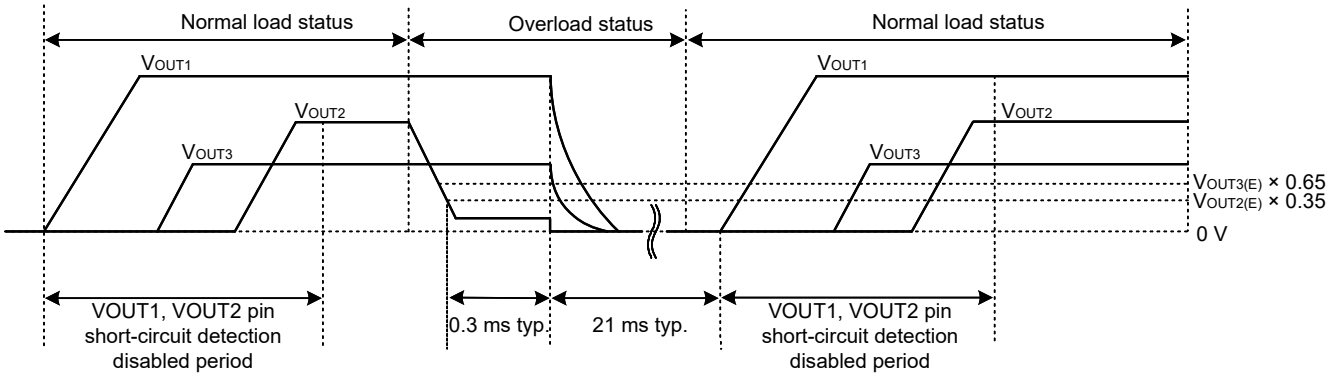


Figure 19 V_{OUT2} Enters Overload Status → Overload Status Is Released

7. 4. 6 SEQ3: V_{OUT3} short-circuit

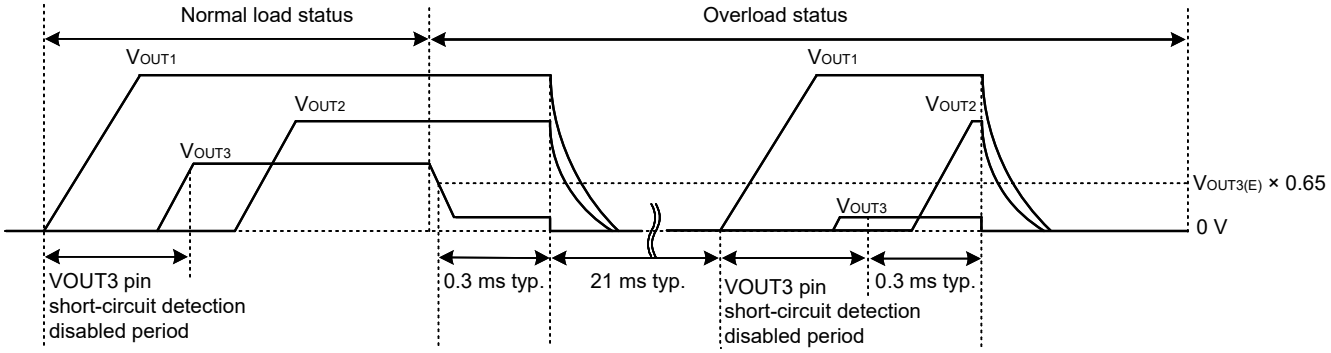


Figure 20 V_{OUT3} Enters Overload Status → Overload Status Continues

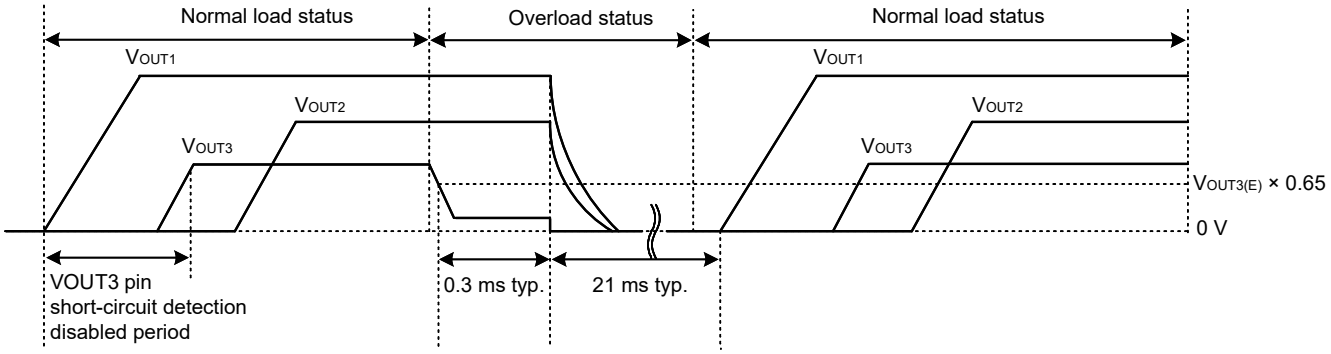


Figure 21 V_{OUT3} Enters Overload Status → Overload Status Is Released

8. Under voltage lockout function (UVLO)

This IC has a built-in UVLO circuit to prevent the IC from malfunctioning due to a transient status at power-on or a momentary drop in the supply voltage. When UVLO status is detected, the high side and low side power MOS FETs of the SW1 pin and SW2 pin and the Pch power MOS FET of the VOUT3 pin are turned off. In products with a discharge shunt function, the SW1 pin, SW2 pin, and VOUT3 pin will be pulled-down to V_{SS}. In addition, the soft start function will also be reset if UVLO status is detected. The startup sequence will start once the UVLO status is released. The IC will enter low current consumption status in the UVLO detection status. Also, there is a hysteresis width for avoiding malfunctions due to generation of noise etc. in the input voltage.

9. Thermal shutdown function

This IC has a built-in thermal shutdown circuit to limit overheating. If the junction temperature increases to 170°C typ., the thermal shutdown circuit will enter the detections status, and both switching operation and VOUT3 pin output will stop.

Once the junction temperature drops to 150°C typ., the thermal shutdown circuit will enter the release status, and switching operation and VOUT3 pin output will restart based on the startup sequence. If the thermal shutdown circuit enters the detection status due to self-heating, each output voltage (V_{OUT1}, V_{OUT2}, and V_{OUT3}) will drop due to the stopping of switching operation and VOUT3 pin output. For this reason, the self-heating is limited and the temperature of the IC decreases. The thermal shutdown circuit will enter release status when the temperature of the IC decreases, the switching operation and VOUT3 pin output are restarted, and the self-heating is generated again. Repeating this procedure makes the waveform of V_{OUT1}, V_{OUT2}, and V_{OUT3} into a pulse-like form. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously. Switching operation and VOUT3 pin output stopping and restarting can be stopped by either lowering the output current (I_{OUT1}, I_{OUT2} and I_{OUT3}) to reduce internal power consumption or decreasing the ambient temperature.

Table 10

Thermal Shutdown Circuit	V_{OUT1}, V_{OUT2}, V_{OUT3}
Release: 150°C typ.*1	Constant value*2
Detection: 170°C typ.*1	Pulled down to V_{SS}*3

***1.** Junction temperature

***2.** A constant value is output due to regulating operation based on the internal resistance.

***3.** Products with a discharge shunt function: The discharge shunt function pulls-down the SW1 pin, SW2 pin, and VOUT3 pin to V_{SS}.

Products without a discharge shunt function: The internal resistance and loads of the VOUT1 pin, VOUT2 pin, and VOUT3 pin will pull-down the VOUT1 pin, VOUT2 pin, and VOUT3 pin to V_{SS}.

Caution If the heat dissipation of the application is not good, self-heating cannot be restricted immediately, and the IC may be destroyed. The actual application should be evaluated carefully to verify that there is no problem.

10. List of protection functions

Table 11

Channel	Item	Detection Level	Protection Operation Details	Release Conditions for Protection Operation
Overall	Under voltage lockout function	V_{REG} ≤ 3.35 V typ.	Output of all channels stops. Hiccup protection is reset. Discharge shunt function is enabled.	V_{REG} ≥ 3.45 V typ.
	Thermal shutdown function	T_j ≥ 170°C typ.	Output of all channels stops. Hiccup protection is reset. Discharge shunt function is enabled.	T_j ≤ 150°C typ.
Ch1	Limit current	I_{L1_max} = 1.2 A typ.	High side power MOS FET is turned OFF.	I_{L1_max} < 1.2 A typ.
	Frequency foldback function	V_{OUT1} ≤ $V_{OUT1(S)}$ × 0.83 typ.	The VOUT1 pin voltage (V_{OUT1}) and the oscillation frequency are in a proportional relationship.*1	V_{OUT1} > $V_{OUT1(S)}$ × 0.83 typ.
	Over current protection (Hiccup)	V_{OUT1} ≤ $V_{OUT1(S)}$ × 0.35 typ.	After 0.3 ms typ. continues. Output of all channels stops. Discharge shunt function is enabled.	Automatic recovery after 21 ms typ. elapses. Startup sequence begins.
Ch2	Limit current	I_{L2_max} = 1.2 A typ.	High side power MOS FET is turned OFF.	I_{L2_max} < 1.2 A typ.
	Frequency foldback function	V_{OUT2} ≤ $V_{OUT2(S)}$ × 0.83 typ.	The VOUT2 pin voltage (V_{OUT2}) and the oscillation frequency are in a proportional relationship.*1	V_{OUT2} > $V_{OUT2(S)}$ × 0.83 typ.
	Over current protection (Hiccup)	V_{OUT2} ≤ $V_{OUT2(S)}$ × 0.35 typ	After 0.3 ms typ. continues. Output of all channels stops. Discharge shunt function is enabled.	Automatic recovery after 21 ms typ. elapses. Startup sequence begins.
Ch3	Limit current	I_{OUT3} = 0 .6 A typ.	Output current is limited to 0.6 A typ.	I_{OUT3} < 0.6 A typ.
	Over current protection (Hiccup)	V_{OUT3} ≤ $V_{OUT3(S)}$ × 0.65 typ.	After 0.3 ms typ. continues. Output of all channels stops. Discharge shunt function is enabled.	Automatic recovery after 21 ms typ. elapses. Startup sequence begins.

***1**. Refer to "**4. 5 Frequency foldback function** " in "**■ Operation**".

11. Internal power supply (VREG)

The major circuits inside the IC operate using VREG pin voltage (V_{REG}) as a power supply. To stabilize this internal power supply, a ceramic capacitor with 1 µF needs to be connected between the VREG pin and the VSS pin. The mounting position of the internal power supply stabilizing capacitor (C_{REG}) is extremely important for stable IC operation. It is recommended that this capacitor be installed as close to the IC as possible. Additionally, note that any external parts other than C_{REG} or any load must not connect to the VREG pin.

12. Thermal design

The power consumption of this IC must be limited to prevent the junction temperature (T_j) from exceeding 150°C.
The junction temperature rated value (T_{jmax}) and power dissipation (P_D) can be estimated using the following relational equation.

$$P_D = (T_{jmax} - Ta) / \theta_{JA}$$

Ta: Ambient temperature
θ_{JA}: Thermal resistance

Thermal resistance (θ_{JA}) varies greatly depending on the pattern and structure of the printed circuit board. Refer to **Table 5**.

The power consumption which occurs in **Figure 22** can be calculated as follows.

$$P = V_{IN} \times I_{IN} - V_{OUT1} \times I_{LOAD1} - V_{OUT2} \times I_{LOAD2} - V_{OUT3} \times I_{LOAD3}$$

V_{IN}:	Input voltage
I_{IN}:	Input current
V_{OUT1}, $V_{OUT\,2}$, V_{OUT3}:	Output voltage for each
I_{LOAD1}, $I_{LOAD\,2}$, $I_{LOAD\,3}$:	Load current for each

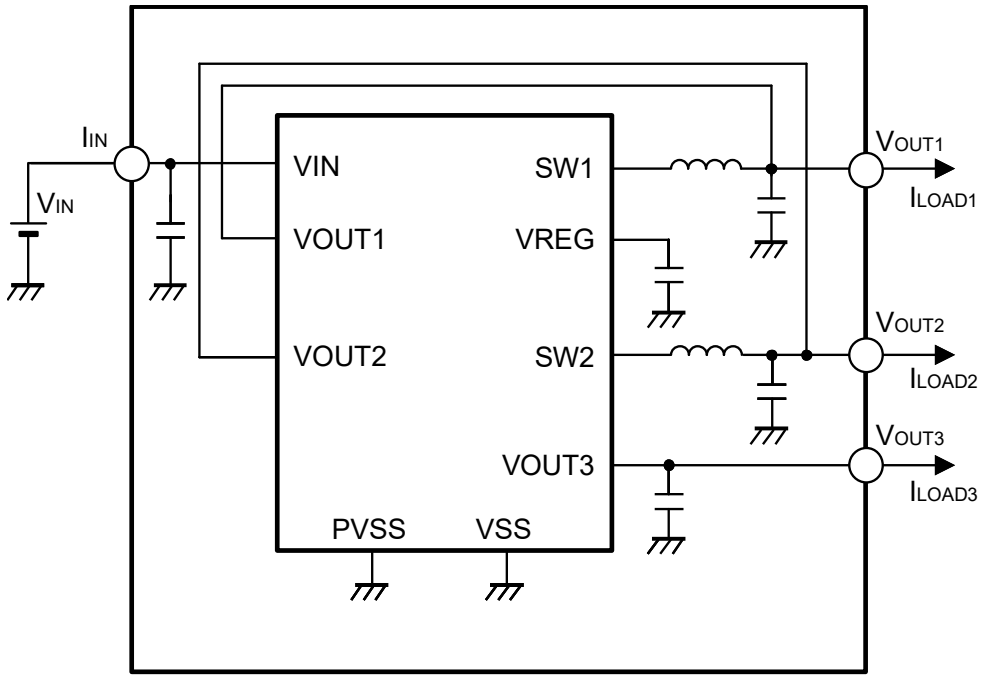


Figure 22

■ Typical Circuits

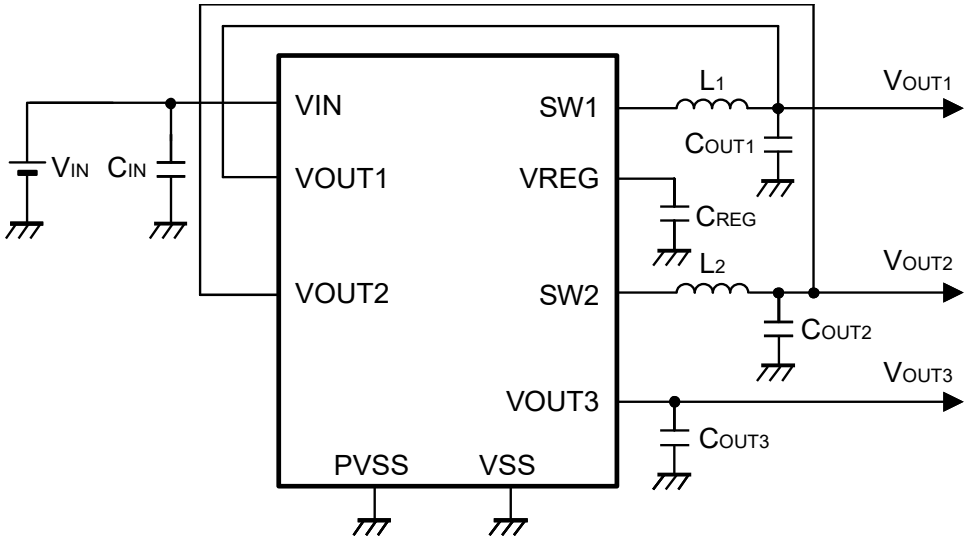


Figure 23

Caution The above connection diagram will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ External Parts Selection

The recommended values for each external part are shown in **Table 12**, and the recommended parts are shown in **Table 13** to **Table 17**. When selecting an input capacitor (C_{IN}), output capacitors (C_{OUT1}, C_{OUT2}, C_{OUT3}), and internal power supply stabilized capacitor (C_{REG}), take into consideration the temperature range and DC bias characteristics of the capacitor to be used.

Table 12

C_{IN}	C_{OUT1}	C_{OUT2}	C_{OUT3}	C_{REG}	L_1	L_2
4.7 µF	10 µF	10 µF	2.2 µF	1 µF	3.3 µH	3.3 µH

Table 13 Recommended Capacitors (C_{IN}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	CGA4J1X7R1E475K125AC	4.7 µF	25 V	2.0 mm × 1.25 mm × 1.25 mm
Murata Manufacturing Co., Ltd.	GCM21BC71E475KE36	4.7 µF	25 V	2.0 mm × 1.25 mm × 1.25 mm

Table 14 Recommended Capacitors (C_{OUT1} and C_{OUT2}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	CGA4J3X7S1A106K125AB	10 µF	10 V	2.0 mm × 1.25 mm × 1.25 mm
Murata Manufacturing Co., Ltd.	GCM188D70J106ME36	10 µF	6.3 V	1.6 mm × 0.8 mm × 0.8 mm

Table 15 Recommended Capacitors (C_{OUT3}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	CGA3E1X7R0J225K080AC	2.2 µF	6.3 V	1.6 mm × 0.8 mm × 0.8 mm
Murata Manufacturing Co., Ltd.	GCM188R70J225KE22	2.2 µF	6.3 V	1.6 mm × 0.8 mm × 0.8 mm

Table 16 Recommended Capacitors (C_{REG}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	CGA3E1X7R1C105K080AC	1 µF	16 V	1.6 mm × 0.8 mm × 0.8 mm
Murata Manufacturing Co., Ltd.	GCM155C71A105KE38	1 µF	10 V	1.0 mm × 0.5 mm × 0.5 mm

Table 17 Recommended inductors (L_1 and L_2) List

Manufacturer	Part Number	Inductance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	TFM252012ALVA3R3MTAA	3.3 µH	40 V	2.5 mm × 2.0 mm × 1.0 mm
Murata Manufacturing Co., Ltd.	DFE252012PD-3R3M	3.3 µH	20 V	2.5 mm × 2.0 mm × 1.2 mm

1. Input Capacitor (C_{IN})

The C_{IN} is used to maintain stable IC operation. It has an effect to suppress the ripple voltage and switching noise to be generated in the power supply line. Ceramic capacitor with 4.7 µF or higher is recommended.

2. Output capacitor (C_{OUT1} and C_{OUT2})

C_{OUT1} and C_{OUT2} are used to smooth output voltage. In general, the ripple voltage (ΔV_{OUT}) which occurs on output V_{OUT} is inversely proportional to the output capacitor C_{OUT}. When selecting a capacitor whose ESR is sufficiently small, ΔV_{OUT} during current continuous mode is calculated by the following expression.

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times f_{OSC} \times C_{OUT}}$$

In addition, because C_{OUT1} and C_{OUT2} contribute to the stability of the feedback loop, a ceramic capacitor with capacitance of 10 µF to 22 µF is recommended. If a capacitor with a capacitance exceeded 22 µF is to be used, make sure to perform thorough evaluation in advance.

3. Output capacitor (C_{OUT3})

This IC requires C_{OUT3} between the VOUT3 pin and the VSS pin for phase compensation. The operation is stabilized by a ceramic capacitor with capacitance of 2.2 µF or more.

4. Inductors (L_1 and L_2)

To suppress the intrinsic subharmonic oscillation in current mode control, the optimal L value needs to be selected. Take the IC internal slope compensation into account and use a 3.3 µH inductor.
When selecting L, note the allowable current. If a current exceeding the allowable current flows through the inductor, magnetic saturation may occur, and there may be risks which substantially lower efficiency and damage the IC as a result of large current.
A current consisting of the ripple current (ΔI_{L1}, ΔI_{L2}) overlaid on the output current (I_{OUT1}, I_{OUT2}) will flow through the inductor. The ΔI_L and peak current (I_{L_max}) which will flow to the inductor during continuous current mode can each be calculated using the following formulas. Make sure I_{L_max} will not exceed the allowable current of inductor.

4. 1 Ch1

$$\Delta I_{L1} = \frac{V_{OUT1} \times (V_{IN} - V_{OUT1})}{f_{OSC} \times L_1 \times V_{IN}}$$

$$I_{L1\_max} = I_{OUT1} + \frac{\Delta I_{L1}}{2}$$

4. 2 Ch2

$$\Delta I_{L2} = \frac{V_{OUT2} \times (V_{OUT1} - V_{OUT2})}{f_{OSC} \times L_2 \times V_{OUT1}}$$

$$I_{L2\_max} = I_{OUT2} + \frac{\Delta I_{L2}}{2}$$

In order to maintain the allowable current of inductor even in cases V_{OUT} shorts to V_{SS} or other fault conditions occur, an inductor with 1.5 A or higher, the maximum value of I_{LIM}, needs to be selected.

5. Internal power supply stabilized capacitor (C_{REG})

C_{REG} is used to stabilize the operation of IC's internal power supply (V_{REG} = 4.5 V typ.). A ceramic capacitor with 1 µF is recommended.

Caution Generally, in a DC-DC converter or LDO regulator, oscillation may occur depending on the selection of the external parts. Perform thorough evaluations including the temperature characteristics with actual applications to confirm no oscillation occurs.

■ Board Layout Guidelines

Note the following cautions when determining the board layout for this IC.

- Place C_{IN} as close to the VIN pin and the VSS pin as possible. Prioritize the layout of C_{IN}.
- Place C_{REG} as close to the VREG pin and the VSS pin as possible.
- Mount C_{IN} and C_{REG} on the same surface layer as the IC. If they are connected through thermal vias, the impedance of the thermal vias may influence the operation, resulting in unstable condition.
- Make the GND pattern as wide as possible.
- Place thermal vias in the GND pattern to ensure sufficient heat dissipation.
- Large current will flow to the SW1 pin and SW2 pin. Make the wiring area of the pattern to be connected to the SW1 pin and SW2 pin small to minimize parasitic capacitance and emission noise.
- Keep the SW1 pin → L_1 → C_{OUT1} → VSS pin, SW2 pin → L_2 → C_{OUT2} → VSS pin loop wiring short. This is an effective way to reduce emission noise.
- Do not wire the SW1 pin or SW2 pin pattern under the IC.

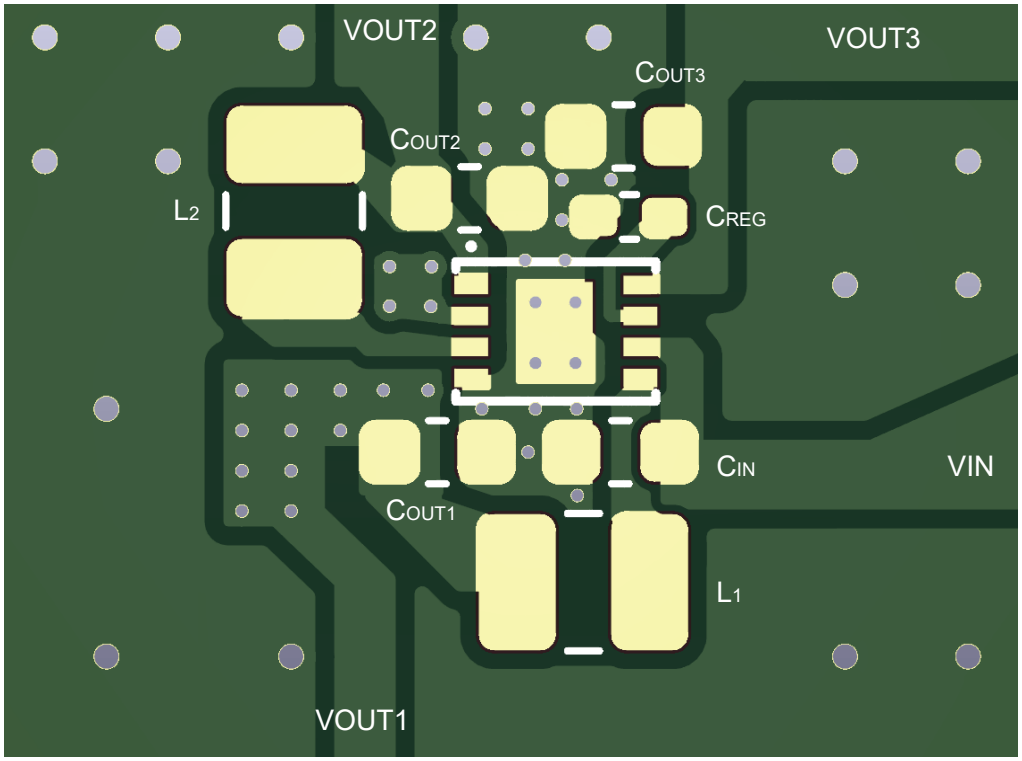


Figure 24 Reference Board Pattern

Caution The above pattern diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to determine the pattern.

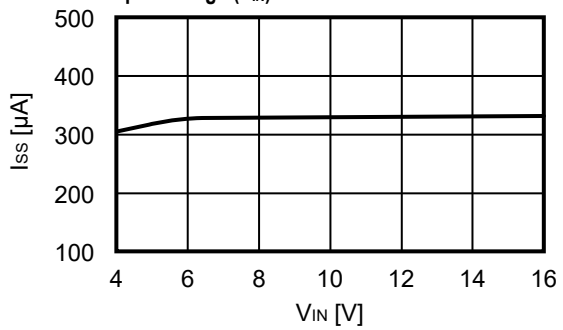
■ Precautions

- Mount external capacitors and inductors as close as possible to the IC, and make single GND.
- Characteristic ripple voltage and spike noise occur in the IC containing DC-DC converters. Moreover rush current flows at the time of a power supply injection. Because these largely depend on the inductor, the capacitor and impedance of power supply to be used, fully check them using an actually mounted model.
- The 4.7 μF capacitor connected between the VIN pin and the VSS pin is a bypass capacitor. It stabilizes the power supply in the IC, and thus effectively works for stable switching regulator operation. Allocate the bypass capacitor as close to the IC as possible, prioritized over other parts.
- Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
- The power dissipation of the IC greatly varies depending on the size and material of the board to be connected. Perform sufficient evaluation using an actual application before designing.
- Generally, when a LDO regulator is used under the condition that the load current value is small (1 mA or less), the output voltage may increase due to the leakage current of an output transistor.
- Generally, when a LDO regulator is used under the condition that the temperature is high, the output voltage may increase due to the leakage current of an output transistor.
- Generally, in a LDO regulator, an oscillation may occur depending on the selection of the external parts. The recommended usage conditions for this IC's Ch3 are noted in "**■ External parts selection**" **Table 15**, but perform a thorough evaluation including the temperature characteristics, through the actual application.
- Generally, in a LDO regulator, the values of an overshoot and an undershoot in the output voltage vary depending on the variation factors of input voltage fluctuation, load fluctuation etc., or the capacitance of C_{OUT} and the value of the equivalent series resistance (ESR), which may cause a problem to the stable operation. Perform thorough evaluation including the temperature characteristics with an actual application to select C_{OUT}.
- Generally, in a LDO regulator, if the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur in the VOUT pin due to resonance phenomenon of the inductance and the capacitance including C_{OUT} on the application. The resonance phenomenon is expected to be weakened by inserting a series resistor into the resonance path, and the negative voltage is expected to be limited by inserting a protection diode between the VOUT pin and the VSS pin.
- When considering the output current value that this IC is able to output, make sure in "**6. Allowable load current for each output**" and "**12. Thermal design**" in "**■ Operation**".
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

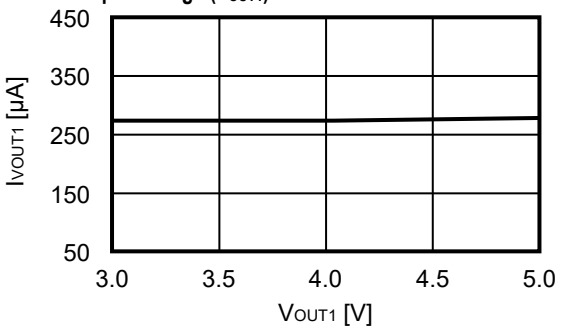
■ Characteristics (Typical Data)

1. Example of major power supply dependence characteristics (Ta = +25°C)

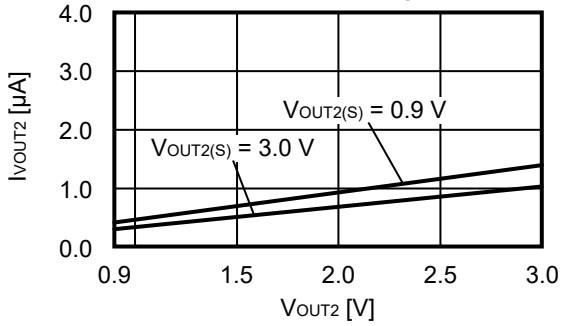
1. 1 VIN pin current consumption during shutdown (I_{SS}) vs. Input voltage (V_{IN})



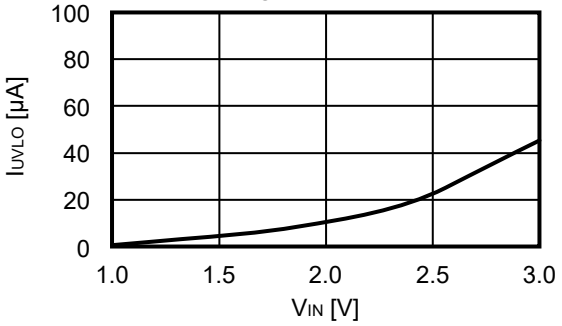
1. 2 VOUT1 pin current consumption during shutdown (I_{VOUT1}) vs. Input voltage (V_{OUT1})



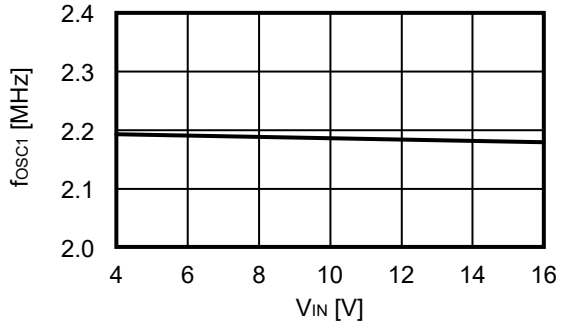
1. 3 VOUT2 pin current consumption during shutdown (I_{VOUT2}) vs. Input voltage (V_{OUT2})



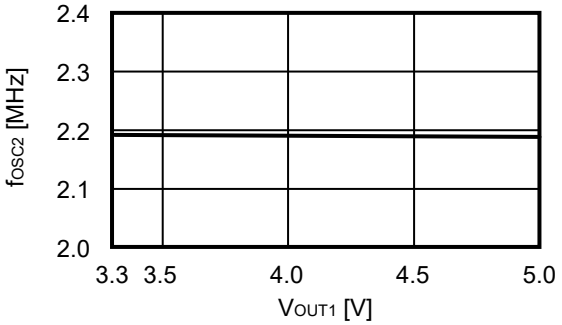
1. 4 Current consumption during UVLO detection (I_{UVLO}) vs. Input voltage (V_{IN})



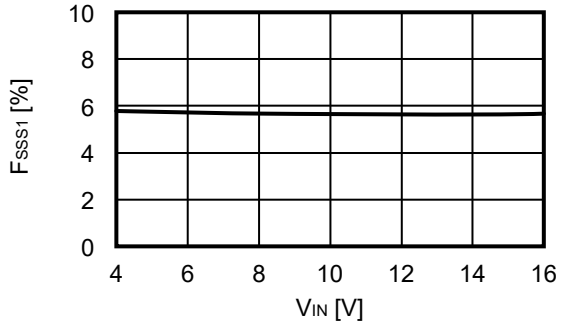
1. 5 Oscillation frequency (f_{OSC1}) vs. Input voltage (V_{IN})



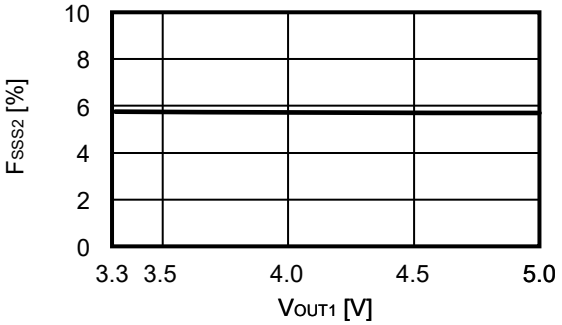
1. 6 Oscillation frequency (f_{OSC2}) vs. Input voltage (V_{OUT1})



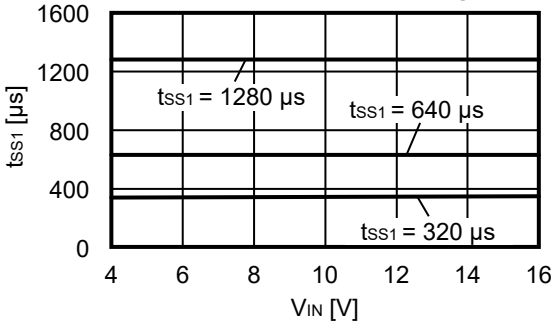
1. 7 Oscillation frequency modulation rate (F_{SSS1}) vs. Input voltage (V_{IN})



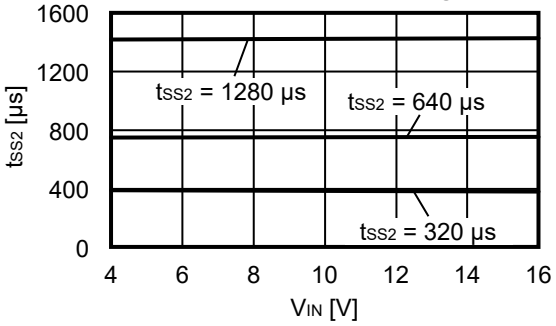
1. 8 Oscillation frequency modulation rate (F_{SSS2}) vs. Input voltage (V_{OUT1})



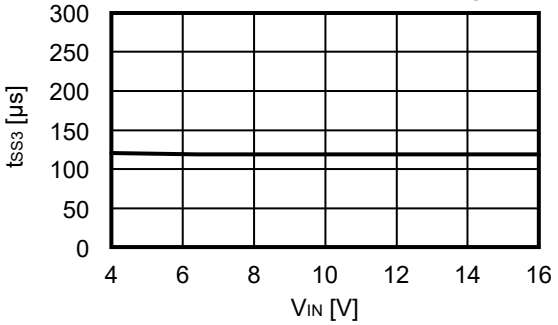
1. 9 Soft-start time (t_{SS1}) vs. Input voltage (V_{IN})



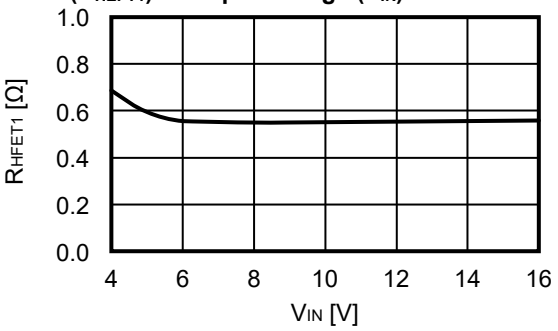
1. 10 Soft-start time (t_{SS2}) vs. Input voltage (V_{IN})



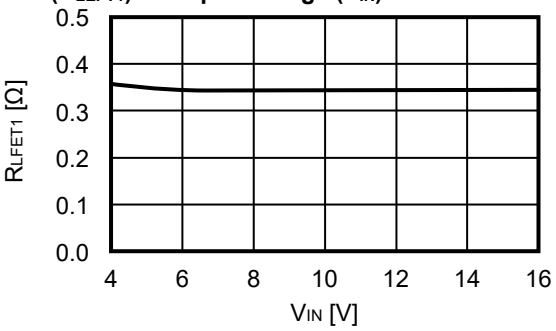
1. 11 Soft-start time (t_{SS3}) vs. Input voltage (V_{IN})



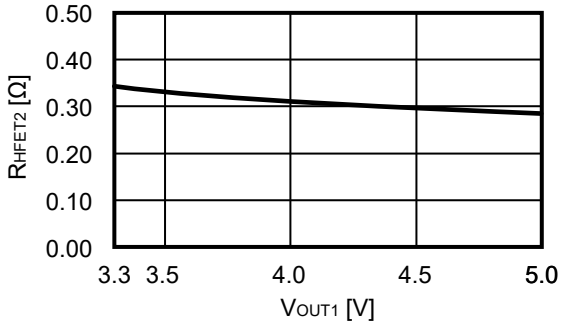
1. 12 High side power MOS FET on-resistance (R_{HEFT1}) vs. Input voltage (V_{IN})



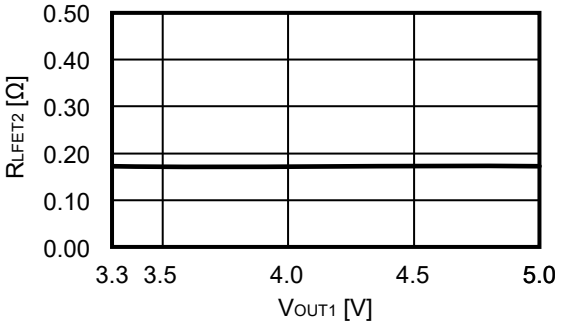
1. 13 Low side power MOS FET on-resistance (R_{LEFT1}) vs. Input voltage (V_{IN})



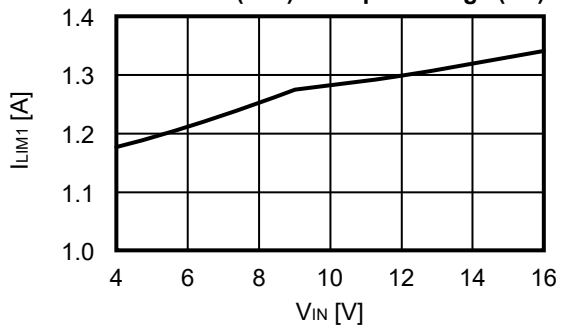
1. 14 High side power MOS FET on-resistance (R_{HEFT2}) vs. Input voltage (V_{OUT1})



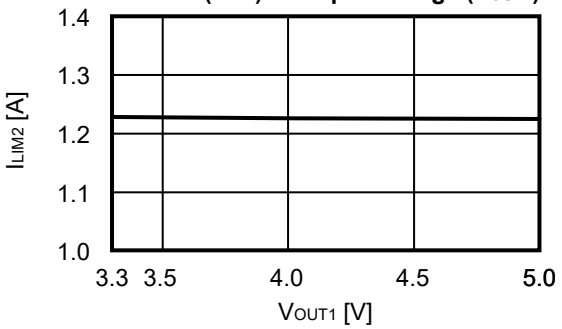
1. 15 Low side power MOS FET on-resistance (R_{LEFT2}) vs. Input voltage (V_{OUT1})



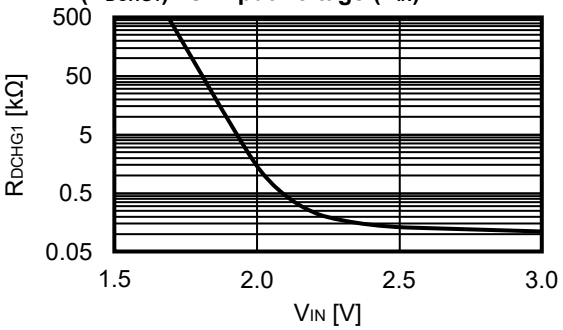
1. 16 Limit current (I_{LIM1}) vs. Input voltage (V_{IN})



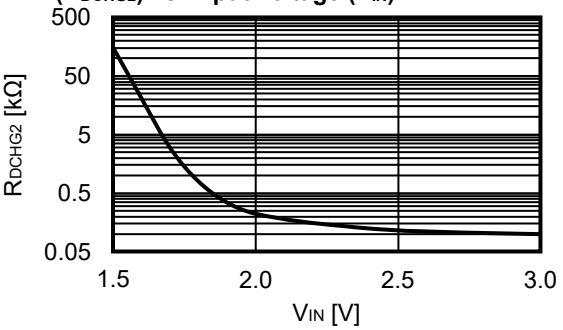
1. 17 Limit current (I_{LIM2}) vs. Input voltage (V_{OUT1})



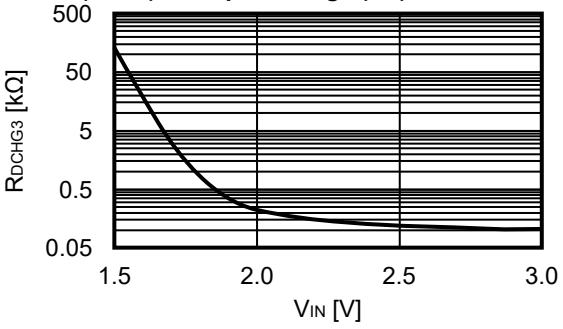
1. 18 SW1 pin discharge switch resistance value (R_{DCHG1}) vs. Input voltage (V_{IN})



1. 19 SW2 pin discharge switch resistance value (R_{DCHG2}) vs. Input voltage (V_{IN})

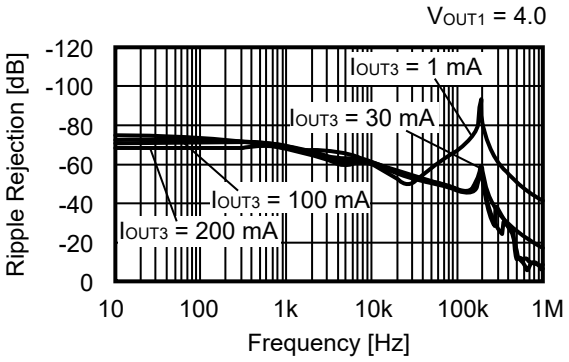


1. 20 VOUT3 pin discharge switch resistance value (R_{DSG3}) vs. Input voltage (V_{IN})

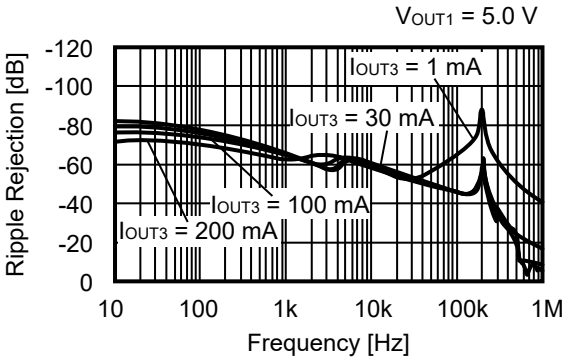


1. 21 Ripple rejection (Ta = +25°C)

1. 21. 1 V_{OUT3} = 1.8 V



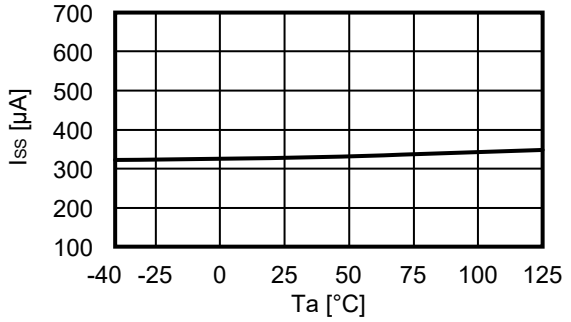
1. 21. 2 V_{OUT3} = 3.3 V



2. Example of major temperature characteristics (Ta = -40°C to +125°C)

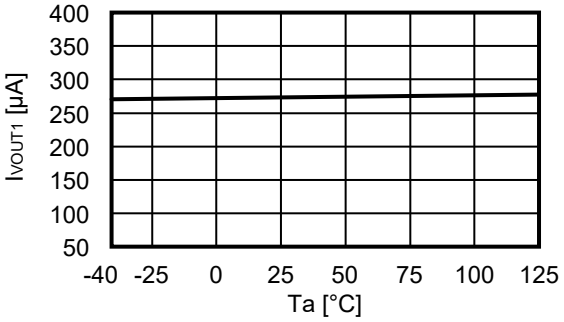
2. 1 VIN pin current consumption during shutdown (I_{SS}) vs. Temperature (Ta)

V_{IN} = 6.0 V, V_{OUT1} = $V_{OUT1(s)}$ × 1.1, V_{OUT2} = $V_{OUT2(s)}$) × 1.1



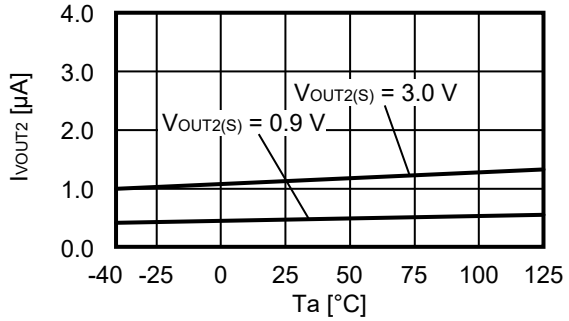
2. 2 VOUT1 pin current consumption during shutdown (I_{VOUT1}) vs. Temperature (Ta)

V_{IN} = 6.0 V, V_{OUT1} = $V_{OUT1(s)}$ × 1.1, V_{OUT2} = $V_{OUT2(s)}$) × 1.1



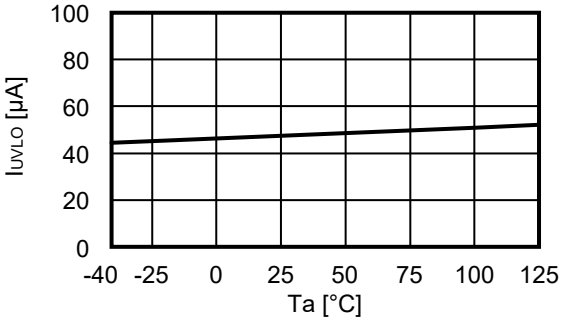
2. 3 VOUT2 pin current consumption during shutdown (I_{VOUT2}) vs. Temperature (Ta)

V_{IN} = 6.0 V, V_{OUT1} = $V_{OUT1(s)}$ × 1.1, V_{OUT2} = $V_{OUT2(s)}$ × 1.1



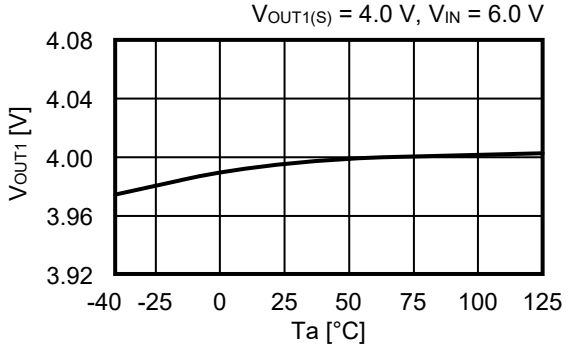
2. 4 Current consumption during UVLO detection (I_{UVLO}) vs. Temperature (Ta)

V_{IN} = 3.0 V



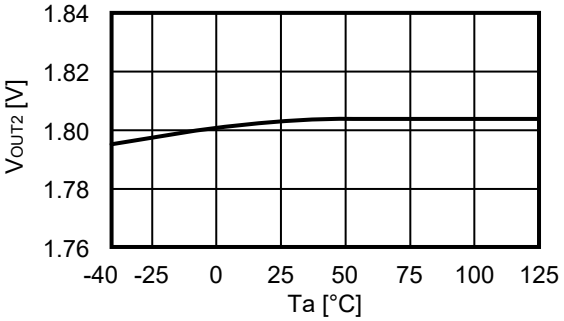
2. 5 VOUT1 pin voltage (V_{OUT1}) vs. Temperature (Ta)

$V_{OUT1(S)}$ = 4.0 V, V_{IN} = 6.0 V



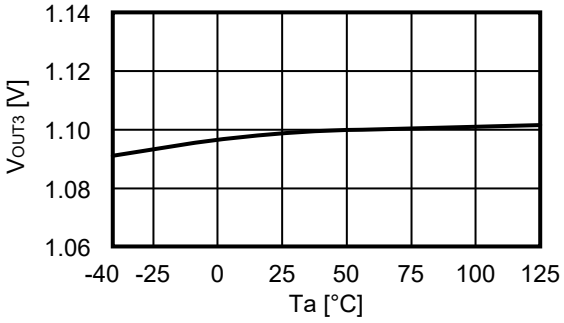
2. 6 VOUT2 pin voltage (V_{OUT2}) vs. Temperature (Ta)

$V_{OUT2(S)}$ = 1.8 V, V_{IN} = 6.0 V, V_{OUT1} = 4.0 V

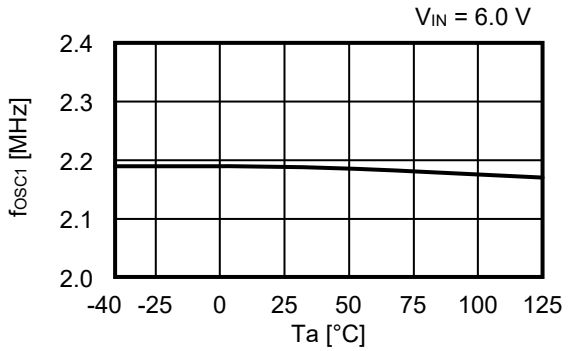


2. 7 VOUT3 pin voltage (V_{OUT3}) vs. Temperature (Ta)

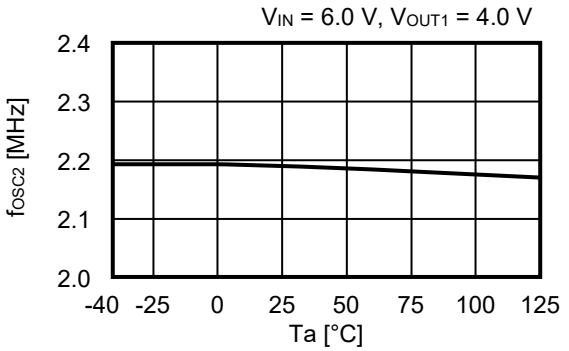
$V_{OUT3(S)}$ = 1.1 V, V_{IN} = 6.0 V, V_{OUT1} = 4.0 V



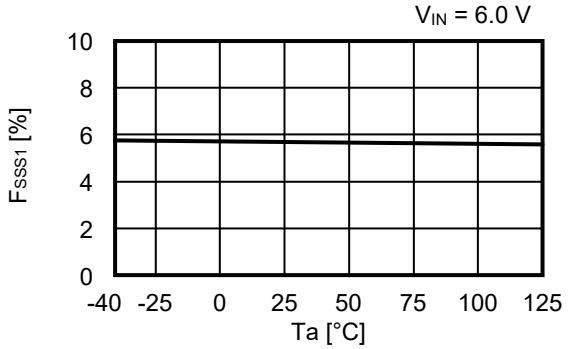
2. 8 Oscillation Frequency (f_{OSC1}) vs. Temperature (Ta)



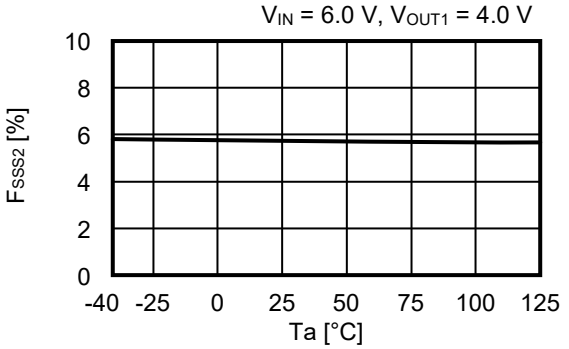
2. 9 Oscillation Frequency (f_{OSC2}) vs. Temperature (Ta)



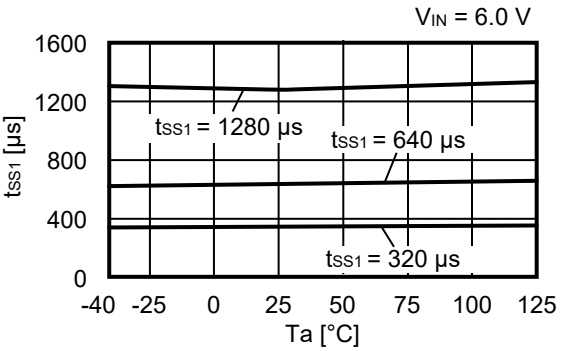
2. 10 Oscillation Frequency modulation rate (F_{SSS1}) vs. Temperature (Ta)



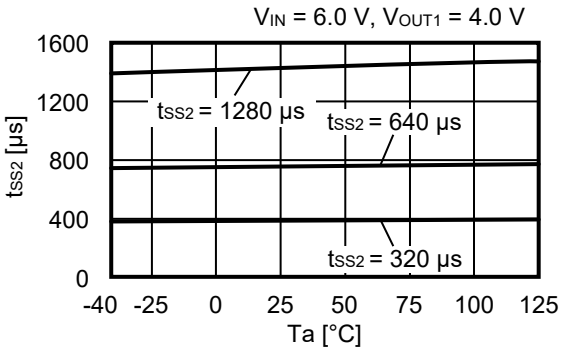
2. 11 Oscillation Frequency modulation rate (F_{SSS2}) vs. Temperature (Ta)



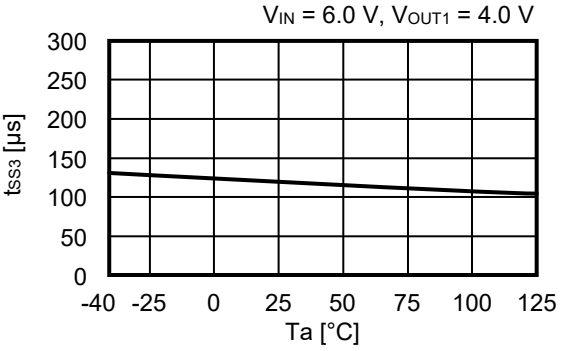
2. 12 Soft-start time (t_{SS1}) vs. Temperature (Ta)



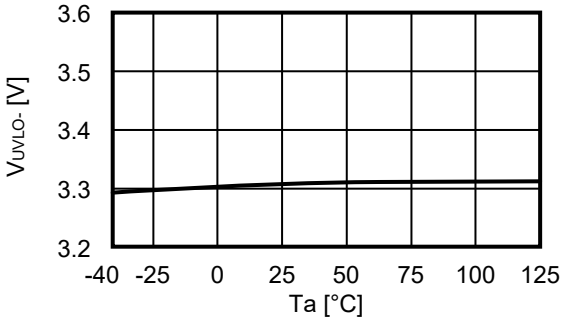
2. 13 Soft-start time (t_{SS2}) vs. Temperature (Ta)



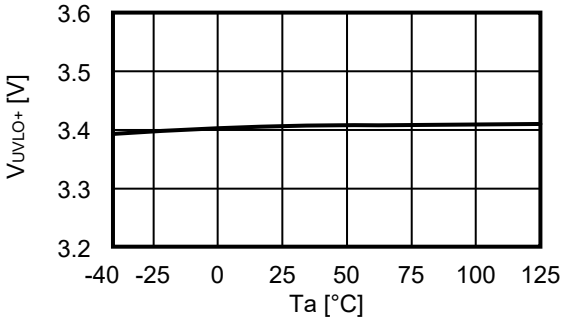
2. 14 Soft-start time (t_{SS3}) vs. Temperature (Ta)



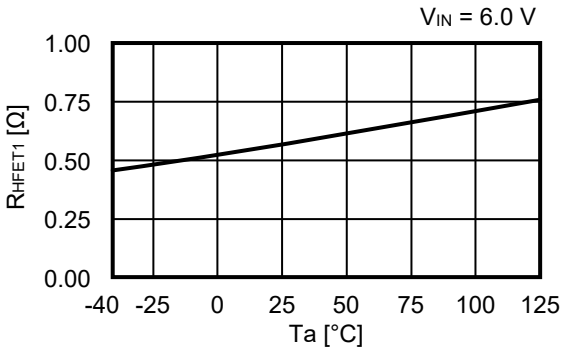
2. 15 UVLO detection voltage (V_{UVLO-}) vs. Temperature (Ta)



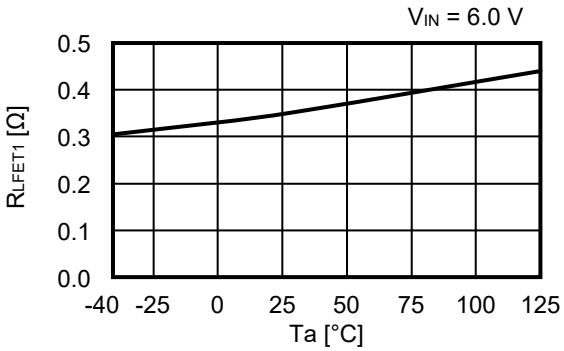
2. 16 UVLO release voltagege (V_{UVLO+}) vs. Temperature (Ta)



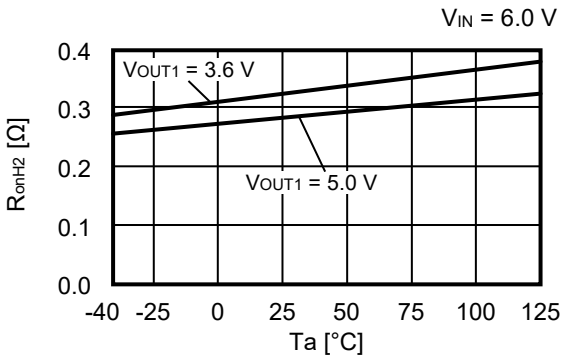
2. 17 High side power MOS FET on-resistance (R_{HEFT1}) vs. Temperature (Ta)



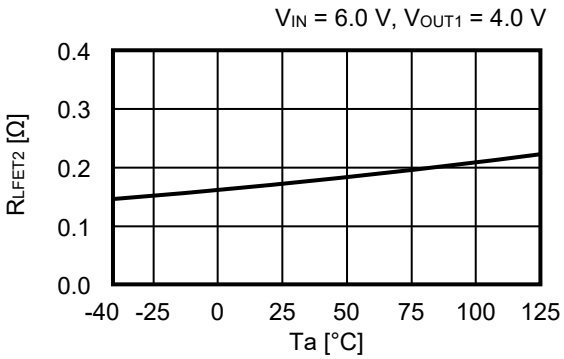
2. 18 Low side power MOS FET on-resistance (R_{LEFT1}) vs. Temperature (Ta)



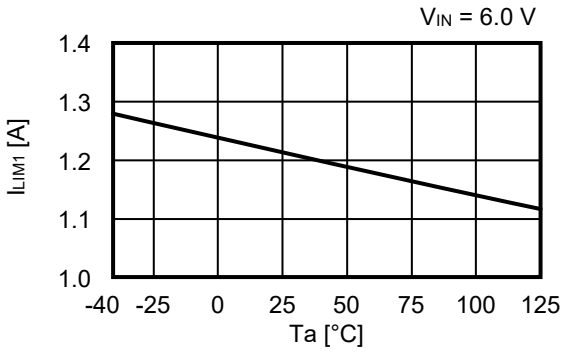
2. 19 High side power MOS FET on-resistance (R_{HEFT2}) vs. Temperature (Ta)



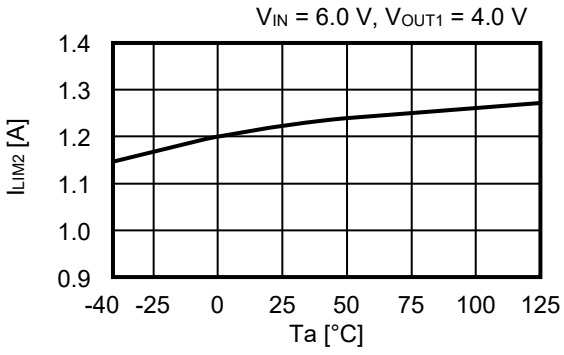
2. 20 Low side power MOS FET on-resistance (R_{LEFT2}) vs. Temperature (Ta)



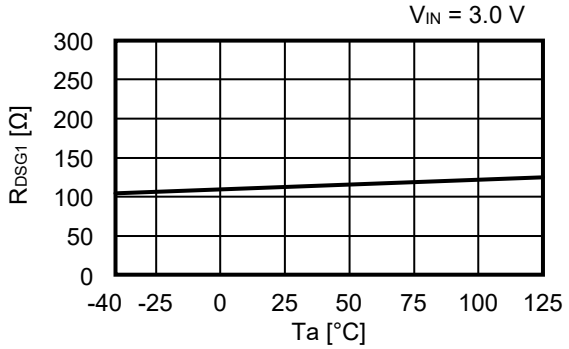
2. 21 Limit current (I_{LIM1}) vs. Temperature (Ta)



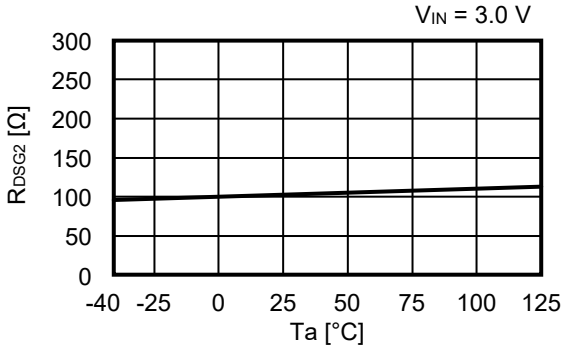
2. 22 Limit current (I_{LIM2}) vs. Temperature (Ta)



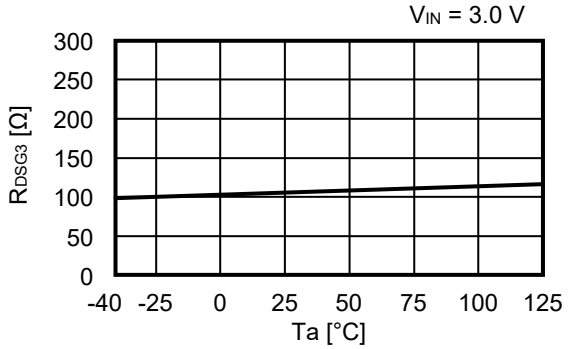
2. 23 SW1 pin discharge switch resistance value (R_{DSG1}) vs. Temperature (Ta)



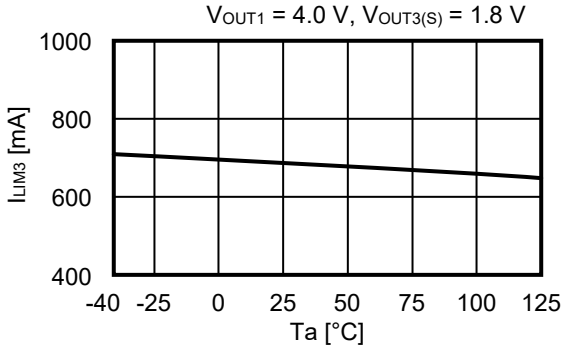
2. 24 SW2 pin discharge switch resistance value (R_{DSG2}) vs. Temperature (Ta)



2. 25 VOUT3 pin discharge switch resistance value (R_{DSG3}) vs. Temperature (Ta)



2. 26 VOUT3 Pin Limit Current (I_{LIM3}) vs Temperature (Ta)



3. Transient response characteristics

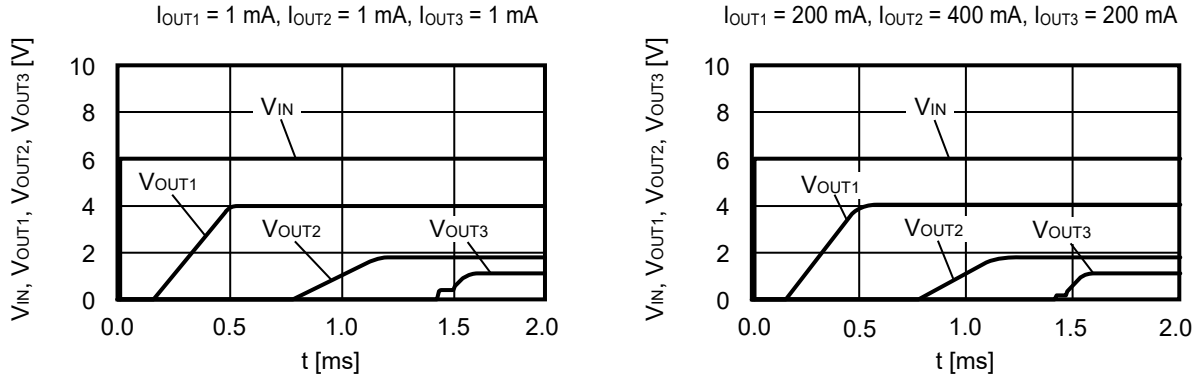
The external parts shown in **Table 18** are used in "**3. Transient response characteristics**".

Table 18

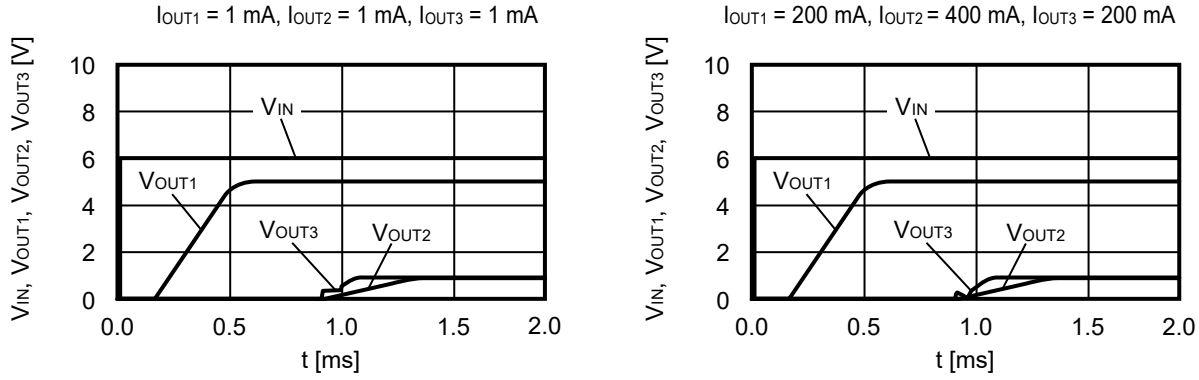
Symbol	Part Number	Constant	Withstanding Voltage	Manufacturer
C_{IN}	CGA4J1X7R1E475K125AC	4.7 µH	25 V	TDK Corporation
C_{OUT1}, C_{OUT2}	CGA4J3X7S1A106K125AB	10 µF	10 V	TDK Corporation
C_{OUT3}	CGA3E1X7R0J225K080AC	2.2 µF	6.3 V	TDK Corporation
C_{REG}	CGA3E1X7R1C105K080AC	1 µF	16 V	TDK Corporation
L_1, L_2	TFM252012ALVA3R3MTAA	3.3 µF	40 V	TDK Corporation

3. 1 Power-on (V_{IN} = 0 0V → 6.0 V, Ta = +25°C)

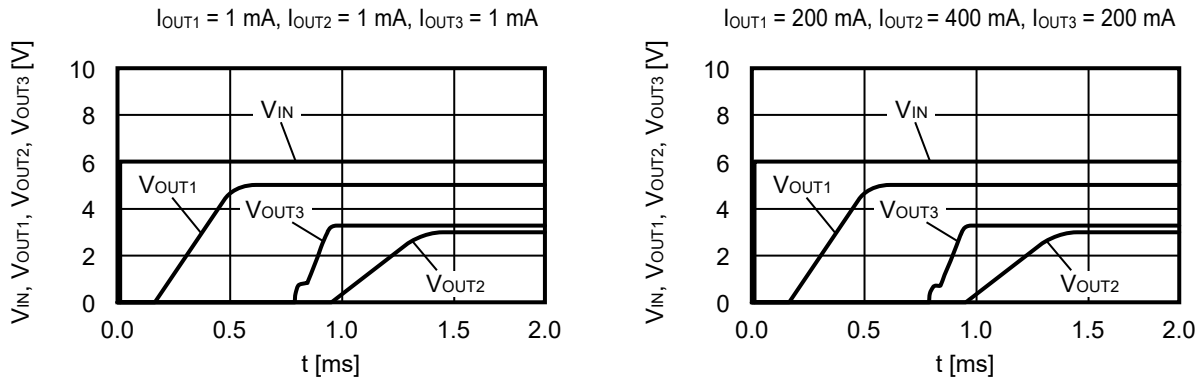
3. 1. 1 SEQ1 (V_{OTUT1} = 4.0 V, V_{OUT2} = 1.8 V, V_{OUT3} = 1.1 V)



3. 1. 2 SEQ2 (V_{OTUT1} = 5.0 V, V_{OUT2} = 0.9 V, V_{OUT3} = 0.9 V)

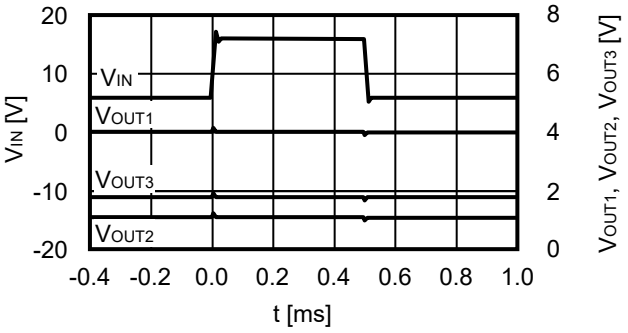


3. 1. 3 SEQ3 (V_{OTUT1} = 5.0 V, V_{OUT2} = 3.0 V, V_{OUT3} = 3.3 V)

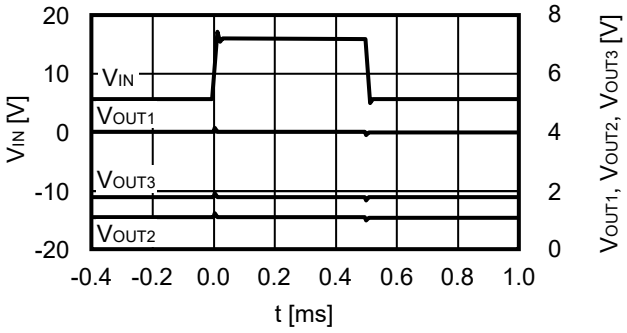


3. 2 Power supply fluctuation (V_{IN} = 6.0 V → 16.0 V → 6.0 V, Ta = +25°C)

I_{OUT1} = 1 mA, I_{OUT2} = 1 mA, I_{OUT3} = 1 mA

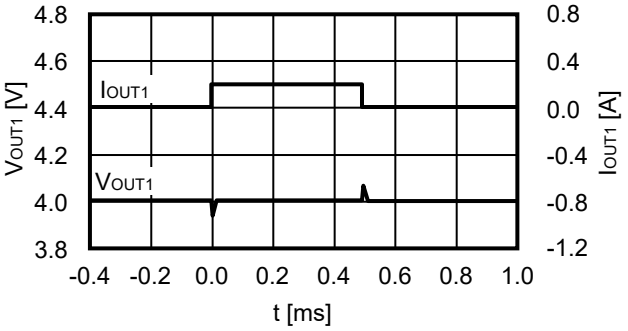


I_{OUT1} = 200 mA, I_{OUT2} = 400 mA, I_{OUT3} = 200 mA

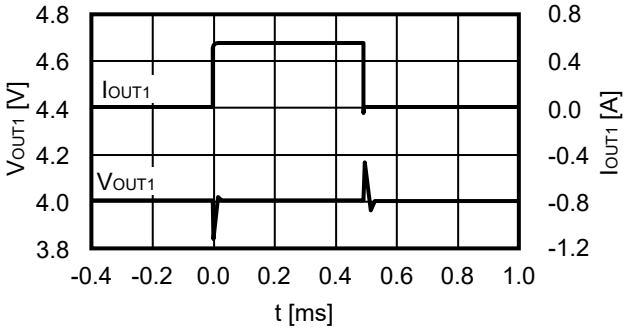


3. 3 Load fluctuation (V_{IN} = 6.0 V, Ta = +25°C)

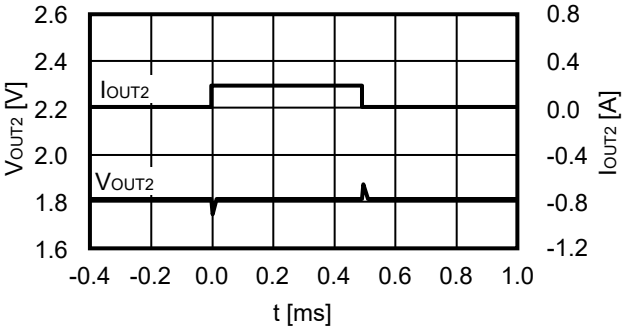
I_{OUT1} = 1 mA → 200 mA → 1 mA



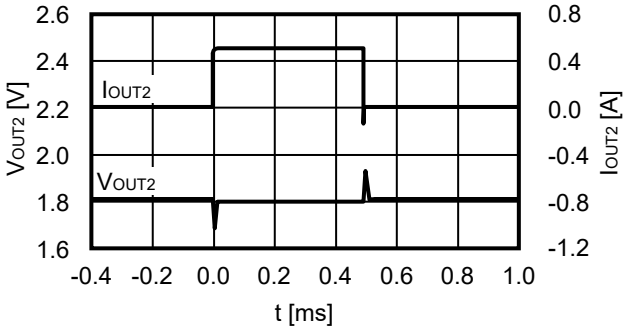
I_{OUT1} = 1 mA → 600 mA → 1 mA



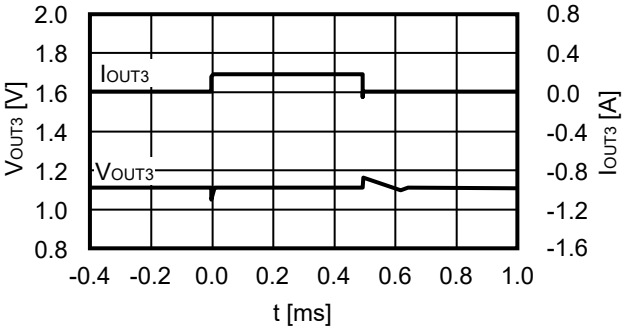
I_{OUT2} = 1 mA → 200 mA → 1 mA



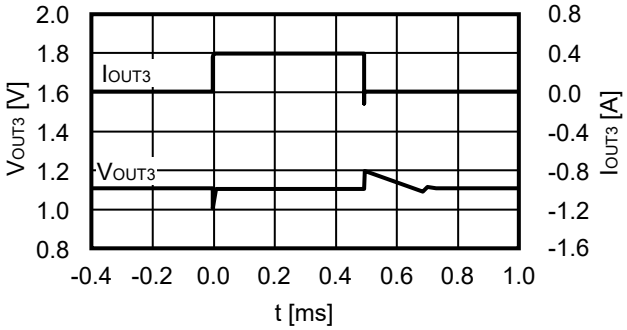
I_{OUT2} = 1 mA → 500 mA → 1 mA



I_{OUT3} = 1 mA → 200 mA → 1 mA



I_{OUT3} = 1 mA → 400 mA → 1 mA



■ Reference Data

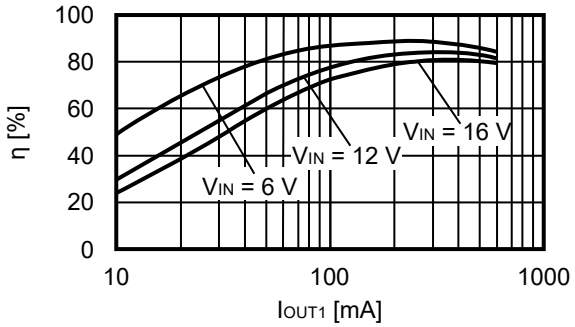
The external parts shown in **Table 19** are used in "**■ Reference Data**".

Table 19

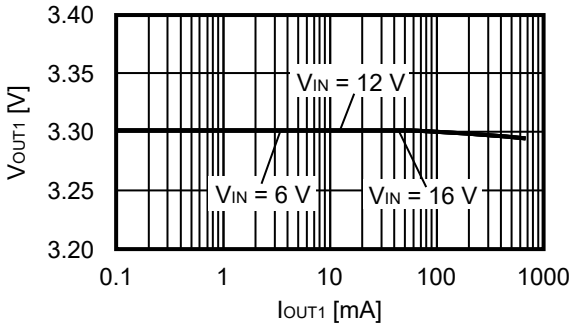
Symbol	Part Number	Constant	Withstanding Voltage	Manufacturer
C_{IN}	CGA4J1X7R1E475K125AC	4.7 µH	25 V	TDK Corporation
C_{OUT1}, C_{OUT2}	CGA4J3X7S1A106K125AB	10 µF	10 V	TDK Corporation
C_{OUT3}	CGA3E1X7R0J225K080AC	2.2 µF	6.3 V	TDK Corporation
C_{REG}	CGA3E1X7R1C105K080AC	1 µF	16 V	TDK Corporation
L_1, L_2	TFM252012ALVA3R3MTAA	3.3 µF	40 V	TDK Corporation

1. V_{OUT1} = 3.3 V

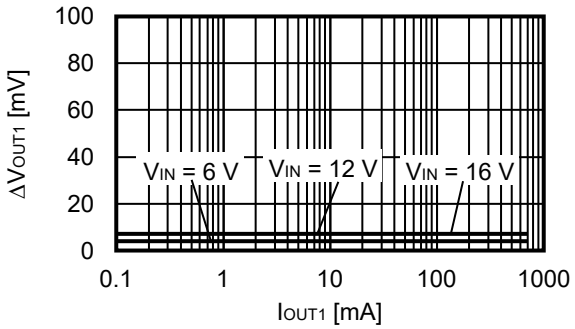
1. 1 Efficiency (η) vs. Output current (I_{OUT1})



1. 2 Output voltage (V_{OUT1}) vs. Output current (I_{OUT1})

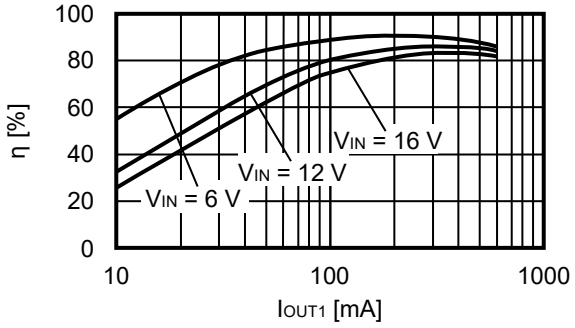


1. 3 Ripple voltage (ΔV_{OUT1}) vs. Output current (I_{OUT1})

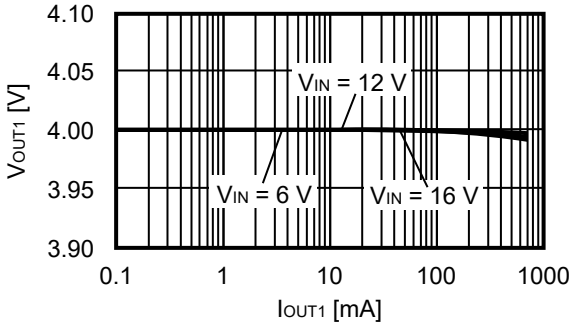


2. V_{OUT1} = 4.0 V

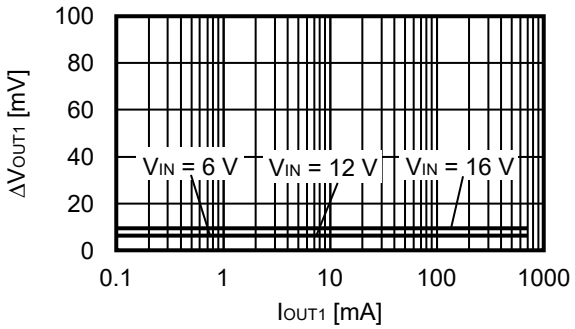
2. 1 Efficiency (η) vs. Output current (I_{OUT1})



2. 2 Output voltage (V_{OUT1}) vs. Output current (I_{OUT1})

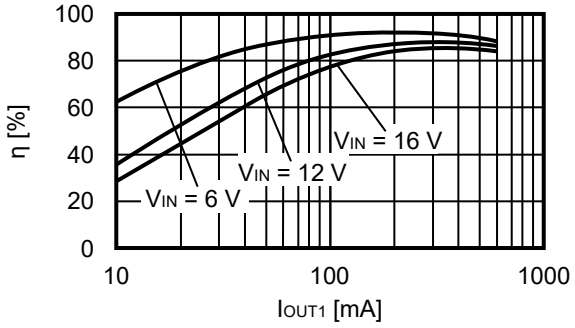


2. 3 Ripple voltage (ΔV_{OUT1}) vs. Output current (I_{OUT1})

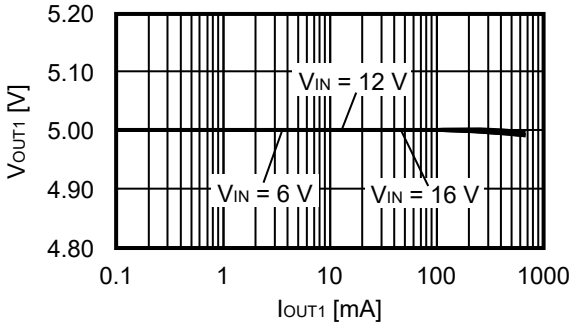


3. V_{OUT1} = 5.0 V

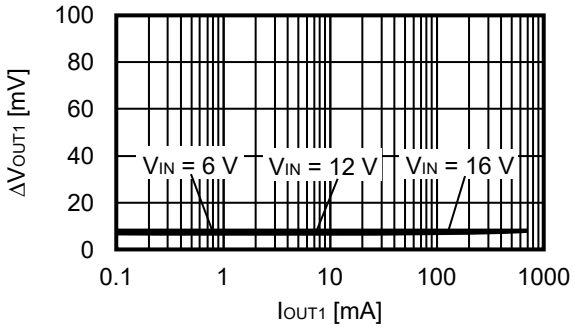
3. 1 Efficiency (η) vs. Output current (I_{OUT1})



3. 2 Output voltage (V_{OUT1}) vs. Output current (I_{OUT1})

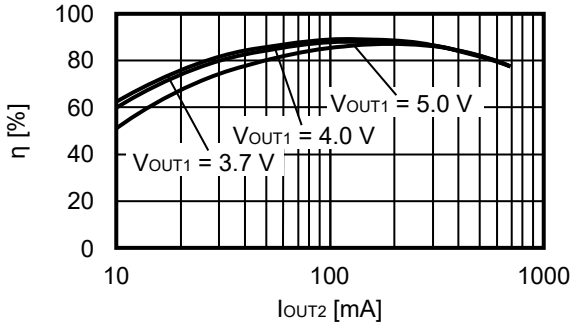


3. 3 Ripple voltage (ΔV_{OUT1}) vs. Output current (I_{OUT1})

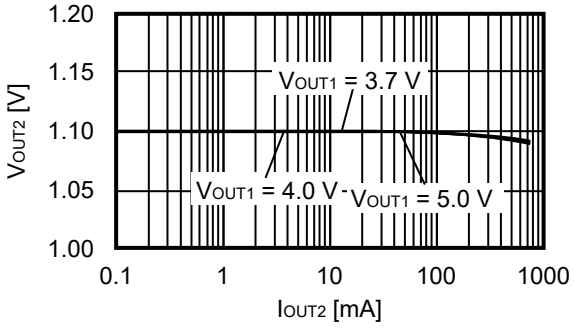


4. V_{OUT2} = 1.1 V

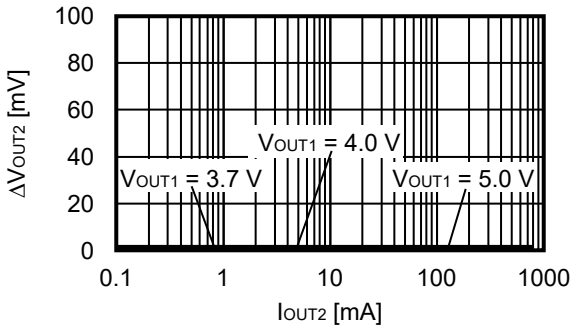
4. 1 Efficiency (η) vs. Output current (I_{OUT2})



4. 2 Output voltage (V_{OUT2}) vs. Output current (I_{OUT2})

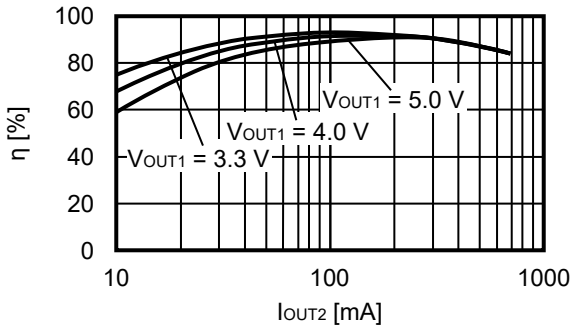


4. 3 Ripple voltage (ΔV_{OUT2}) vs. Output current (I_{OUT2})

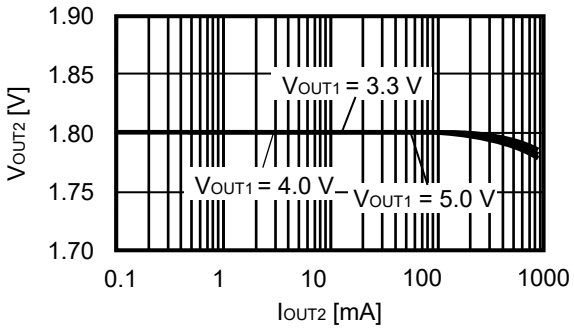


5. V_{OUT2} = 1.8 V

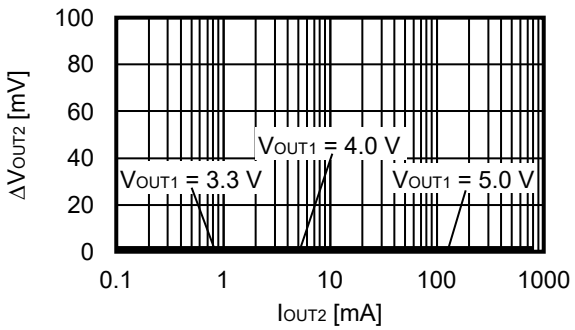
5. 1 Efficiency (η) vs. Output current (I_{OUT2})



5. 2 Output voltage (V_{OUT2}) vs. Output current (I_{OUT2})

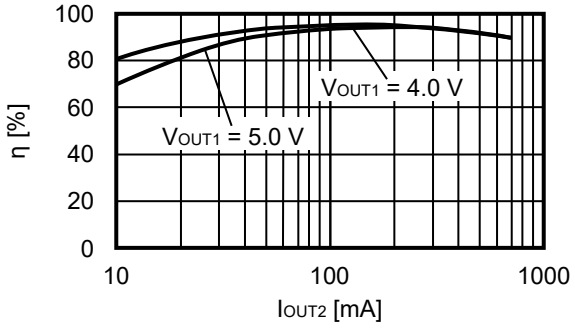


5. 3 Ripple voltage (ΔV_{OUT2}) vs. Output current (I_{OUT2})

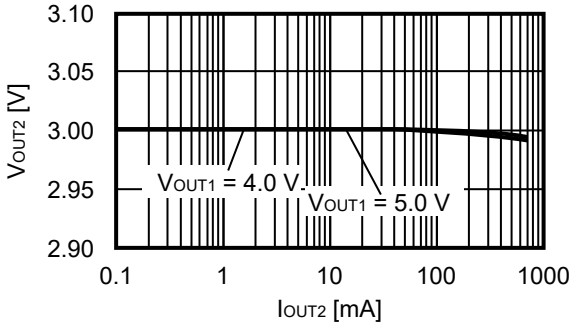


6. V_{OUT2} = 3.0 V

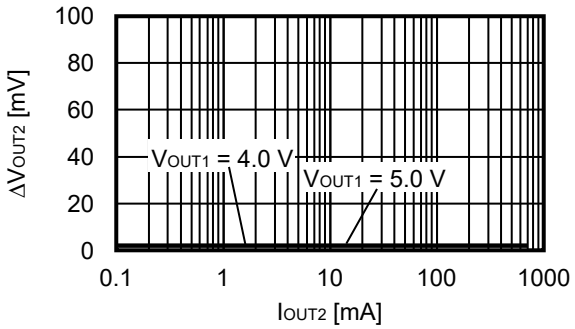
6. 1 Efficiency (η) vs. Output current (I_{OUT2})



6. 2 Output voltage (V_{OUT2}) vs. Output current (I_{OUT2})

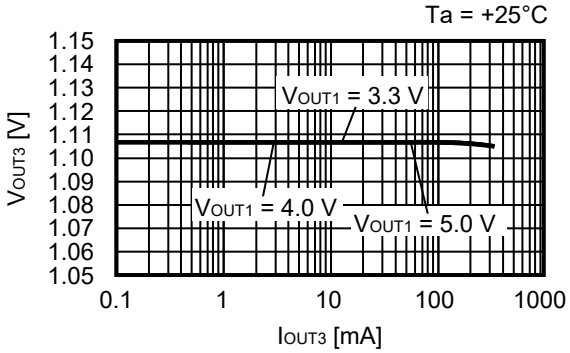


6. 3 Ripple voltage (ΔV_{OUT2}) vs. Output current (I_{OUT2})



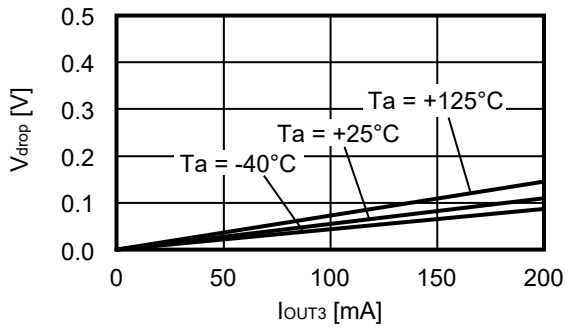
7. V_{OUT3} = 1.1 V

7. 1 Output voltage (V_{OUT3}) vs. Output current (I_{OUT3})

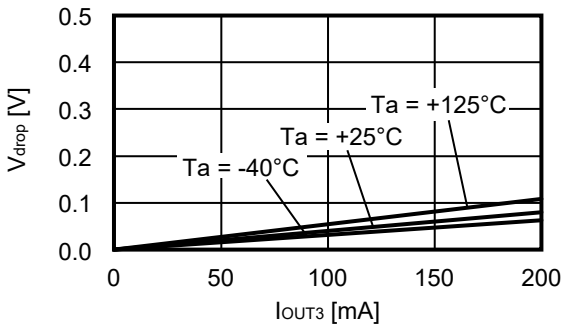


8. Dropout voltage (V_{drop}) - Output current (I_{OUT3})

8. 1 V_{OUT3} = 1.8 V

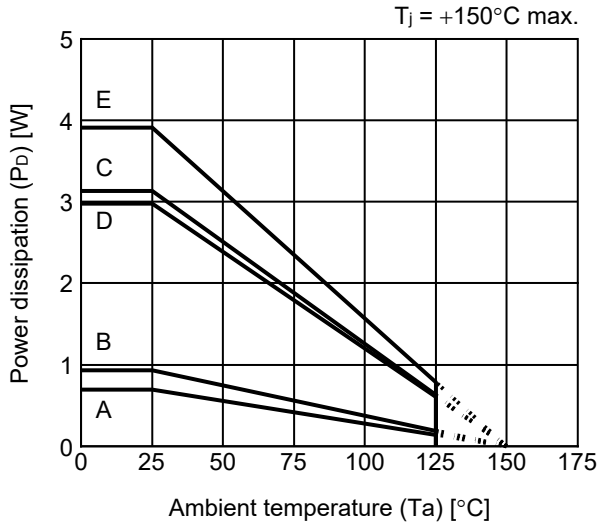


8. 2 V_{OUT3} = 3.3 V



■ Power Dissipation

HSNT-8(2030)

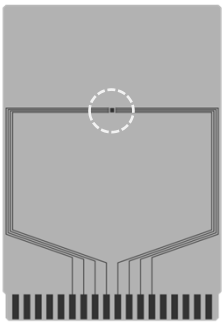


Board	Power Dissipation (P_D)
A	0.69 W
B	0.93 W
C	3.13 W
D	2.98 W
E	3.91 W

HSNT-8(2030) Test Board

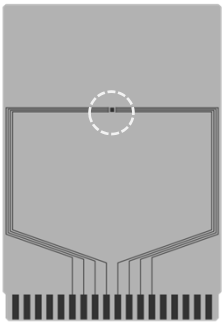
IC Mount Area

(1) Board A



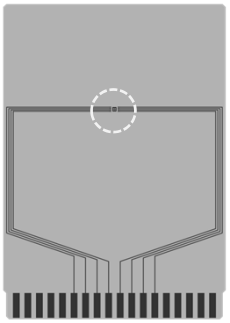
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

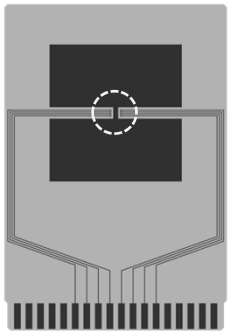
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-A-Board-SD-2.0

HSNT-8(2030) Test Board

IC Mount Area

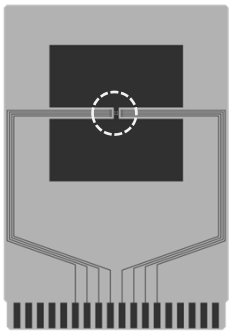
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

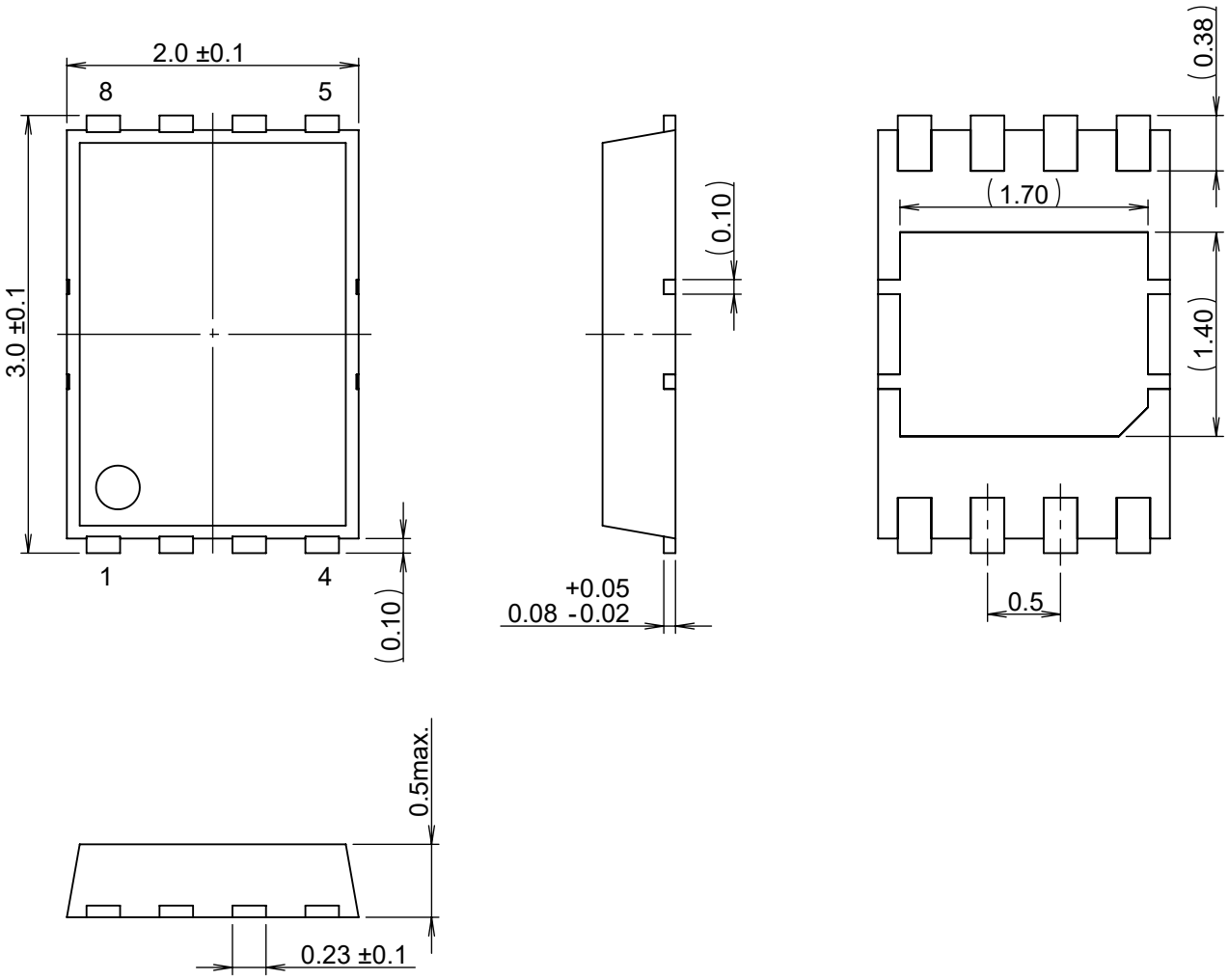
(5) Board E



enlarged view

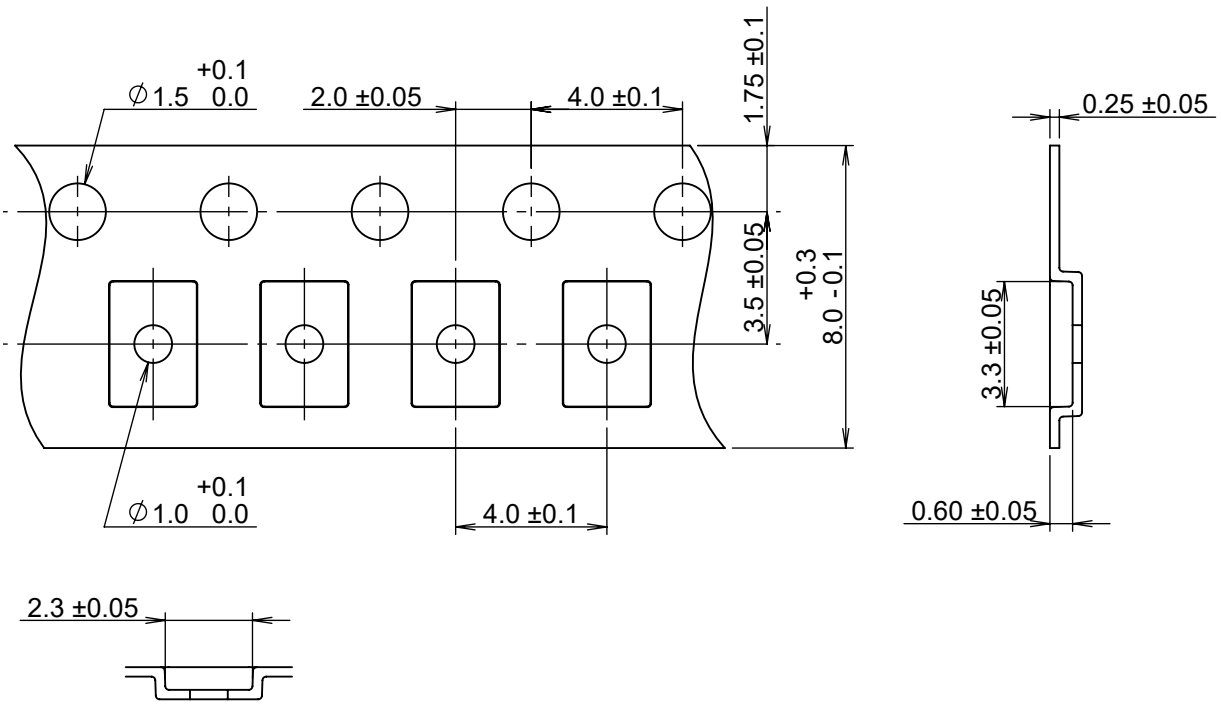
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

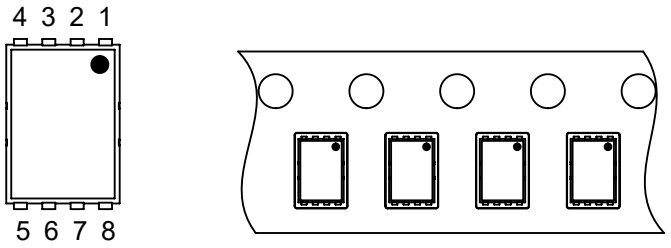
No. HSNT8-A-Board-SD-2.0



No. PP008-A-P-SD-3.0

TITLE	HSNT-8-A-PKG Dimensions
No.	PP008-A-P-SD-3.0
ANGLE	
UNIT	mm
ABLIC Inc.	

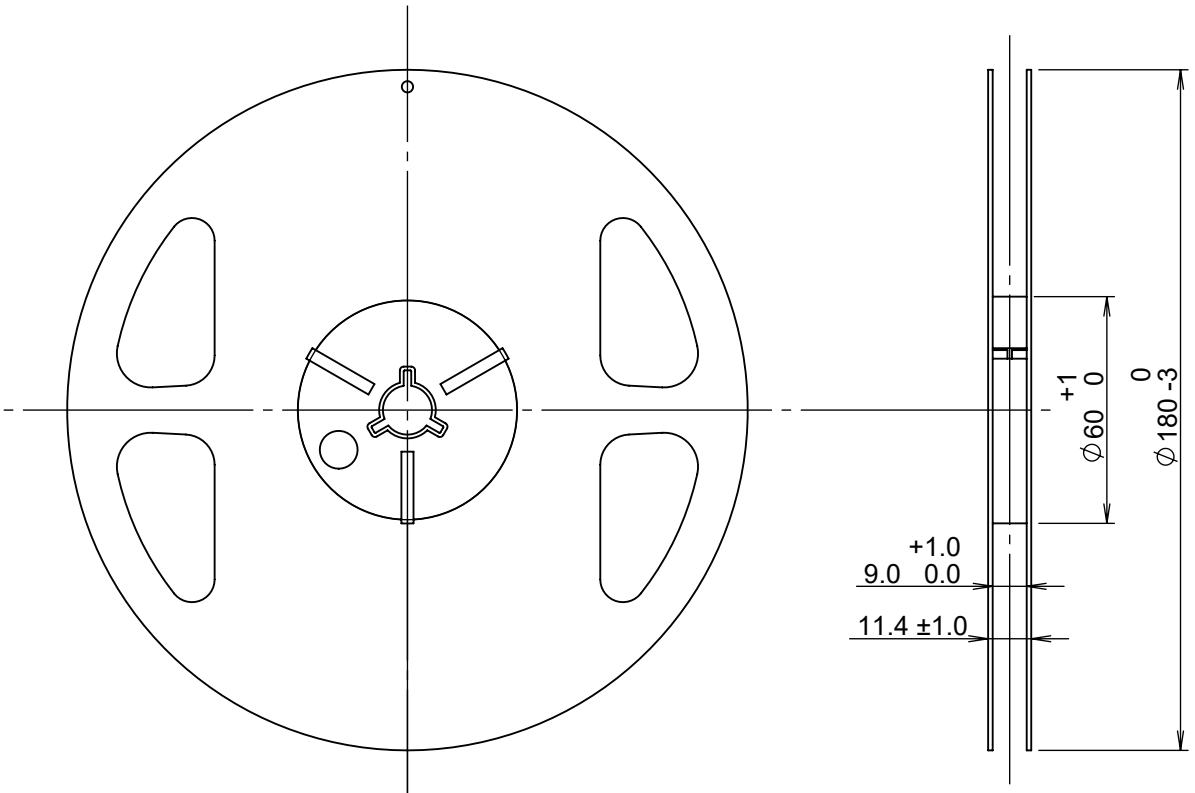




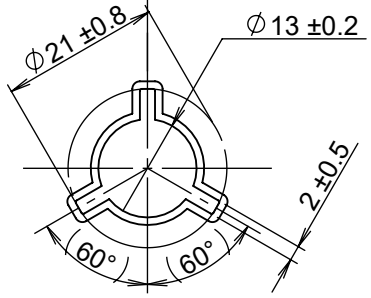
Feed direction

No. PP008-A-C-SD-1.0

TITLE	HSNT-8-A-Carrier Tape
No.	PP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

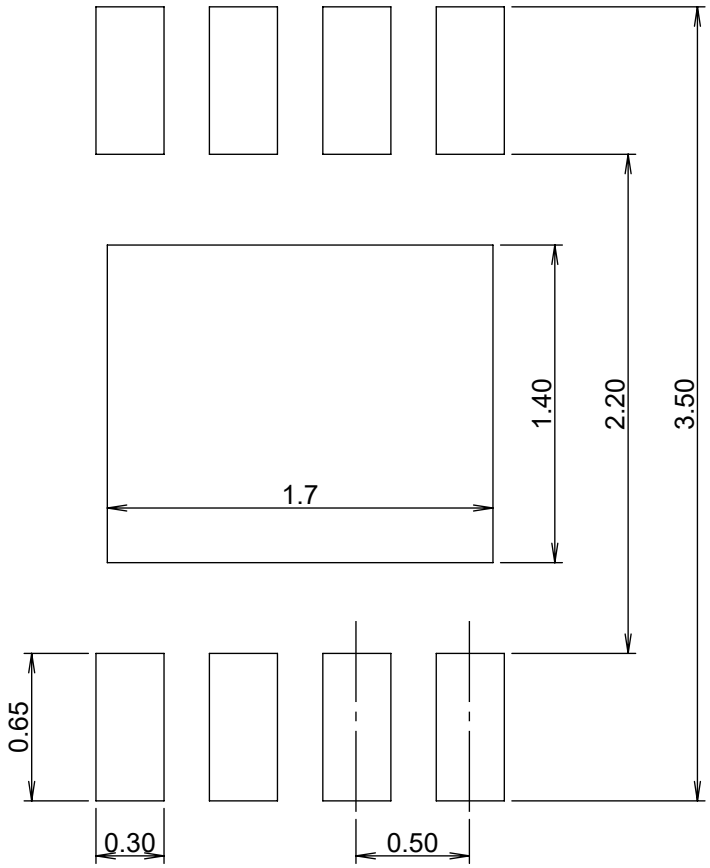


Enlarged drawing in the central part



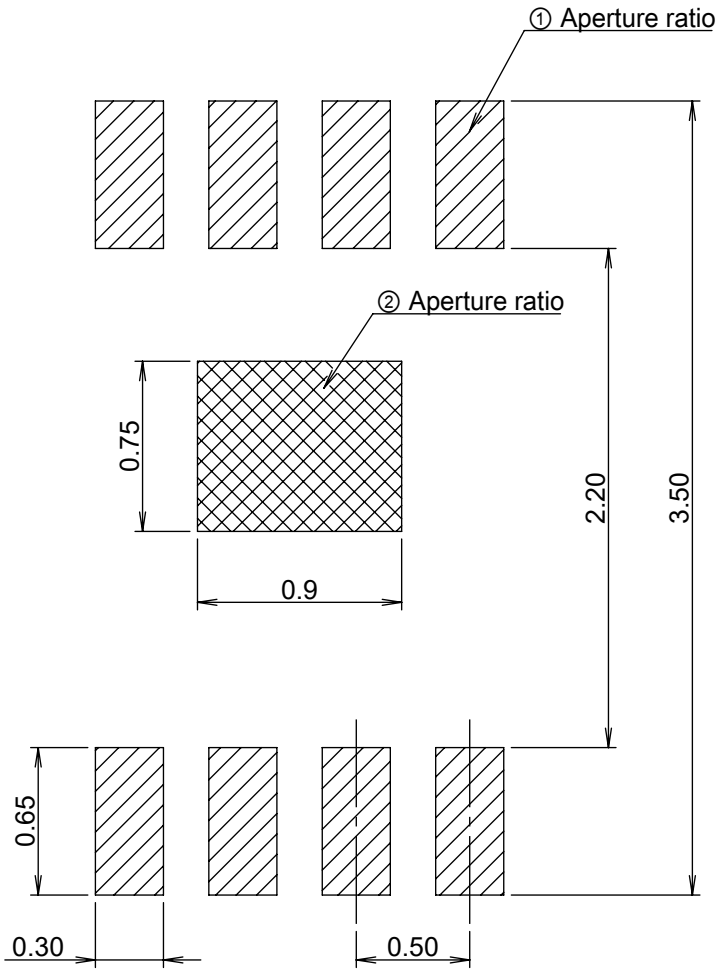
No. PP008-A-R-SD-2.0

TITLE	HSNT-8-A-Reel		
No.	PP008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



No. PP008-A-L-SD-2.0

TITLE	HSNT-8-A -Land Recommendation
No.	PP008-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is approximately 30%.
③ Mask thickness: t0.12mm
④ Reflow atmosphere: Nitrogen atmosphere is recommended.
(Oxygen concentration: 1000ppm or less)

注意 ① リード実装部のマスク開口率：100%
② 放熱板実装のマスク開口率：約30%
③ マスク厚み：t0.12mm
④ リフロー雰囲気：窒素雰囲気(酸素濃度1000ppm以下)推奨

No. PP008-A-L-S1-2.0

TITLE	HSNT-8-A-Stencil Opening
No.	PP008-A-L-S1-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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