S-93C76A H Series

FOR AUTOMOTIVE 105°C OPERATION
3-WIRE SERIAL E^{2}PROM

www.ablicinc.com

The S-93C76A H Series is a high temperature operation 3-wire serial E^{2}PROM for automotive components. The S-93C76A H Series has the capacity of 8 K-bit, and the organizztion is 512-word × 16-bit respectively. It is capable of sequential read, at which time addresses are automatically incremented in 16-bit blocks.
The communication method is by the Microwire bus.

■ Features

- Operating voltage range: Read 2.7 V to 5.5 V (Ta = −40°C to +105°C)
  Write 2.7 V to 5.5 V (Ta = −40°C to +105°C)
- Operation frequency: 1.0 MHz (V_{CC} = 4.5 V to 5.5 V, Ta = −40°C to +105°C)
- Write time: 10.0 ms max.
- Sequential read capable
- Write protect function during the low power supply voltage
- Endurance: 10^6 cycles/word*1 (Ta = +85°C)
  5×10^5 cycles/word*1 (Ta = +105°C)
- Data retention: 100 years (Ta = +25°C)
  20 years (Ta = +105°C)
- Memory capacity: 8 K-bit
- Initial delivery state: FFFFh
- Operation temperature range: Ta = −40°C to +105°C
- Lead-free (Sn 100%), halogen-free*2

***1.** For each address (Word: 16-bit)
***2.** Refer to "■ **Product Name Structure**" for details.

■ Packages

- 8-Pin SOP (JEDEC)
- 8-Pin TSSOP
- TMSOP-8

Caution **Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

■ Pin Configurations

8-Pin SOP(JEDEC)
Top view

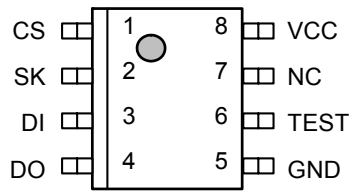


Figure 1

S-93C76ADFJ-TBH-U

Table 1

Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

8-Pin TSSOP
Top view

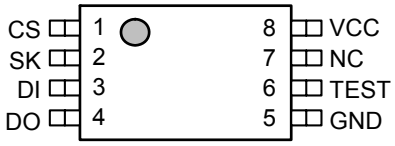


Figure 2

S-93C76AFT-TBH-U

Table 2

Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

TMSOP-8
Top view

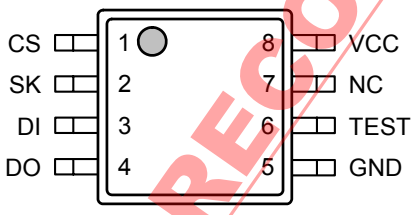


Figure 3

S-93C76AFM-TFH-U

Table 3

Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

Remark See Dimensions for details of the package drawings.

■ Block Diagram

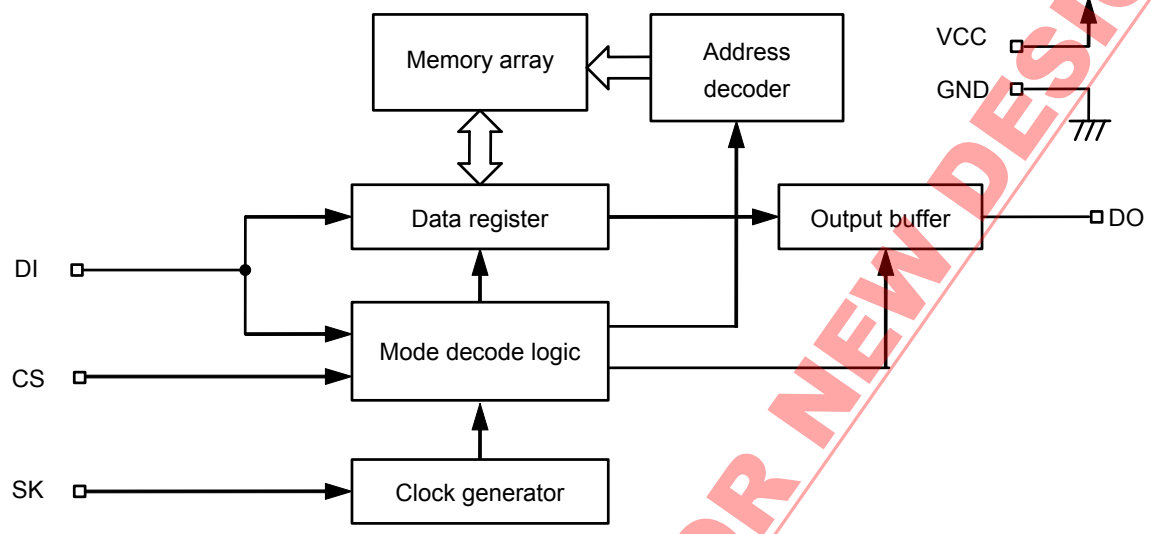


Figure 4

■ Instruction Sets

Table 4

Instruction	Start Bit	Operation Code		Address										Data
SK input clock	1	2	3	4	5	6	7	8	9	10	11	12	13	14 to 29
READ (Read data)	1	1	0	x	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Output *1
WRITE (Write data) *2	1	0	1	x	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Input
ERASE (Erase data) *2	1	1	1	x	A8	A7	A6	A5	A4	A3	A2	A1	A0	—
WRAL (Write all) *2	1	0	0	0	1	x	x	x	x	x	x	x	x	D15 to D0 Input
ERAL (Erase all) *2	1	0	0	1	0	x	x	x	x	x	x	x	x	—
EWEN (Write enable) *2	1	0	0	1	1	x	x	x	x	x	x	x	x	—
EWDS (Write disable)	1	0	0	0	0	x	x	x	x	x	x	x	x	—

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.
***2.** WRITE, ERASE, WRAL, ERAL, and EWEN are guaranteed only at $V_{CC} \geq 2.7$ V.

Remark x: Don't care

■ Absolute Maximum Ratings

Table 5

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}	V
Operating ambient temperature	T_{opr}	−40 to +105	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

■ Recommended Operating Conditions

Table 6

Item	Symbol	Conditions	−40 to +85°C		+85 to +105°C		Unit
			Min.	Max.	Min.	Max.	
Power supply voltage	V_{CC}	READ, EWDS	1.8	5.5	2.7	5.5	V
		WRITE, ERASE, EWEN	2.7	5.5	2.7	5.5	V
		WRAL, ERAL	2.7	5.5	4.5	5.5	V
High level input voltage	V_{IH}	V_{CC} = 4.5 to 5.5 V	2.0	V_{CC}	2.0	V_{CC}	V
		V_{CC} = 2.7 to 4.5 V	0.8 × V_{CC}	V_{CC}	0.8 × V_{CC}	V_{CC}	V
		V_{CC} = 1.8 to 2.7 V	0.8 × V_{CC}	V_{CC}	—	—	V
Low level input voltage	V_{IL}	V_{CC} = 4.5 to 5.5 V	0.0	0.8	0.0	0.8	V
		V_{CC} = 2.7 to 4.5 V	0.0	0.2 × V_{CC}	0.0	0.2 × V_{CC}	V
		V_{CC} = 1.8 to 2.7 V	0.0	0.15 × V_{CC}	—	—	V

■ Pin Capacitance

Table 7

(Ta = +25°C, f = 1.0 MHz, V_{CC} = 5.0 V)

Item	Symbol	Conditions	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	—	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	—	10	pF

■ Endurance

Table 8

Item	Symbol	Operating Ambient Temperature	Min.	Max.	Unit
Endurance	N_W	−40 to +85°C	10^6	—	cycles/word*1
		+85 to +105°C	5×10^5	—	cycles/word*1

***1.** For each address (Word: 16 bits)

■ Data Retention

Table 9

Item	Symbol	Operating Ambient Temperature	Min.	Max.	Unit
Data Retention	—	+25°C	100	—	year
		−40 to +105°C	20	—	year

■ DC Electrical Characteristics

Table 10 (1/2)

Item	Symbol	Conditions	−40 to +85°C						Unit
			V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.5 to 4.5 V		V_{CC} = 1.8 to 2.5 V		
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	DO no load	—	0.8	—	0.5	—	0.4	mA

Table 10 (2/2)

Item	Symbol	Conditions	+85 to +105°C				Unit
			V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.7 to 4.5 V		
			Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	DO no load	—	0.8	—	0.5	mA

Table 11 (1/2)

Item	Symbol	Conditions	−40 to +85°C				Unit
			V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.7 to 4.5 V		
			Min.	Max.	Min.	Max.	
Current consumption (WRITE)	I_{CC2}	DO no load	—	2.0	—	1.5	mA

Table 11 (2/2)

Item	Symbol	Conditions	+85 to +105°C		Unit
			V_{CC} = 2.7 to 5.5 V		
			Min.	Max.	
Current consumption (WRITE)	I_{CC2}	DO no load	—	2.0	mA

Table 12 (1/2)

Item	Symbol	Conditions	−40 to +85°C						Unit
			V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.5 to 4.5 V		V_{CC} = 1.8 to 2.5 V		
			Min.	Max.	Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	CS = GND, DO = Open, Other inputs to V_{CC} or GND	—	2.0	—	2.0	—	2.0	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	1.0	—	1.0	—	1.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	1.0	—	1.0	—	1.0	μA
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	—	0.4	—	—	—	—	V
		I_{OL} = 100 μA	—	0.1	—	0.1	—	0.1	V
High level output voltage	V_{OH}	I_{OH} = −400 μA	2.4	—	—	—	—	—	V
		I_{OH} = −100 μA	V_{CC}− 0.3	—	V_{CC}− 0.3	—	—	—	V
		I_{OH} = −10 μA	V_{CC}− 0.2	—	V_{CC}− 0.2	—	V_{CC}− 0.2	—	V
Data hold voltage of write enable latch	V_{DH}	Only program disable mode	1.5	—	1.5	—	1.5	—	V

Table 12 (2/2)

Item	Symbol	Conditions	+85 to +105°C				Unit
			V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.7 to 4.5 V		
			Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	CS = GND, DO = Open, Other inputs to V_{CC} or GND	—	2.0	—	2.0	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	1.0	—	1.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	1.0	—	1.0	μA
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	—	0.4	—	—	V
		I_{OL} = 100 μA	—	0.1	—	0.1	V
High level output voltage	V_{OH}	I_{OH} = −400 μA	2.4	—	—	—	V
		I_{OH} = −100 μA	V_{CC}− 0.3	—	V_{CC}− 0.3	—	V
		I_{OH} = −10 μA	V_{CC}− 0.2	—	V_{CC}− 0.2	—	V
Data hold voltage of write enable latch	V_{DH}	Only program disable mode	1.5	—	1.5	—	V

■ AC Electrical Characteristics

Table 13 Measurement Conditions

Input pulse voltage	0.1 × V_{CC} to 0.9 × V_{CC}
Output reference voltage	0.5 × V_{CC}
Output load	100 pF

Table 14 (1/2)

Item	Symbol	−40 to +85°C						Unit
		V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.5 to 4.5 V		V_{CC} = 1.8 to 2.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
CS setup time	t_{CSS}	0.2	—	0.4	—	1.0	—	µs
CS hold time	t_{CSH}	0	—	0	—	0	—	µs
CS deselect time	t_{CDS}	0.2	—	0.2	—	0.4	—	µs
Data setup time	t_{DS}	0.1	—	0.2	—	0.4	—	µs
Data hold time	t_{DH}	0.1	—	0.2	—	0.4	—	µs
Output delay time	t_{PD}	—	0.4	—	0.8	—	2.0	µs
Clock frequency*1	f_{SK}	0	2.0	0	0.5	0	0.25	MHz
SK clock time "L" *1	t_{SKL}	0.1	—	0.5	—	1.0	—	µs
SK clock time "H" *1	t_{SKH}	0.1	—	0.5	—	1.0	—	µs
Output disable time	t_{HZ1}, t_{HZ2}	0	0.15	0	0.5	0	1.0	µs
Output enable time	t_{SV}	0	0.15	0	0.5	0	1.0	µs

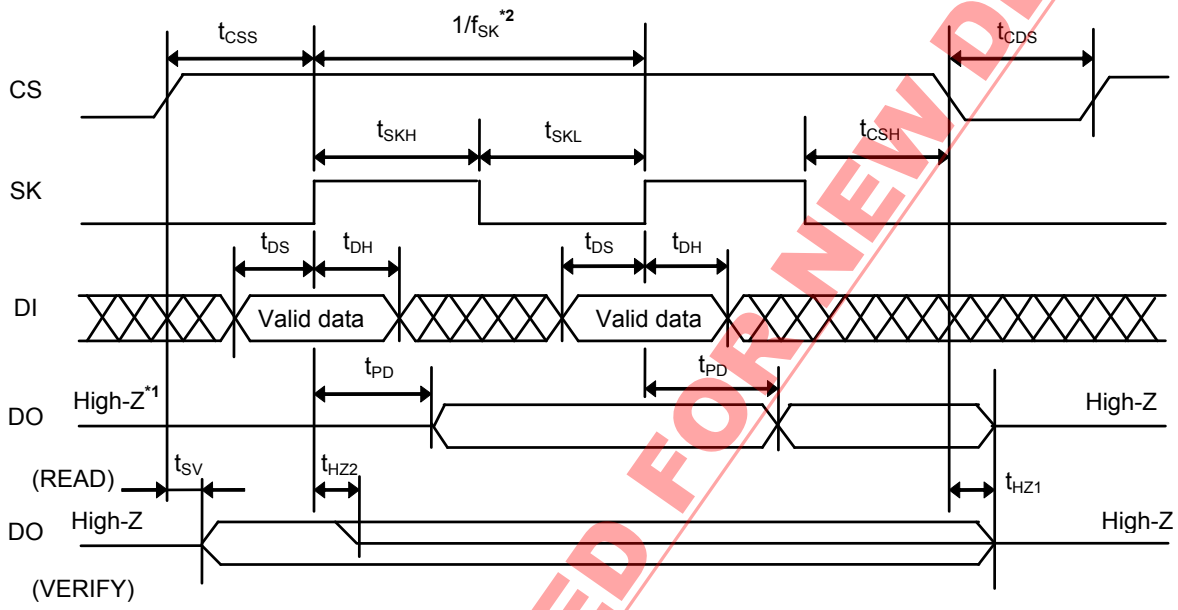
Table 14 (2/2)

Item	Symbol	+85 to +105°C				Unit
		V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.7 to 4.5 V		
		Min.	Max.	Min.	Max.	
CS setup time	t_{CSS}	0.2	—	0.4	—	µs
CS hold time	t_{CSH}	0	—	0	—	µs
CS deselect time	t_{CDS}	0.2	—	0.2	—	µs
Data setup time	t_{DS}	0.1	—	0.2	—	µs
Data hold time	t_{DH}	0.1	—	0.2	—	µs
Output delay time	t_{PD}	—	0.6	—	0.8	µs
Clock frequency*1	f_{SK}	0	1.0	0	0.5	MHz
SK clock time "L" *1	t_{SKL}	0.25	—	0.5	—	µs
SK clock time "H" *1	t_{SKH}	0.25	—	0.5	—	µs
Output disable time	t_{HZ1}, t_{HZ2}	0	0.15	0	0.5	µs
Output enable time	t_{SV}	0	0.15	0	0.5	µs

***1.** The clock cycle of the SK clock (frequency: f_{SK}) is $1/f_{SK}$ µs. This clock cycle is determined by a combination of several AC characteristics, so be aware that even if the SK clock cycle time is minimized, the clock cycle ($1/f_{SK}$) cannot be made equal to t_{SKL}(Min.) + t_{SKH}(Min.).

Table 15

Item	Symbol	−40 to +85°C			+85 to +105°C			Unit
		V_{CC} = 2.7 to 5.5 V			V_{CC} = 2.7 to 5.5 V			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Write time	t_{PR}	—	4.0	10.0	—	4.0	10.0	ms



***1.** Indicates high impedance.

***2.** $1/f_{SK}$ is the SK clock cycle. This clock cycle is determined by a combination of several AC characteristics, so be aware that even if the SK clock cycle time is minimized, the clock cycle ($1/f_{SK}$) cannot be made equal to t_{SKL}(Min.) + t_{SKH}(Min.).

Figure 5 Timing Chart

■ Initial Delivery State

Initial delivery state of all addresses is "FFFFh".

■ Operation

All instructions are executed by making CS "H" and then inputting DI at the rising edge of the SK pulse. An instruction is input in the order of its start bit, instruction, address, and data. The start bit is recognized when "H" of DI is input at the rising edge of SK after CS has been made "H". As long as DI remains "L", therefore, the start bit is not recognized even if the SK pulse is input after CS has been made "H". The SK clock input while DI is "L" before the start bit is input is called a dummy clock. By inserting as many dummy clocks as required before the start bit, the number of clocks the internal serial interface of the CPU can send out and the number of clocks necessary for operation of the serial memory IC can be adjusted. Inputting the instruction is complete when CS is made "L". CS must be made "L" once during the period of t_{CDS} in between instructions.
"L" of CS indicates a standby status. In this status, input of SK and DI is invalid, and no instruction is accepted.

1. Reading (READ)

The READ instruction is used to read the data at a specified address. When this instruction is executed, the address A_0 is input at the rising edge of SK and the DO pin, which has been in a high-impedance (High-Z) state, outputs "L". Subsequently, 16 bits of data are sequentially output at the rising edge of SK.
If SK is output after the 16-bit data of the specified address has been output, the address is automatically incremented, and the 16-bit data of the next address is then output. By inputting SK sequentially with CS kept at "H", the data of the entire memory space can be read. When the address is incremented from the last address (A_8 … A_1 A_0 = 1 … 1 1), it returns to the first address (A_8 … A_1 A_0 = 0 … 0 0).

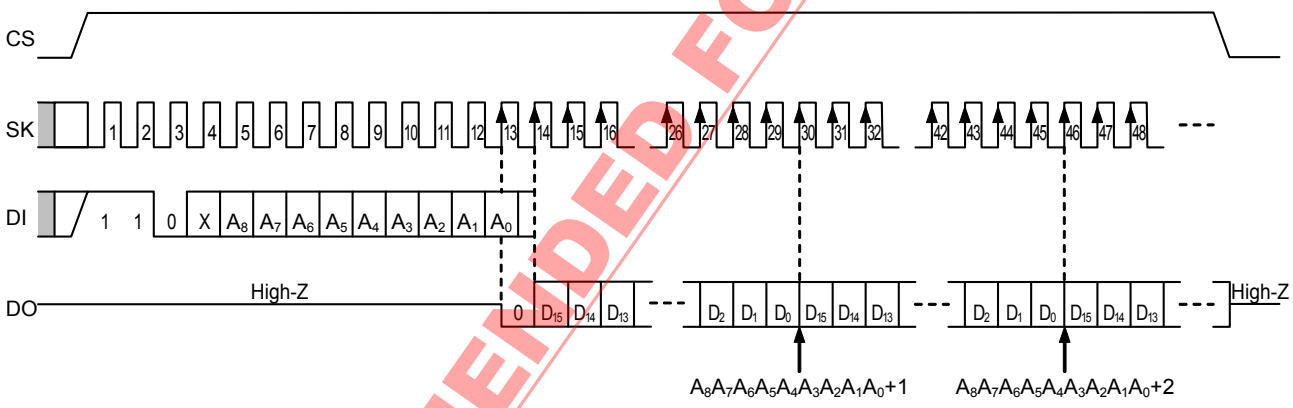


Figure 6 Read Timing

2. Writing (WRITE, ERASE, WRAL, ERAL)

Write instructions (WRITE, ERASE, WRAL, and ERAL) are used to start writing data to the non-volatile memory by making CS "L" after the specified number of clocks has been input.

The write operation is completed within the write time t_{PR} (10 ms) no matter which write instruction is used. The typical write time is less than half 10 ms. If the end of the write operation is known, therefore, the write cycle can be minimized. To ascertain the end of a write operation, make CS "L" to start the write operation and then make CS "H" again to check the status of the DO output pin. This series of operations is called a verify operation.

If DO outputs "L" during the verify operation period in which CS is "H", it indicates that a write operation is in progress. If DO outputs "H", it indicates that the write operation is finished. The verify operation can be executed as many times as required. This operation can be executed in two ways. One is detecting the positive transition of DO output from "L" to "H" while holding CS at "H". The other is detecting the positive transition of DO output from "L" to "H" by making CS "H" once and checking DO output, and then returning CS to "L".

During the write period, SK and DI are invalid. Do not input any instructions during this period. Input an instruction while the DO pin is outputting "H" or is in a high-impedance state. Even while the DO pin is outputing "H", DO immediately goes into a high-impedance (High-Z) state if "H" of DI (start bit) is input at the rising edge of SK.

Keep DI "L" during the verify operation period.

2. 1 Writing data (WRITE)

This instruction is used to write 16-bit data to a specified address.

After making CS "H", input a start bit, the WRITE instruction, an address, and 16-bit data. If data of more than 16 bits is input, the written data is sequentially shifted at each clock, and the 16 bits input last are the valid data. The write operation is started when CS is made "L". It is not necessary to set data to "1" before it is written.

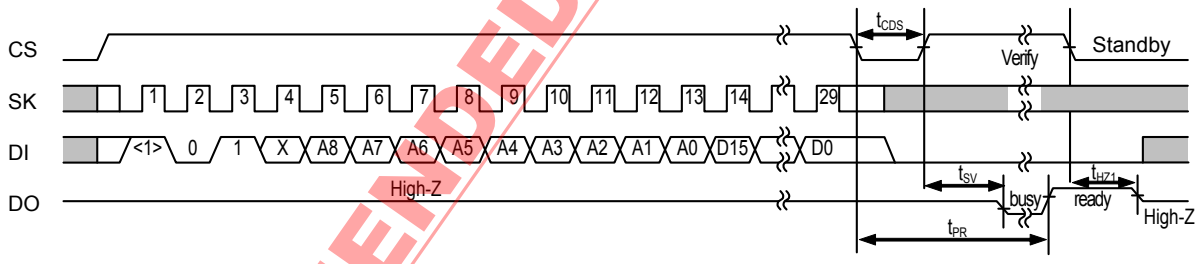


Figure 7 Data Write Timing

2. 2 Erasing data (ERASE)

This instruction is used to erase specified 16-bit data. All the 16 bits of the data are "1". After making CS "H", input a start bit, the ERASE instruction, and an address. It is not necessary to input data. The data erase operation is started when CS is made "L".

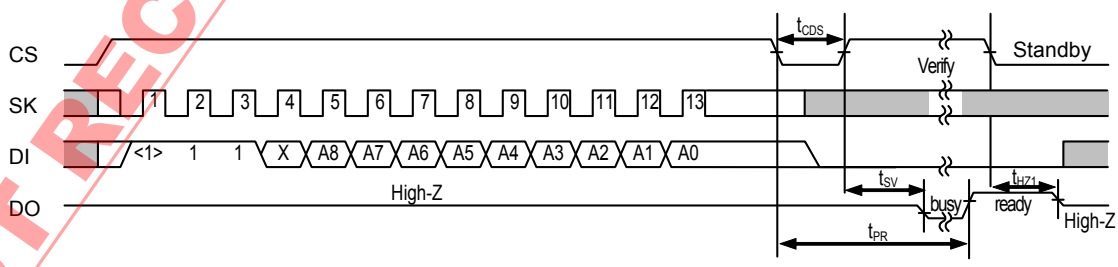


Figure 8 Data Erase Timing

2. 3 Writing to chip (WRAL)

This instruction is used to write the same 16-bit data to the entire address space of the memory.
After making CS "H", input a start bit, the WRAL instruction, an address, and 16-bit data. Any address may be input. If data of more than 16 bits is input, the written data is sequentially shifted at each clock, and the 16-bit data input last is the valid data. The write operation is started when CS is made "L". It is not necessary to set the data to "1" before it is written.

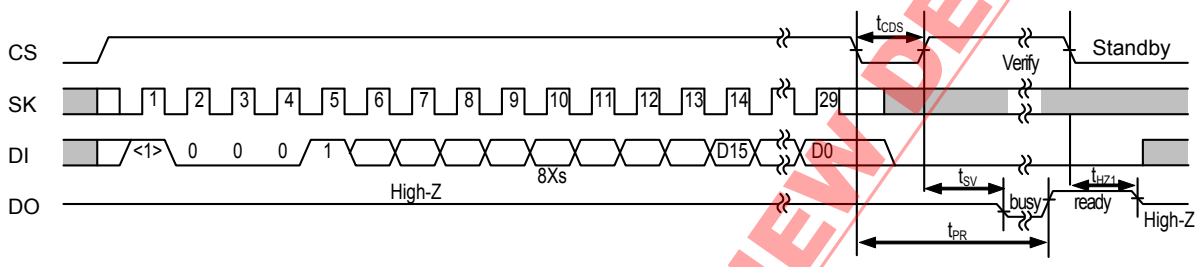


Figure 9 Chip Write Timing

2. 4 Erasing chip (ERAL)

This instruction is used to erase the data of the entire address space of the memory.
All the data is "1". After making CS "H", input a start bit, the ERAL instruction, and an address. Any address may be input. It is not necessary to input data. The chip erase operation is started when CS is made "L".

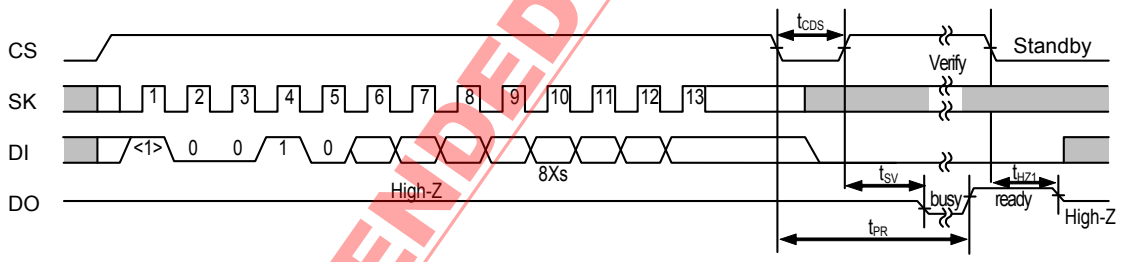


Figure 10 Chip Erase Timing

3. Write enable (EWEN) and write disable (EWDS)

The EWEN instruction is used to enable a write operation. The status in which a write operation is enabled is called the program-enabled mode.
The EWDS instruction is used to disable a write operation. The status in which a write operation is disabled is called the program-disabled mode.
The write operation is disabled upon power application and detection of a low supply voltage. To prevent an unexpected write operation due to external noise or a CPU malfunctions, it should be kept in write disable mode except when performing write operations, after power-on and before shutdown.

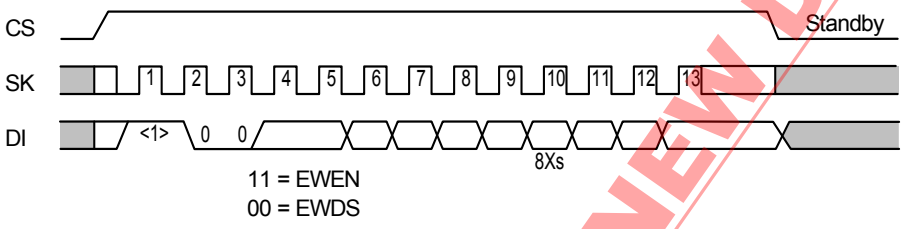


Figure 11 Write Enable/Disable Timing

■ Start Bit

A start bit is recognized by latching the high level of DI at the rising edge of SK after changing CS to high (start bit recognition). A write operation begins by inputting the write instruction and setting CS to low. Subsequently, by setting CS to high again, the DO pin outputs a low level if the write operation is still in progress and a high level if the write operation is complete (verify operation). Therefore, only after a write operation, in order to input the next command, CS is set to high, which switches the DO pin from a high-impedance state (High-Z) to a data output state. However, if start bit is recognized, the DO pin returns to the high-impedance state (refer to **Figure 5 Timing Chart**).
Make sure that data output from the CPU does not interfere with the data output from the serial memory IC when configuring a 3 -wire interface by connecting the DI input pin and DO output pin, as such interference may cause a start bit fetch problem. Take the measures described in "**■ 3-Wire Interface (Direct Connection between DI and DO)**".

■ Write Protect Function during the Low Power Supply Voltage

The S-93C76A provides a built-in detector to detect a low power supply voltage and disable writing. When the power supply voltage is low or at power application, the write instructions (WRITE, ERASE, WRAL, and ERAL) are cancelled, and the write disable state (EWDS) is automatically set. The detection voltage is 1.75 V typ., the release voltage is 2.05 V typ., and there is a hysteresis of about 0.3 V (refer to **Figure 12**). Therefore, when a write operation is performed after the power supply voltage has dropped and then risen again up to the level at which writing is possible, a write enable instruction (EWEN) must be sent before a write instruction (WRITE, ERASE, WRAL, or ERAL) is executed.
When the power supply voltage drops during a write operation, the data being written to an address at that time is not guaranteed.

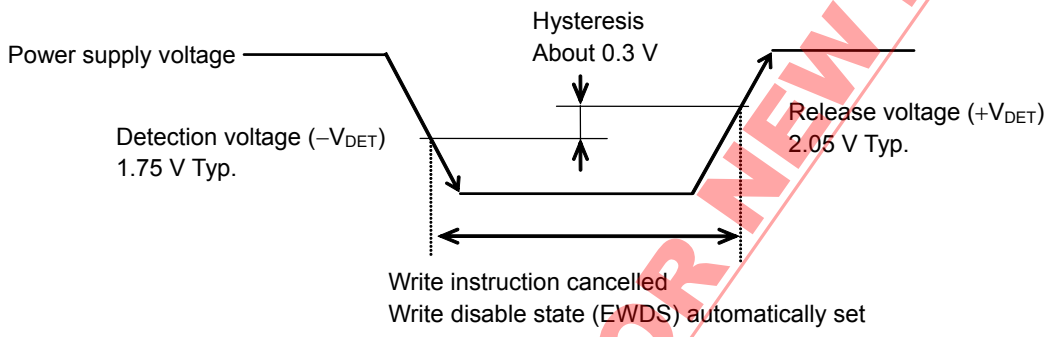


Figure 12 Operation during Low Power Supply Voltage

■ 3-Wire Interface (Direct Connection between DI and DO)

There are two types of serial interface configurations: a 4-wire interface configured using the CS, SK, DI, and DO pins, and a 3-wire interface that connects the DI input pin and DO output pin.
When the 3-wire interface is employed, a period in which the data output from the CPU and the data output from the serial memory collide may occur, causing a malfunction. To prevent such a malfunction, connect the DI and DO pins of the S-93C76A via a resistor (10 kΩ to 100 kΩ) so that the data output from the CPU takes precedence in being input to the DI pin (refer to **Figure 13**).

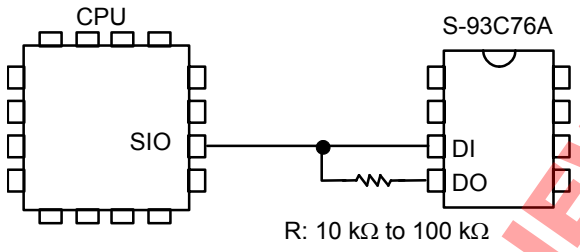


Figure 13 Connection of 3-Wire Interface

■ I/O Pin

1. Connection of input pins

All the input pins of the S-93C76A employ a CMOS structure, so design the equipment so that high impedance will not be input while the S-93C76A is operating. Especially, deselect the CS input (a low level) when turning on/off power and during standby. When the CS pin is deselected (a low level), incorrect data writing will not occur. Connect the CS pin to GND via a resistor (10 kΩ to 100 kΩ pull-down resistor). To prevent malfunction, it is recommended to use equivalent pull-down resistors for pins other than the CS pin.

2. Equivalent circuit of input and output pin

The following shows the equivalent circuits of input pins of the S-93C76A. None of the input pins incorporate pull-up and pull-down elements, so special care must be taken when designing to prevent a floating status.
Output pins are high-level/low-level/high-impedance tri-state outputs. The TEST pin is disconnected from the internal circuit by a switching transistor during normal operation. As long as the absolute maximum rating is satisfied, the TEST pin and internal circuit will never be connected.

2. 1 Input pin

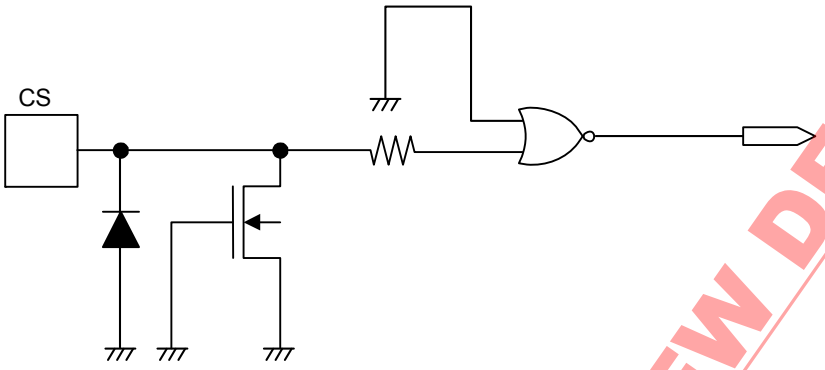


Figure 14 CS Pin

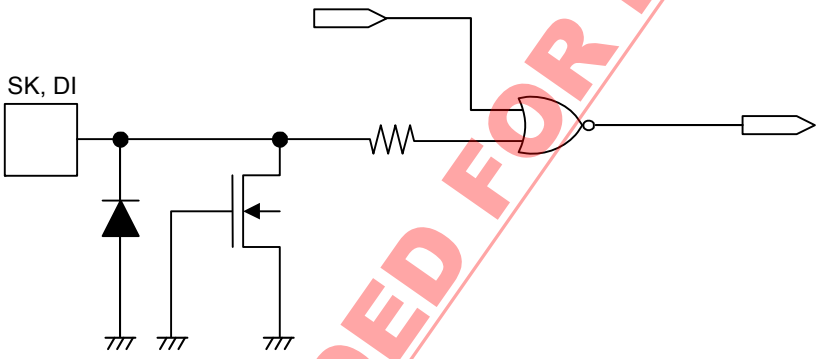


Figure 15 SK DI Pin

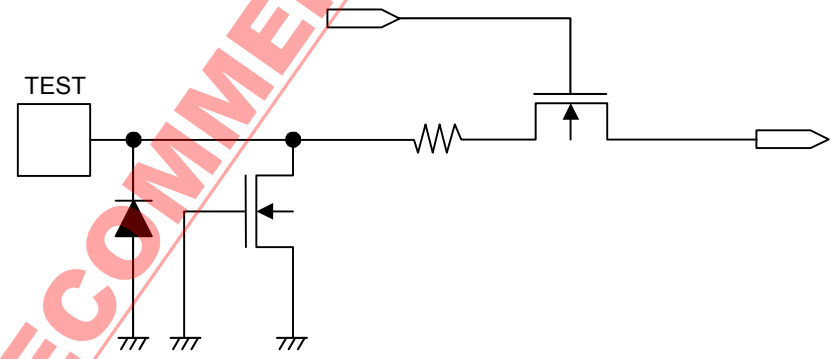


Figure 16 TEST Pin

2. 2 Output pin

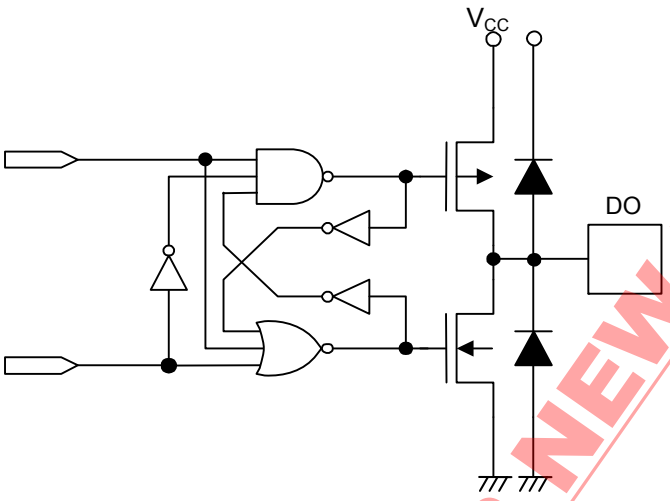


Figure 17 DO Pin

3. Input pin noise elimination time

The S-93C76A includes a built-in low-pass filter to eliminate noise at the SK, DI, and CS pins. This means that if the supply voltage is 5.0 V (at room temperature), noise with a pulse width of 20 ns or less can be eliminated.
Note, therefore, that noise with a pulse width of more than 20 ns will be recognized as a pulse if the voltage exceeds V_{IH}/V_{IL}.

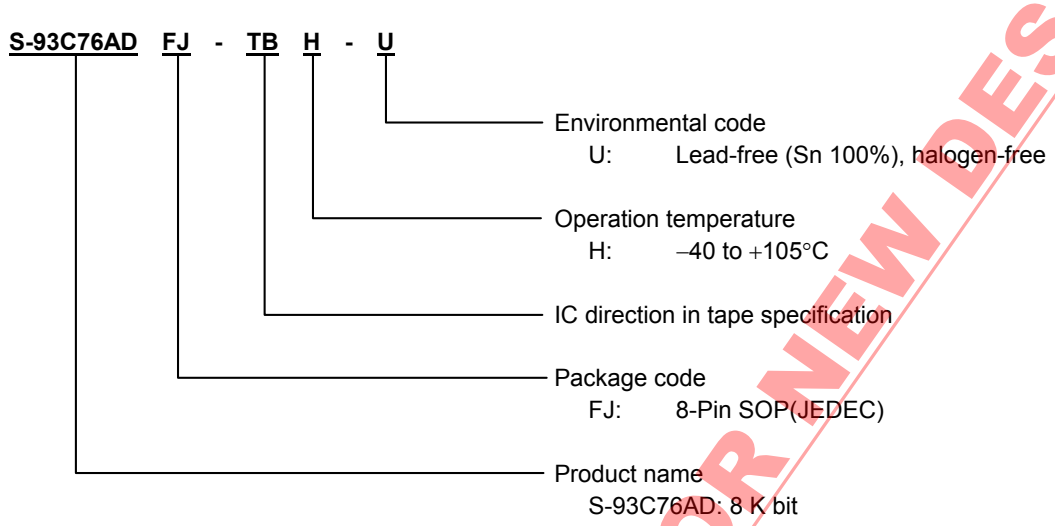
■ Precaution

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

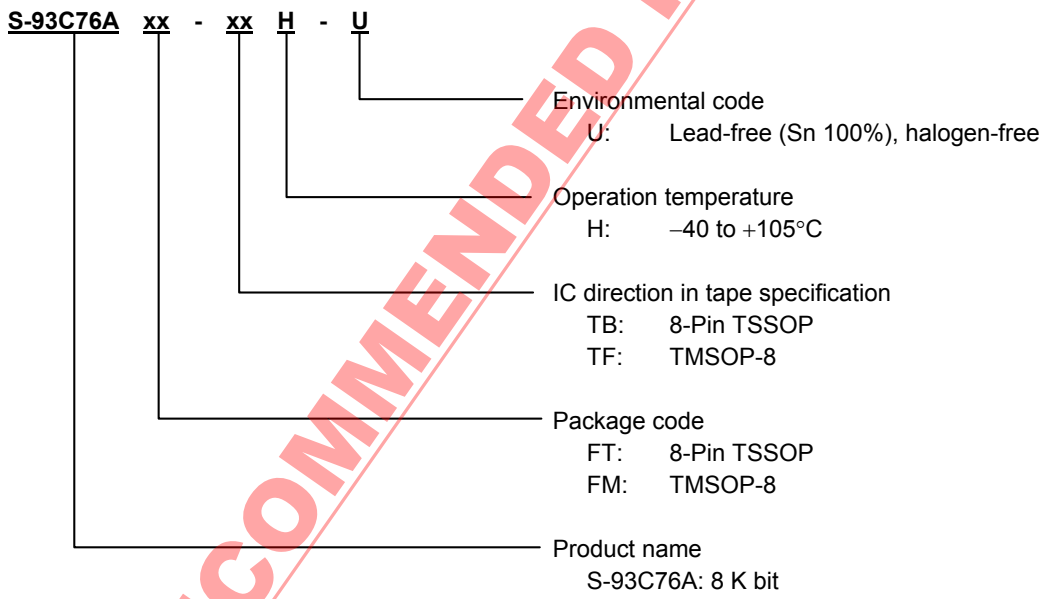
■ Product Name Structure

1. Product name

(1) 8-Pin SOP (JEDEC)



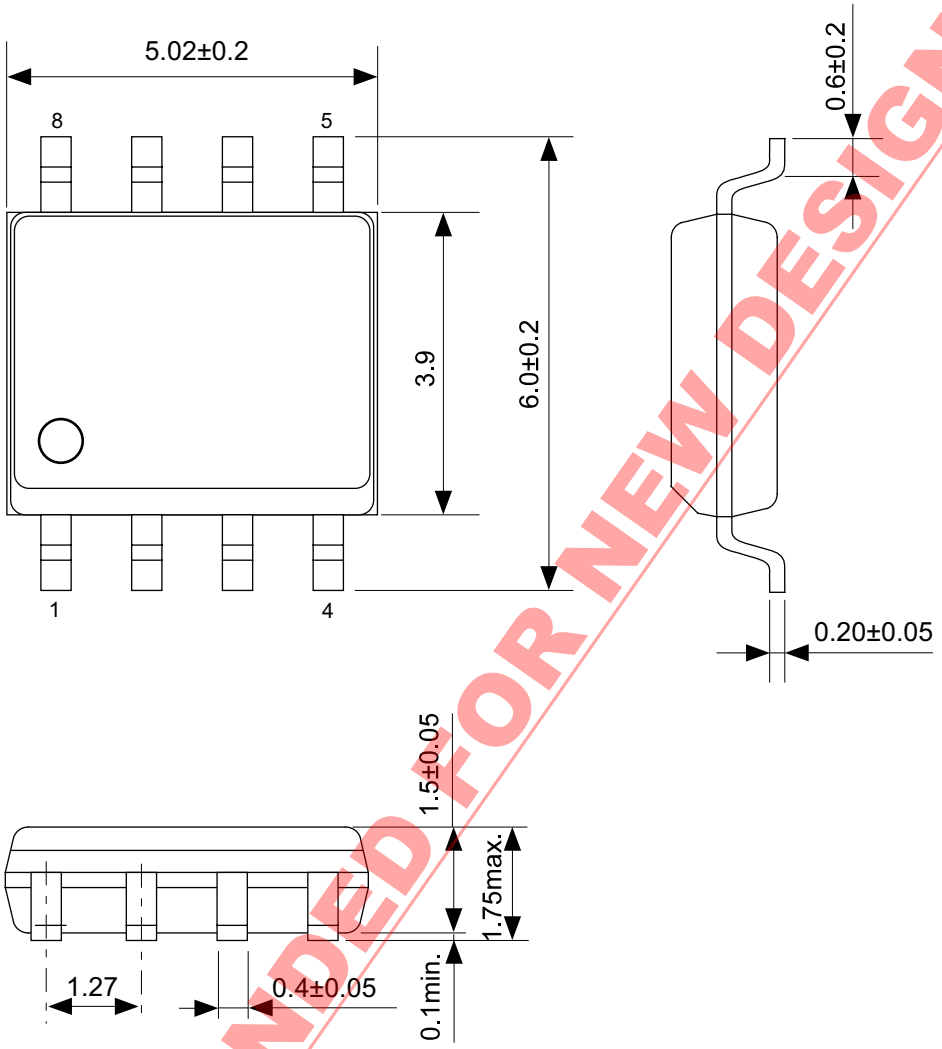
(2) 8-Pin TSSOP, TMSOP-8



Remark Please contact our sales office for products with product name structure other than those specified above.

2. Package

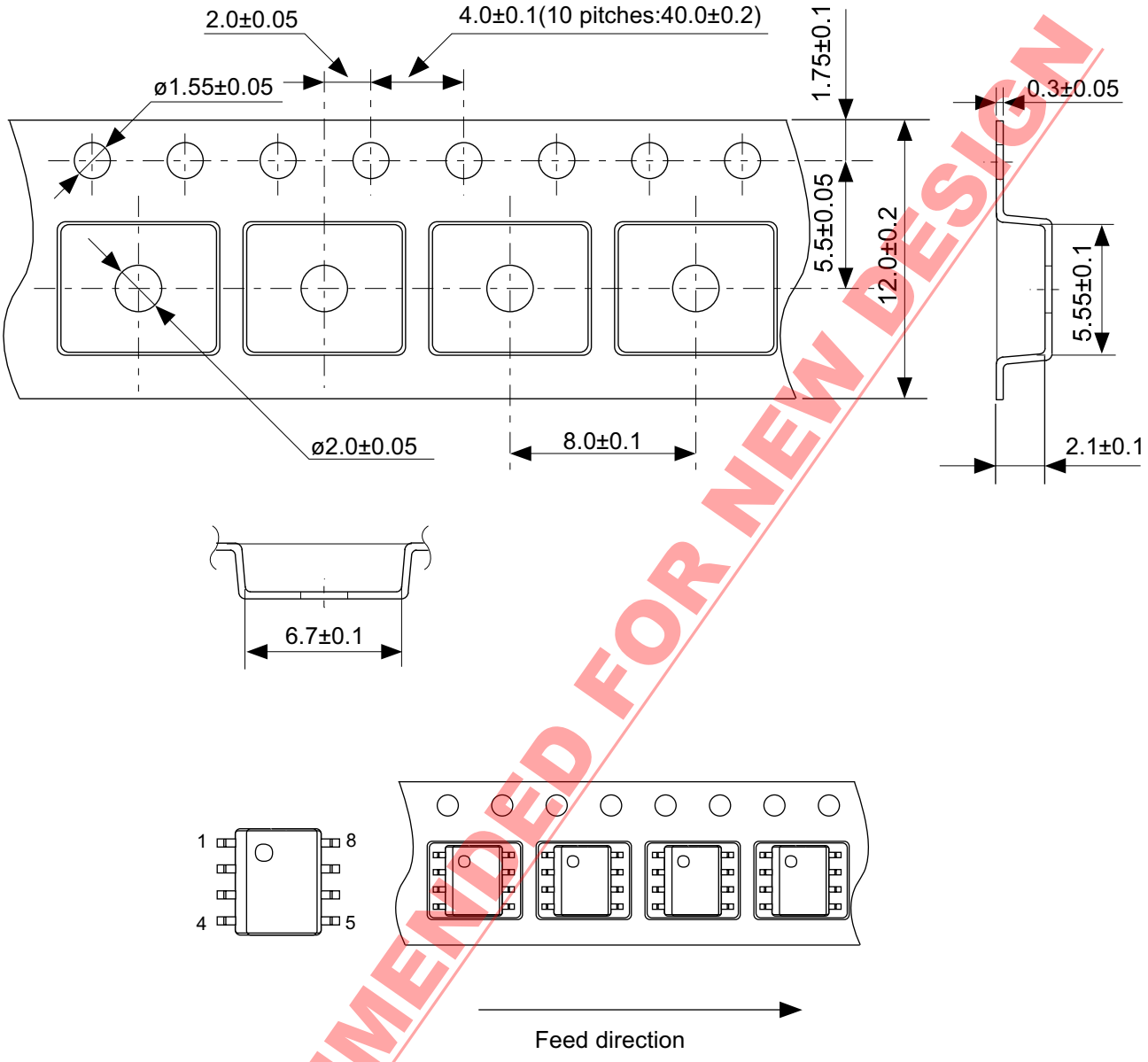
Package name	Drawing code		
	Package	Tape	Reel
8-Pin SOP (JEDEC)	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-SD
8-Pin TSSOP	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD



No. FJ008-A-P-SD-2.2

TITLE	SOP8J-D-PKG Dimensions
No.	FJ008-A-P-SD-2.2
ANGLE	
UNIT	mm

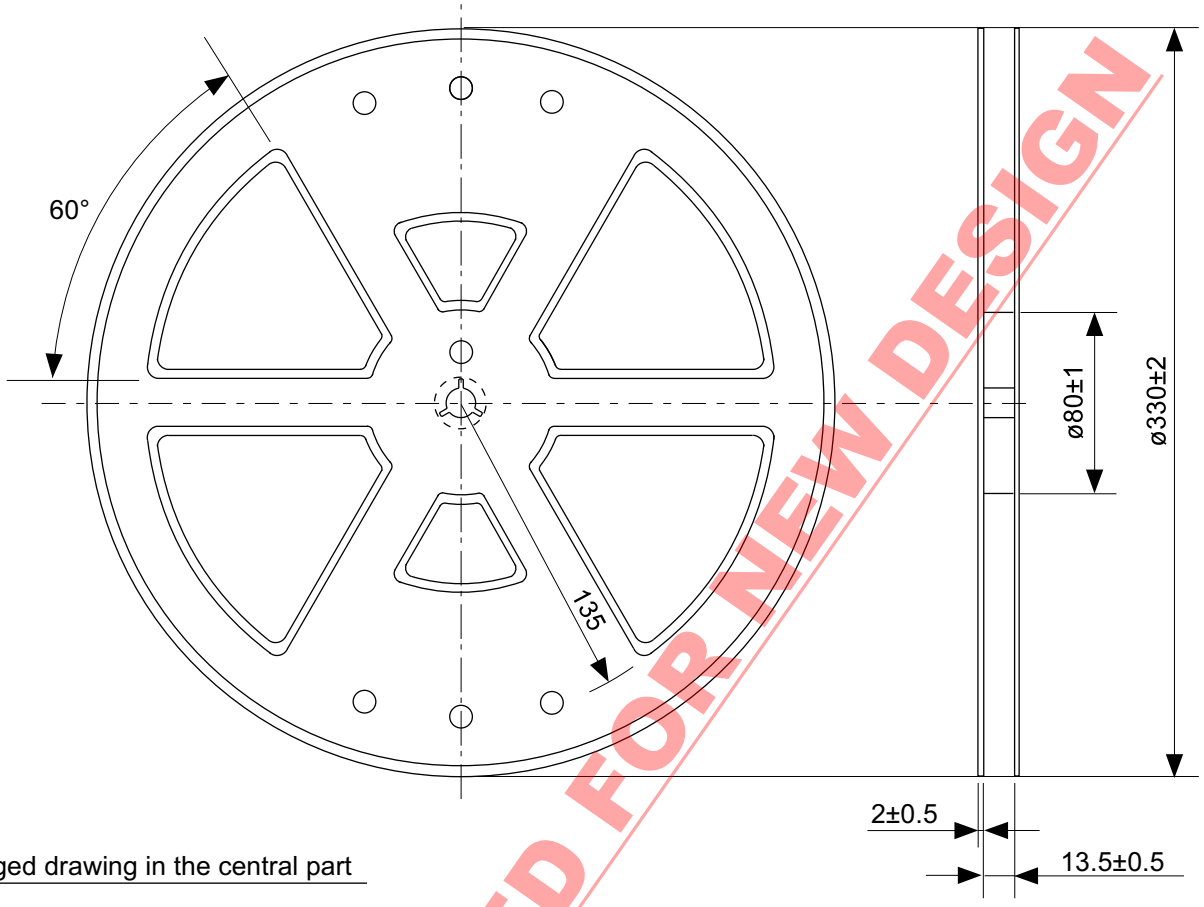
ABLIC Inc.



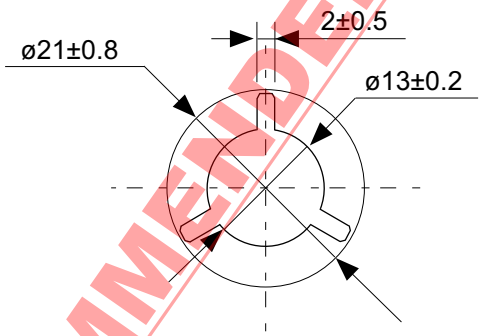
No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
ANGLE	
UNIT	mm

ABLIC Inc.



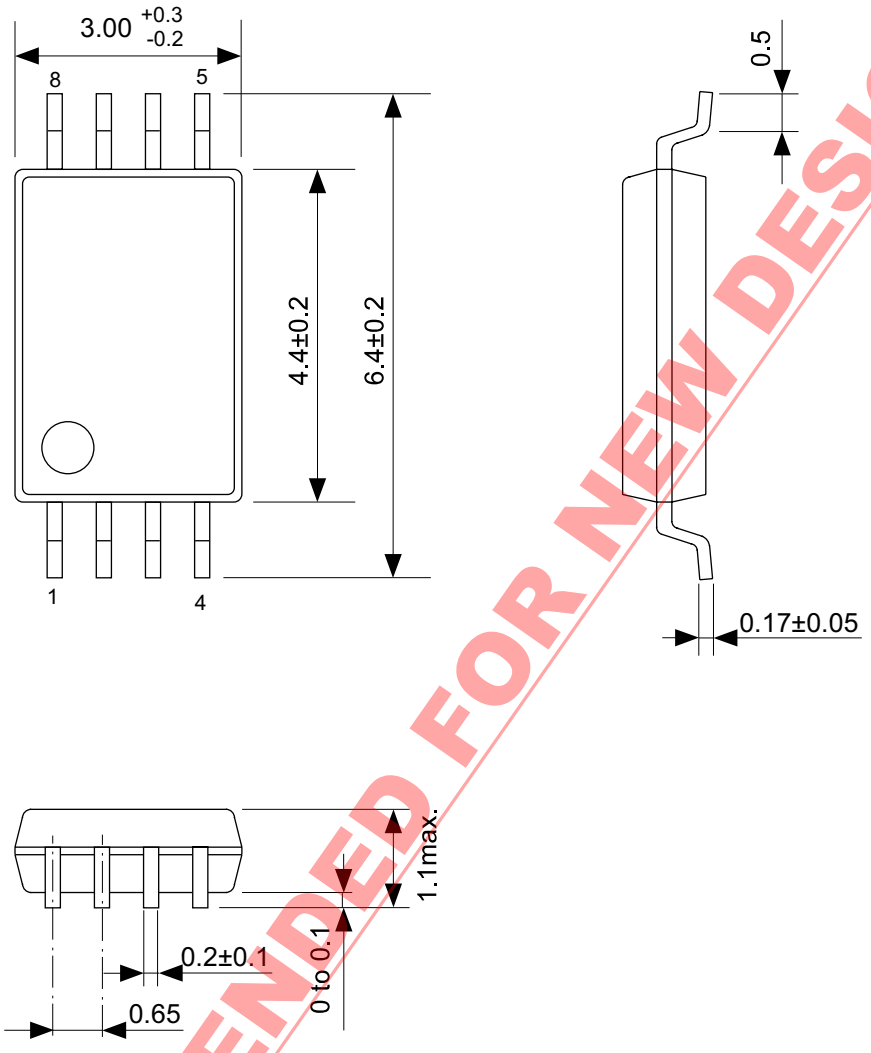
Enlarged drawing in the central part



No. FJ008-D-R-SD-1.1

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-SD-1.1		
ANGLE		QTY.	2,000
UNIT	mm		

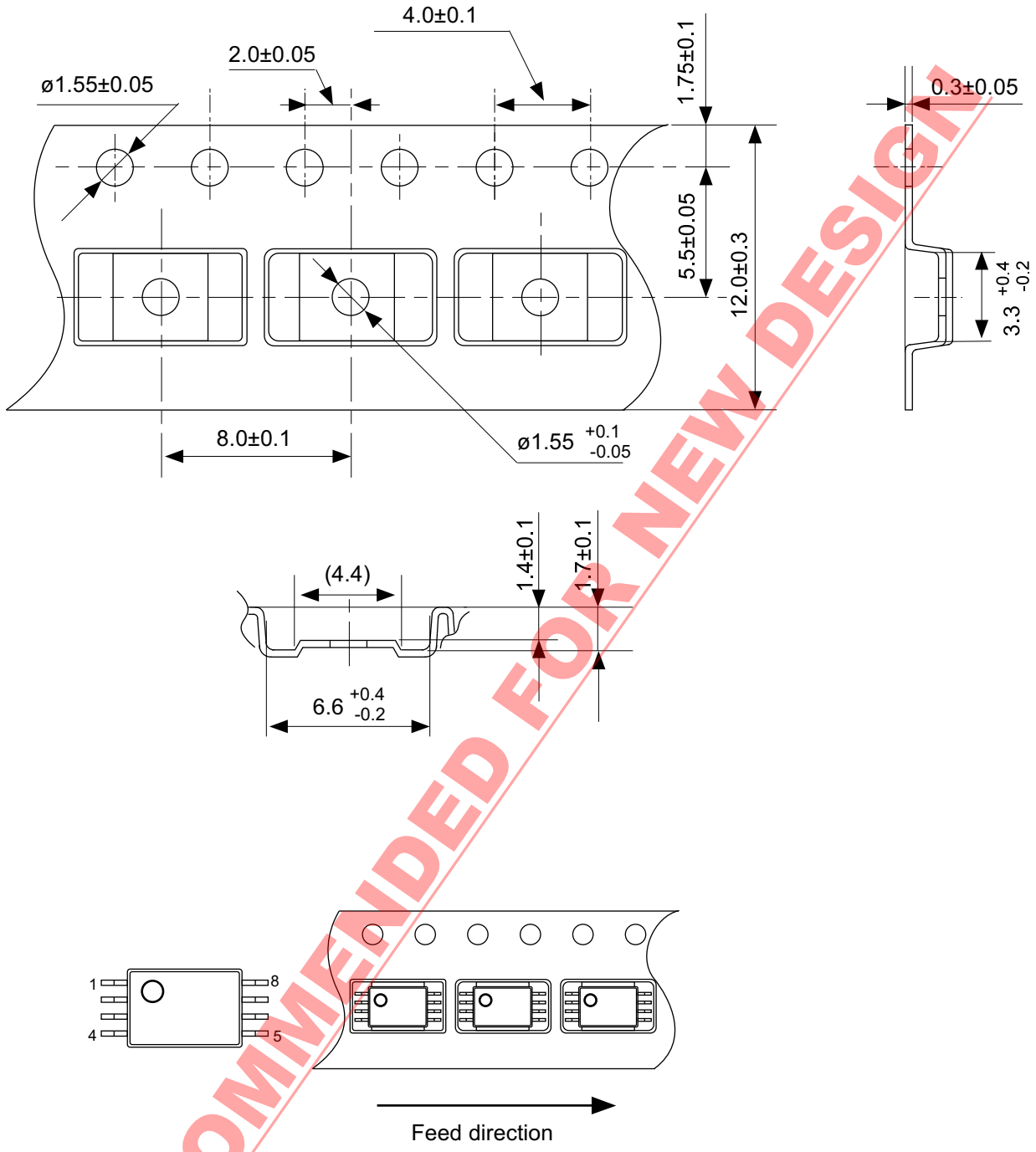
ABLIC Inc.



No. FT008-A-P-SD-1.2

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.2
ANGLE	
UNIT	mm

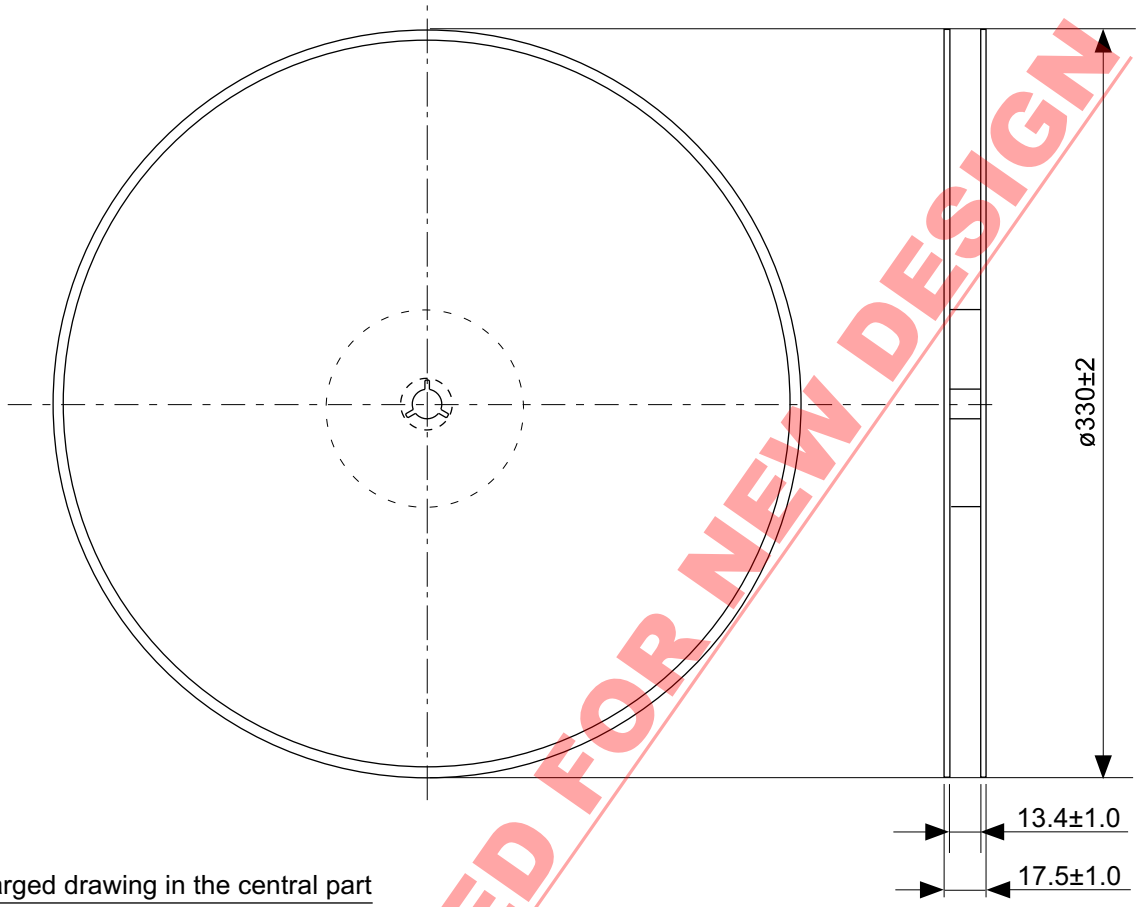
ABLIC Inc.



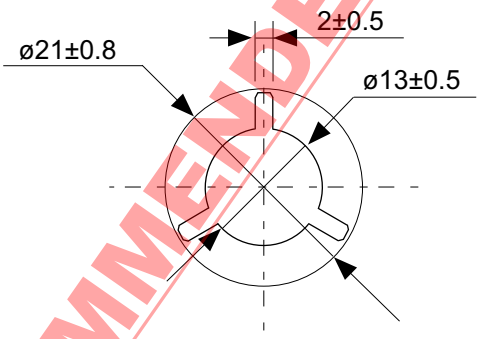
No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



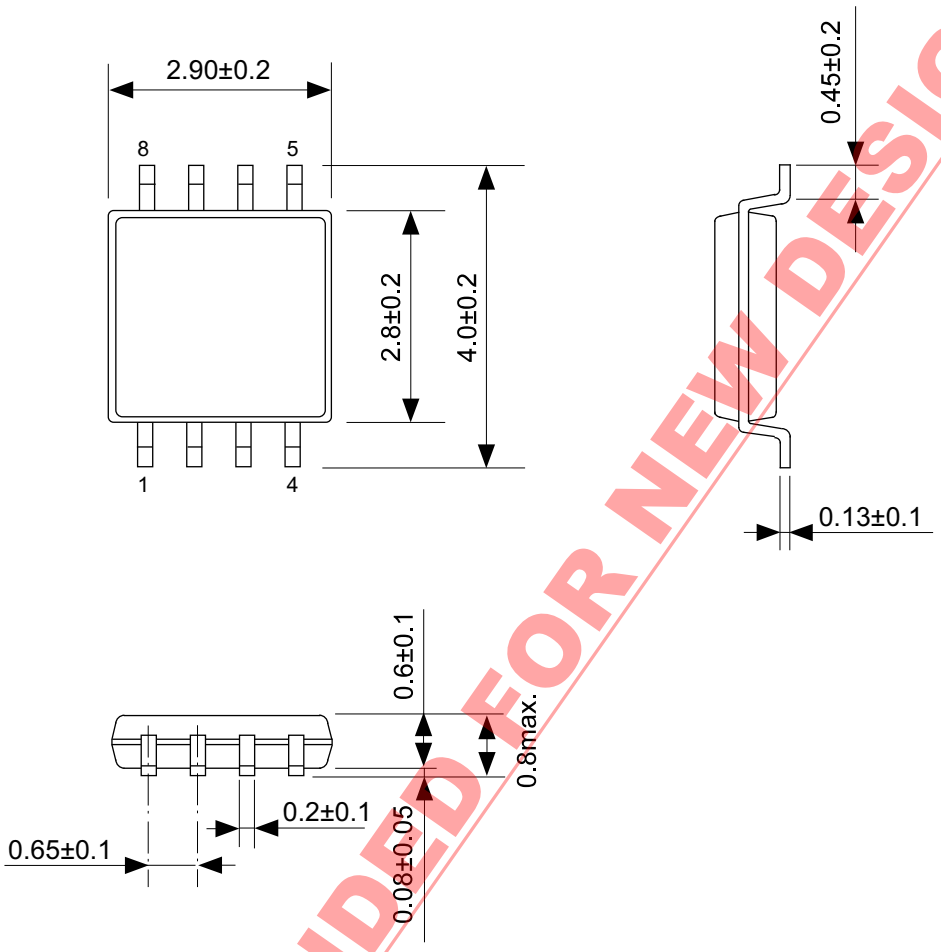
Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		

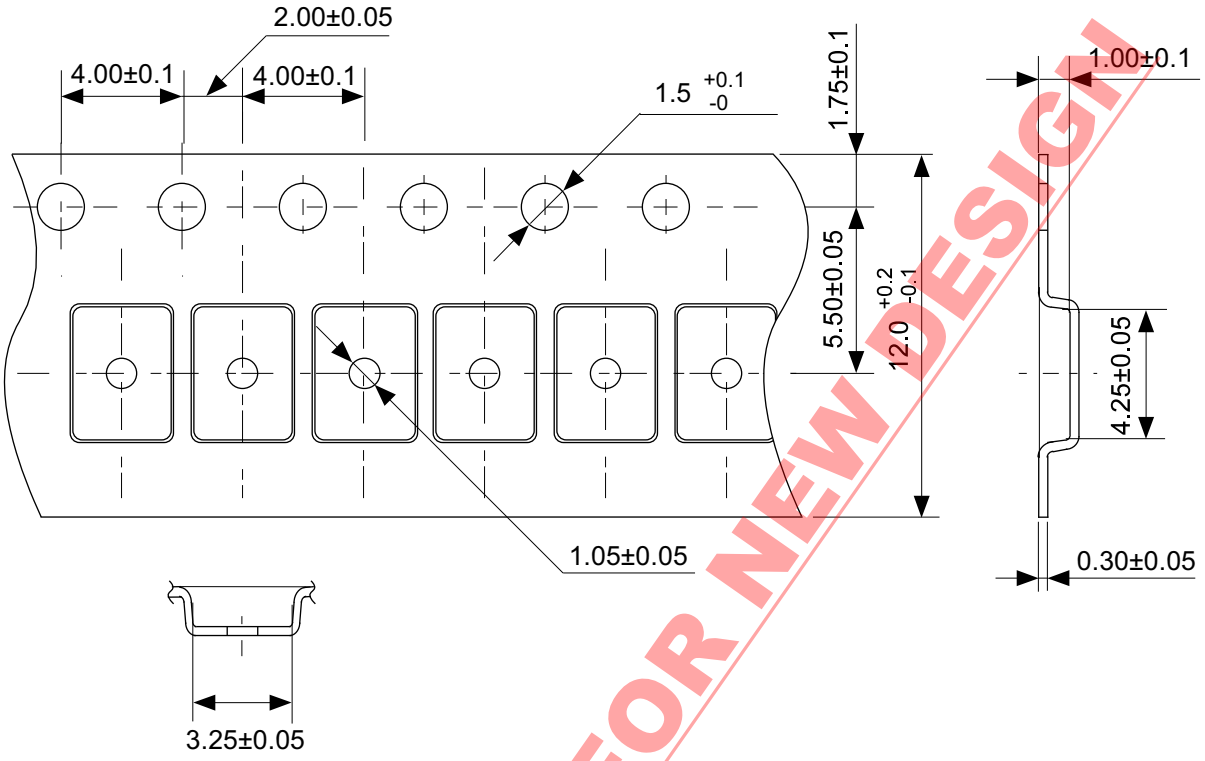
ABLIC Inc.

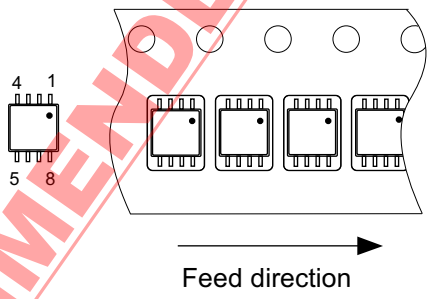


No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm

ABLIC Inc.

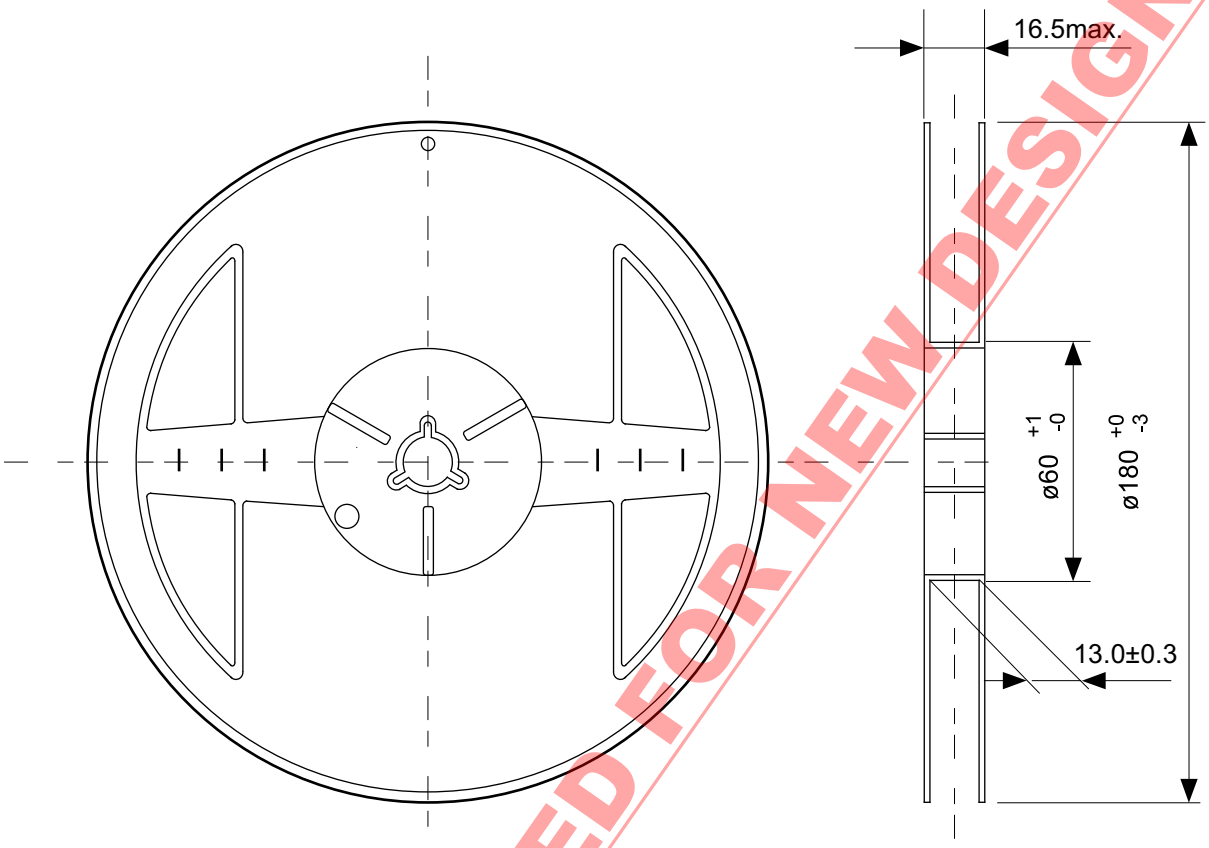




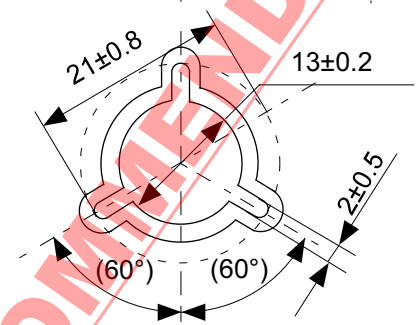
No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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