

The S-8471 Series is Wireless Power Receiver Control IC, which is configured with an overvoltage detection circuit, a high temperature detection circuit, an ON / OFF circuit, etc.

## ■ Features

- Current consumption:
  - During operation:  $I_{SS1} = 30 \mu\text{A typ.}$
  - During power-off:  $I_{SS2} = 1.0 \mu\text{A max.}$
- Overvoltage detection voltage range: 4.00 V to 5.50 V, selectable in 50 mV step
- Overvoltage detection accuracy:  $\pm 2.0\%$
- ON / OFF pin control logic is selectable: Active "H", active "L"
- ON / OFF pin internal resistor connection is selectable: Unavailable, pull-up, pull-down
- Built-in ON / OFF circuit
- Over temperature protection function: Available by connecting a thermistor to the TH pin.
- Operation temperature range:  $T_a = -40^\circ\text{C to } +85^\circ\text{C}$
- Lead-free (Sn 100%), halogen-free

## ■ Applications

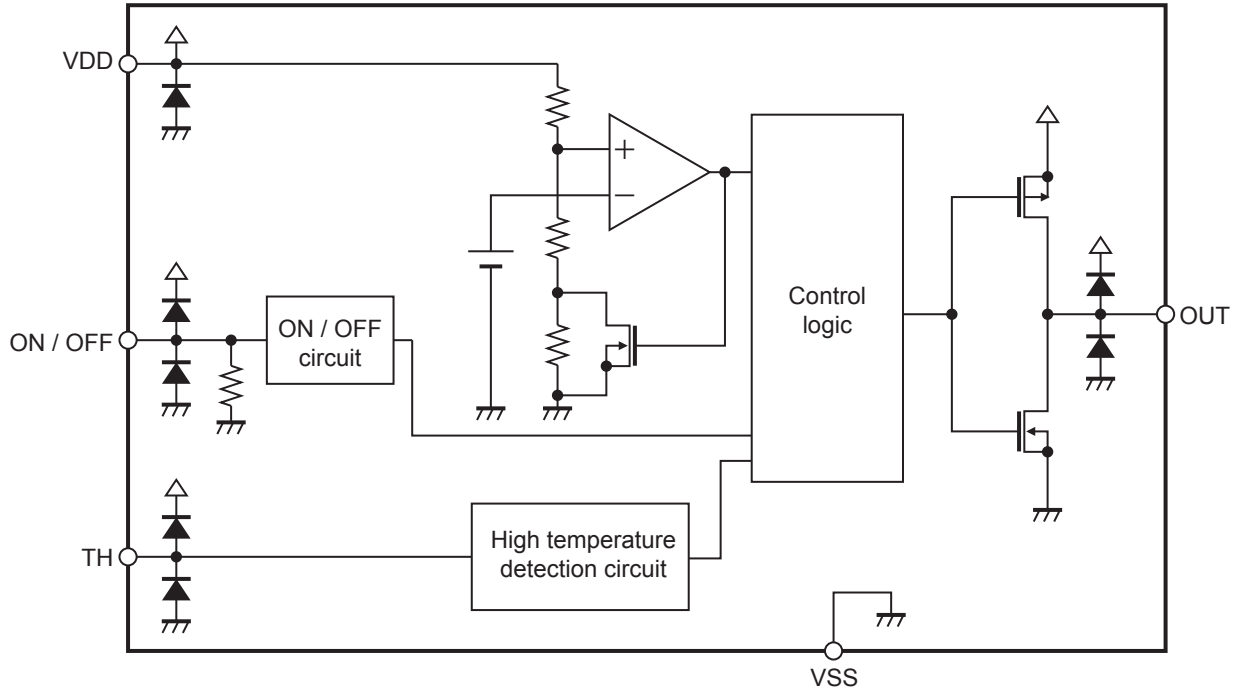
- Device for wireless power
- Small-sized wireless charging system

## ■ Package

- SNT-6A

■ **Block Diagrams**

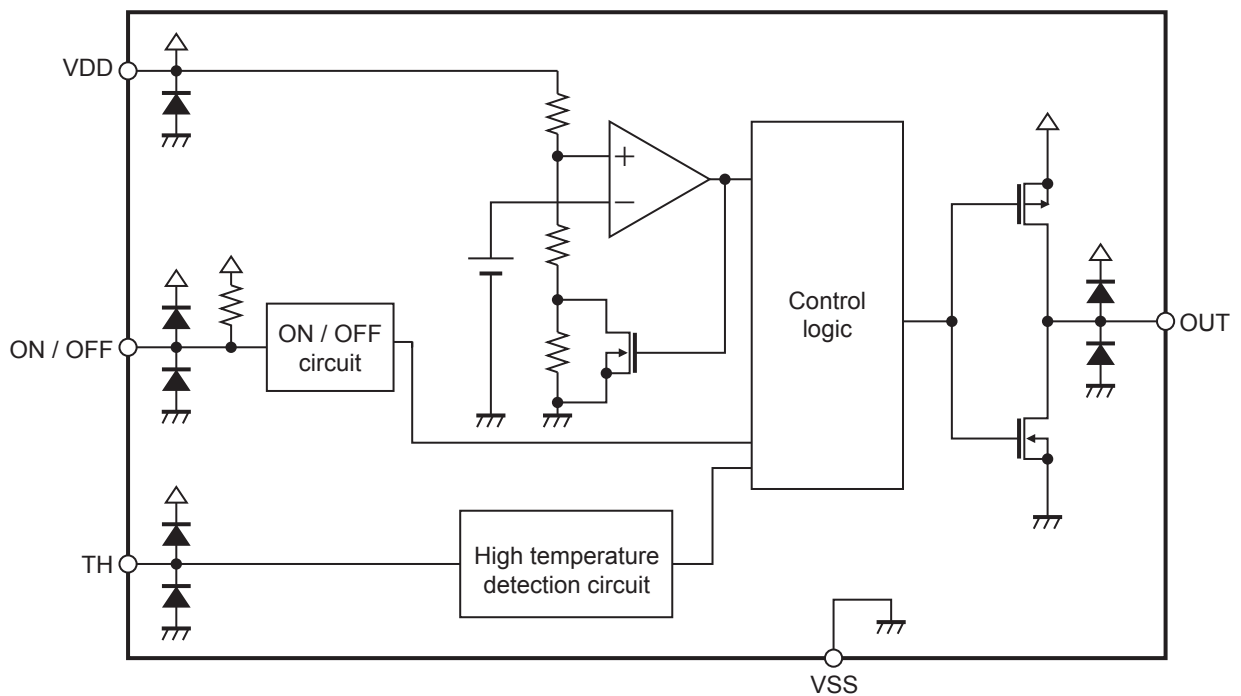
**1. ON / OFF pin internal resistor connection "pull-down"**



**Remark** All the diodes shown in the figure are parasitic diodes.

**Figure 1**

**2. ON / OFF pin internal resistor connection "pull-up"**

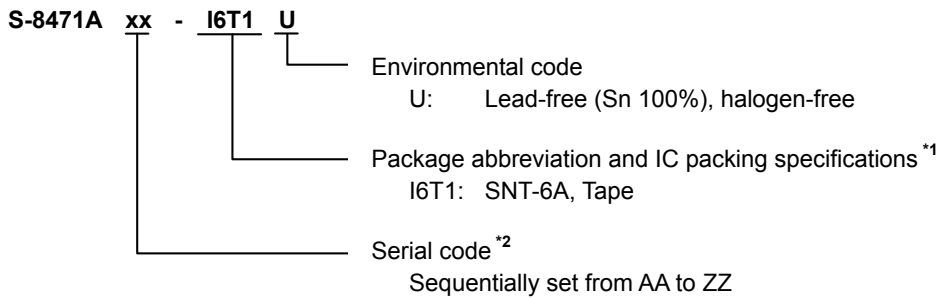


**Remark** All the diodes shown in the figure are parasitic diodes.

**Figure 2**

■ **Product Name Structure**

1. **Product name**



\*1. Refer to the tape drawing

\*2. Refer to "3. Product name list".

2. **Package**

**Table 1 Package Drawing Codes**

Package Name	Dimension	Tape	Reel	Land
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. **Product name list**

**Table 2**

Product Name	Overvoltage Detection Voltage [V <sub>OVP</sub> ]	ON / OFF Pin	
		Control Logic*1	Internal Resistor Connection*2
S-8471AAA-I6T1U	5.00 V	Active "H"	Pull-down

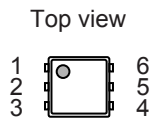
\*1. ON / OFF pin control logic is selectable: Active "H", active "L"

\*2. ON / OFF pin internal resistor connection is selectable: Unavailable, pull-up, pull-down

**Remark** Please contact our sales office for products other than the above.

■ **Pin Configuration**

1. **SNT-6A**



**Figure 3**

**Table 3**

Pin No.	Symbol	Description
1	VDD	Power supply voltage pin
2	ON / OFF	ON / OFF pin
3	TH	Thermistor connection pin
4	NC <sup>*1</sup>	No connection
5	VSS	GND pin
6	OUT	FET gate drive pin for resonance

\*1. The NC pin is electrically open.

■ **Absolute Maximum Ratings**

**Table 4**

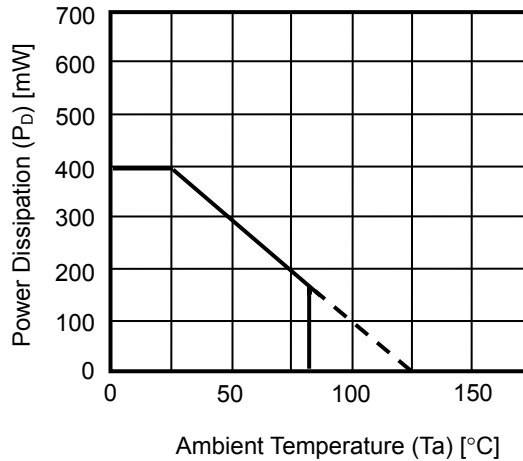
(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V <sub>DD</sub>	VDD	V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 7.0	V
Input pin voltage	V <sub>IN</sub>	ON / OFF, TH	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
Output pin voltage	V <sub>OUT</sub>	OUT	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
Power dissipation	P <sub>D</sub>	-	400 <sup>*1</sup>	mW
Operation ambient temperature	T <sub>opr</sub>	-	-40 to +85	°C
Storage temperature	T <sub>stg</sub>	-	-40 to +125	°C

\*1. When mounted on board  
[Mounted board]

- (1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
- (2) Board name: JEDEC STANDARD51-7

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



**Figure 4 Power Dissipation of Package (When Mounted on Board)**

■ **Electrical Characteristics**

**Table 5**

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operation voltage	V <sub>DD</sub>	–	0.95	–	6.5	V
Current consumption during operation	I <sub>SS1</sub>	V <sub>DD</sub> = V <sub>OVP</sub> + 1.0 V	–	30	50	μA
Current consumption during power-off	I <sub>SS2</sub>	V <sub>DD</sub> = V <sub>OVP</sub> + 1.0 V, ON / OFF pin = OFF	–	0.3	1.0	μA
Overshoot detection voltage	V <sub>OVP</sub>	–	V <sub>OVP</sub> × 0.98	V <sub>OVP</sub>	V <sub>OVP</sub> × 1.02	V
Hysteresis width	V <sub>HYS</sub>	–	85	100	115	mV
OUT pin sink current	I <sub>OUTN</sub>	V <sub>DD</sub> = V <sub>OVP</sub> + 0.3 V, V <sub>OUT</sub> = 0.5 V	1.5	–	–	mA
OUT pin source current	I <sub>OUTP</sub>	V <sub>DD</sub> = V <sub>OVP</sub> – 0.3 V, V <sub>OUT</sub> = V <sub>DD</sub> – 0.5 V	–	–	–1.4	mA
ON / OFF pin input voltage "H"	V <sub>SH</sub>	V <sub>DD</sub> = V <sub>OVP</sub> – 1.0 V	1.5	–	–	V
ON / OFF pin input voltage "L"	V <sub>SL</sub>	V <sub>DD</sub> = V <sub>OVP</sub> – 1.0 V	–	–	0.3	V
ON / OFF pin input current "H"	I <sub>SH</sub>	V <sub>ON / OFF</sub> = V <sub>DD</sub> , ON / OFF pin internal resistor connection "pull-down"	0.1	–	1.0	μA
		V <sub>ON / OFF</sub> = V <sub>DD</sub> , ON / OFF pin internal resistor connection "pull-up"	–0.1	–	0.1	μA
ON / OFF pin input current "L"	I <sub>SL</sub>	V <sub>ON / OFF</sub> = 0 V, ON / OFF pin internal resistor connection "pull-down"	–0.1	–	0.1	μA
		V <sub>ON / OFF</sub> = 0 V, ON / OFF pin internal resistor connection "pull-up"	–1.0	–	–0.1	μA
ON / OFF pin internal resistance	R <sub>ON / OFF</sub>	–	12.5	25.0	50.0	MΩ
TH pin detection resistance	R <sub>TH</sub>	V <sub>DD</sub> = V <sub>OVP</sub> – 1.0 V	37	41	45	kΩ

■ Test Circuit

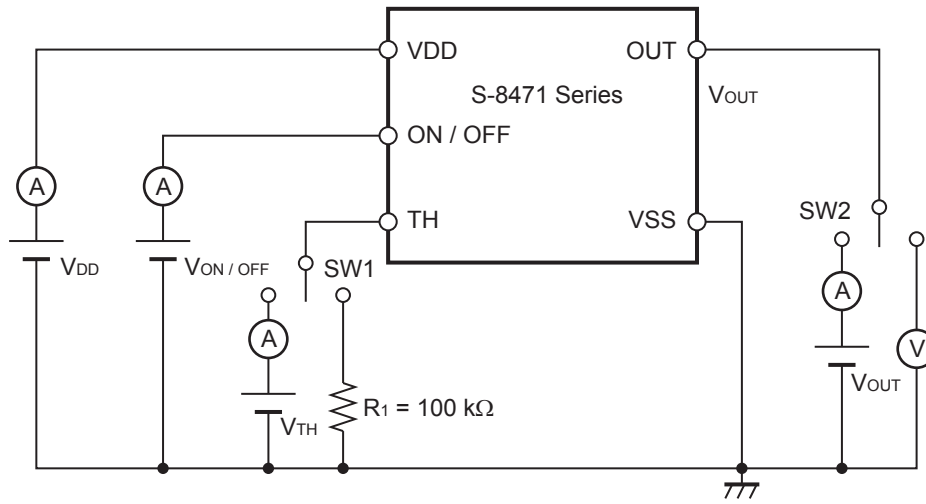


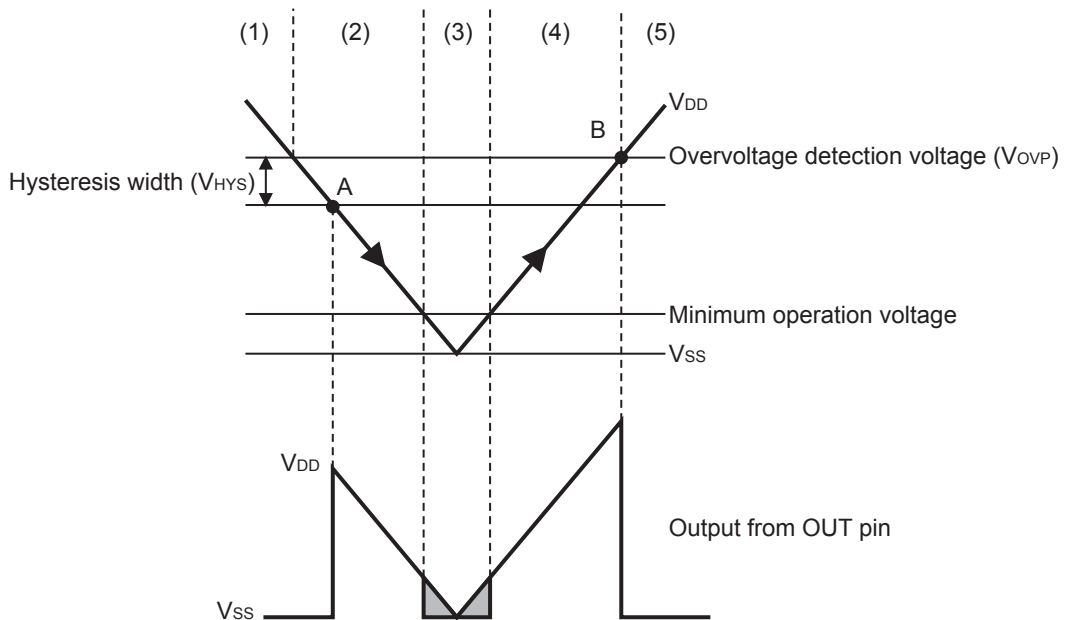
Figure 5

■ **Operation**

**Remark** Refer to "■ Standard Circuit".

**1. Basic operation**

- (1) When the power supply voltage ( $V_{DD}$ ) is the overvoltage detection voltage ( $V_{OVP}$ ) or higher,  $V_{SS}$  ("L") is output from the OUT pin.
- (2) Even if  $V_{DD}$  decreases to  $V_{OVP}$  or lower,  $V_{SS}$  is output from the OUT pin when  $V_{DD}$  is higher than  $V_{OVP} - V_{HYS}$ .  
 $V_{DD}$  further decreases to  $V_{OVP} - V_{HYS}$  (A point in **Figure 6**) or lower,  $V_{DD}$  ("H") is output from the OUT pin.
- (3) When  $V_{DD}$  additionally decreases to the minimum operation voltage (0.95 V) or lower, the output from the OUT pin is unstable.
- (4) When  $V_{DD}$  increases to the minimum operation voltage or higher,  $V_{DD}$  is output from the OUT pin.  
 Also, even if  $V_{DD}$  exceeds  $V_{OVP} - V_{HYS}$ ,  $V_{DD}$  is output from the OUT pin when it is lower than  $V_{OVP}$ .
- (5)  $V_{DD}$  further increases to  $V_{OVP}$  (B point in **Figure 6**) or higher,  $V_{SS}$  is output from the OUT pin.



**Remark** When  $V_{DD}$  is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

**Figure 6**



## 2. ON / OFF pin

This pin starts and stops the operations of all internal circuits.

When the ON / OFF pin is set to OFF level, the operations of all internal circuits are stopped, reducing the current consumption significantly.

Note that the current consumption increases when a voltage of 0.3 V to 1.5 V is applied to the ON / OFF pin.

### 2.1 ON / OFF pin control logic active "H"

When the ON / OFF pin voltage is the ON / OFF pin input voltage "L" ( $V_{SL}$ ) or lower, the operations of all internal circuits are stopped, and  $V_{SS}$  is output from the OUT pin. When the ON / OFF pin voltage is ON / OFF pin input voltage "H" ( $V_{SH}$ ) or higher, the operations of all internal circuits are started, and the OUT pin outputs depending on the status.

#### 2.1.1 ON / OFF pin internal resistor connection "pull-down"

Since the ON / OFF pin is pulled down to the VSS pin internally in a floating status, the operations of all circuits are stopped and  $V_{SS}$  is output from the OUT pin.

#### 2.1.2 ON / OFF pin internal resistor connection "pull-up"

Since the ON / OFF pin is pulled up to the VDD pin internally in a floating status, the operations of all circuits are started and the OUT pin outputs the level depending on the status.

#### 2.1.3 ON / OFF pin internal resistor connection "unavailable"

Since the ON / OFF pin is neither pulled down nor pulled up internally, do not use it in floating status. When not using the ON / OFF pin, connect it to the VDD pin.

### 2.2 ON / OFF pin control logic active "L"

When the ON / OFF pin voltage is the ON / OFF pin input voltage "H" ( $V_{SH}$ ) or higher, the operations of all internal circuits are stopped, and  $V_{SS}$  is output from the OUT pin. When the ON / OFF pin voltage is the ON / OFF pin input voltage "L" ( $V_{SL}$ ) or lower, the operations of all internal circuits are started, and the OUT pin outputs depending on the status.

#### 2.2.1 ON / OFF pin internal resistor connection "pull-down"

Since the ON / OFF pin is pulled down to the VSS pin internally in a floating status, the operations of all circuits are started and the OUT pin outputs the level depending on the status.

#### 2.2.2 ON / OFF pin internal resistor connection "pull-up"

Since the ON / OFF pin is pulled up to the VDD pin internally in a floating status, the operations of all circuits are stopped and  $V_{SS}$  is output from the OUT pin.

#### 2.2.3 ON / OFF pin internal resistor connection "unavailable"

Since the ON / OFF pin is neither pulled down nor pulled up internally, do not use it in a floating status. When not using the ON / OFF pin, connect it to the VSS pin.

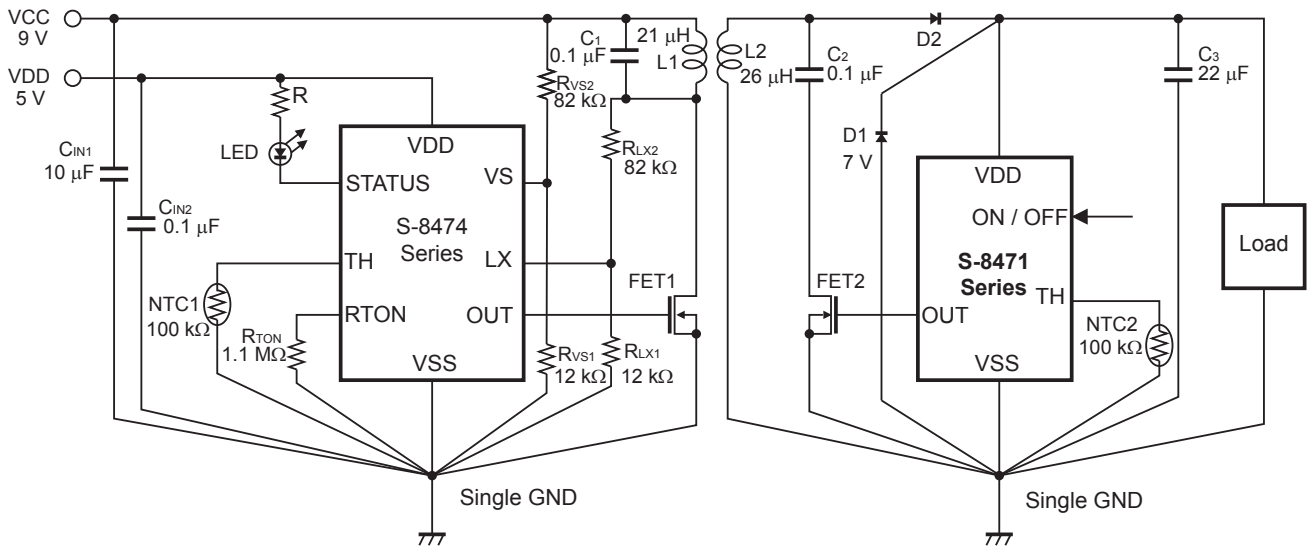
### 3. Over temperature protection function

By connecting an external thermistor to the TH pin, a potential over temperature status (due to external component heat generation) can be prevented. When external component heat generation decreases and the thermistor resistance drops to the TH pin detection resistance ( $R_{TH}$ ), the over temperature protection function begins operation, and then  $V_{SS}$  is output from the OUT pin. When external component heat generation increases and the thermistor resistance increases to approximately 15 k $\Omega$  typ. above  $R_{TH}$ , the over temperature protection function stops operating, and then the OUT pin outputs depending on the status.

When  $V_{DD}$  decreases to 2.0 V typ., the operation of the high temperature detection circuit is stopped and  $V_{DD}$  is output from the OUT pin. The operation of the high temperature detection circuit is restarted when  $V_{DD}$  increases to 2.1 V typ. or higher.

Connect a thermistor between the TH pin and the VSS pin. An NTC thermistor of  $R = 100$  k $\Omega$  at  $T_a = +25^\circ\text{C}$  ( $R_{25}$ ) is recommended. For example, if an NTC thermistor of  $R_{25}$  and  $B_{25/50}$  (B constant ( $25^\circ\text{C}/50^\circ\text{C}$ )) = 4250 K is used, the over temperature protection function begins to operate at approximately  $+45^\circ\text{C}$ . When not using the over temperature protection function, set the TH pin open or connect a resistor of 100 k $\Omega$  or greater.

■ **Standard Circuit**



**Figure 7**

**Caution** The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

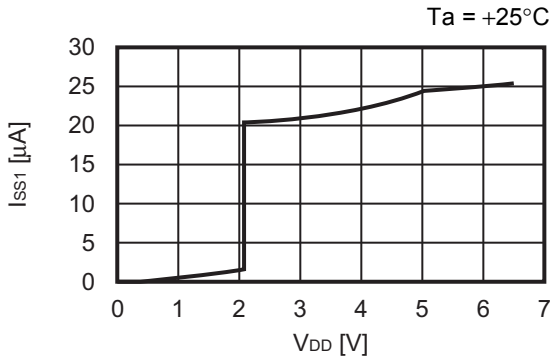
■ **Precautions**

- The application conditions for the input voltage, the output voltage, and the load current should not exceed the package power dissipation.
- In this IC, the feed-through current flows at detecting and releasing of the overvoltage. For this reason, when the impedance of the VDD pin is high, a malfunction may be caused by the voltage drop due to the feed-through current at releasing of the overvoltage.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

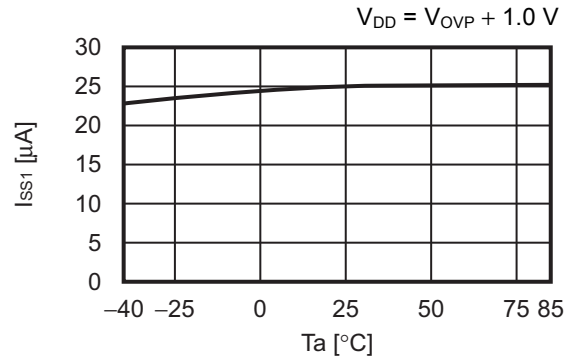
**■ Characteristics (Typical Data)**

**1. Current consumption**

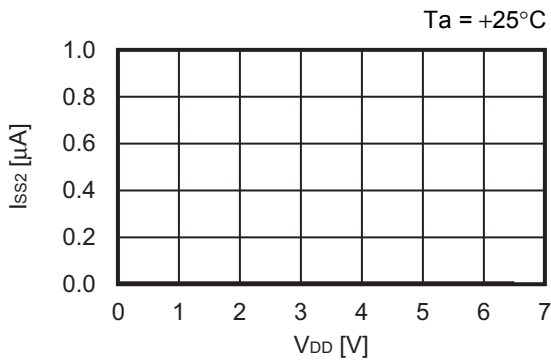
**1.1  $I_{SS1}$  vs.  $V_{DD}$**



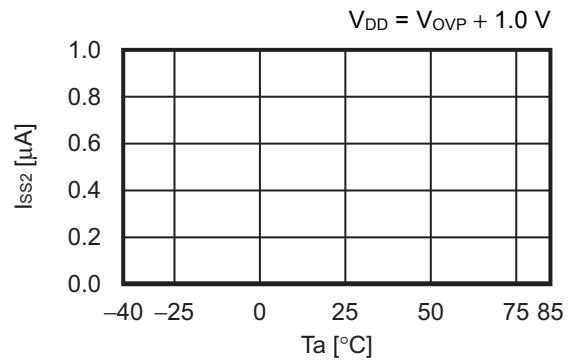
**1.2  $I_{SS1}$  vs.  $T_a$**



**1.3  $I_{SS2}$  vs.  $V_{DD}$**

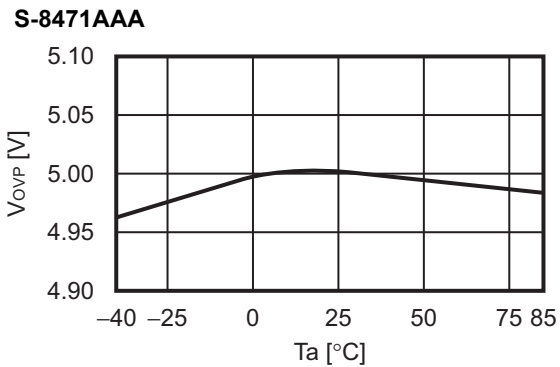


**1.4  $I_{SS2}$  vs.  $T_a$**

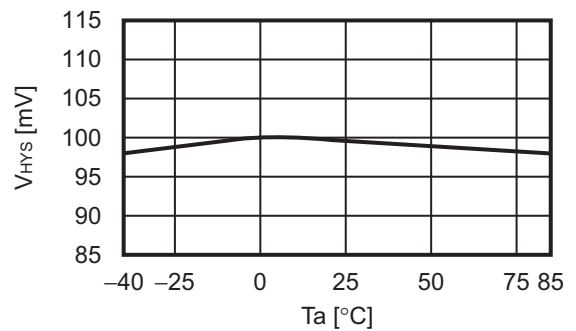


**2. Overvoltage detection voltage, hysteresis width, UVLO detection voltage**

**2.1  $V_{OVP}$  vs.  $T_a$**

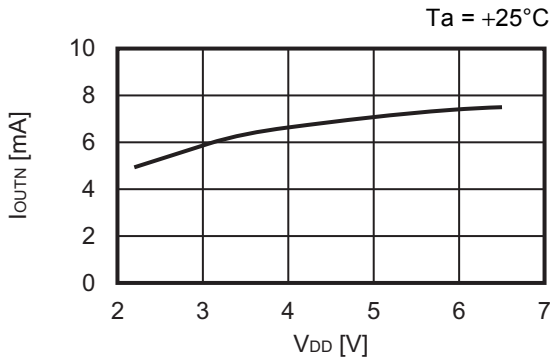


**2.2  $V_{HYS}$  vs.  $T_a$**

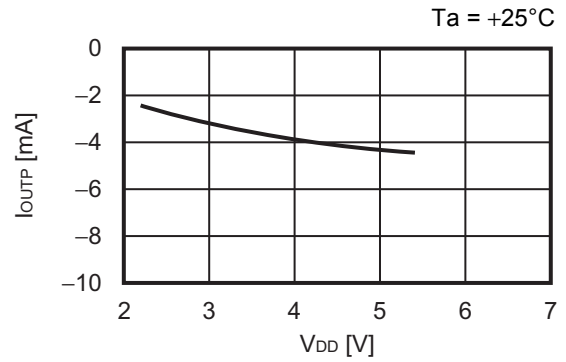


**3. OUT pin sink current, OUT pin source current**

**3.1  $I_{OUTN}$  vs.  $V_{DD}$**

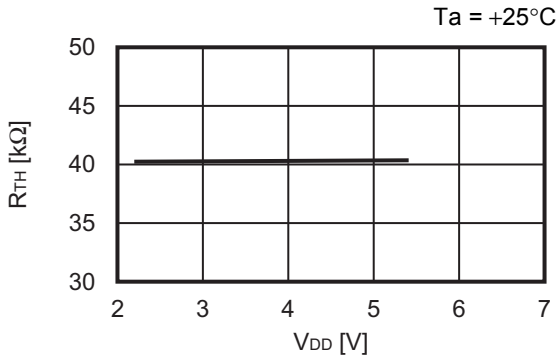


**3.2  $I_{OUTP}$  vs.  $V_{DD}$**

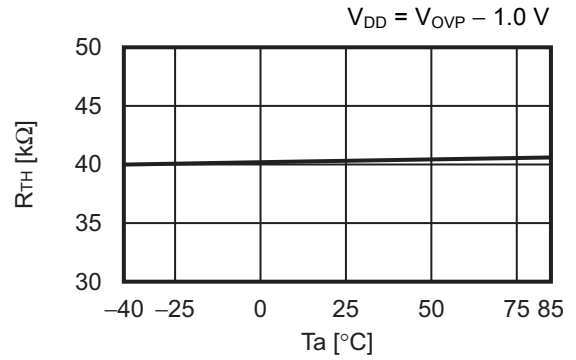


**4. TH pin detection resistance**

**4.1  $R_{TH}$  vs.  $V_{DD}$**



**4.2  $R_{TH}$  vs.  $T_a$**





No. PG006-A-P-SD-2.1

TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



Feed direction →

No. PG006-A-C-SD-2.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-2.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	





Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
<b>ABLIC Inc.</b>			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.).  
 ※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

- 注意
1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
  2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm以下にしてください。
  3. マスク開口サイズと開口位置はランドパターンと合わせてください。
  4. 詳細は“SNTパッケージ活用の手引き”を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).  
 ※2. Do not widen the land pattern to the center of the package ( 1.30 mm ~ 1.40 mm ).

- Caution**
1. Do not do silkscreen printing and solder printing under the mold resin of the package.
  2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
  3. Match the mask aperture size and aperture position with the land pattern.
  4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.).  
 ※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

- 注意
1. 请勿在树脂型封装的下面印刷丝网、焊锡。
  2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
  3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
  4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

## Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.  
The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07