S-US5591

32-CHANNEL PROGRAMMABLE 3-LEVEL ULTRASOUND TRANSMIT BEAMFORMER

Rev.1.1_00

The ABLIC S-US5591 is a 32-channel programmable 3-level ultrasound transmit beamformer.
Each channel comprises high voltage 3-level pulser (3LP) and active T/R switch.

■ Function

- 32-channel programmable 3-level ultrasound transmit beamformer.

■ Features

3-level pulser (3LP)

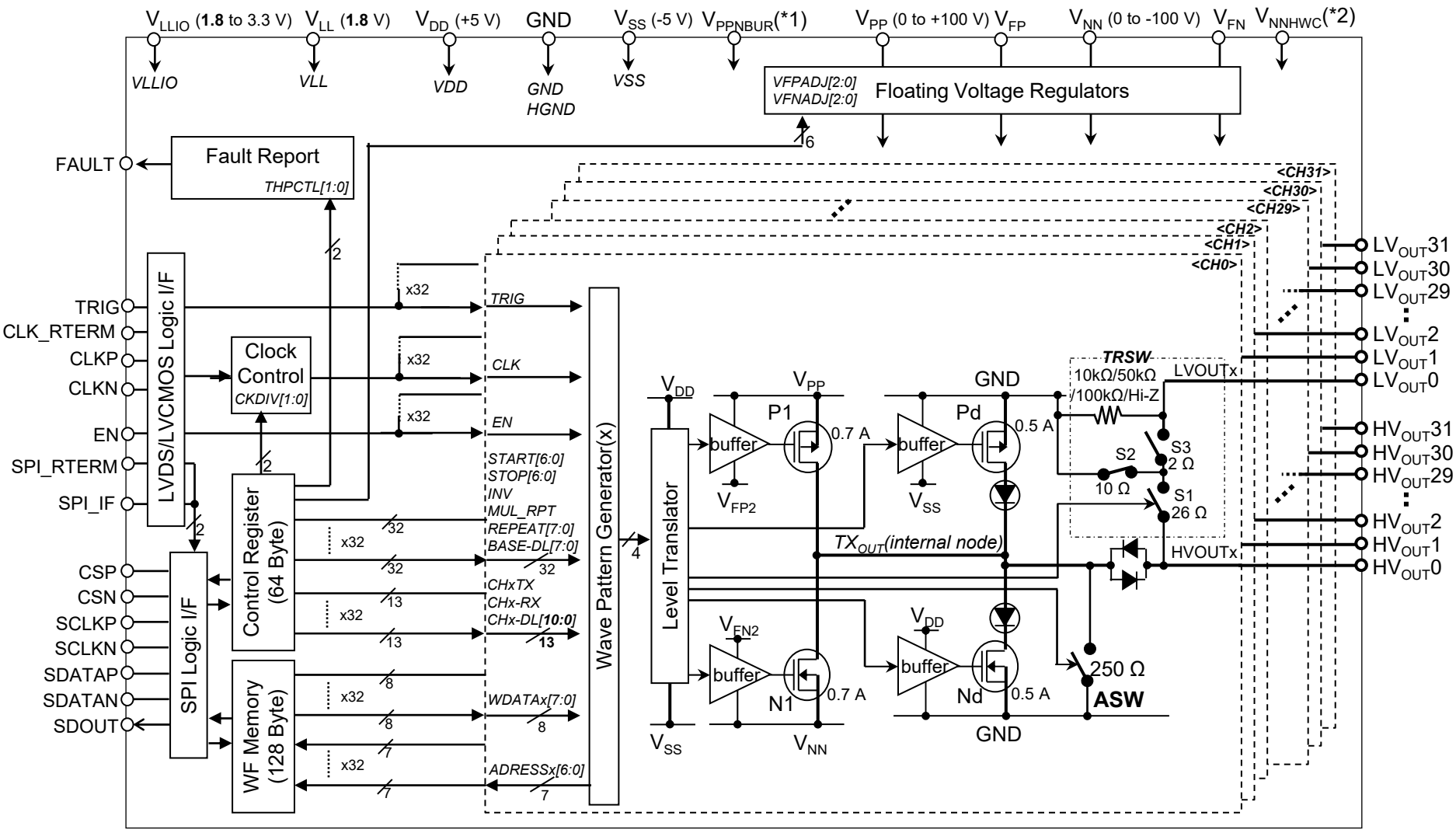
- 0 to ±100 V output voltage
- ±0.7 A source and sink current for high-voltage pulses
- ±0.5 A source and sink active ground clamp
- 10 ns min. pulse width with 5 ns resolution at 100 MHz clock
- Inversion and repetition control of Tx waveform data
- 0.16 to 40.96 µs common delay to all channel at 100 MHz clock
- 0 to 10.235 µs channel delay range with 5 ns resolution at 100 MHz clock
- Individual active Tx channel control

Common

- Up to 100 MHz LVDS/CMOS clock (dual edge operation)
- Serial Peripheral Interface ports (LVDS or 1.8 to 3.3 V CMOS)
- Automatic thermal protection with indicator
- 128 Byte Waveform Memory and 64 Byte control Register
- 314 pin 13 x 13 mm BGA package (RoHS compliant)

■ Contents

■ Block Diagram



*1: V_{PPNBUR} is positive high-voltage for protection and must be higher than V_{PP} and V_{NN}.
*2: V_{NNHWC} is negative high-voltage for protection and must be lower than V_{PP} and V_{NN}.

■ Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Item	Symbol	Value	Unit	Condition
Positive high-voltage for protection	V_{PPNBUR}	-0.5 to +110	V	Must be Higher than V_{PP} and V_{NN}
Positive high-voltage	V_{PP}	-0.5 to +110	V	Tx
Negative high-voltage	V_{NN}	-110 to +0.5	V	Tx
Negative high-voltage for protection	V_{NNHWC}	-110 to +0.5	V	Must be lower than V_{PP} and V_{NN}
Positive voltage	V_{DD}	-0.5 to +7	V	Tx, Rx
Negative voltage	V_{SS}	-7 to +0.5	V	Tx, Rx
Logic I/F voltage	V_{LLIO}	-0.5 to +4	V	FPGA I/F
Logic voltage	V_{LL}	-0.5 to +2.3	V	Logic
High-voltage outputs (x = 0 to 31)	$HV_{OUT}x$	-110 to +110	V	
Low-voltage outputs (x = 0 to 31)	$LV_{OUT}x$	-1 to 1	V	
THP (Thermal Protection) output	FAULT	-0.5 to +7	V	
All logic input/output voltages	TRIG etc.	-0.5 to +7	V	TRIG, CLK_RTERM, CLKP/N, EN, SPI_IF, SPI_RTERM,CSP/N, SDATAP/N, SDOUT
Operating junction temperature	TJop	-20 to +150	°C	
Storage temperature	TSTG	-55 to +150	°C	
VPP, VNN, VPPNBUR, VNNHWC slew rate	SR_{MAX}	<25	V/ms	

NOTE: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

■ Supply Voltages and Clock Signals

Operating supply voltages

Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
Positive high-voltage for protection	V_{PPNBUR}	V	0	-	100	Must be Higher than V_{PP} and V_{NN}
Positive high-voltage	V_{PP}	V	0	-	100	Tx
Negative high-voltage	V_{NN}	V	-100	-	0	Tx
Negative high-voltage for protection	V_{NNHWC}	V	-100	-	0	Must be lower than V_{PP} and V_{NN}
Positive voltage	V_{DD}	V	4.75	5	5.25	Tx, Rx
Negative voltage	V_{SS}	V	-5.25	-5	-4.75	Tx, Rx
LOGIC I/F Voltage	V_{LLIO}	V	1.71	1.8 to 3.3	3.465	IFPGA /F
Logic voltage	V_{LL}	V	1.71	1.8	1.89	Logic

Clock signal

Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
Clock (CLKP/CLKN)	F_{CLK}	MHz	-	100	-	Differential clock Selectable LVDS or LVCMOS

■ Power Sequence

1. VPPNBUR is connected to VPP and VNNHWC is connected to VNN.

Power-Up Sequence

1. Power on the V_{LL} first, and then power on other Low voltage supplies (V_{LLIO}, V_{DD}, V_{SS}).
   If power on V_{LL} at the same time as other low voltage supplies, power-up of V_{LL} must not be delayed by more than 1 msec from power-up of V_{DD}.
2. Then, V_{PP} (V_{PPNBUR}) can be set from 0 V to +100 V and V_{NN} (V_{NNHWC}) can be set from 0 V to -100 V

Power-Down Sequence

1. First, power-down V_{PP} (V_{PPNBUR}) and V_{NN} (V_{NNHWC}).
2. Then, power-down low voltage supplies (V_{LLIO}, V_{LL}, V_{DD}, V_{SS}).

2. VPPNBUR is separately from VPP and VNNHWC is separately from VNN

Power-up sequence

1. First, V_{PPNBUR} is set to ≥ max V_{PP} to use, and V_{NNHWC} is set to ≤ min V_{NN} to use.
   If +80 V and -80 V are used for max V_{PP} and min V_{NN}, V_{PPNBUR} and V_{NNHWC} should be ≥ +80 V and ≤ -80 V, respectively. For example, you can use fixed +100 V for V_{PPNBUR}, and fixed -100 V for V_{NNHWC}.
2. Power on the V_{LL} first, and then power on other Low voltage supplies (V_{LLIO}, V_{DD}, V_{SS}).
   If power on V_{LL} at the same time as other low voltage supplies, power-up of V_{LL} must not be delayed by more than 1 msec from power-up of V_{DD}.
3. Then, V_{PP} (V_{PPNBUR}) can be set from 0 V to +100 V and V_{NN} (V_{NNHWC}) can be set from 0 V to -100 V

Power-down sequence

1. First, power-down V_{PP} and V_{NN}.
2. Next, power-down Low voltage supplies (V_{LLIO}, V_{LL}, V_{DD}, V_{SS}).
3. Then, power-down V_{PPNBUR} and V_{NNHWC}.

■ LVDS I/F Inputs

CLKP/CLKN,CSP/CSN,SCLKP/SCLKN,SDATAP/SDATAN

Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
High-level input voltage	V_{IH}	V	1.265	-	-	V_{IHCMR}(Typ) + V_{DIFF}(Min)/2
Low-level input voltage	V_{IL}	V	-	-	1.135	V_{IHCMR}(Typ) - V_{DIFF}(Min)/2
Differential input voltage range	$V_{DIFF(range)}$	±V	0.13	0.35	0.49	same as voltage swing
Differential input voltage p-p swing	$V_{DIFF(p-p)}$	V_{pp}	0.26	0.7	0.98	Differential peak-to-peak absolute voltage swing
Input voltage common range	V_{IHCMR}	V	0.84	1.2	1.56	
Differential input impedance	R_{IN}	Ω	60	100	140	
High-level input current	I_{IH}	mA	-	-	8.17	
Low-level input current	I_{IL}	mA	-	-	8.17	
Input rise/fall time	t_r , t_f	ps	-	-	600	20% to 80% of V_{DIFF}
Input clock frequency	f_{CLK}	MHz	-	-	100	CLKP/CLKN
Clock duty cycle	D_{CLK}	%	45	50	55	f_{CLK} = 1/T_{CLK}, D_{CLK} = HTCLK/T_{CLK}

Note:
Internal or external 100 Ω should be connected between differential LVDS inputs of clock and SPI inputs.

■ CMOS I/F Inputs and Outputs

CLKP/CLKN,CSP/CSN,SCLKP/SCLKN,SDATAP/SDATAN (*2)
TRIG,EN,SPI_IF,CLK_RTERM,SPI_RTERM,SDOUT

Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
High-level logic input voltage	V_{IH}	V	0.8 x V_{LLIO}	-	V_{LLIO}	
Low-level logic input voltage	V_{IL}	V	0	-	0.2 x V_{LLIO}	
Logic input capacitance	C_{IN}	pF	-	5	-	
Logic input high current	I_{IH}	µA	-10	-	10	
Logic input low current (*1)	I_{IL}	µA	-10	-	10	
Pull-up/Pull-down Resister	R_{PU_PD}	kΩ	-	50	-	
Input rise/fall time	t_r , t_f	ns	-	-	2	10 to 90% of signal
TRIG fall to clock rise setup time	$t_{SU\_TRFtoCKR}$	ns	1.5	-	-	
TRIG fall to clock rise hold time	$t_{HLD\_TRFtoCKR}$	ns	1.5	-	-	
TRIG width	t_{W_TRIG}	ns	$3T_{CLK}$	-	-	
High-level logic output voltage	V_{OH}	V	0.8 x V_{LLIO}	-	V_{LLIO}	SDOUT @ 2.5 kΩ load
Low-level logic output voltage	V_{OL}	V	0	-	0.2 x V_{LLIO}	SDOUT @ 2.5 kΩ load
Logic output off leak current	$I_{OFFLEAK}$	µA	-10	-	10	SDOUT Hi-Z output

NOTE:
*1) EN,SPI_IF,CLK_RTERM and SPI_RTERM has 36 µA leakage at V_{LLIO} = 1.8 V due to 50 kΩ internal pull-up resistor.
*2) Differential CMOS or Single-ended CMOS is also available for CLKP/N,CSP/N,SCLKP/N and SDATAP/N.
When using CMOS inputs, termination resistor must be disabled.
In case of single-ended CMOS, N-terminals (CLKN,CSPN,SCLKN,SDATAN) need to be connected to half of V_{LLIO} (V_{LLIO}/2).
If SPI_IF is set to “Hi”, half of V_{LLIO} (V_{LLIO}/2) are internally connected to N-terminals of SPI pins (CSPN,SCLKN and SDATAN).
In this case, differential CMOS is not available for SPI pins.

■ Open Drain I/F Output

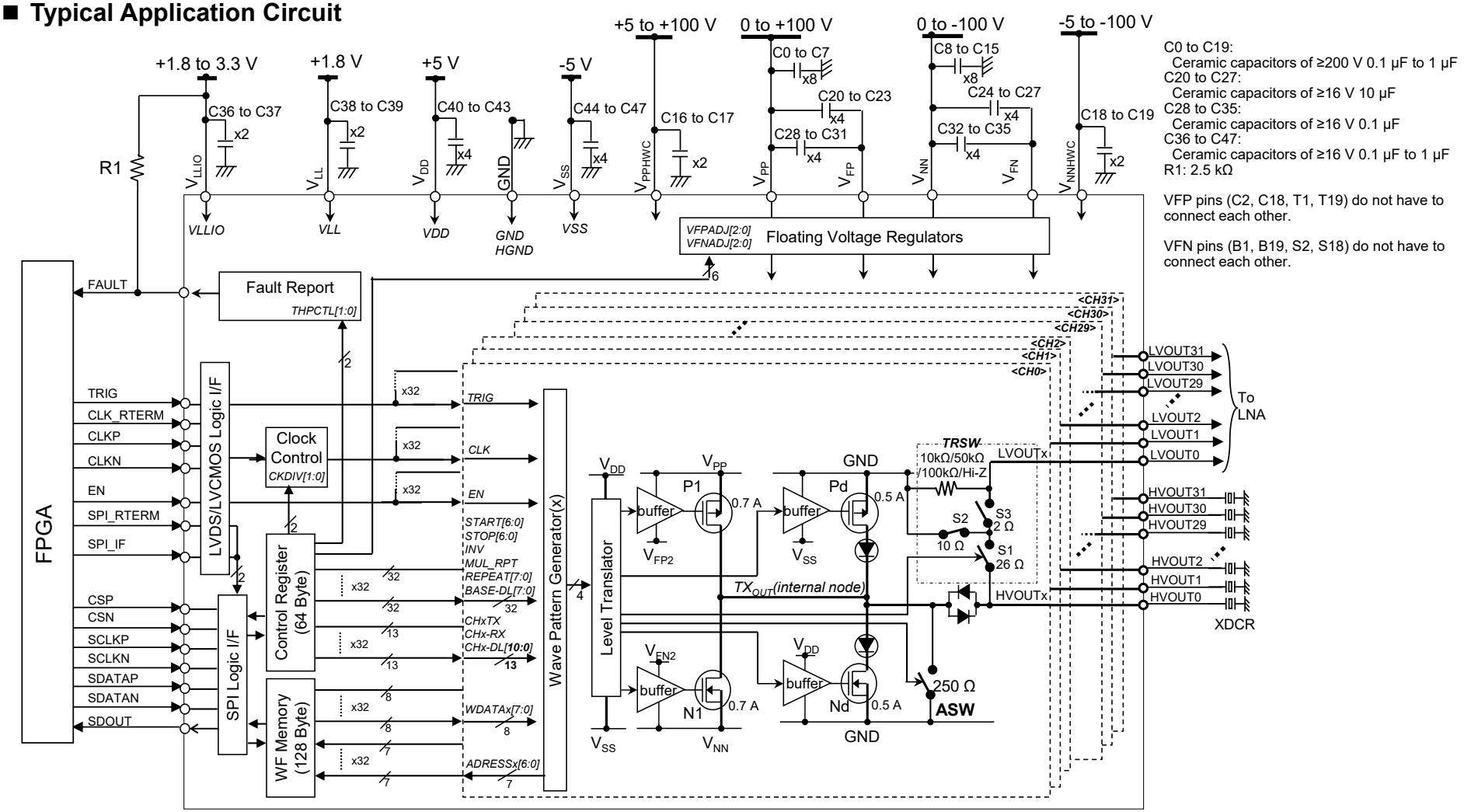
Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
Pull-up voltage	$V_{PUFAULT}$	V	-	-	VLLIO	Connected to VLLIO with R1
Output low voltage	$V_{OLFAULT}$	V	-	-	0.5	Active, V_{LLIO} = 1.8 V, R1 = 2.5 kΩ
Output current	I_{FAULT}	mA	-	0.7	-	V_{LLIO} = 1.8 V, R1 = 2.5 kΩ
Off leak current	$I_{OFFLEAK}$	µA	-10	-	10	Disabled (Hi-Z)

■ SPI I/F

SPI I/F spec

Item		Symbol	Unit	Spec			Condition
				Min.	Typ.	Max.	
Serial clock (SCLK) frequency	Write	f_{SCLK}	MHz	-	-	100	Serial clock period $T_{SCLK} = 1/f_{SCLK}$
	Read			-	-	50	
CS setup time		t_{SU_CS}	ns	2.5	-	-	CS to SCLK
CS hold time		t_{HLD_CS}		2.5	-	-	
CS interval time		t_{INT_CS}	ns	10	-	-	
CS (Hi) to TRIG rise interval time		$t_{INT\_CS\_TRIG}$	ns	20	-	-	Overlap of CS “Hi” and TRIG “Hi” is prohibited.
CS width (SPI Write time) = (8 × Data + 2) × T_{SCLK} T_{SCLK} = 10 ns (f_{SCLK} = 100 MHz)		t_{W_CS}	µs	10.42	-	-	Data Write to Memory with SDATA0 (Data = 1 + 128 + 1 Bytes)
			µs	5.30	-	-	Data Write to Tx All Register (Data = 1 + 64 + 1 Bytes)
			µs	0.82	-	-	Data Write to TX #0 to 7 Register (Data = 1 + 8 + 1 Bytes)
			µs	0.82	-	-	Data Write to TX #8 to 15 Register (Data = 1 + 8 + 1 Bytes)
			µs	2.10	-	-	Data Write to Tx #16 to 39 or #40 to 63 Register (Data = 1 + 24 + 1 Bytes)
CS width (SDI Read time) = (16 + 8 × Data + 2) × T_{SCLK} T_{SCLK} = 20 ns (f_{SCLK} = 50 MHz)			µs	20.84	-	-	Data Read from Memory (Data = 128 Bytes)
			µs	10.6	-	-	Data Read from Tx All Register (Data = 64 Bytes)
			µs	1.64	-	-	Data Read from TX #0 to 7 Register (Data = 8 Bytes)
			µs	1.64	-	-	Data Read from TX #8 to 15 Register (Data = 8 Bytes)
			µs	4.20	-	-	Data Read from Tx #16 to 39 or #40 to 63 Register (Data = 24 Bytes)
			µs	0.68	-	-	Data Read from CRC_X and CAL_CRC_X (x = 0 to 3) (Data = 2 Bytes)
			µs	0.52	-	-	Data Read from Error Register (Data = 1 Byte)
SDATA setup time		t_{SU_SDATA}	ns	2.5	-	-	SDATA to SCLK
SDATA hold time		t_{HLD_SDATA}	ns	2.5	-	-	SDATA to SCLK
SDOUT propagation delay		t_{D_SDOUT}	ns	7	11	19	

■ Typical Application Circuit



Note:

1. High-voltage power supply pins, V_{PP}/V_{NN}, can draw fast transient currents up to ±0.7 A. Therefore, ceramic capacitors of ≥200 V 0.1 µF to 1 µF (C0 to C19) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of ≥16 V 10 µF (C20 to C27), ≥16 V 0.1 µF (C28 to C35), and ≥16 V 0.1 µF to 1 µF (C36 to C47) should also be connected between high-voltage power supply pins and corresponding floating voltage pins V_{FP}/V_{FN}, and low-voltage power supply pins for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. V_{PPNBUR} is positive high-voltage for protection and must be higher than VPP and VNN.
5. V_{NNHWC} is negative high-voltage for protection and must be lower than VPP and VNN.
6. External 100 Ω should be connected between differential LVDS inputs of SPI and Clock when internal termination resisters are disabled.

■ Power Supply Current

V_{LLIO} = 1.8 V, VLL = 1.8 V, V_{DD}/V_{SS} = ±5 V, Ta = 25°C, probe load = 80 pF unless otherwise specified.

Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
V_{LLIO} Current (SPI_IF = H)	$I_{VLLIOQD}$	mA	-	0.2	-	IC disabled
V_{LLIO} Current (SPI_IF = L)			-	0.2	-	
V_{LL} Current	I_{VLLQD}	mA	-	0.2	-	EN = H VPP/VNN = ±100 V
V_{DD} Current (SPI_IF = H)	I_{VDDQD}	mA	-	10	-	
V_{DD} Current (SPI_IF = L)			-	3	-	
V_{SS} Current	I_{VSSQD}	mA	-	0.3	-	
V_{PP} Current	I_{VPPQD}	mA	-	0.1	-	
V_{NN} Current	I_{VNNQD}	mA	-	0.1	-	
V_{LLIO} Current (SPI_IF = H)	$I_{VLLIORX1}$	mA	-	0.2	-	Rx operation-1
V_{LLIO} Current (SPI_IF = L)			-	0.2	-	
V_{LL} Current	I_{VLLRX1}	mA	-	11	-	EN = L all channel active (Rx mode after burst) VPP/VNN = ±40 V
V_{DD} Current (SPI_IF = H)	I_{VDDRX1}	mA	-	12	-	
V_{DD} Current (SPI_IF = L)			-	6	-	
V_{SS} Current	I_{VSSRX1}	mA	-	0.5	-	
V_{PP} Current	I_{VPPRX1}	mA	-	0.3	-	
V_{NN} Current	I_{VNNRX1}	mA	-	0.3	-	

V_{LLIO} = 1.8 V, V_{LL} = 1.8 V, V_{DD}/V_{SS} = ±5 V, Ta = 25°C, probe load = 80 pF unless otherwise specified.

Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
V_{LLIO} Current (SPI_IF = H)	$I_{VLLIORX2}$	mA	-	0.2	-	Tx PW operation EN = L all channel active PRT = 200 µs 5 MHz BIP 2 cycle VPP/VNN = ±40 V Probe load: 80 pF
V_{LLIO} Current (SPI_IF = L)			-	0.2	-	
V_{LL} Current	I_{VLLRX2}	mA	-	40	-	
V_{DD} Current (SPI_IF = H)	I_{VDDRX2}	mA	-	15	-	
V_{DD} Current (SPI_IF = L)			-	9	-	
V_{SS} Current	I_{VSSRX2}	mA	-	1	-	
V_{PP} Current	I_{VPPRX2}	mA	-	3	-	
V_{NN} Current	I_{VNNRX2}	mA	-	3	-	
V_{LLIO} Current (SPI_IF = H)	$I_{VLLIOPW1}$	mA	-	0.2	-	TX (CW) operation-1 EN = L all channel active VPP/VNN = ±5 V 5 MHz BIP continuous wave Probe load: 80 pF
V_{LLIO} Current (SPI_IF = L)			-	0.2	-	
V_{LL} Current	I_{VLLPW1}	mA	-	100	-	
V_{DD} Current (SPI_IF = H)	I_{VDDPW1}	mA	-	64	-	
V_{DD} Current (SPI_IF = L)			-	56	-	
V_{SS} Current	I_{VSSPW1}	mA	-	25	-	
V_{PP} Current	I_{VPPPW1}	mA	-	320	-	
V_{NN} Current	I_{VNNPW1}	mA	-	320	-	

■ 3LP + TRSW Electrical Characteristics

V_{LLIO} = 1.8 V, V_{LL} = 1.8 V, V_{DD}/V_{SS} = ±5 V, V_{PP}/V_{NN} = ±40 V, Ta = 25°C, probe load = 80 pF unless otherwise specified.

Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
Output voltage	HV_{OUT}	V	-100	-	100	
P-side drive on-resistance	R_{onP}	Ω	-	30	-	I_{DS} = 100 mA
N-side drive on-resistance	R_{onN}	Ω	-	30	-	I_{DS} = 100 mA
P-side clamp on-resistance	R_{onPCL}	Ω	-	25	-	I_{DS} = 100 mA
N-side clamp on-resistance	R_{onNCL}	Ω	-	25	-	I_{DS} = 100 mA
P-side output drive current	I_{DRVP}	A	-	0.7	-	V_{DS} = 140 V
N-side output drive current	I_{DRVN}	A	-	0.7	-	V_{DS} = 140 V
P-side GND clamp current	I_{clampP}	A	-	0.5	-	V_{DS} = 100 V
N-side GND clamp current	I_{clampN}	A	-	0.5	-	V_{DS} = 100 V
Rise time	T_r	ns	-	13	-	BIP 5 MHz 2 cycle burst, VPP/VNN = ±40 V 80 pF
Fall time	T_f	ns	-	13	-	
3LP driver propagation delay (rise)	T_{pdr}	ns	-	24	-	BIP 5 MHz 2 cycle burst, VPP/VNN = ±40 V 80 pF
3LP driver propagation delay (fall)	T_{pdf}	ns	-	24	-	
Pulse cancellation	HDPC	dBc	-	-40	-	BIP 5 MHz 2 cycle burst, VPP/VNN = ±40 V 80 pF
	HDPC2	dBc	-	-40	-	
ASW On resistance	R_{ASWON}	Ω	-	250	-	IF = 0.1 mA
TRSW On resistance	R_{TRSWON}	Ω	-	28	-	
Capacitance (TRSW On)	C_{on}	pF	-	5	-	Include LNA Cin
Capacitance (TRSW Off)	C_{off}	pF	-	62	-	
Turn on time	T_{tron}	ns	-	400	-	
Turn off time	T_{troff}	ns	-	100	-	

■ Digital Controlled Tx Pulse Width & Delay

Clock (CLKP/CLKN) frequency is 100 MHz (T_{CLK} = 10 ns) unless otherwise specified.

Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
Tx delay time resolution (ch-to-ch) = N_{DIV} x T_{CLK}/2	-	ns	5	-	-	CKDIV[1:0] = 00 N_{DIV} = 1
			10	-	-	CKDIV[1:0] = 01 N_{DIV} = 2
			15	-	-	CKDIV[1:0] = 10 N_{DIV} = 3
			20	-	-	CKDIV[1:0] = 11 N_{DIV} = 4
Common delay time = 16 x N_{DIV} x (BASE-DL + 1) x T_{CLK} BASE-DL = 0 to 255	-	µs	0.16	-	40.96	CKDIV[1:0] = 00 N_{DIV} = 1
			0.32	-	81.92	CKDIV[1:0] = 01 N_{DIV} = 2
			0.48	-	122.88	CKDIV[1:0] = 10 N_{DIV} = 3
			0.64	-	163.84	CKDIV[1:0] = 11 N_{DIV} = 4
Tx channel delay range = CHx-DL x N_{DIV} x T_{CLK}/2 CHx-DL = 0 to 2047	-	µs	0	-	10.235	CKDIV[1:0] = 00 N_{DIV} = 1
			0	-	20.47	CKDIV[1:0] = 01 N_{DIV} = 2
			0	-	30.705	CKDIV[1:0] = 10 N_{DIV} = 3
			0	-	40.94	CKDIV[1:0] = 11 N_{DIV} = 4
Pulse width with 1 Byte memory = N_{DIV} x T_{CLK}/2 x (WIDTHx + 2) WIDTHx = 0 to 63 x (= 0–127) is memory number	-	ns	10	-	325	CKDIV[1:0] = 00 N_{DIV} = 1
			20	-	650	CKDIV[1:0] = 01 N_{DIV} = 2
			30	-	975	CKDIV[1:0] = 10 N_{DIV} = 3
			40	-	1300	CKDIV[1:0] = 11 N_{DIV} = 4
Pulse width resolution = N_{DIV} x T_{CLK}/2	-	ns	5	-	-	CKDIV[1:0] = 00 N_{DIV} = 1
			10	-	-	CKDIV[1:0] = 01 N_{DIV} = 2
			15	-	-	CKDIV[1:0] = 10 N_{DIV} = 3
			20	-	-	CKDIV[1:0] = 11 N_{DIV} = 4

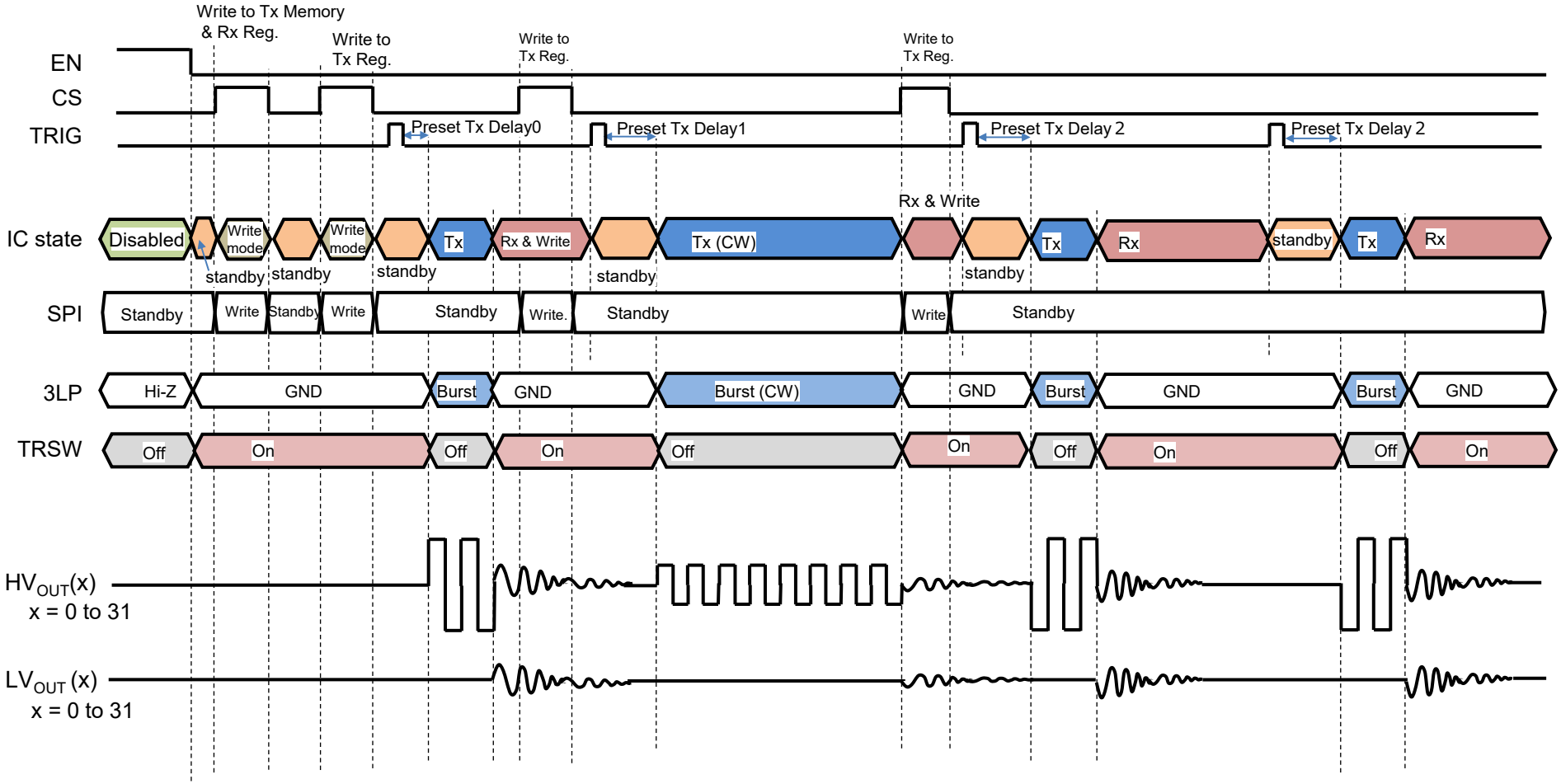
■ THP Function

Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
THP temperature threshold	T_{THP}	°C	-	110	-	THPCTL[1:0] = 00
			-	130	-	THPCTL[1:0] = 01
			-	150	-	THPCTL[1:0] = 10
			Disabled			THPCTL[1:0] = 11
THP reset hysteresis	T_{HYST}	°C	-	10	-	

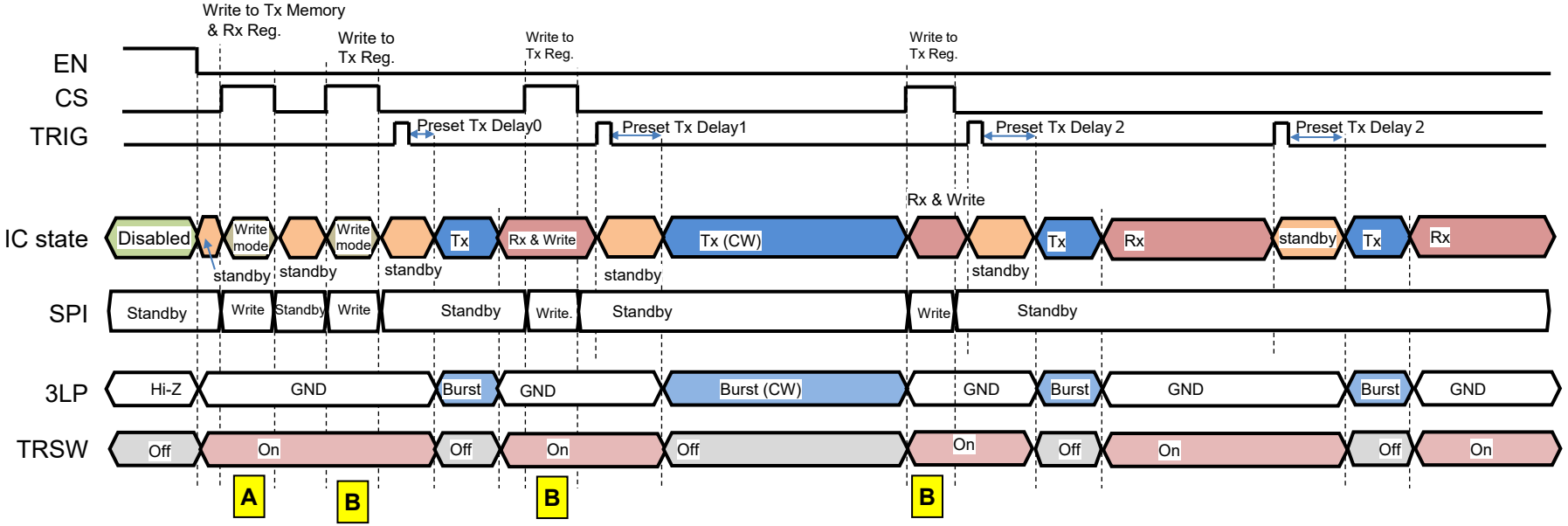
■ Memory and Control Registers

Item	Symbol	Unit	Spec			Condition
			Min.	Typ.	Max.	
Tx WFM	-	Byte	-	128	-	1-byte = 1-state = 1-level (+HV/-HV/GND/Hi-Z/Rx) + 1-width (10 to 310 ns)
Tx control register	-	Byte	-	64	-	Common: 8 Byte Channel: 56 Byte

■ Example of Tx Operating Sequence

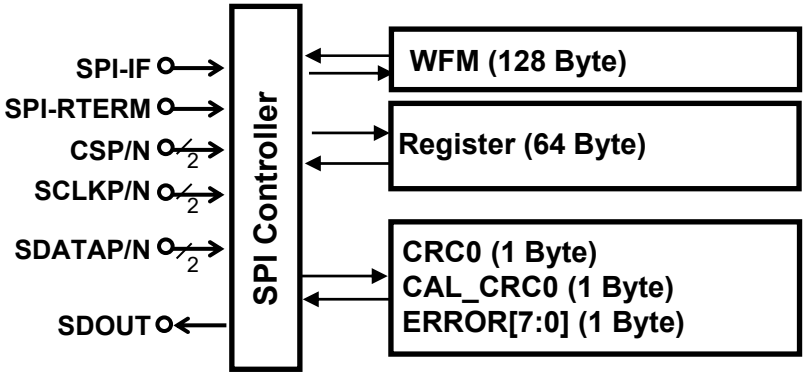


■ SPI: Write Mode Examples



A : Writing to Memory (Waveform data)

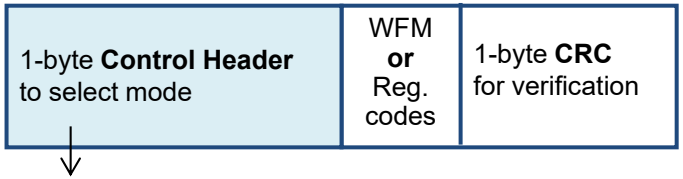
B : Writing to Registers (Tx control parameter)



■ SPI: Control Headers

✓ Each SDATA comprises a series of 1-byte Control Header, WFM or Ctrl Reg. codes, and 1-byte **CRC** code.
✓ When CS = 1 and the Control Header is set to either one of Write modes, the rest of SDATA is loaded in accordance with the operation mode.

SDATA component

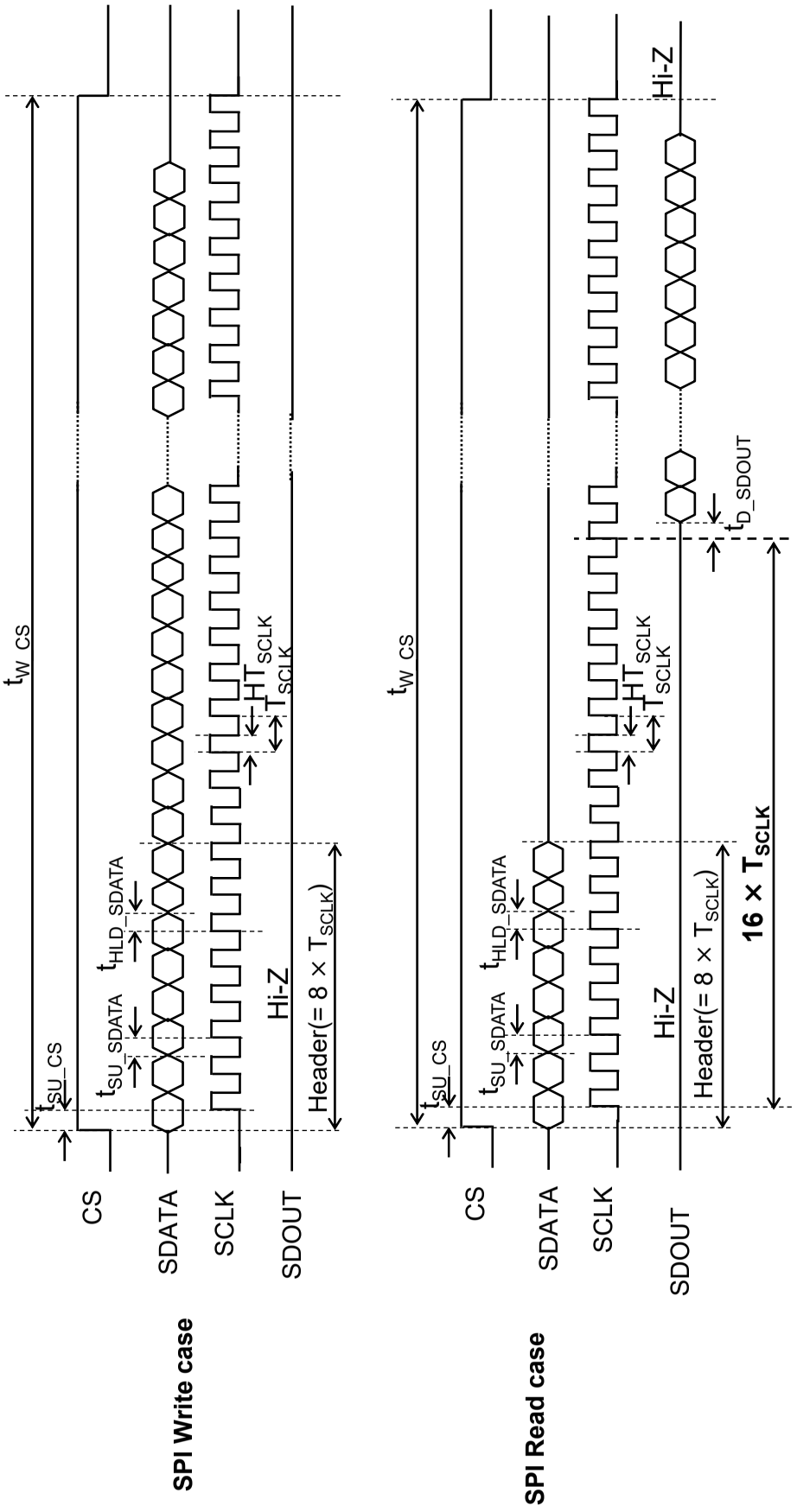


< Transfer Error checking >
Please calculate the “8 bit CRC” of transfer data include header data
with polynomial equation “$X^8 + X^5 + X^4 + 1$” and add it as “CRC[7:0]” after transfer data.
Initial value of CRC is 0000000.
Internal logic circuit also calculate the “8bit CRC”, and writes it into CAL_CRC[7:0].
If CRC[7:0] and CAL_CRC[7:0] is unmatched, ERROR[0] is set to be 1 and
FAULT pin reports the error

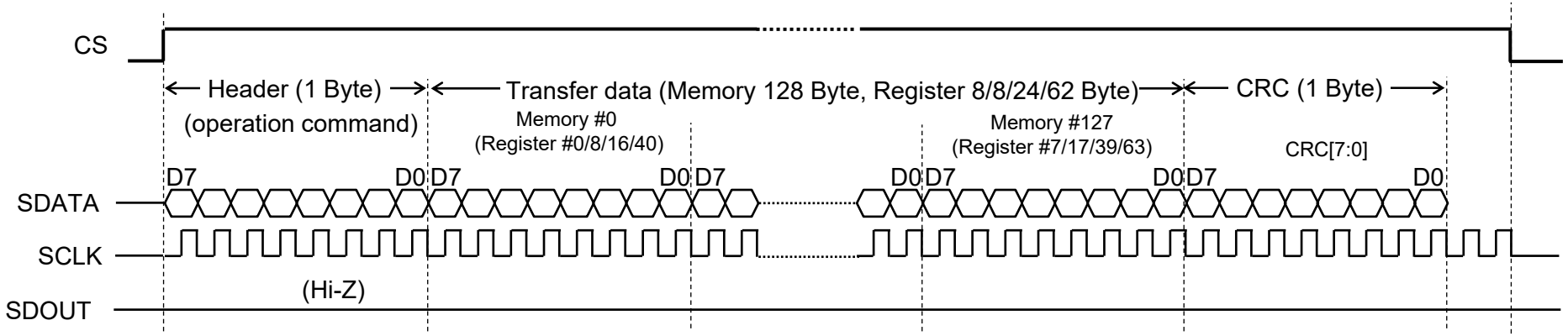
Table of SDATA Control Headers

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Operation mode
0	*	*	*	*	*	*	*	Hold previous data
1	0	0	0	0	0	0	0	Write to Waveform Memory (128 Byte) and CRC0 (1 Byte)
1	0	0	0	0	0	0	1	Write to Control all Register (64 Byte) and CRC0 (1 Byte)
1	0	0	0	0	0	1	0	Write to Control #0 to 7 Register (8 Byte) and CRC0 (1 Byte)
1	0	0	0	0	0	1	1	Write to Control #8 to 15 Register (8 Byte) CRC0 (1 Byte)
1	0	0	0	0	1	0	0	Write to Control #16 to 39 Register (24 Byte) CRC0 (1 Byte)
1	0	0	0	0	1	0	1	Write to Control #40 to 63 Register (24 Byte) CRC0 (1 Byte)
1	0	0	0	0	1	1	0	N/A
1	0	0	0	0	1	1	1	N/A
1	0	0	0	1	0	0	0	Read from Waveform Memory (128 Byte)
1	0	0	0	1	0	0	1	Read from Control all Register (64 Byte)
1	0	0	0	1	0	1	0	Read from Control #0 to 7 Register (8 Byte)
1	0	0	0	1	0	1	1	Read from Control #8 to 15 Register (8 Byte)
1	0	0	0	1	1	0	0	Read from Control #16 to 39 Register (24 Byte)
1	0	0	0	1	1	0	1	Read from Control #40 to 63 Register (24 Byte)
1	0	0	0	1	1	1	0	Read from CRC0 (1 Byte) & CAL_CRC0 (1 Byte) (for Debug)
1	0	0	0	1	1	1	1	Read from ERROR[7:0] (for Debug)
1	0	0	1	0	*	*	*	N/A (reserved for testing)
1	0	0	1	1	*	*	*	N/A (reserved for testing)
1	0	1	*	*	*	*	*	N/A
1	1	0	*	*	*	*	*	N/A
1	1	1	*	*	*	*	*	N/A

■ SPI: Timing Diagram

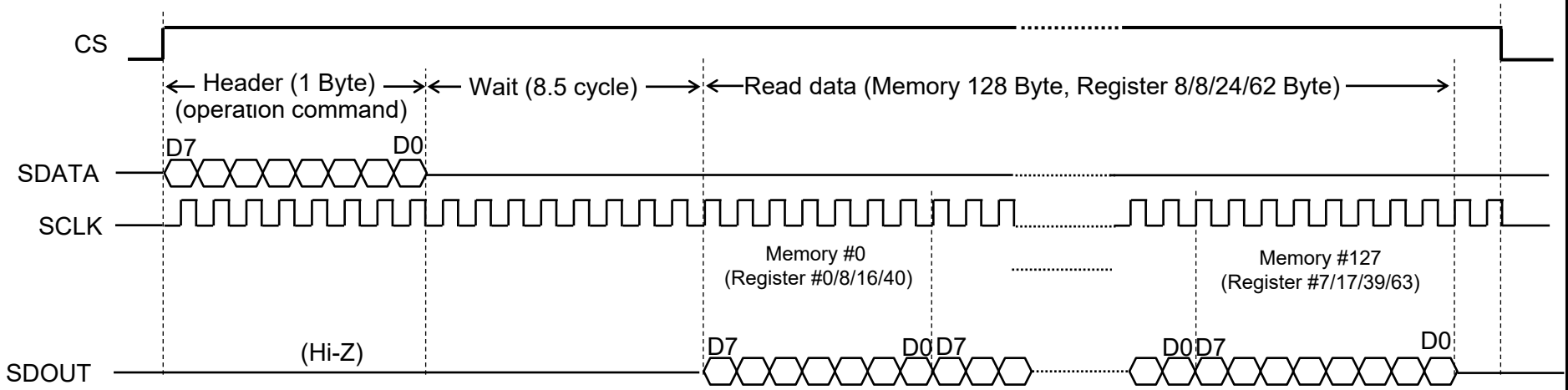


1. SPI Write to Memory or Registers Operation



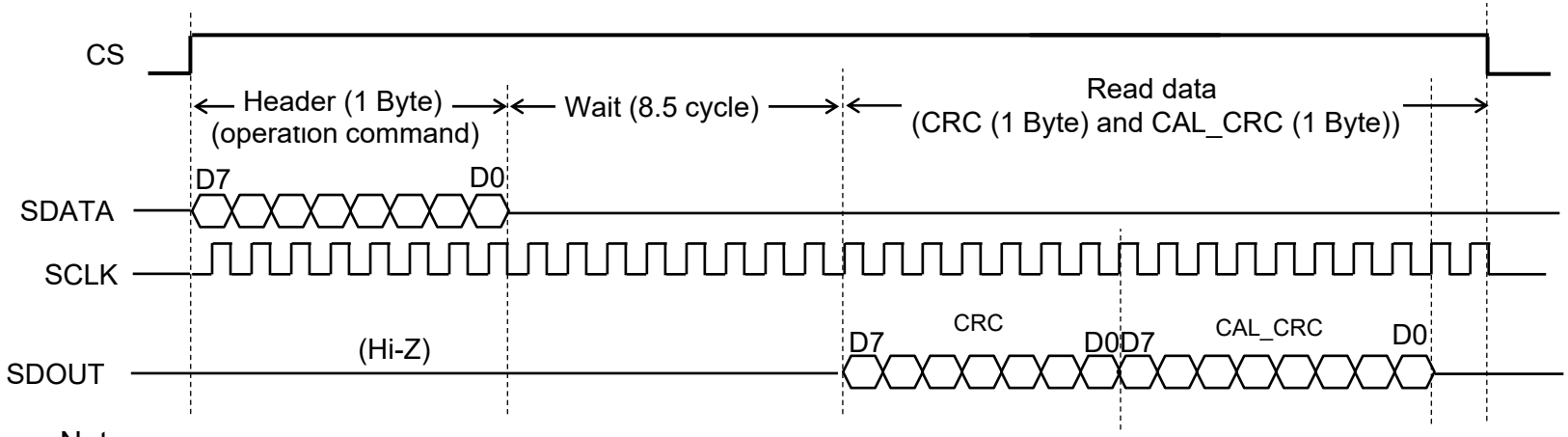
< CRC Conditions>
CRC initial value = 00000000
CRC Polynomial equation is $X^8 + X^5 + X^4 + 1$
In SPI “WRITE” operation, internal logic circuit also calculates the CRC, and writes it to internal Register CAL_CRC[7:0].
If CRC[7:0] and CAL_CRC[7:0] is unmatched, FAULT pin reports the error unless fault conditions is released.

2. SPI Read from Memory or Registers Operation



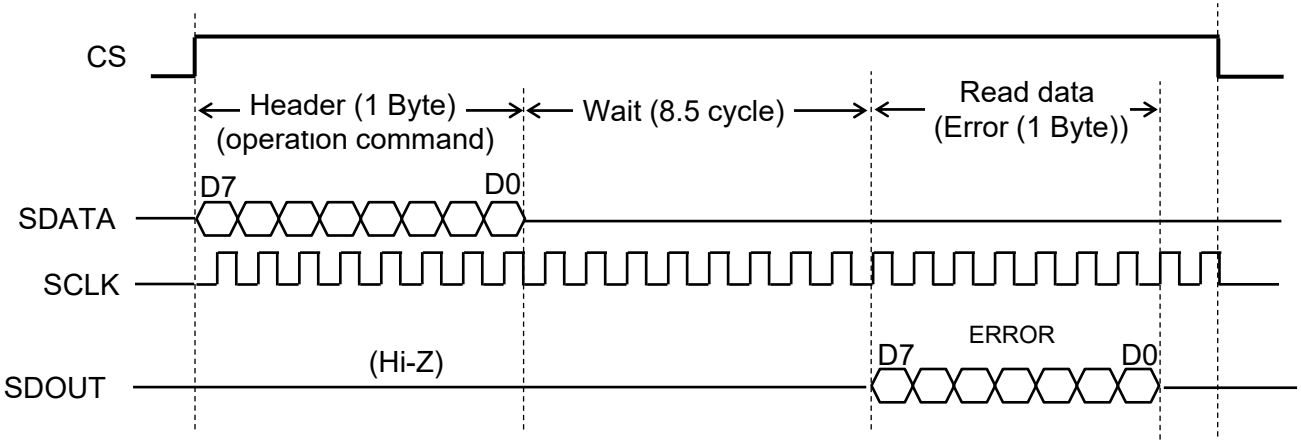
Note: In case of “READ” operation, SDATA inputs except for Header are ignored. (CRC error detection is disabled)

3. SPI Read from CRC and CAL_CRC Register



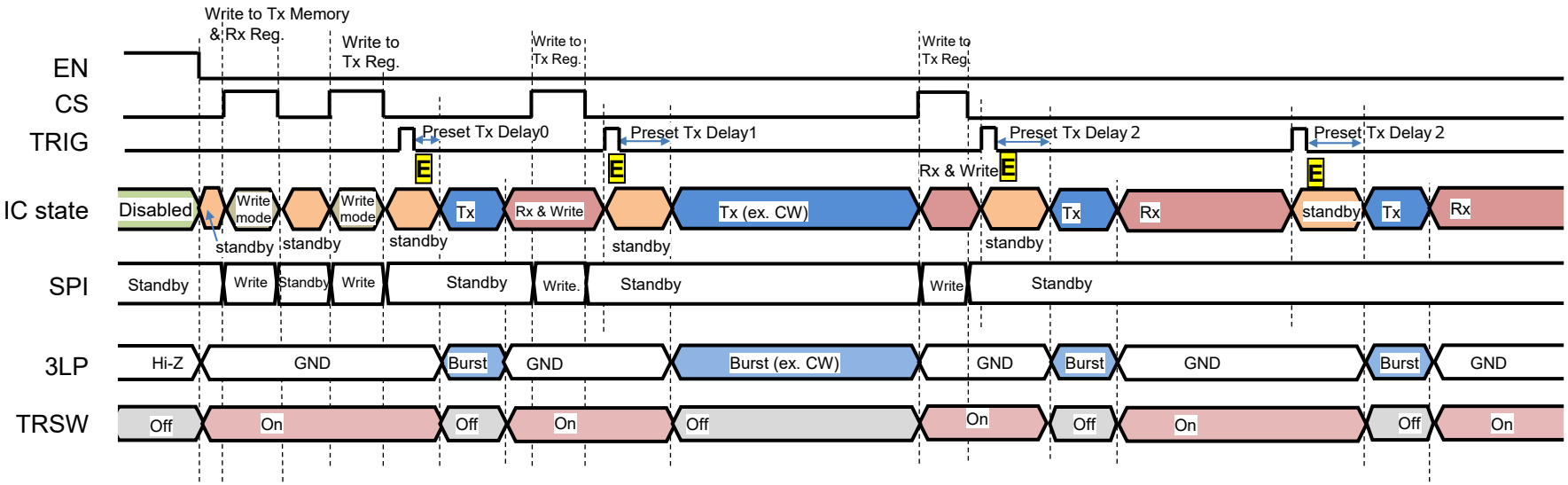
Note:
In case of “READ” operation, SDATA inputs except for Header are ignored. (CRC error detection is disabled)
Readout CRC data is the received CRC data from FPGA in previous “WRITE” operation to Memory or Register.

4. SPI Read from Error Register



Note: In case of Read, SDATA inputs except for Header are ignored. (CRC error detection is disabled)

■ Example of 3LP + TRSW Operation



E Tx starts with TRIG fall edge with preset delay time.
TRSW turns on except for Tx Burst period or IC-disabled.

Generating Tx WF Pattern

CODE_[1:0] = output state (+/-HV, GND) see Truth Table
Pulse width = 5 ns × (W_[5:0] + 2) (decimal, 10 ns to 325 ns)
START [6:0] = starting address of Waveform Memory to generate Tx burst pattern
STOP [6:0] = stopping address of Waveform Memory to generate Tx burst pattern
Repeat count(s) = 1, 1 × REPEAT[7:0], 16 × REPEAT[7:0], CW
CW mode ends with CS = 1 or TRIG = 1.

Generating Tx Delay (32ch)

CHx delay time from TRIG fall edge = BASE-DELAY + CHx-DELAY
BASE-DELAY(common) = 160 ns × (BASE-DL[7:0] + 1)
(decimal, 0.16 µs to 40.96 µs)
CHX-DELAY(/ch) = 5 ns × (CHx-DL[10:0])
(decimal, 0 to 10.235 µs)
Delay time resolution = 5 ns

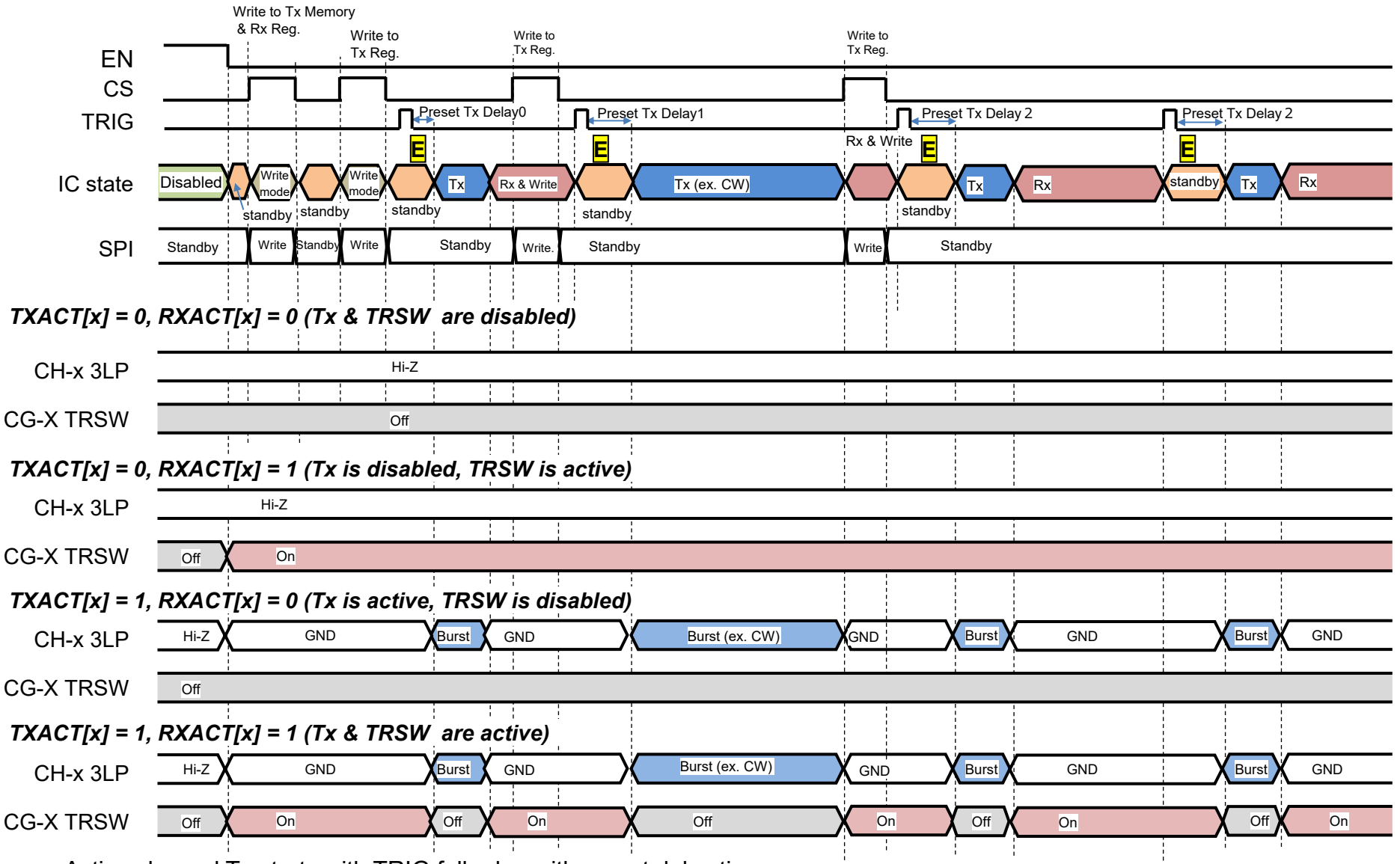
Waveform MEMORY

M#	Item	D7	D6	D5	D4	D3	D2	D1	D0
0	pulse#0	CODE0[1:0]		WIDTH0[5:0]					
1	pulse#1	CODE1[1:0]		WIDTH1[5:0]					
2	pulse#2	CODE2[1:0]		WIDTH2[5:0]					
:	:	:		:					
126	pulse#126	CODE126[1:0]		WIDTH126[5:0]					
127	pulse#127	CODE127[1:0]		WIDTH127[5:0]					

Register

R#	D7	D6	D5	D4	D3	D2	D1	D0
0	Reserved	START[6:0]						
1	Reserved	STOP[6:0]						
2	RLVO[1]	RLVO[0]	CKDIV[1:0]		INV	THPCTL[1:0]		MULRPT
3	REPEAT[7:0]							
4	BASE-DL[7:0]							
5	Reserved	Reserved	Reserved	Reserved	Reserved	VFPADJ[2:0]		
6	Reserved	Reserved	Reserved	Reserved	Reserved	VFNADJ[2:0]		
:	:	:	:	:	:	:	:	:
16	Reserved	CH0-DL[10:4]						
17	CH0-DL[3:0]				Reserved	CH1-DL[10:8]		
18	CH1-DL[7:0]							
:	:	:	:	:	:	:	:	:
60	Reserved	CH30-DL[10:4]						
62	CH30-DL[3:0]				Reserved	CH31-DL[10:8]		
63	CH31-DL[7:0]							

■ Active/Disabled channel operation

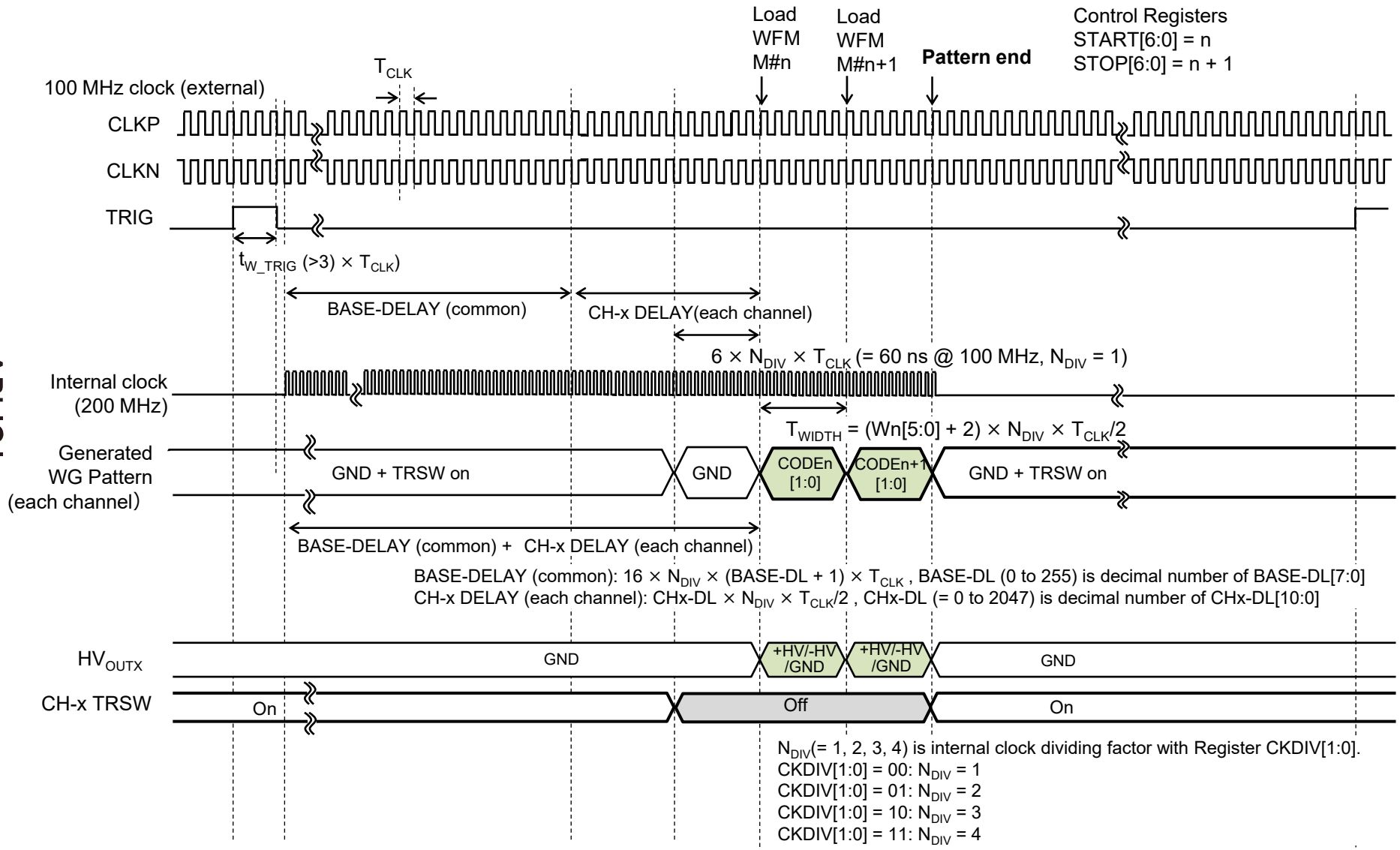


E : Active channel Tx starts with TRIG fall edge with preset delay time.
Active channel TRSW turns on except for Tx Burst period or IC-disabled.

■ Operation Truth Table

IC status		External singal			Control Register		Internal Tx-PT(x)	WFM CODE[1:0]		Control Register	WG Output		CH_x Logic Output (decoder output etc.)				CHx 3LP MOSFET/ASW/TRSW state						CHx Output state	
mode	SPI	EN	CS	TRIG	TXACT-CH[x]	RXACT-CH[x]		[1]	[0]	INV	D[1]	D[0]	TXIN[3] (GP)	TXIN[2] (GN)	TXIN[1] (GG)	TXIN[0] (GTR)	P1	N1	Pd	Nd	250 Ω ASW	TRSW	**$TXOUT_x$**	$LVOUT_x$
IC disabled	**no op.**	**1**	0	*	*	*	none	*	*	*	0	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	Hi-Z	10 kΩ
	Mem. W	**1**	**1**	*	*	*	none	*	*	*	0	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	Hi-Z	10 kΩ
Rx & SPI W/R & Tx Reset	**Memory or Register W/R**	0	**1**	*	0	0	none	*	*	*	0	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	Hi-Z	10 kΩ
		0	**1**	*	0	**1**	none	*	*	*	0	0	0	0	0	**1**	OFF	OFF	OFF	OFF	OFF	ON	Hi-Z	$HVOUT_x$
		0	**1**	*	**1**	0	none	*	*	*	0	0	0	0	**1**	0	OFF	OFF	ON	ON	ON	OFF	GND	10 kΩ
		0	**1**	*	**1**	**1**	none	*	*	*	0	0	0	0	**1**	**1**	OFF	OFF	ON	ON	ON	ON	GND	$HVOUT_x$
Rx & Tx Reset	**no op.**	0	0	**1**	0	0	none	*	*	*	0	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	Hi-Z	10 kΩ
		0	0	**1**	0	**1**	none	*	*	*	0	0	0	0	0	**1**	OFF	OFF	OFF	OFF	OFF	ON	Hi-Z	$HVOUT_x$
		0	0	**1**	**1**	0	none	*	*	*	0	0	0	0	**1**	0	OFF	OFF	ON	ON	ON	OFF	GND	10 kΩ
		0	0	**1**	**1**	**1**	none	*	*	*	0	0	0	0	**1**	**1**	OFF	OFF	ON	ON	ON	ON	GND	$HVOUT_x$
Rx	**no op.**	0	0	0	0	0	none	*	*	*	0	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	Hi-Z	10 kΩ
		0	0	0	0	**1**	none	*	*	*	0	0	0	0	0	**1**	OFF	OFF	OFF	OFF	OFF	ON	Hi-Z	$HVOUT_x$
		0	0	0	**1**	0	none	*	*	*	0	0	0	0	**1**	0	OFF	OFF	ON	ON	ON	OFF	GND	10 kΩ
		0	0	0	**1**	**1**	none	*	*	*	0	0	0	0	**1**	**1**	OFF	OFF	ON	ON	ON	ON	GND	$HVOUT_x$
Tx	**no op.**	0	0	0	**1**	*	**Gen.**	0	0	*	**1**	**1**	0	0	**1**	0	OFF	OFF	ON	ON	ON	OFF	GND	10 kΩ
		0	0	0	**1**	*	**Gen.**	0	**1**	0	0	**1**	**1**	0	0	0	ON	OFF	OFF	OFF	OFF	OFF	+HV	10 kΩ
		0	0	0	**1**	*	**Gen.**	0	**1**	**1**	**1**	0	0	**1**	0	0	OFF	ON	OFF	OFF	OFF	OFF	-HV	10 kΩ
		0	0	0	**1**	*	**Gen.**	**1**	0	0	**1**	0	0	**1**	0	0	OFF	ON	OFF	OFF	OFF	OFF	-HV	10 kΩ
		0	0	0	**1**	*	**Gen.**	**1**	0	**1**	0	**1**	**1**	0	0	0	ON	OFF	OFF	OFF	OFF	OFF	+HV	10 kΩ
		0	0	0	**1**	*	**Gen.**	**1**	**1**	*	**1**	**1**	0	0	**1**	0	N/A						N/A	

■ Tx Operation Timing Chart



■ Waveform Memory Map

Memory #	D7	D6	D5	D4	D3	D2	D1	D0
0	CODE0[1:0]		WIDTH0[5:0]					
1	CODE1[1:0]		WIDTH1[5:0]					
2	CODE2[1:0]		WIDTH2[5:0]					
3	CODE3[1:0]		WIDTH3[5:0]					
⋮	⋮		⋮					
124	CODE124[1:0]		WIDTH124[5:0]					
125	CODE125[1:0]		WIDTH125[5:0]					
126	CODE126[1:0]		WIDTH126[5:0]					
127	CODE127[1:0]		WIDTH127[5:0]					

In Memory Map, each 1-byte code consists of upper 2-bit CODEx[1:0] and lower 6-bit WIDTHx[5:0].
Suffix “x” corresponds to 1-byte Memory number (x = 0 to 127)
CODEx[1:0] stands for an output state of Tx burst as shown in Truth Table.
WIDTHx[5:0] expresses the pulse width (T_{WIDTH}) which is calculated as follows.

$$T_{WIDTH}\ [ns] = N_{DIV} \times T_{CLK}/2 \times (WIDTHx + 2)$$

Where, T_{CLK} is the CLKP/CLKN clock period, WIDTHx (= 0 to 63) is decimal number of WIDTHx[5:0] and N_{DIV} (= 1,2,3,4) is internal clock dividing factor with Register CKDIV[1:0].

In case of 100 MHz CLK,
CKDIV[1:0] = 00: N_{DIV} = 1, T_{WIDTH} [ns] is 10 ns to 325 ns (5 ns step)
CKDIV[1:0] = 01: N_{DIV} = 2, T_{WIDTH} [ns] is 20 ns to 650 ns (10 ns step)
CKDIV[1:0] = 10: N_{DIV} = 3, T_{WIDTH} [ns] is 30 ns to 975 ns (15 ns step)
CKDIV[1:0] = 11: N_{DIV} = 4, T_{WIDTH} [ns] is 40 ns to 1300 ns (20 ns step)

■ Control Register Function Table

Items	Register	Type	Function
WFM read address (start)	START[6:0]	common	Starting address of the Waveform Memory for generating the Tx waveform pattern
WFM read address (stop)	STOP[6:0]	common	Stop address of the Waveform Memory for generating the Tx waveform pattern
Tx clock dividing	CKDIV[1:0]	common	Internal clock dividing factor selection (00: 1, 01: 2, 10: 3, 11: 4)
TX waveform control	INV	common	Inversion control of generating Tx waveform pattern
THP detection control	THPCTL[1:0]	common	THP detection control (00: 110°C, 01: 130°C , 10: 150°C, 11: Disabled)
Wave generation repeat control	MUL-RPT	common	Multiplying factor selection for REPEAT[7:0] (0: 1 × REPEAT[7:0], 1: 16 × REPEAT[7:0])
	REPEAT[7:0]	common	Repeat counts control of Tx waveform pattern generation REPEAT[7:0] = 00000000: Pulse Wave Repeat counts = 1 REPEAT[7:0] = 00000001 to 11111110: Repetitive Pulse Wave Repeat counts = 1 × REPEAT[7:0] @ MUL-RPT = 0 Repeat counts = 16 × REPEAT[7:0] @ MUL-RPT = 1 REPEAT[7:0] = 11111111: Continuous Wave Tx pattern is repeated until chip disable (EN = Hi), SPI access (CSP = Hi), next trigger (TRIG = Hi) or fault detection.
Active channel control for Tx	TXACT[31:0]	/channel	Active channel control of 3LP
Active channel control for Rx	RXACT[31:0]	/channel	Active channel control of T/R-SW
TX delay control	BASE-DL[7:0]	common	Tx offset delay (common to all channel) = 160 ns × (BASE-DL + 1) BASE-DL (= 0 to 255) is decimal number of BASE-DL[7:0]
	CHx-DL[10:0]	/channel	Tx delay for channel x (x = 0 to 31) = 5 ns × CHx-DL CHx-DL (= 0 to 2047) is decimal number of CHx-DL[10:0]
Tx driver P1 current adjustment with VFP	VFPADJ[2:0]	common	VFP = 4.5 V, P1 Current = 0.648A @ 000 / VFP = 4.5 V, P1 Current = 0.648A @ 100 VFP = 4.6 V, P1 Current = 0.684A @ 001 / VFP = 4.4 V, P1 Current = 0.613A @ 101 VFP = 4.7 V, P1 Current = 0.721A @ 010 / VFP = 4.3 V, P1 Current = 0.579A @ 110 VFP = 4.8 V, P1 Current = 0.754A @ 011 / VFP = 4.2 V, P1 Current = 0.545A @ 111
Tx driver N1 current adjustment with VFN	VFNADJ[2:0]	common	VFN = 2.70 V, N1 Current = 0.673A @ 000 / VFN = 2.70 V, N1 Current = 0.673A @ 100 VFN = 2.75 V, N1 Current = 0.711A @ 001 / VFN = 2.65 V, N1 Current = 0.635A @ 101 VFN = 2.80 V, N1 Current = 0.749A @ 010 / VFN = 2.60 V, N1 Current = 0.598A @ 110 VFN = 2.85 V, N1 Current = 0.788A @ 011 / VFN = 2.55 V, N1 Current = 0.562A @ 111
Pull-down resistor at LVOUTx (x = 0 to 31)	RLVO[1:0]	common	Pull-down resistor at LVOUTx (x = 0 to 31) selection (00: Hi-Z , 01: 10 kΩ , 10: 50 kΩ, 11: 100 kΩ)

■ Control Register Map

R#	D7	D6	D5	D4	D3	D2	D1	D0
0	Reserved	START[6]	START[5]	START[4]	START[3]	START[2]	START[1]	START[0]
1	Reserved	STOP[6]	STOP[5]	STOP[4]	STOP[3]	STOP[2]	STOP[1]	STOP[0]
2	RLVO[1]	RLVO[0]	CKDIV[1]	CKDIV[0]	INV	THPCTL[1]	THPCTL[0]	MULRPT
3	REPEAT[7]	REPEAT[6]	REPEAT[5]	REPEAT[4]	REPEAT[3]	REPEAT[2]	REPEAT[1]	REPEAT[0]
4	BASEDL[7]	BASEDL[6]	BASEDL[5]	BASEDL[4]	BASEDL[3]	BASEDL[2]	BASEDL[1]	BASEDL[0]
5	Reserved	Reserved	Reserved	Reserved	Reserved	VFPADJ[2]	VFPADJ[1]	VFPADJ[0]
6	Reserved	Reserved	Reserved	Reserved	Reserved	VFNADJ[2]	VFNADJ[1]	VFNADJ[0]
7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
8	RXACT0	RXACT1	RXACT2	RXACT3	RXACT4	RXACT5	RXACT6	RXACT7
9	RXACT8	RXACT9	RXACT10	RXACT11	RXACT12	RXACT13	RXACT14	RXACT15
10	RXACT16	RXACT17	RXACT18	RXACT19	RXACT20	RXACT21	RXACT22	RXACT23
11	RXACT24	RXACT25	RXACT26	RXACT27	RXACT28	RXACT29	RXACT30	RXACT31
12	TXACT0	TXACT1	TXACT2	TXACT3	TXACT4	TXACT5	TXACT6	TXACT7
13	TXACT8	TXACT9	TXACT10	TXACT11	TXACT12	TXACT13	TXACT14	TXACT15
14	TXACT16	TXACT17	TXACT18	TXACT19	TXACT20	TXACT21	TXACT22	TXACT23
15	TXACT24	TXACT25	TXACT26	TXACT27	TXACT28	TXACT29	TXACT30	TXACT31
16	Reserved	CH0DL[10]	CH0DL[9]	CH0DL[8]	CH0DL[7]	CH0DL[6]	CH0DL[5]	CH0DL[4]
17	CH0DL[3]	CH0DL[2]	CH0DL[1]	CH0DL[0]	Reserved	CH1DL[10]	CH1DL[9]	CH1DL[8]
18	CH1DL[7]	CH1DL[6]	CH1DL[5]	CH1DL[4]	CH1DL[3]	CH1DL[2]	CH1DL[1]	CH1DL[0]
19	Reserved	CH2DL[10]	CH2DL[9]	CH2DL[8]	CH2DL[7]	CH2DL[6]	CH2DL[5]	CH2DL[4]
20	CH2DL[3]	CH2DL[2]	CH2DL[1]	CH2DL[0]	Reserved	CH3DL[10]	CH3DL[9]	CH3DL[8]
21	CH3DL[7]	CH3DL[6]	CH3DL[5]	CH3DL[4]	CH3DL[3]	CH3DL[2]	CH3DL[1]	CH3DL[0]
22	Reserved	CH4DL[10]	CH4DL[9]	CH4DL[8]	CH4DL[7]	CH4DL[6]	CH4DL[5]	CH4DL[4]
23	CH4DL[3]	CH4DL[2]	CH4DL[1]	CH4DL[0]	Reserved	CH5DL[10]	CH5DL[9]	CH5DL[8]
24	CH5DL[7]	CH5DL[6]	CH5DL[5]	CH5DL[4]	CH5DL[3]	CH5DL[2]	CH5DL[1]	CH5DL[0]
25	Reserved	CH6DL[10]	CH6DL[9]	CH6DL[8]	CH6DL[7]	CH6DL[6]	CH6DL[5]	CH6DL[4]
26	CH6DL[3]	CH6DL[2]	CH6DL[1]	CH6DL[0]	Reserved	CH7DL[10]	CH7DL[9]	CH7DL[8]
27	CH7DL[7]	CH7DL[6]	CH7DL[5]	CH7DL[4]	CH7DL[3]	CH7DL[2]	CH7DL[1]	CH7DL[0]
28	Reserved	CH8DL[10]	CH8DL[9]	CH8DL[8]	CH8DL[7]	CH8DL[6]	CH8DL[5]	CH8DL[4]
29	CH8DL[3]	CH8DL[2]	CH8DL[1]	CH8DL[0]	Reserved	CH9DL[10]	CH9DL[9]	CH9DL[8]
30	CH9DL[7]	CH9DL[6]	CH9DL[5]	CH9DL[4]	CH9DL[3]	CH9DL[2]	CH9DL[1]	CH9DL[0]
31	CH10DL[11]	CH10DL[10]	CH10DL[9]	CH10DL[8]	CH10DL[7]	CH10DL[6]	CH10DL[5]	CH10DL[4]
32	CH10DL[3]	CH10DL[2]	CH10DL[1]	CH10DL[0]	CH11DL[11]	CH11DL[10]	CH11DL[9]	CH11DL[8]
33	CH11DL[7]	CH11DL[6]	CH11DL[5]	CH11DL[4]	CH11DL[3]	CH11DL[2]	CH11DL[1]	CH11DL[0]
34	CH12DL[11]	CH12DL[10]	CH12DL[9]	CH12DL[8]	CH12DL[7]	CH12DL[6]	CH12DL[5]	CH12DL[4]
35	CH12DL[3]	CH12DL[2]	CH12DL[1]	CH12DL[0]	CH13DL[11]	CH13DL[10]	CH13DL[9]	CH13DL[8]
36	CH13DL[7]	CH13DL[6]	CH13DL[5]	CH13DL[4]	CH13DL[3]	CH13DL[2]	CH13DL[1]	CH13DL[0]
37	CH14DL[11]	CH14DL[10]	CH14DL[9]	CH14DL[8]	CH14DL[7]	CH14DL[6]	CH14DL[5]	CH14DL[4]
38	CH14DL[3]	CH14DL[2]	CH14DL[1]	CH14DL[0]	CH15DL[11]	CH15DL[10]	CH15DL[9]	CH15DL[8]
39	CH15DL[7]	CH15DL[6]	CH15DL[5]	CH15DL[4]	CH15DL[3]	CH15DL[2]	CH15DL[1]	CH15DL[0]
40	CH16DL[11]	CH16DL[10]	CH16DL[9]	CH16DL[8]	CH16DL[7]	CH16DL[6]	CH16DL[5]	CH16DL[4]
41	CH16DL[3]	CH16DL[2]	CH16DL[1]	CH16DL[0]	CH17DL[11]	CH17DL[10]	CH17DL[9]	CH17DL[8]
42	CH17DL[7]	CH17DL[6]	CH17DL[5]	CH17DL[4]	CH17DL[3]	CH17DL[2]	CH17DL[1]	CH17DL[0]
43	CH18DL[11]	CH18DL[10]	CH18DL[9]	CH18DL[8]	CH18DL[7]	CH18DL[6]	CH18DL[5]	CH18DL[4]
44	CH18DL[3]	CH18DL[2]	CH18DL[1]	CH18DL[0]	CH19DL[11]	CH19DL[10]	CH19DL[9]	CH19DL[8]
45	CH19DL[7]	CH19DL[6]	CH19DL[5]	CH19DL[4]	CH19DL[3]	CH19DL[2]	CH19DL[1]	CH19DL[0]
46	CH20DL[11]	CH20DL[10]	CH20DL[9]	CH20DL[8]	CH20DL[7]	CH20DL[6]	CH20DL[5]	CH20DL[4]
47	CH20DL[3]	CH20DL[2]	CH20DL[1]	CH20DL[0]	CH21DL[11]	CH21DL[10]	CH21DL[9]	CH21DL[8]
48	CH21DL[7]	CH21DL[6]	CH21DL[5]	CH21DL[4]	CH21DL[3]	CH21DL[2]	CH21DL[1]	CH21DL[0]
49	CH22DL[11]	CH22DL[10]	CH22DL[9]	CH22DL[8]	CH22DL[7]	CH22DL[6]	CH22DL[5]	CH22DL[4]
50	CH22DL[3]	CH22DL[2]	CH22DL[1]	CH22DL[0]	CH23DL[11]	CH23DL[10]	CH23DL[9]	CH23DL[8]
51	CH23DL[7]	CH23DL[6]	CH23DL[5]	CH23DL[4]	CH23DL[3]	CH23DL[2]	CH23DL[1]	CH23DL[0]
52	CH24DL[11]	CH24DL[10]	CH24DL[9]	CH24DL[8]	CH24DL[7]	CH24DL[6]	CH24DL[5]	CH24DL[4]
53	CH24DL[3]	CH24DL[2]	CH24DL[1]	CH24DL[0]	CH25DL[11]	CH25DL[10]	CH25DL[9]	CH25DL[8]
54	CH25DL[7]	CH25DL[6]	CH25DL[5]	CH25DL[4]	CH25DL[3]	CH25DL[2]	CH25DL[1]	CH25DL[0]
55	CH26DL[11]	CH26DL[10]	CH26DL[9]	CH26DL[8]	CH26DL[7]	CH26DL[6]	CH26DL[5]	CH26DL[4]
56	CH26DL[3]	CH26DL[2]	CH26DL[1]	CH26DL[0]	CH27DL[11]	CH27DL[10]	CH27DL[9]	CH27DL[8]
57	CH27DL[7]	CH27DL[6]	CH27DL[5]	CH27DL[4]	CH27DL[3]	CH27DL[2]	CH27DL[1]	CH27DL[0]
58	CH28DL[11]	CH28DL[10]	CH28DL[9]	CH28DL[8]	CH28DL[7]	CH28DL[6]	CH28DL[5]	CH28DL[4]
59	CH28DL[3]	CH28DL[2]	CH28DL[1]	CH28DL[0]	CH29DL[11]	CH29DL[10]	CH29DL[9]	CH29DL[8]
60	CH29DL[7]	CH29DL[6]	CH29DL[5]	CH29DL[4]	CH29DL[3]	CH29DL[2]	CH29DL[1]	CH29DL[0]
61	CH30DL[11]	CH30DL[10]	CH30DL[9]	CH30DL[8]	CH30DL[7]	CH30DL[6]	CH30DL[5]	CH30DL[4]
62	CH30DL[3]	CH30DL[2]	CH30DL[1]	CH30DL[0]	CH31DL[11]	CH31DL[10]	CH31DL[9]	CH31DL[8]
63	CH31DL[7]	CH31DL[6]	CH31DL[5]	CH31DL[4]	CH31DL[3]	CH31DL[2]	CH31DL[1]	CH31DL[0]

: Re-latched parameter with TRIG rise edge

■ CRC & Error Register

1. CRC, Calculated CRC and ERROR Register MAP

Register	D7	D6	D5	D4	D3	D2	D1	D0
CRC0	CRC[7:0]							
Calculated CRC0	CAL_CRC0[7:0]							
Error	ERROR[7:0]							

2. CRC, Calculated CRC and ERROR Register function

CRC[7:0]	Transferred CRCx data in SDATA CRC initial value = 00000000 CRC polynomial equation is $X^8 + X^5 + X^4 + 1$
CAL_CRC[7:0]	Calculated CRC values with transferred SDATA signal.
ERROR[7:0]	When Error has occurred, ERROR register corresponding to error type is set to be “1”. ERROR[7]: N/A ERROR[6]: SPI transfer error (CRC un-match) has occurred in SDATA “Register #40 to 63 Write” ERROR[5]: SPI transfer error (CRC un-match) has occurred in SDATA “Register #16 to 39 Write” ERROR[4]: SPI transfer error (CRC un-match) has occurred in SDATA “Register #8 to 15 Write” ERROR[3]: SPI transfer error (CRC un-match) has occurred in SDATA “Register #0 to 7 Write” ERROR[2]: SPI transfer error (CRC un-match) has occurred in SDATA “Memory Write” ERROR[1]: threshold over of the junction temperature set in advance ERROR[0]: start and stop address for Tx waveform pattern generation are same.

Note:
Error[7:0] are cleared when IC is powered on, data is re-transferred normally or “EN” becomes from “high” to “low” (fall edge) except for Error[2].
Error[2] is cleared when IC is powered on or data is re-transferred normally.

■ Pin Configuration (Table)

NO.	Pin Name	NO.	Pin Name	NO.	Pin Name	NO.	Pin Name	NO.	Pin Name	NO.	Pin Name	NO.	Pin Name	NO.	Pin Name	NO.	Pin Name	NO.	Pin Name
A1	NC	C1	HVOUT0	E1	HVOUT2	G1	HVOUT4	J1	HVOUT6	L1	HVOUT9	N1	HVOUT11	Q1	HVOUT13	S1	HVOUT15	U1	NC
A2	LVOUT0	C2	VFP	E2	VNN	G2	VPP	J2	HGND	L2	HGND	N2	VNN	Q2	VPP	S2	VFN	U2	LVOUT15
A3	LVOUT2	C3	HGND	E3	HGND	G3	HGND	J3	HGND	L3	HGND	N3	HGND	Q3	HGND	S3	HGND	U3	LVOUT13
A4	LVOUT4	C4	GND	-	-	-	-	-	-	-	-	-	-	-	-	S4	GND	U4	LVOUT11
A5	LVOUT6	C5	GND	E5	GND(T)	G5	GND(T)	J5	GND(T)	L5	GND(T)	N5	GND(T)	Q5	GND(T)	S5	GND	U5	LVOUT9
A6	VDD	C6	GND	E6	GND(T)	G6	GND(T)	J6	GND(T)	L6	GND(T)	N6	GND(T)	Q6	GND(T)	S6	GND	U6	VDD
A7	VLLIO	C7	GND	E7	GND(T)	G7	GND(T)	J7	GND(T)	L7	GND(T)	N7	GND(T)	Q7	GND(T)	S7	GND	U7	SPI_IF
A8	VLL	C8	GND	E8	GND(T)	G8	GND(T)	J8	GND(T)	L8	GND(T)	N8	GND(T)	Q8	GND(T)	S8	GND	U8	CSP
A9	TRIG	C9	GND	E9	GND(T)	G9	GND(T)	J9	GND(T)	L9	GND(T)	N9	GND(T)	Q9	GND(T)	S9	GND	U9	SCLKP
A10	CLKP	C10	GND	E10	GND(T)	G10	GND(T)	J10	GND(T)	L10	GND(T)	N10	GND(T)	Q10	GND(T)	S10	GND	U10	SDATAP
A11	EN	C11	GND	E11	GND(T)	G11	GND(T)	J11	GND(T)	L11	GND(T)	N11	GND(T)	Q11	GND(T)	S11	GND	U11	SDOUT
A12	GND	C12	GND	E12	GND(T)	G12	GND(T)	J12	GND(T)	L12	GND(T)	N12	GND(T)	Q12	GND(T)	S12	GND	U12	VLL
A13	GND	C13	GND	E13	GND(T)	G13	GND(T)	J13	GND(T)	L13	GND(T)	N13	GND(T)	Q13	GND(T)	S13	GND	U13	VLLIO
A14	VDD	C14	GND	E14	GND(T)	G14	GND(T)	J14	GND(T)	L14	GND(T)	N14	GND(T)	Q14	GND(T)	S14	GND	U14	VDD
A15	LVOUT25	C15	GND	E15	GND(T)	G15	GND(T)	J15	GND(T)	L15	GND(T)	N15	GND(T)	Q15	GND(T)	S15	GND	U15	LVOUT22
A16	LVOUT27	C16	GND													S16	GND	U16	LVOUT20
A17	LVOUT29	C17	HGND	E17	HGND	G17	HGND	J17	HGND	L17	HGND	N17	HGND	Q17	HGND	S17	HGND	U17	LVOUT18
A18	LVOUT31	C18	VFP	E18	VNN	G18	VPP	J18	HGND	L18	HGND	N18	VNN	Q18	VPP	S18	VFN	U18	LVOUT16
A19	NC	C19	HVOUT31	E19	HVOUT29	G19	HVOUT27	J19	HVOUT25	L19	HVOUT22	N19	HVOUT20	Q19	HVOUT18	S19	HVOUT16	U19	NC
B1	VFN	D1	VPP	F1	VNN_HWC	H1	VNN	K1	HVOUT7	M1	VPP	P1	VPP_NBUR	R1	VNN	T1	VFP		
B2	HGND	D2	HVOUT1	F2	HVOUT3	H2	HVOUT5	K2	HVOUT8	M2	HVOUT10	P2	HVOUT12	R2	HVOUT14	T2	HGND		
B3	LVOUT1	D3	HGND	F3	HGND	H3	HGND	K3	HGND	M3	HGND	P3	HGND	R3	HGND	T3	LVOUT14		
B4	LVOUT3	D4	NC(index)	-	-	-	-	-	-	-	-	-	-	-	-	T4	LVOUT12		
B5	LVOUT5	-	-	F5	GND(T)	H5	GND(T)	K5	GND(T)	M5	GND(T)	P5	GND(T)	-	-	T5	LVOUT10		
B6	LVOUT7	-	-	F6	GND(T)	H6	GND(T)	K6	GND(T)	M6	GND(T)	P6	GND(T)	-	-	T6	LVOUT8		
B7	VSS	-	-	F7	GND(T)	H7	GND(T)	K7	GND(T)	M7	GND(T)	P7	GND(T)	-	-	T7	VSS		
B8	GND	-	-	F8	GND(T)	H8	GND(T)	K8	GND(T)	M8	GND(T)	P8	GND(T)	-	-	T8	SPI_RTERM		
B9	CLK_RTERM	-	-	F9	GND(T)	H9	GND(T)	K9	GND(T)	M9	GND(T)	P9	GND(T)	-	-	T9	CSN		
B10	CLKN	-	-	F10	GND(T)	H10	GND(T)	K10	GND(T)	M10	GND(T)	P10	GND(T)	-	-	T10	SCLKN		
B11	FAULT	-	-	F11	GND(T)	H11	GND(T)	K11	GND(T)	M11	GND(T)	P11	GND(T)	-	-	T11	SDATAN		
B12	GND	-	-	F12	GND(T)	H12	GND(T)	K12	GND(T)	M12	GND(T)	P12	GND(T)	-	-	T12	GND		
B13	VSS	-	-	F13	GND(T)	H13	GND(T)	K13	GND(T)	M13	GND(T)	P13	GND(T)	-	-	T13	VSS		
B14	LVOUT24	-	-	F14	GND(T)	H14	GND(T)	K14	GND(T)	M14	GND(T)	P14	GND(T)	-	-	T14	LVOUT23		
B15	LVOUT26	-	-	F15	GND(T)	H15	GND(T)	K15	GND(T)	M15	GND(T)	P15	GND(T)	-	-	T15	LVOUT21		
B16	LVOUT28	-	-	-	-	-	-	-	-	-	-	-	-	-	-	T16	LVOUT19		
B17	LVOUT30	D17	HGND	F17	HGND	H17	HGND	K17	HGND	M17	HGND	P17	HGND	R17	HGND	T17	LVOUT17		
B18	HGND	D18	HVOUT30	F18	HVOUT28	H18	HVOUT26	K18	HVOUT24	M18	HVOUT21	P18	HVOUT19	R18	HVOUT17	T18	HGND		
B19	VFN	D19	VPP	F19	VNN_HWC	H19	VNN	K19	HVOUT23	M19	VPP	P19	VPP_NBUR	R19	VNN	T19	VFP		

■ Pin Configuration (Map)

TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U
1	NC	VFN	HVOUT 0	VPP	HVOUT 2	VNN_ HWC	HVOUT 4	VNN	HVOUT 6	HVOUT 7	HVOUT 9	VPP	HVOUT 11	VPP _NBUR	HVOUT 13	VNN	HVOUT 15	VFP	NC
2	LVOUT 0	HGND	VFP	HVOUT 1	VNN	HVOUT 3	VPP	HVOUT 5	HGND	HVOUT 8	HGND	HVOUT 10	VNN	HVOUT 12	VPP	HVOUT 14	VFN	HGND	LVOUT 15
3	LVOUT 2	LVOUT 1	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	LVOUT 14	LVOUT 13
4	LVOUT 4	LVOUT 3	GND	NC (index)													GND	LVOUT 12	LVOUT 11
5	LVOUT 6	LVOUT 5	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	LVOUT 10	LVOUT 9
6	VDD	LVOUT 7	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	LVOUT 8	VDD
7	VLLIO	VSS	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	VSS	SPI_IF
8	VLL	GND	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	SPI_ RTERM	CSP
9	TRIG	CLK_ RTERM	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	CSN	SCLKP
10	CLKP	CLKN	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	SCLKN	SDATAP
11	EN	FAULT	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	SDATAN	SDOUT
12	GND	GND	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	GND	VLL
13	GND	VSS	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	VSS	VLLIO
14	VDD	LVOUT 24	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	LVOUT 23	VDD
15	LVOUT 25	LVOUT 26	GND		GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)		GND	LVOUT 21	LVOUT 22
16	LVOUT 27	LVOUT 28	GND														GND	LVOUT 19	LVOUT 20
17	LVOUT 29	LVOUT 30	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	HGND	LVOUT 17	LVOUT 18
18	LVOUT 31	HGND	VFP	HVOUT 30	VNN	HVOUT 28	VPP	HVOUT 26	HGND	HVOUT 24	HGND	HVOUT 21	VNN	HVOUT 19	VPP	HVOUT 17	VFN	HGND	LVOUT 16
19	NC	VFN	HVOUT 31	VPP	HVOUT 29	VNN_ HWC	HVOUT 27	VNN	HVOUT 25	HVOUT 23	HVOUT 22	VPP	HVOUT 20	VPP_ NBUR	HVOUT 18	VNN	HVOUT 16	VFP	NC

■ Pin Function

Pin Name	Function	Pin Name	Function	Pin Name	Function	Pin Name	Function
VPP_NBUR	Positive high voltage for protection (0 to +100 V) (highest voltage in the IC power supplies)	VLLIO	Positive low voltage power supply for Logic I/F (+1.8 to 3.3 V)	CLKP	Positive LVDS clock input	CSP	Positive SPI Chip Select signal (LVDS/CMOS)
VPP	Positive high voltage power supply (0 to +100 V)	VLL	Positive low voltage power supply for Logic (+1.8 V)	CLKN	Negative LVDS clock Input	CSN	Negative SPI Chip Select signal (LVDS/CMOS)
VFP	Built-in power supply for P-MOS (P1) gate drive	VDD	Positive low voltage power supply for Tx Circuit (+5 V)	TRIG	Tx Trigger singal (CMOS)	SCLKP	Positive SPI clock signal (LVDS/CMOS)
VNN	Negative high voltage power supply (0 to -100 V)	VSS	Negative low voltage power supply for Tx Circuit (-5 V)	CLK RTERM	Clock Termination Resister On/Off control (H: Off (default), L: On)	SCLKN	Negative SPI clock signal (LVDS/CMOS)
VFN	Built-in power supply for N-MOS (N1) gate drive	GND	Ground for low voltage circuit	SPI_RTERM	SPI Termination Resister On/Off control (H: Off (default), L: On)	SDATAP	Positive SPI serial input data 0 for Memory and Reg#0 (LVDS/CMOS)
VNN_HWC	Negative high voltage for protection (0 to -100 V) (lowest voltage in the IC power supplies)	GND(T)	Ground for Thermal heat sink	SPI_IF	I/F selection for SPI (H: CMOS (default), L: LVDS)	SDATAN	Negative SPI serial input data 0 for Memory and Reg#0 (LVDS/CMOS)
HGND	Drive power ground (0 V)	EN	IC Enable/Disable control (H: Disabled (default), L: Enable)	FAULT	Fault output flag, Open N-MOS Drain (H: Normal, L: Fault)	SDOUT	SPI serial output data (tri-state)
HVOUT0	High voltage output of channel 0	HVOUT16	High voltage output of channel 16	LVOUT0	Low voltage output of channel 0	LVOUT16	Low voltage output of channel 16
HVOUT1	High voltage output of channel 1	HVOUT17	High voltage output of channel 17	LVOUT1	Low voltage output of channel 1	LVOUT17	Low voltage output of channel 17
HVOUT2	High voltage output of channel 2	HVOUT18	High voltage output of channel 18	LVOUT2	Low voltage output of channel 2	LVOUT18	Low voltage output of channel 18
HVOUT3	High voltage output of channel 3	HVOUT19	High voltage output of channel 19	LVOUT3	Low voltage output of channel 3	LVOUT19	Low voltage output of channel 19
HVOUT4	High voltage output of channel 4	HVOUT20	High voltage output of channel 20	LVOUT4	Low voltage output of channel 4	LVOUT20	Low voltage output of channel 20
HVOUT5	High voltage output of channel 5	HVOUT21	High voltage output of channel 21	LVOUT5	Low voltage output of channel 5	LVOUT21	Low voltage output of channel 21
HVOUT6	High voltage output of channel 6	HVOUT22	High voltage output of channel 22	LVOUT6	Low voltage output of channel 6	LVOUT22	Low voltage output of channel 22
HVOUT7	High voltage output of channel 7	HVOUT23	High voltage output of channel 23	LVOUT7	Low voltage output of channel 7	LVOUT23	Low voltage output of channel 23
HVOUT8	High voltage output of channel 8	HVOUT24	High voltage output of channel 24	LVOUT8	Low voltage output of channel 8	LVOUT24	Low voltage output of channel 24
HVOUT9	High voltage output of channel 9	HVOUT25	High voltage output of channel 25	LVOUT9	Low voltage output of channel 9	LVOUT25	Low voltage output of channel 25
HVOUT10	High voltage output of channel 10	HVOUT26	High voltage output of channel 26	LVOUT10	Low voltage output of channel 10	LVOUT26	Low voltage output of channel 26
HVOUT11	High voltage output of channel 11	HVOUT27	High voltage output of channel 27	LVOUT11	Low voltage output of channel 11	LVOUT27	Low voltage output of channel 27
HVOUT12	High voltage output of channel 12	HVOUT28	High voltage output of channel 28	LVOUT12	Low voltage output of channel 12	LVOUT28	Low voltage output of channel 28
HVOUT13	High voltage output of channel 13	HVOUT29	High voltage output of channel 29	LVOUT13	Low voltage output of channel 13	LVOUT29	Low voltage output of channel 29
HVOUT14	High voltage output of channel 14	HVOUT30	High voltage output of channel 30	LVOUT14	Low voltage output of channel 14	LVOUT30	Low voltage output of channel 30
HVOUT15	High voltage output of channel 15	HVOUT31	High voltage output of channel 31	LVOUT15	Low voltage output of channel 15	LVOUT31	Low voltage output of channel 31

■ Package

Package Name	Dimension	Tray	Marking	Land	Packing
BGA-314(1313)A	RA314-A-P-S1	RA314-A-T-SD	RA314-A-M-SD	RA314-A-L-SD	RA314-A-K-SD

■ Storage, Mounting

1. Storage conditions

1. 1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Figure 1 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

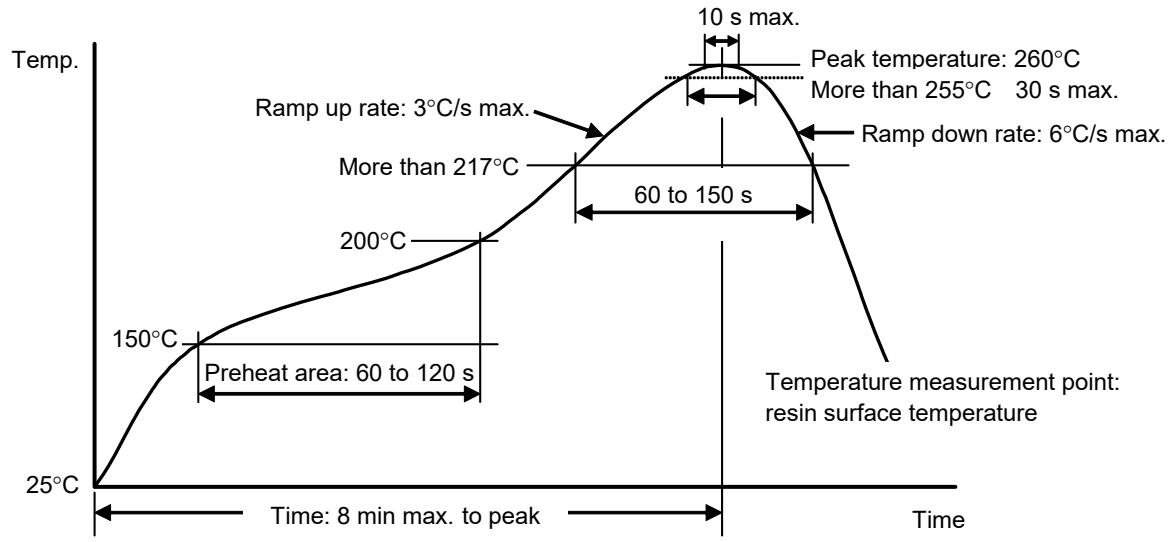


Figure 1 Resistance to Soldering Heat Condition for Package (Reflow Method)

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■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.

1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1. 4 Prevent friction with other materials made with high polymer.

1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

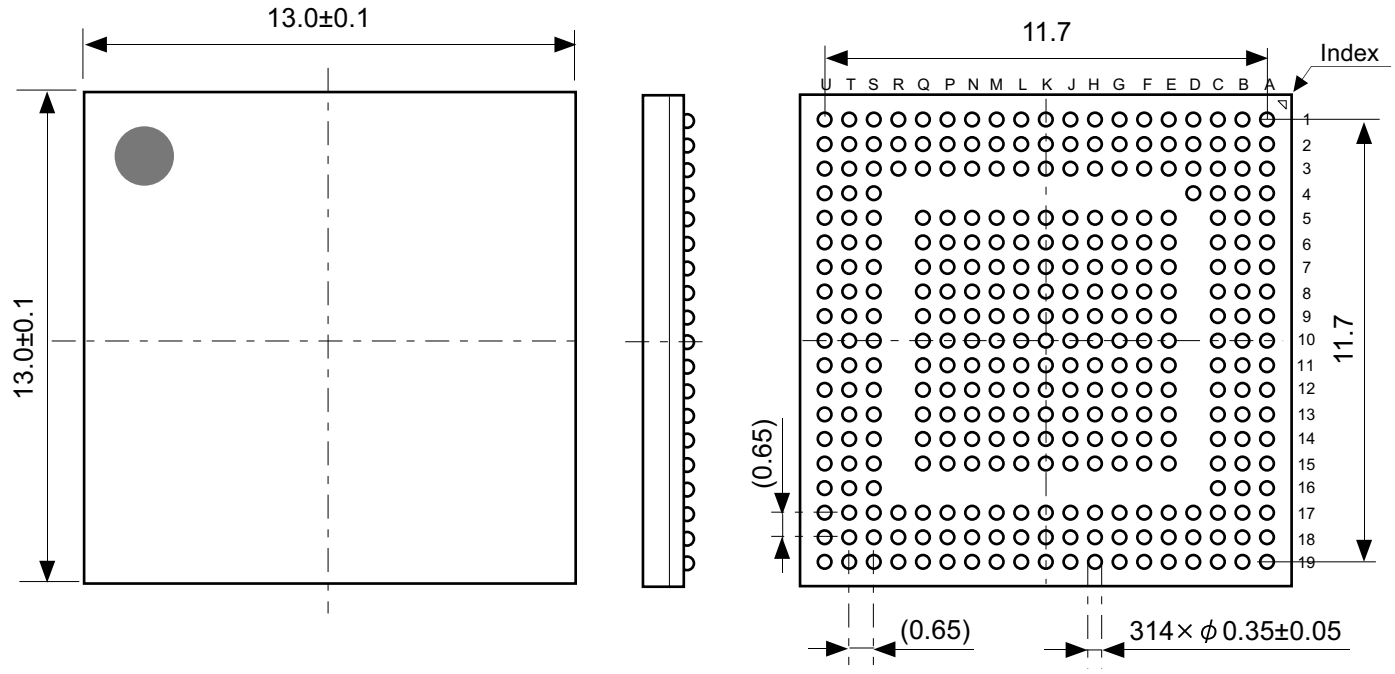
1. 6 Avoid dealing with or storing products in an extremely arid environment.

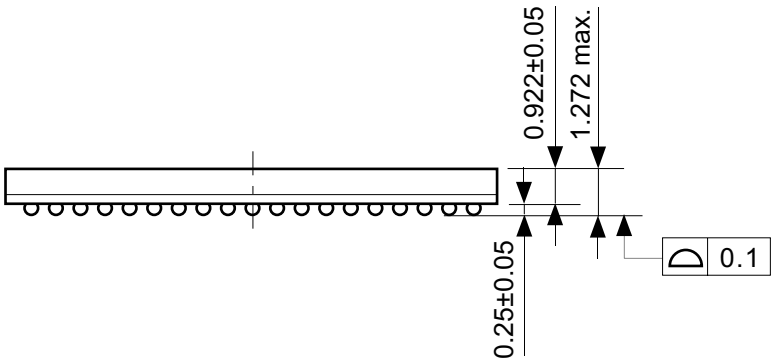
2. “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

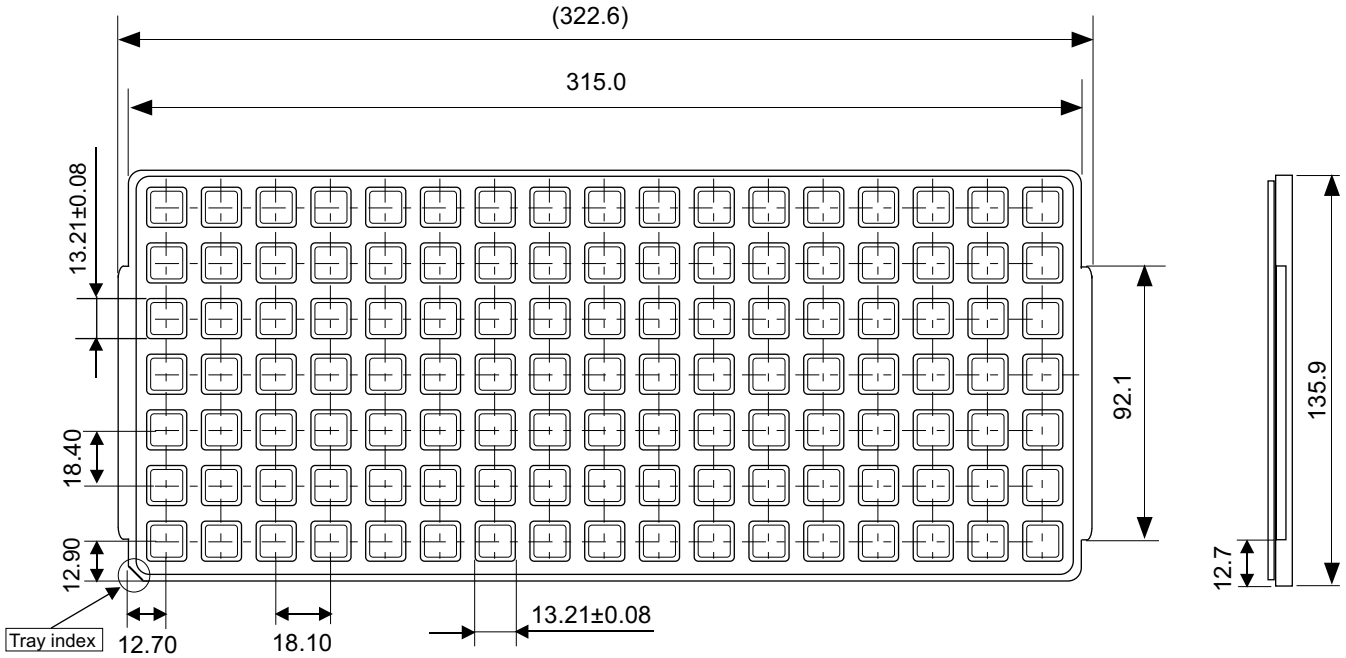


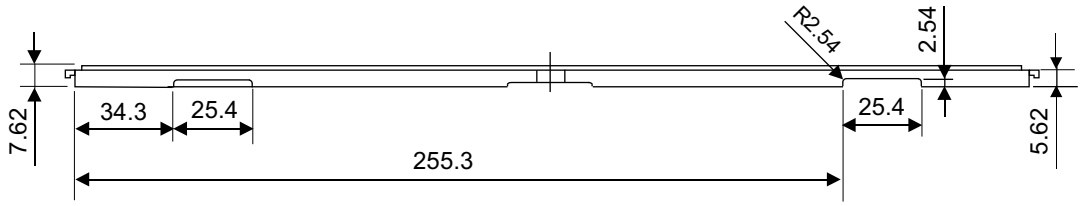


No. RA314-A-P-S1-1.0

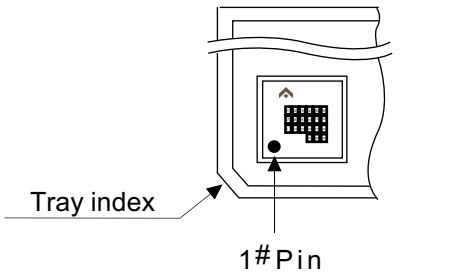
TITLE	BGA314-A-PKG Dimensions (S-US5591)
No.	RA314-A-P-S1-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



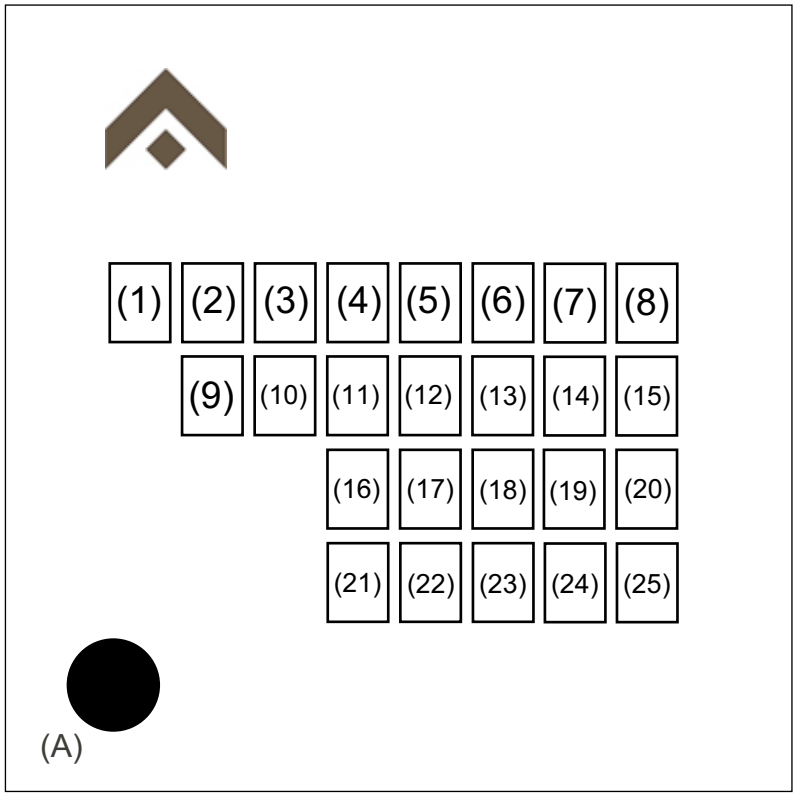


(Direction of IC in tray)



No. RA314-A-T-SD-2.0

TITLE	BGA314-A-Tray		
No.	RA314-A-T-SD-2.0		
ANGLE		QTY.	119
UNIT	mm		
	ABLIC Inc.		



(1) to (10) : Product code

(11) , (12) : Quality control code

(13) : Year of assembly

(14) : Month of assembly

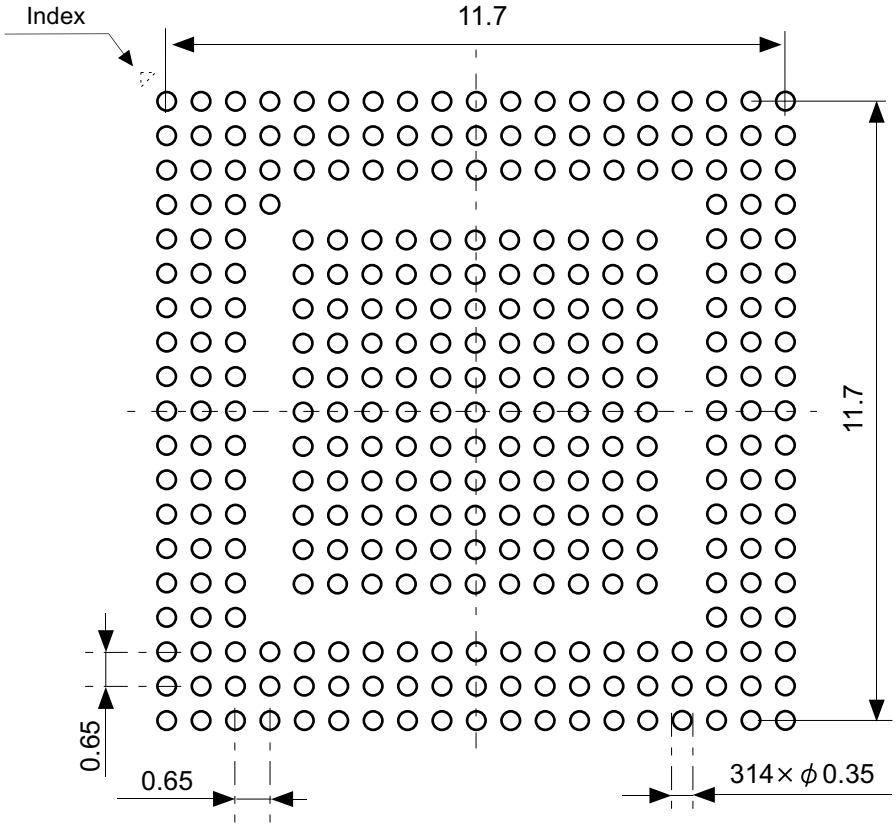
(15) : Week of assembly

(16) to (25) : Quality control code

(A) : 1-pin mark

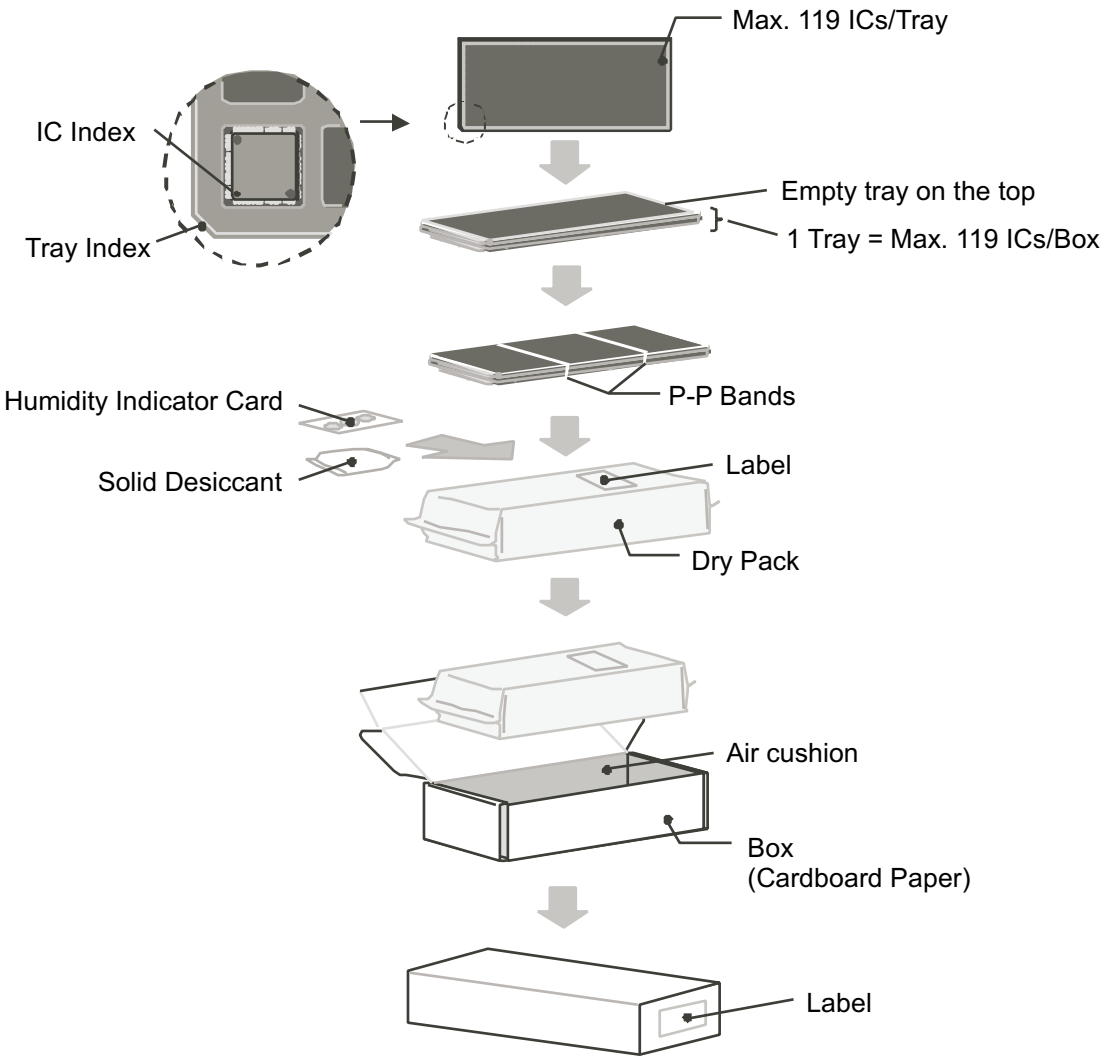
No. RA314-A-M-SD-1.0

TITLE	BGA314-A-Markings		
No.	RA314-A-M-SD-1.0		
ANGLE			
UNIT		TYPE	LASER
	ABLIC Inc.		



No. RA314-A-L-SD-2.0

TITLE	BGA314-A -Land Recommendation
No.	RA314-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



TITLE	BGA314-A -Packing Procedure
No.	RA314-A-K-SD-1.0
ANGLE	
UNIT	
ABLIC Inc.	

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   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
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2.4-2019.07