HDL6V5541

QUAD ±100V 2A 5-LEVEL ULTRASOUND PULSER

Rev.2.1_00

The ABLIC Inc. HDL6V5541 is a four-channel, unconditional five-level, high-voltage, high-speed pulser with active ground damping for medical ultrasound imaging applications.
The HDL6V5541 consists of logic interfaces, level translators, MOSFET gate drive buffers employing direct coupling topology, high-voltage, high-current MOSFETs, and active T/R switches.
The HDL6V5541 adopts a 3-to-6 decoder with user-selectable clock/transparent mode control.

Functions

- 4-channel, 5-level pulser with active ground damping and active T/R switch with 3-input/channel

Features

- 0 to ±100V output voltage
- ±2.0A source and sink peak current without output blocking high-voltage (HV) diodes
- ±1.4A source and sink peak current with ±0.6A active clamping with output blocking HV diodes
- ±1.0A source and sink peak current for active ground damping with output blocking HV diodes
- 500Ω (±50mA) active ground damping without output blocking HV diodes (Analog SW type)
- Mutually symmetrical positive and negative pulse waveforms for low 2nd order distortion
- 3-to-6 decoder with clock/transparent mode control
- 10Ω active T/R switch with logic-input/direct-input mode control
- Up to 20MHz operation frequency (@±60V output, 220pF load)
- 1.8V to 5V CMOS logic interface
- Noise-cut low-voltage (LV) diodes at each output
- 4-mode output drive current control for power saving
- Thermal protection
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- 64-lead 9x9mm QFN package (RoHS compliant)

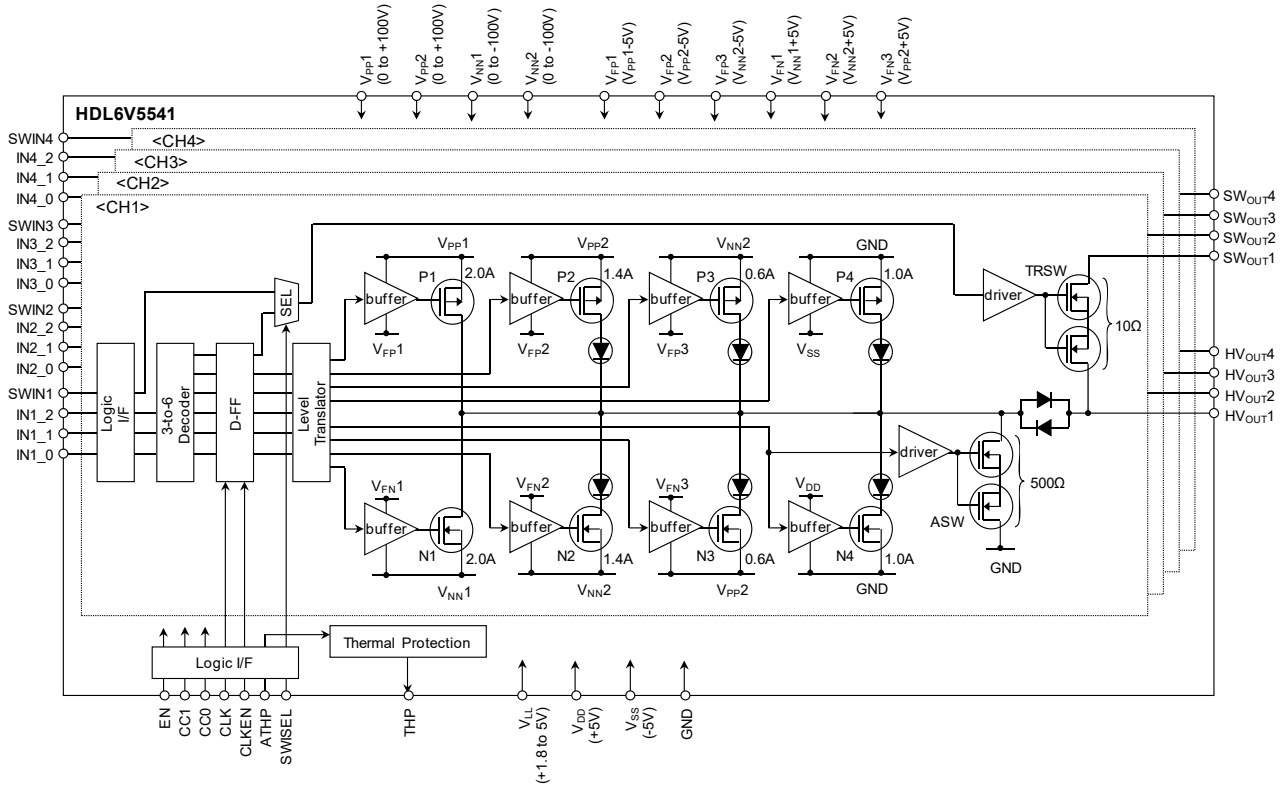


Fig.1 Block diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Positive logic supply	V_{LL}	-0.4 to +7	V	
2	Positive logic and level translator supply	V_{DD}	-0.4 to +7	V	
3	Negative logic and level translator supply	V_{SS}	-7 to +0.4	V	
4	Differential high voltage supplies	($V_{PP}1$ - $V_{NN}1$), ($V_{PP}2$ - $V_{NN}2$)	+210	V	
5	Positive high voltage supplies	$V_{PP}1$, $V_{PP}2$	-0.5 to +105	V	
6	Negative high voltage supplies	$V_{NN}1$, $V_{NN}2$	-105 to +0.5	V	
7	$V_{PP}1$ to $V_{PP}2$ voltage difference	($V_{PP}1$-$V_{PP}2$)	-105 to +105	V	$HV_{OUT}x$=HiZ or GND
			-0.5 to +105	V	Other than above
8	$V_{NN}1$ to $V_{NN}2$ voltage difference	($V_{NN}1$-$V_{NN}2$)	-105 to +105	V	$HV_{OUT}x$=HiZ or GND
			-105 to +0.5	V	Other than above
9	High voltage outputs (x=1~4)*	$HV_{OUT}x$	-105 to +105	V	
10	Floating gate drive voltages	($V_{PP}1$- $V_{FP}1$), ($V_{PP}2$- $V_{FP}2$), ($V_{NN}2$- $V_{FP}3$), ($V_{FN}1$- $V_{NN}1$), ($V_{FN}2$- $V_{NN}2$), ($V_{FN}3$- $V_{PP}2$)	-0.4 to +7	V	
11	THP (Thermal Protection) output	THP	-0.4 to +7	V	
12	All Logic input voltages (x=1~4, y=0~2)	INx_y, SWINx, SWISEL, EN, CLK, CLKEN, CC1, CC0, ATHP	-0.4 to +7	V	
13	Operating junction temperature	T_{Jop}	-20 to +150	°C	
14	Storage temperature	T_{STG}	-55 to +150	°C	
15	Maximum power dissipation	P_{Dmax}	4	W	

Note: * Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Conditions, and Circuits (Recommended)

2.1 Operating Supply Voltages and Conditions

Table 2 Recommended Operating Supply Voltages and Conditions

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic voltage supply	V_{LL}	2.4	2.5 to 5	V_{DD}	V	Clock mode (≤80MHz)
			2.6	2.7 to 5	V_{DD}	V	Clock mode (≤100MHz)
			1.7	1.8 to 5	V_{DD}	V	Transparent mode
2	Differential high voltage supply	($V_{PP}1$ - $V_{NN}1$), ($V_{PP}2$ - $V_{NN}2$)	0	-	200	V	
3	Positive high voltage supply	$V_{PP}1$, $V_{PP}2$	0	-	100	V	
4	Negative high voltage supply	$V_{NN}1$, $V_{NN}2$	-100	-	0	V	
5	$V_{PP}1$ to $V_{PP}2$ voltage difference	($V_{PP}1$-$V_{PP}2$)	0	-	100	V	
6	$V_{NN}1$ to $V_{NN}2$ voltage difference	($V_{NN}1$-$V_{NN}2$)	-100	-	0	V	

Table 2 Recommended Operating Supply Voltages and Conditions (cont.)

No	Items	Symbol	Min	Typ	Max	Units	Condition
7	Positive logic and level translator supply	V_{DD}	4.75	5	5.25	V	
8	Negative logic and level translator supply	V_{SS}	-5.25	-5	-4.75	V	
9	P-ch floating gate drive supply 1	$V_{FP}1$	$V_{PP}1$-5.25	$V_{PP}1$-5	$V_{PP}1$-4.75	V	
10	P-ch floating gate drive supply 2	$V_{FP}2$	$V_{PP}2$-5.25	$V_{PP}2$-5	$V_{PP}2$-4.75	V	
11	P-ch floating gate drive supply 3	$V_{FP}3$	$V_{NN}2$-5.25	$V_{NN}2$-5	$V_{NN}2$-4.75	V	
12	N-ch floating gate drive supply 1	$V_{FN}1$	$V_{NN}1$+4.75	$V_{NN}1$+5	$V_{NN}1$+5.25	V	
13	N-ch floating gate drive supply 2	$V_{FN}2$	$V_{NN}2$+4.75	$V_{NN}2$+5	$V_{NN}2$+5.25	V	
14	N-ch floating gate drive supply 3	$V_{FN}3$	$V_{PP}2$+4.75	$V_{PP}2$+5	$V_{PP}2$+5.25	V	
15	High-level logic input voltage	V_{IH}	0.8V_{LL}	-	V_{LL}	V	
16	Low-level logic input voltage	V_{IL}	0	-	0.2V_{LL}	V	
17	IC substrate voltage *	V_{SUB}	-	0	-	V	
18	Slew rate limit of $V_{PP}x$, $V_{NN}x$ (x=1,2)	SR_{MAX}	-	-	25	V/ms	
19	Operating Free-air Temperature	T_A	0	25	75	ºC	

Note: * Substrate bottom is internally connected to the central thermal pad on the bottom of the package. It must be soldered to the ground.

2.2 Power-Up/Down Sequence

Power-Up Sequence

1	V_{LL}
2	V_{DD}, V_{SS}
3	Set EN=1 ($HV_{OUT}x$=HiZ)
4	($V_{PP}1$-$V_{FP}1$), ($V_{PP}2$-$V_{FP}2$), ($V_{NN}2$-$V_{FP}3$), ($V_{FN}1$-$V_{NN}1$), ($V_{FN}2$-$V_{NN}2$), ($V_{FN}3$-$V_{PP}2$)
5	$V_{PP}1$, $V_{PP}2$, $V_{NN}1$, $V_{NN}2$
6	Logic control signals

Power-Down Sequence

1	Set EN=1 ($HV_{OUT}x$=HiZ)
2	$V_{PP}1$, $V_{PP}2$, $V_{NN}1$, $V_{NN}2$
3	($V_{PP}1$-$V_{FP}1$), ($V_{PP}2$-$V_{FP}2$), ($V_{NN}2$-$V_{FP}3$), ($V_{FN}1$-$V_{NN}1$), ($V_{FN}2$-$V_{NN}2$), ($V_{FN}3$-$V_{PP}2$)
4	V_{DD}, V_{SS}
5	V_{LL}

High-voltage Change Sequence during operation

1	Set EN=1 ($HV_{OUT}x$=HiZ)
2	Change $V_{PP}1$, $V_{PP}2$, $V_{NN}1$, $V_{NN}2$
3	Logic control signals

Note: It is indispensable to avoid the occurrence of the excessive voltage beyond the maximum rating in applying and cutting of the power supplies.

2.3 Application Circuits

(a) Clock Mode (CLKEN=0, CLK=100MHz)

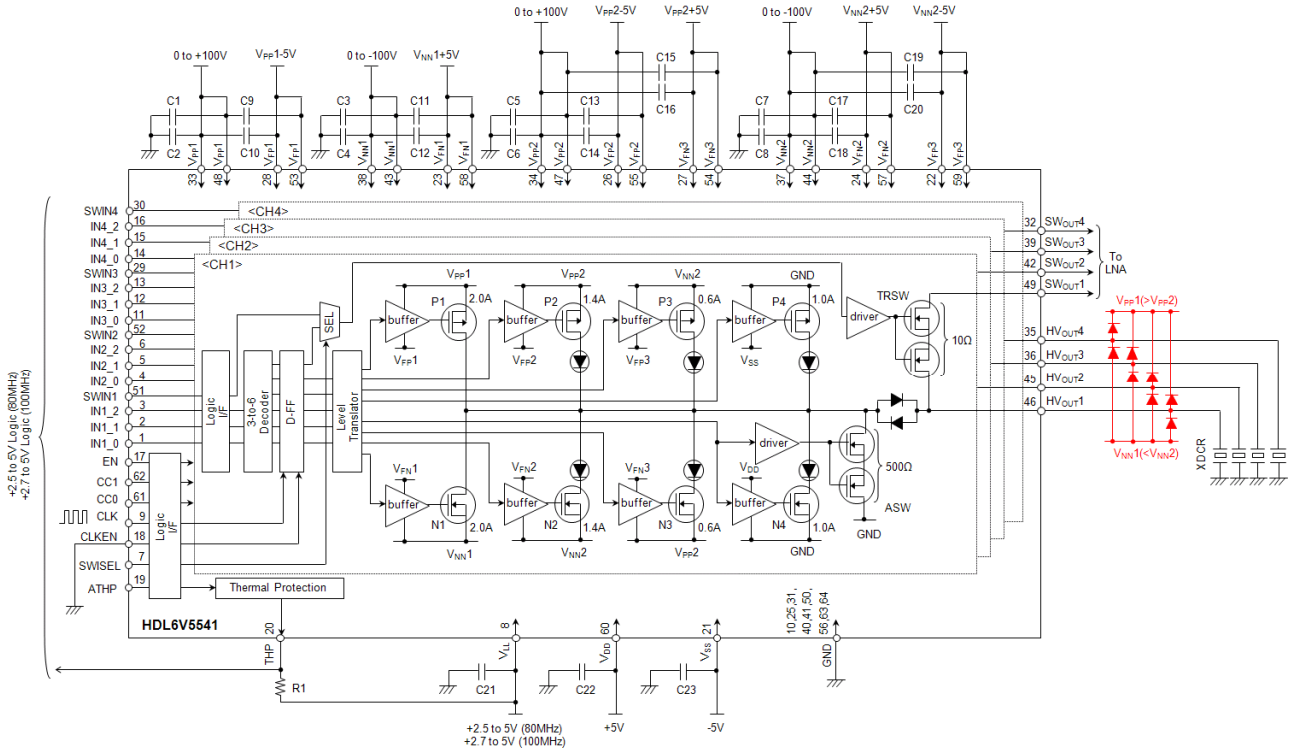


Fig. 2-(a) Typical Application Circuit-1
(Clock Mode)

Note:

1. Power supply pins, $V_{PP}x/V_{NN}x$ (x=1,2), can draw fast transient currents up to ±2.0A. Therefore, ceramic capacitors of 0.1uF to 1uF (C1~8) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of ≥16V 0.1uF to 1uF (C9~20) also should be connected between each floating voltage pin, $V_{FP}y/V_{FN}y$ (y=1~3) and power supply pin for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be connected to the GND.
5. **[PRECAUTION]** External high-voltage clamp diodes between $HV_{OUT}x$ and $V_{PP}1/V_{NN}1$(highest voltage) as shown in Fig.2-(a) are strongly recommended to avoid excessive voltage overshoot caused by a reflection from a probe.

(b) Transparent Mode (CLKEN=1, CLK=0)

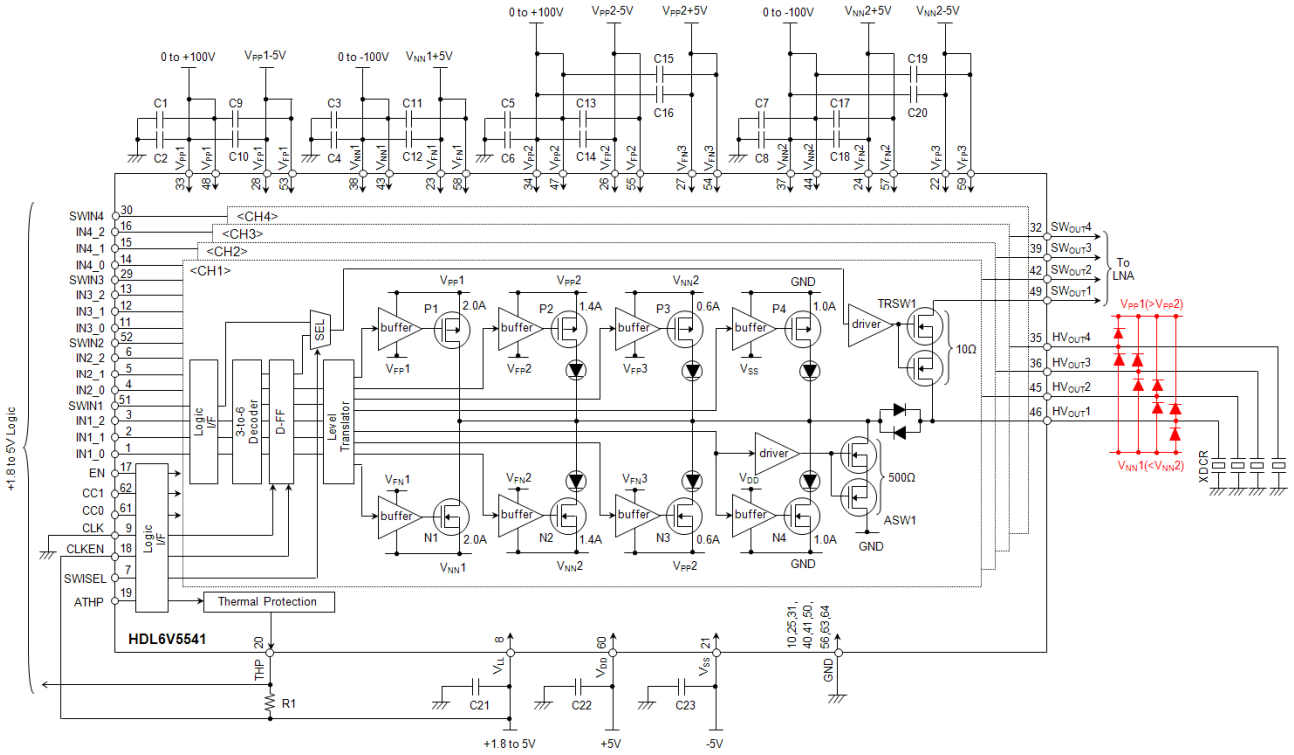


Fig. 2-(b) Typical Application Circuit-2
(Transparent Mode)

Note:

1. Power supply pins, $V_{PP}x/V_{NN}x$ (x=1,2), can draw fast transient currents up to ±2.0A. Therefore, ceramic capacitors of 0.1uF to 1uF (C1~8) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of ≥16V 0.1uF to 1uF (C9~20) also should be connected between each floating voltage pin, $V_{FP}y/V_{FN}y$ (y=1~3) and power supply pin for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be connected to the GND.
5. **[PRECAUTION]** External high-voltage clamp diodes between $HV_{OUT}x$ and $V_{PP}1/V_{NN}1$(highest voltage) as shown in Fig.2-(b) are strongly recommended to avoid excessive voltage overshoot caused by a reflection from a probe.

3. Electrical Characteristics

3.1 Clock Mode (CLKEN=0, CLK=100MHz)

DC Characteristics

Table 3 DC Characteristics (Clock mode)

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, $V_{FP}x=V_{PP}x$-5V, $V_{FP}3=V_{NN}2$-5V, $V_{FN}x=V_{NN}x$+5V, $V_{FN}3=V_{PP}2$+5V, T_A=25°C, 220pF//1kΩ load, CLK=100MHz, CLKEN=0, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	I_{IH}	-10	-	10	μA	INx_2, INx_1, INx_0, EN, CC1, CC0, CLK, CLKEN, SWINx
			-	66	-	μA	ATHP, SWISEL 50kΩ internal pull-down resistor
2	Input logic low current	I_{IL}	-10	-	10	μA	INx_2, INx_1, INx_0, CLK, ATHP, SWISEL
			-	66	-	μA	EN, CC1, CC0, CLKEN, SWINx 50kΩ internal pull-up resistor
3	Input logic capacitance	C_{IN}	-	2	-	pF	-
4	V_{LL} current	I_{LLQD}	-	0.53	-	mA	Quiescent current-1 EN=1(Disable), ATHP=0 Current mode=4 $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V INx_y=0 (x=1~4, y=0~2)
5	V_{DD} current	I_{DDQD}	-	10	-	mA	
6	V_{SS} current	I_{SSQD}	-	0.10	-	mA	
7	$V_{PP}1$ current	I_{PP1QD}	-	0	-	μA	
8	$V_{NN}1$ current	I_{NN1QD}	-	0	-	μA	
9	$V_{PP}2$ current	I_{PP2QD}	-	0.15	-	mA	
10	$V_{NN}2$ current	I_{NN2QD}	-	0.12	-	mA	
11	$V_{FP}1$ current	I_{FP1QD}	-	0	-	μA	
12	$V_{FP}2$ current	I_{FP2QD}	-	0.08	-	mA	
13	$V_{FP}3$ current	I_{FP3QD}	-	0	-	μA	
14	$V_{FN}1$ current	I_{FN1QD}	-	0	-	μA	
15	$V_{FN}2$ current	I_{FN2QD}	-	0.05	-	mA	
16	$V_{FN}3$ current	I_{FN3QD}	-	0	-	μA	
17	V_{LL} current	I_{LLQE}	-	0.60	-	mA	Quiescent current-2 EN=0(Enable), ATHP=0 Current mode=4 $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V INx_y=0 (x=1~4, y=0~2)
18	V_{DD} current	I_{DDQE}	-	10	-	mA	
19	V_{SS} current	I_{SSQE}	-	0.10	-	mA	
20	$V_{PP}1$ current	I_{PP1QE}	-	0	-	μA	
21	$V_{NN}1$ current	I_{NN1QE}	-	0	-	μA	
22	$V_{PP}2$ current	I_{PP2QE}	-	0.15	-	mA	
23	$V_{NN}2$ current	I_{NN2QE}	-	0.12	-	mA	
24	$V_{FP}1$ current	I_{FP1QE}	-	0	-	μA	
25	$V_{FP}2$ current	I_{FP2QE}	-	0.08	-	mA	
26	$V_{FP}3$ current	I_{FP3QE}	-	0	-	μA	
27	$V_{FN}1$ current	I_{FN1QE}	-	0	-	μA	
28	$V_{FN}2$ current	I_{FN2QE}	-	0.05	-	mA	
29	$V_{FN}3$ current	I_{FN3QE}	-	0	-	μA	

Table 3 DC Characteristics (Clock mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
30	V_{LL} current	I_{LLPW}	-	0.80	-	mA	Operating current-1 4-channel active Bipolar 3-level 1-cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-60V EN=0, ATHP=0 Current mode=4
31	V_{DD} current	I_{DDPW}	-	13	-	mA	
32	V_{SS} current	I_{SSPW}	-	2.8	-	mA	
33	$V_{PP}1$ current	I_{PP1PW}	-	0.50	-	mA	
34	$V_{NN}1$ current	I_{NN1PW}	-	0.85	-	mA	
35	$V_{PP}2$ current	I_{PP2PW}	-	0.15	-	mA	
36	$V_{NN}2$ current	I_{NN2PW}	-	0.12	-	mA	
37	$V_{FP}1$ current	I_{FP1PW}	-	0.02	-	mA	
38	$V_{FP}2$ current	I_{FP2PW}	-	0.08	-	mA	
39	$V_{FP}3$ current	I_{FP3PW}	-	0	-	µA	
40	$V_{FN}1$ current	I_{FN1PW}	-	0.01	-	mA	
41	$V_{FN}2$ current	I_{FN2PW}	-	0.05	-	mA	
42	$V_{FN}3$ current	I_{FN3PW}	-	0	-	µA	
43	V_{LL} current	I_{LLPW}	-	0.60	-	mA	Operating current-2 4-channel active Bipolar 5-level 1-cycle f=3.3MHz, PRT=200µs $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-30V EN=0, ATHP=0 Current mode=4 See Fig.6
44	V_{DD} current	I_{DDPW}	-	13	-	mA	
45	V_{SS} current	I_{SSPW}	-	2.8	-	mA	
46	$V_{PP}1$ current	I_{PP1PW}	-	0.40	-	mA	
47	$V_{NN}1$ current	I_{NN1PW}	-	0.50	-	mA	
48	$V_{PP}2$ current	I_{PP2PW}	-	0.25	-	mA	
49	$V_{NN}2$ current	I_{NN2PW}	-	0.40	-	mA	
50	$V_{FP}1$ current	I_{FP1PW}	-	0.02	-	mA	
51	$V_{FP}2$ current	I_{FP2PW}	-	0.10	-	mA	
52	$V_{FP}3$ current	I_{FP3PW}	-	0.01	-	mA	
53	$V_{FN}1$ current	I_{FN1PW}	-	0.01	-	mA	
54	$V_{FN}2$ current	I_{FN2PW}	-	0.07	-	mA	
55	$V_{FN}3$ current	I_{FN3PW}	-	0.01	-	mA	
56	V_{LL} current	I_{LLCW4}	-	0.70	-	mA	Operating current-3 4-channel active Bipolar 3-level Continuous Current mode=4 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
57	V_{DD} current	I_{DDCW4}	-	20	-	mA	
58	V_{SS} current	I_{SSCW4}	-	5.0	-	mA	
59	$V_{PP}1$ current	I_{PP1CW4}	-	0	-	µA	
60	$V_{NN}1$ current	I_{NN1CW4}	-	0	-	µA	
61	$V_{PP}2$ current	I_{PP2CW4}	-	76	-	mA	
62	$V_{NN}2$ current	I_{NN2CW4}	-	71	-	mA	
63	$V_{FP}1$ current	I_{FP1CW4}	-	0	-	µA	
64	$V_{FP}2$ current	I_{FP2CW4}	-	15	-	mA	
65	$V_{FP}3$ current	I_{FP3CW4}	-	5.5	-	mA	
66	$V_{FN}1$ current	I_{FN1CW4}	-	0	-	µA	
67	$V_{FN}2$ current	I_{FN2CW4}	-	10	-	mA	
68	$V_{FN}3$ current	I_{FN3CW4}	-	4.2	-	mA	

Table 3 DC Characteristics (Clock mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
69	V_{LL} current	I_{LLCW3}	-	0.75	-	mA	Operating current-4 4-channel active Bipolar 3-level Continuous Current mode=3 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
70	V_{DD} current	I_{DDCW3}	-	20	-	mA	
71	V_{SS} current	I_{SSCW3}	-	5.0	-	mA	
72	$V_{PP}1$ current	I_{PP1CW3}	-	0	-	µA	
73	$V_{NN}1$ current	I_{NN1CW3}	-	0	-	µA	
74	$V_{PP}2$ current	I_{PP2CW3}	-	73	-	mA	
75	$V_{NN}2$ current	I_{NN2CW3}	-	70	-	mA	
76	$V_{FP}1$ current	I_{FP1CW3}	-	0	-	µA	
77	$V_{FP}2$ current	I_{FP2CW3}	-	11	-	mA	
78	$V_{FP}3$ current	I_{FP3CW3}	-	0.20	-	mA	
79	$V_{FN}1$ current	I_{FN1CW3}	-	0	-	µA	
80	$V_{FN}2$ current	I_{FN2CW3}	-	7.8	-	mA	
81	$V_{FN}3$ current	I_{FN3CW3}	-	0.20	-	mA	
82	V_{LL} current	I_{LLCW2}	-	0.75	-	mA	Operating current-5 4-channel active Bipolar 3-level Continuous Current mode=2 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
83	V_{DD} current	I_{DDCW2}	-	20	-	mA	
84	V_{SS} current	I_{SSCW2}	-	5.0	-	mA	
85	$V_{PP}1$ current	I_{PP1CW2}	-	0	-	µA	
86	$V_{NN}1$ current	I_{NN1CW2}	-	0	-	µA	
87	$V_{PP}2$ current	I_{PP2CW2}	-	67	-	mA	
88	$V_{NN}2$ current	I_{NN2CW2}	-	66	-	mA	
89	$V_{FP}1$ current	I_{FP1CW2}	-	0	-	µA	
90	$V_{FP}2$ current	I_{FP2CW2}	-	8.0	-	mA	
91	$V_{FP}3$ current	I_{FP3CW2}	-	0.20	-	mA	
92	$V_{FN}1$ current	I_{FN1CW2}	-	0	-	µA	
93	$V_{FN}2$ current	I_{FN2CW2}	-	5.8	-	mA	
94	$V_{FN}3$ current	I_{FN3CW2}	-	0.20	-	mA	
95	V_{LL} current	I_{LLCW1}	-	0.80	-	mA	Operating current-6 4-channel active Bipolar 3-level Continuous Current mode=1 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
96	V_{DD} current	I_{DDCW1}	-	19	-	mA	
97	V_{SS} current	I_{SSCW1}	-	5.0	-	mA	
98	$V_{PP}1$ current	I_{PP1CW1}	-	0	-	µA	
99	$V_{NN}1$ current	I_{NN1CW1}	-	0	-	µA	
100	$V_{PP}2$ current	I_{PP2CW1}	-	59	-	mA	
101	$V_{NN}2$ current	I_{NN2CW1}	-	59	-	mA	
102	$V_{FP}1$ current	I_{FP1CW1}	-	0	-	µA	
103	$V_{FP}2$ current	I_{FP2CW1}	-	4.4	-	mA	
104	$V_{FP}3$ current	I_{FP3CW1}	-	0.20	-	mA	
105	$V_{FN}1$ current	I_{FN1CW1}	-	0	-	µA	
106	$V_{FN}2$ current	I_{FN2CW1}	-	3.3	-	mA	
107	$V_{FN}3$ current	I_{FN3CW1}	-	0.20	-	mA	

AC Characteristics

Table 4 AC Characteristics (Clock mode)

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, $V_{FP}x=V_{PP}x$-5V, $V_{FP}3=V_{NN}2$-5V, $V_{FN}x=V_{NN}x$+5V, $V_{FN}3=V_{PP}2$+5V, T_A=25ºC, 220pF//1kΩ load, EN=0, CLK=100MHz, CLKEN=0, 4-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input clock frequency	f_{CLK}	-	100	-	MHz	See Fig.3 D=τ/T
2	Duty cycle	D	40	50	60	%	
3	Setup time	t_{SU}	0.8	-	-	ns	
4	Hold time	t_{HOLD}	2.8	-	-	ns	
5	Delay time on outputs rise	$t_{dr(on)}$	-	65	-	ns	Bipolar half cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode=4 See Fig.4
6	Delay time on outputs fall	$t_{df(on)}$	-	65	-	ns	
7	Delay time off outputs rise	$t_{dr(off)}$	-	65	-	ns	
8	Delay time off outputs fall	$t_{df(off)}$	-	65	-	ns	
9	$\|t_{dr(on)}-t_{df(on)}\|$ Delay time matching	$\Delta t_{delay(on)}$	-	±1	±3	ns	
10	$\|t_{dr(off)}-t_{df(off)}\|$ Delay time matching	$\Delta t_{delay(off)}$	-	±1	±3	ns	
11	Output frequency range	f_{OUT}	-	-	20	MHz	Bipolar 2-cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode=4 See Fig.5
12	Output rise time	t_r	-	14	-	ns	
13	Output fall time	t_f	-	14	-	ns	
14	Second harmonic distortion	HD2	-	-40	-	dBc	
15	Second harmonic distortion	HD2	-	-40	-	dBc	Bipolar 5-level 1-cycle, f=3.3MHz PRT=200µs, Current mode=4 $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-30V, See Fig.6
16	Delay jitter on rise or fall	t_{Jr}, t_{Jf}	-	15	-	ps	Bipolar Continuous, f=5MHz $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-5V Current mode=1, See Fig.7
17	Enable time	t_{EN}	-	65	-	ns	EN fall edge to output burst
18	Disable time	t_{DIS}	-	65	-	ns	EN rise edge to output HiZ
19	Clock Enable time	t_{CLKEN}	-	65	-	ns	CLKEN fall edge to output burst
20	Clock Disable time	t_{CLKDIS}	-	65	-	ns	CLKEN rise edge to output HiZ
21	T/R switch spike voltage on $HV_{OUT}x$ and $SW_{OUT}x$	V_{TRN}	-	-	50	mVpp	50pF//200Ω load on $HV_{OUT}x$ 20pF//200Ω load on $SW_{OUT}x$
22	Delay time from input to T/R switch control start	t_{dTR}	-	45	-	ns	SWISEL=0 (logic input mode) See Fig.8
			-	30	-	ns	SWISEL=1 (direct input mode) See Fig.8
23	Delay time from T/R switch control start to T/R switch on	t_{dTRON}	-	300	-	ns	50pF//200Ω load on $HV_{OUT}x$ 20pF//200Ω load on $SW_{OUT}x$ See Fig.8
24	Delay time from T/R switch control start to T/R switch off	t_{dTROFF}	-	10	-	ns	

Thermal Protection Characteristics

Table 5 Thermal Protection Characteristics

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	1.0	V	V_{LL}=3.3V, I_{THP}=1mA
4	THP temperature threshold	T_{THP}	90	110	130	ºC	
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	ºC	

Device Characteristics

Table 6 Output P-Channel MOSFET Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	I_{OUT}P1	-	-2.0	-	A	Vgs=-5V, Vds=-100V
		I_{OUT}P2	-	-1.4	-	A	
		I_{OUT}P3	-	-0.6	-	A	
		I_{OUT}P4	-	-1.0	-	A	
2	Channel resistance	R_{ON}P1	-	6.5	-	Ω	Vgs=-5V, Id=-1A
		R_{ON}P2	-	9	-	Ω	Vgs=-5V, Id=-0.5A
		R_{ON}P3	-	21	-	Ω	Vgs=-5V, Id=-0.2A
		R_{ON}P4	-	13	-	Ω	Vgs=-5V, Id=-0.4A
3	Output capacitance	C_{OSS}P1	-	30	-	pF	Vgs=0V, Vds=-10V, f=1MHz

Note: These items above are not tested when shipped.

Table 7 Output N-Channel MOSFET Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	I_{OUT}N1	-	2.0	-	A	Vgs=5V, Vds=100V
		I_{OUT}N2	-	1.4	-	A	
		I_{OUT}N3	-	0.6	-	A	
		I_{OUT}N4	-	1.0	-	A	
2	Channel resistance	R_{ON}N1	-	6.5	-	Ω	Vgs=5V, Id=1A
		R_{ON}N2	-	9	-	Ω	Vgs=5V, Id=0.5A
		R_{ON}N3	-	21	-	Ω	Vgs=5V, Id=0.2A
		R_{ON}N4	-	13	-	Ω	Vgs=5V, Id=0.4A
3	Output capacitance	C_{OSS}N1	-	12	-	pF	Vgs=0V, Vds=10V, f=1MHz

Note: These items above are not tested when shipped.

Table 8 Analog Switch Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	On-state resistance (ASWx)	R_{ONASW}	-	500	-	Ω	Vgs=5V, Id=0.01A

Table 9 Output Blocking HV Diode Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V_{FDHV}	-	1.0	-	V	I_F=100mA
2	Reverse voltage	V_{RDHV}	200	-	-	V	I_R=1μA

Table 10 Output Noise-cut LV Diode Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V_{FDNC}	-	0.85	-	V	I_F=100mA

Table 11 T/R Switch Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	On-state resistance (TRSWx)	R_{ONTRSW}	-	10	-	Ω	Vgs=5V, Vds=0.1V
2	Capacitance to the ground	C_{dbTRSW}	-	9.5	-	pF	Vgs=5V, Vds=0.1V

3.2 Transparent Mode (CLKEN=1, CLK=0)

DC Characteristics

Table 12 DC Characteristics (Transparent mode)

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, $V_{FP}x=V_{PP}x$-5V, $V_{FP}3=V_{NN}2$-5V, $V_{FN}x=V_{NN}x$+5V, $V_{FN}3=V_{PP}2$+5V, T_A=25°C, 220pF//1kΩ load, CLK=0, CLKEN=1, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	I_{IH}	-10	-	10	μA	INx_2, INx_1, INx_0, EN, CC1, CC0, CLK, CLKEN, SWINx
			-	66	-	μA	ATHP, SWISEL 50kΩ internal pull-down resistor
2	Input logic low current	I_{IL}	-10	-	10	μA	INx_2, INx_1, INx_0, CLK, ATHP, SWISEL
			-	66	-	μA	EN, CC1, CC0, CLKEN, SWINx 50kΩ internal pull-up resistor
3	Input logic capacitance	C_{IN}	-	2	-	pF	-
4	V_{LL} current	I_{LLQD}	-	0	-	μA	Quiescent current-1 EN=1(Disable), ATHP=0 Current mode=4 $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V INx_y=0 (x=1~4, y=0~2)
5	V_{DD} current	I_{DDQD}	-	1.0	-	mA	
6	V_{SS} current	I_{SSQD}	-	0.14	-	mA	
7	$V_{PP}1$ current	I_{PP1QD}	-	0	-	μA	
8	$V_{NN}1$ current	I_{NN1QD}	-	0	-	μA	
9	$V_{PP}2$ current	I_{PP2QD}	-	0.15	-	mA	
10	$V_{NN}2$ current	I_{NN2QD}	-	0.12	-	mA	
11	$V_{FP}1$ current	I_{FP1QD}	-	0	-	μA	
12	$V_{FP}2$ current	I_{FP2QD}	-	0.08	-	mA	
13	$V_{FP}3$ current	I_{FP3QD}	-	0	-	μA	
14	$V_{FN}1$ current	I_{FN1QD}	-	0	-	μA	
15	$V_{FN}2$ current	I_{FN2QD}	-	0.05	-	mA	
16	$V_{FN}3$ current	I_{FN3QD}	-	0	-	μA	
17	V_{LL} current	I_{LLQE}	-	0.07	-	mA	Quiescent current-2 EN=0(Enable), ATHP=0 Current mode=4 $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V INx_y=0 (x=1~4, y=0~2)
18	V_{DD} current	I_{DDQE}	-	1.3	-	mA	
19	V_{SS} current	I_{SSQE}	-	0.14	-	mA	
20	$V_{PP}1$ current	I_{PP1QE}	-	0	-	μA	
21	$V_{NN}1$ current	I_{NN1QE}	-	0	-	μA	
22	$V_{PP}2$ current	I_{PP2QE}	-	0.15	-	mA	
23	$V_{NN}2$ current	I_{NN2QE}	-	0.12	-	mA	
24	$V_{FP}1$ current	I_{FP1QE}	-	0	-	μA	
25	$V_{FP}2$ current	I_{FP2QE}	-	0.08	-	mA	
26	$V_{FP}3$ current	I_{FP3QE}	-	0	-	μA	
27	$V_{FN}1$ current	I_{FN1QE}	-	0	-	μA	
28	$V_{FN}2$ current	I_{FN2QE}	-	0.05	-	mA	
29	$V_{FN}3$ current	I_{FN3QE}	-	0	-	μA	

Table 12 DC Characteristics (Transparent mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
30	V_{LL} current	I_{LLPW}	-	0.33	-	mA	Operating current-1 4-channel active Bipolar 3-level 1-cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-60V EN=0, ATHP=0 Current mode=4
31	V_{DD} current	I_{DDPW}	-	3.5	-	mA	
32	V_{SS} current	I_{SSPW}	-	2.8	-	mA	
33	$V_{PP}1$ current	I_{PP1PW}	-	0.50	-	mA	
34	$V_{NN}1$ current	I_{NN1PW}	-	0.85	-	mA	
35	$V_{PP}2$ current	I_{PP2PW}	-	0.15	-	mA	
36	$V_{NN}2$ current	I_{NN2PW}	-	0.12	-	mA	
37	$V_{FP}1$ current	I_{FP1PW}	-	0.02	-	mA	
38	$V_{FP}2$ current	I_{FP2PW}	-	0.08	-	mA	
39	$V_{FP}3$ current	I_{FP3PW}	-	0	-	µA	
40	$V_{FN}1$ current	I_{FN1PW}	-	0.01	-	mA	
41	$V_{FN}2$ current	I_{FN2PW}	-	0.05	-	mA	
42	$V_{FN}3$ current	I_{FN3PW}	-	0	-	µA	
43	V_{LL} current	I_{LLPW}	-	0.37	-	mA	Operating current-2 4-channel active Bipolar 5-level 1-cycle f=3.3MHz, PRT=200µs $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-30V EN=0, ATHP=0 Current mode=4 See Fig.6
44	V_{DD} current	I_{DDPW}	-	3.7	-	mA	
45	V_{SS} current	I_{SSPW}	-	2.8	-	mA	
46	$V_{PP}1$ current	I_{PP1PW}	-	0.40	-	mA	
47	$V_{NN}1$ current	I_{NN1PW}	-	0.50	-	mA	
48	$V_{PP}2$ current	I_{PP2PW}	-	0.25	-	mA	
49	$V_{NN}2$ current	I_{NN2PW}	-	0.40	-	mA	
50	$V_{FP}1$ current	I_{FP1PW}	-	0.02	-	mA	
51	$V_{FP}2$ current	I_{FP2PW}	-	0.10	-	mA	
52	$V_{FP}3$ current	I_{FP3PW}	-	0.01	-	mA	
53	$V_{FN}1$ current	I_{FN1PW}	-	0.01	-	mA	
54	$V_{FN}2$ current	I_{FN2PW}	-	0.07	-	mA	
55	$V_{FN}3$ current	I_{FN3PW}	-	0.01	-	mA	
56	V_{LL} current	I_{LLCW4}	-	0.18	-	mA	Operating current-3 4-channel active Bipolar 3-level Continuous Current mode=4 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
57	V_{DD} current	I_{DDCW4}	-	11	-	mA	
58	V_{SS} current	I_{SSCW4}	-	5.7	-	mA	
59	$V_{PP}1$ current	I_{PP1CW4}	-	0	-	µA	
60	$V_{NN}1$ current	I_{NN1CW4}	-	0	-	µA	
61	$V_{PP}2$ current	I_{PP2CW4}	-	76	-	mA	
62	$V_{NN}2$ current	I_{NN2CW4}	-	71	-	mA	
63	$V_{FP}1$ current	I_{FP1CW4}	-	0	-	µA	
64	$V_{FP}2$ current	I_{FP2CW4}	-	15	-	mA	
65	$V_{FP}3$ current	I_{FP3CW4}	-	5.5	-	mA	
66	$V_{FN}1$ current	I_{FN1CW4}	-	0	-	µA	
67	$V_{FN}2$ current	I_{FN2CW4}	-	10	-	mA	
68	$V_{FN}3$ current	I_{FN3CW4}	-	4.2	-	mA	

Table 12 DC Characteristics (Transparent mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
69	V_{LL} current	I_{LLCW3}	-	0.24	-	mA	Operating current-4 4-channel active Bipolar 3-level Continuous Current mode=3 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
70	V_{DD} current	I_{DDCW3}	-	11	-	mA	
71	V_{SS} current	I_{SSCW3}	-	5.6	-	mA	
72	$V_{PP}1$ current	I_{PP1CW3}	-	0	-	µA	
73	$V_{NN}1$ current	I_{NN1CW3}	-	0	-	µA	
74	$V_{PP}2$ current	I_{PP2CW3}	-	73	-	mA	
75	$V_{NN}2$ current	I_{NN2CW3}	-	70	-	mA	
76	$V_{FP}1$ current	I_{FP1CW3}	-	0	-	µA	
77	$V_{FP}2$ current	I_{FP2CW3}	-	11	-	mA	
78	$V_{FP}3$ current	I_{FP3CW3}	-	0.20	-	mA	
79	$V_{FN}1$ current	I_{FN1CW3}	-	0	-	µA	
80	$V_{FN}2$ current	I_{FN2CW3}	-	7.8	-	mA	
81	$V_{FN}3$ current	I_{FN3CW3}	-	0.20	-	mA	
82	V_{LL} current	I_{LLCW2}	-	0.24	-	mA	Operating current-5 4-channel active Bipolar 3-level Continuous Current mode=2 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
83	V_{DD} current	I_{DDCW2}	-	11	-	mA	
84	V_{SS} current	I_{SSCW2}	-	5.5	-	mA	
85	$V_{PP}1$ current	I_{PP1CW2}	-	0	-	µA	
86	$V_{NN}1$ current	I_{NN1CW2}	-	0	-	µA	
87	$V_{PP}2$ current	I_{PP2CW2}	-	67	-	mA	
88	$V_{NN}2$ current	I_{NN2CW2}	-	66	-	mA	
89	$V_{FP}1$ current	I_{FP1CW2}	-	0	-	µA	
90	$V_{FP}2$ current	I_{FP2CW2}	-	8.0	-	mA	
91	$V_{FP}3$ current	I_{FP3CW2}	-	0.20	-	mA	
92	$V_{FN}1$ current	I_{FN1CW2}	-	0	-	µA	
93	$V_{FN}2$ current	I_{FN2CW2}	-	5.8	-	mA	
94	$V_{FN}3$ current	I_{FN3CW2}	-	0.20	-	mA	
95	V_{LL} current	I_{LLCW1}	-	0.30	-	mA	Operating current-6 4-channel active Bipolar 3-level Continuous Current mode=1 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
96	V_{DD} current	I_{DDCW1}	-	10	-	mA	
97	V_{SS} current	I_{SSCW1}	-	5.2	-	mA	
98	$V_{PP}1$ current	I_{PP1CW1}	-	0	-	µA	
99	$V_{NN}1$ current	I_{NN1CW1}	-	0	-	µA	
100	$V_{PP}2$ current	I_{PP2CW1}	-	59	-	mA	
101	$V_{NN}2$ current	I_{NN2CW1}	-	59	-	mA	
102	$V_{FP}1$ current	I_{FP1CW1}	-	0	-	µA	
103	$V_{FP}2$ current	I_{FP2CW1}	-	4.4	-	mA	
104	$V_{FP}3$ current	I_{FP3CW1}	-	0.20	-	mA	
105	$V_{FN}1$ current	I_{FN1CW1}	-	0	-	µA	
106	$V_{FN}2$ current	I_{FN2CW1}	-	3.3	-	mA	
107	$V_{FN}3$ current	I_{FN3CW1}	-	0.20	-	mA	

AC Characteristics

Table 13 AC Characteristics (Transparent mode)

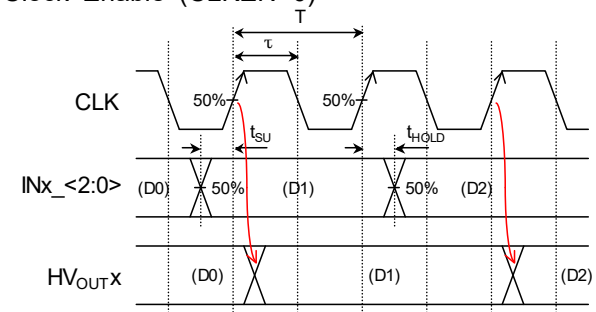
V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, $V_{FP}x$=$V_{PP}x$-5V, $V_{FP}3$=$V_{NN}2$-5V, $V_{FN}x$=$V_{NN}x$+5V, $V_{FN}3$=$V_{PP}2$+5V, T_A=25°C, 220pF//1kΩ load, EN=0, CLK=0, CLKEN=1, 4-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Delay time on outputs rise	$t_{dr(on)}$	-	60	-	ns	Bipolar half cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode=4 See Fig.4
2	Delay time on outputs fall	$t_{df(on)}$	-	60	-	ns	
3	Delay time off outputs rise	$t_{dr(off)}$	-	60	-	ns	
4	Delay time off outputs fall	$t_{df(off)}$	-	60	-	ns	
5	$\|t_{dr(on)}-t_{df(on)}\|$ Delay time matching	$\Delta t_{delay(on)}$	-	±1	±3	ns	
6	$\|t_{dr(off)}-t_{df(off)}\|$ Delay time matching	$\Delta t_{delay(off)}$	-	±1	±3	ns	
7	Output frequency range	f_{OUT}	-	-	20	MHz	Bipolar 2-cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode=4 See Fig.5
8	Output rise time	t_r	-	14	-	ns	
9	Output fall time	t_f	-	14	-	ns	
10	Second harmonic distortion	HD2	-	-40	-	dBc	
11	Second harmonic distortion	HD2	-	-40	-	dBc	Bipolar 5-level 1-cycle, f=3.3MHz PRT=200µs, Current mode=4 $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-30V, See Fig.6
12	Delay jitter on rise or fall	t_{Jr}, t_{Jf}	-	15	-	ps	Bipolar Continuous, f=5MHz $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-5V Current mode=1, See Fig.7
13	Enable time	t_{EN}	-	60	-	ns	EN fall edge to output burst
14	Disable time	t_{DIS}	-	60	-	ns	EN rise edge to no output
15	Clock Enable time	t_{CLKEN}	-	65	-	ns	CLKEN fall edge to output burst
16	Clock Disable time	t_{CLKDIS}	-	65	-	ns	CLKEN rise edge to output HiZ
17	T/R switch spike voltage on HVOUTx and SWOUTx	VTRN	-	-	50	mVpp	50pF//200Ω load on HVOUTx 20pF//200Ω load on SWOUTx
18	Delay time from input to T/R switch control start	t_{dTR}	-	45	-	ns	SWISEL=0 (logic input mode) See Fig.8
			-	30	-	ns	SWISEL=1 (direct input mode) See Fig.8
19	Delay time from T/R switch control start to T/R switch on	t_{dTRON}	-	300	-	ns	50pF//200Ω load on HVOUTx 20pF//200Ω load on SWOUTx See Fig.8
20	Delay time from T/R switch control start to T/R switch off	t_{dTROFF}	-	10	-	ns	

See Table 5 through 11 for the characteristics of Thermal Protection, and Devices.

4. Switching Time Diagram (EN=0)

Clock Enable (CLKEN=0)



Clock Disable (CLKEN=1)

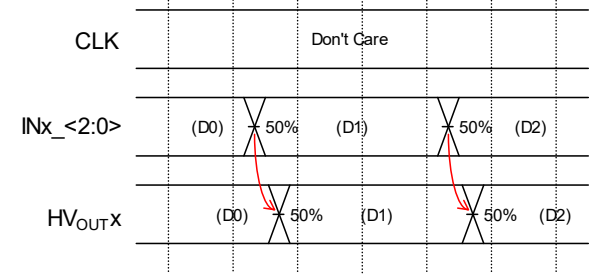


Fig. 3 Setup/hold time

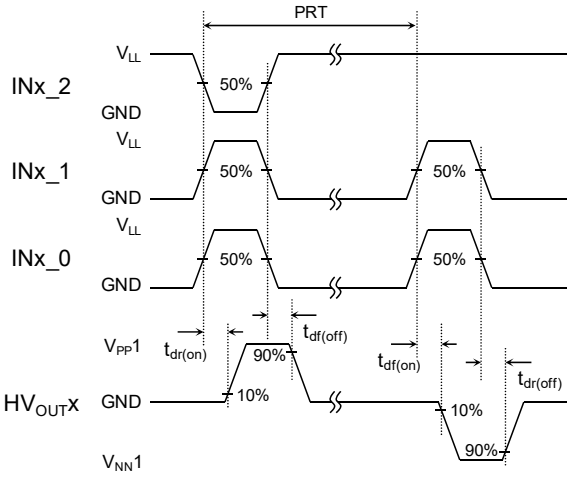


Fig. 4 Propagation delay time

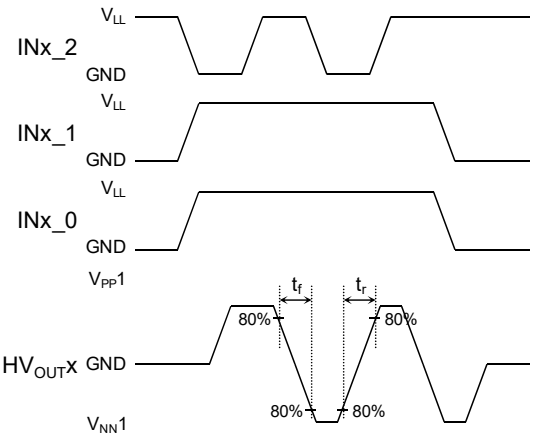


Fig. 5 Output rise/fall time

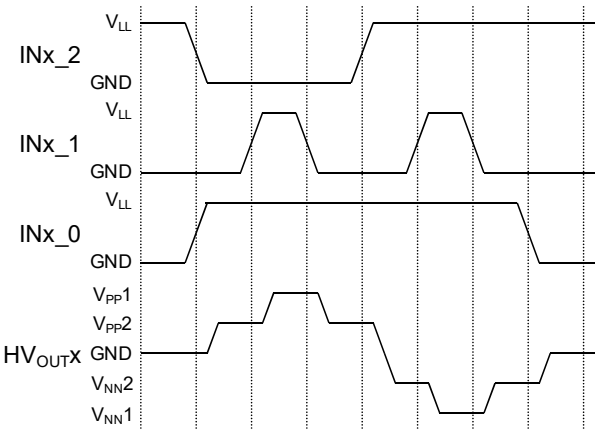


Fig. 6 5-level 1-cycle operation

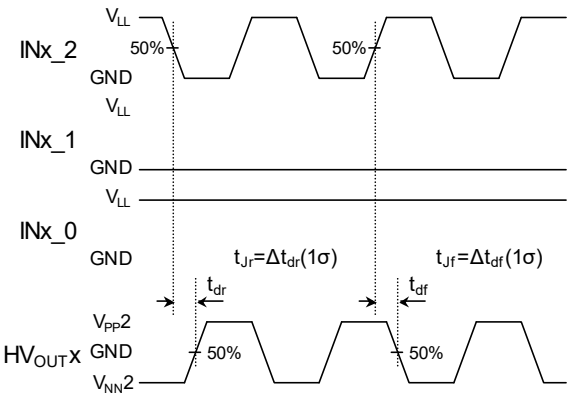
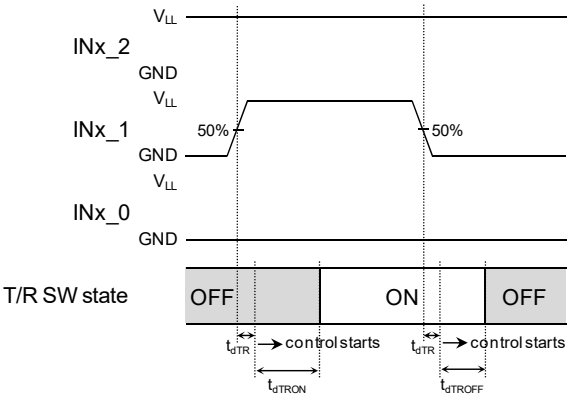


Fig. 7 Delay jitter on rise/fall

Logic input mode (SWISEL=0)



Direct input mode (SWISEL=1)

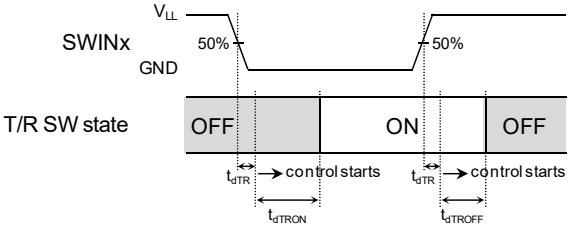


Fig. 8 T/R switch delay time

5. Truth Table

Table 14 Truth table

Logic Inputs				HV MOSFET status										Output
EN	**INx_2**	**INx_1**	**INx_0**	**P1**	**N1**	**P2**	**N2**	**P3**	**N3**	**P4**	**N4**	**ASW**	**TRSW**	**$HV_{OUT}x$**
	PoI	HV1	HV2	+HV1	-HV1	+HV2	-HV2	-HV2	+HV2	GND	GND	GND		
0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	HiZ
0	0	0	1	OFF	OFF	**ON**	OFF	OFF	**ON** *1	OFF	OFF	OFF	OFF	+HV2
0	0	1	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	HiZ + TRSW ON
0	0	1	1	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	+HV1
0	1	0	0	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	OFF	GND
0	1	0	1	OFF	OFF	OFF	**ON**	**ON** *1	OFF	OFF	OFF	OFF	OFF	-HV2
0	1	1	0	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	**ON**	GND + TRSW ON
0	1	1	1	OFF	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	-HV1
1	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	HiZ

*1) When current mode is other than 4, both P3 and N3 are always off-state.

Note:
- SWISEL=0 (logic input mode)
- $V_{PP}1$/ $V_{NN}1$=+/-HV1, $V_{PP}2$/ $V_{NN}2$=+/-HV2
- x=1~4

6. Current Mode Control Table

Table 15 Drive current mode control table

			I_{OUT} [A] *1	
Current Mode	**CC1**	**CC0**	**P2**	**N2**
1	0	0	0.35	0.35
2	0	1	0.7	0.7
3	1	0	1.05	1.05
4	1	1	1.4	1.4

Note:

*1) Output saturation current @ |Vds|=100V

Following current mode is recommended:
- Current mode=4 for high voltage, short pulse train operations (e.g. $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V, 2-cycle, PRT=200us)
- Current mode=2 for low voltage, long pulse train or even continuous wave operations (e.g. $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-3V, continuous wave)

7. Pin Configuration

Table 16 Pin Configuration

Pin#	Pin Name	I/O	Function
1	IN1_0	I	Input logic control of the least significant bit of channel 1, HV2 control
2	IN1_1	I	Input logic control of 2nd significant bit of channel 1, HV1 control
3	IN1_2	I	Input logic control of the most significant bit of channel 1, polarity control
4	IN2_0	I	Input logic control of the least significant bit of channel 2, HV2 control
5	IN2_1	I	Input logic control of 2nd significant bit of channel 2, HV1 control
6	IN2_2	I	Input logic control of the most significant bit of channel 2, polarity control
7	SWISEL	I	Control of T/R SW input mode, Hi=direct pin input, Low=logic input (50kΩ internal pull-down resistor)
8	VLL	-	Positive voltage supply of low voltage interface (+3.3V)
9	CLK	I	Clock Input (100MHz)
10	GND	-	Drive power ground (0V)
11	IN3_0	I	Input logic control of the least significant bit of channel 3, HV2 control
12	IN3_1	I	Input logic control of 2nd significant bit of channel 3, HV1 control
13	IN3_2	I	Input logic control of the most significant bit of channel 3, polarity control
14	IN4_0	I	Input logic control of the least significant bit of channel 4, HV2 control
15	IN4_1	I	Input logic control of 2nd significant bit of channel 4, HV1 control
16	IN4_2	I	Input logic control of the most significant bit of channel 4, polarity control
17	EN	I	Control of drive output enable, Hi=off, Low=on (50kΩ internal pull-up resistor)
18	CLKEN	I	Control of clock enable, Hi=clock disable, Low=clock enable (50kΩ internal pull-up resistor)
19	ATHP	I	Control of active THP enable, Hi=disable, Low=enable (50kΩ internal pull-down resistor)
20	THP	O	Thermal protection output, open N-MOS drain
21	VSS	-	Negative low voltage power supply (-5V)
22	VFP3	-	P-MOS (P3) floating gate drive power supply (VNN2-5V)
23	VFN1	-	N-MOS (N1) floating gate drive power supply (VNN1+5V)
24	VFN2	-	N-MOS (N2) floating gate drive power supply (VNN2+5V)
25	GND	-	Drive power ground (0V)
26	VFP2	-	P-MOS (P2) floating gate drive power supply (VPP2-5V)
27	VFN3	-	N-MOS (N3) floating gate drive power supply (VPP2+5V)
28	VFP1	-	P-MOS (P1) floating gate drive power supply (VPP1-5V)
29	SWIN3	I	Control of T/R switch of channel 3 @SWISEL=Hi, Hi=off, Low=on (50kΩ internal pull-up resistor)
30	SWIN4	I	Control of T/R switch of channel 4 @SWISEL=Hi, Hi=off, Low=on (50kΩ internal pull-up resistor)
31	GND	-	Drive power ground (0V)
32	SWOUT4	O	Output of T/R switch of channel 4

Table 16 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
33	VPP1	-	Positive high voltage power supply 1 for channel 3,4 (0 to +100V)
34	VPP2	-	Positive high voltage power supply 2 for channel 3,4 (0 to +100V, VPP2<VPP1)
35	HVOUT4	O	Output high voltage for channel 4
36	HVOUT3	O	Output high voltage for channel 3
37	VNN2	-	Negative high voltage power supply 2 for channel 3,4 (0 to -100V, VNN2>VNN1)
38	VNN1	-	Negative high voltage power supply 1 for channel 3,4 (0 to -100V)
39	SWOUT3	O	Output of T/R switch of channel 3
40	GND	-	Drive power ground (0V)
41	GND	-	Drive power ground (0V)
42	SWOUT2	O	Output of T/R switch of channel 2
43	VNN1	-	Negative high voltage power supply 1 for channel 1,2 (0 to -100V)
44	VNN2	-	Negative high voltage power supply 2 for channel 1,2 (0 to -100V, VNN2>VNN1)
45	HVOUT2	O	Output high voltage for channel 2
46	HVOUT1	O	Output high voltage for channel 1
47	VPP2	-	Positive high voltage power supply 2 for channel 1,2 (0 to +100V)
48	VPP1	-	Positive high voltage power supply 1 for channel 1,2 (0 to +100V)
49	SWOUT1	O	Output of T/R switch of channel 1
50	GND	-	Drive power ground (0V)
51	SWIN1	I	Control of T/R switch of channel 1 @SWISEL=Hi, Hi=off, Low=on (50kΩ internal pull-up resistor)
52	SWIN2	I	Control of T/R switch of channel 2 @SWISEL=Hi, Hi=off, Low=on (50kΩ internal pull-up resistor)
53	VFP1	-	P-MOS (P1) floating gate drive power supply (VPP1-5V)
54	VFN3	-	N-MOS (N3) floating gate drive power supply (VPP2+5V)
55	VFP2	-	P-MOS (P2) floating gate drive power supply (VPP2-5V)
56	GND	-	Drive power ground (0V)
57	VFN2	-	N-MOS (N2) floating gate drive power supply (VNN2+5V)
58	VFN 1	-	N-MOS (N1) floating gate drive power supply (VNN1+5V)
59	VFP3	-	P-MOS (P3) floating gate drive power supply (VNN2-5V)
60	VDD	-	Positive low voltage power supply (+5V)
61	CC0	I	Control of drive current mode 0 (50kΩ internal pull-up resistor)
62	CC1	I	Control of drive current mode 1 (50kΩ internal pull-up resistor)
63	GND	-	Drive power ground (0V)
64	GND	-	Drive power ground (0V)

■ Package

Table 17 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-64(0909)B	QN064-B-P-SD	QFN9x9-B-T-SD	QN064-B-M-S4	QN064-B-L-SD	QN064-B-K-SD

■ Storage, Mounting

1. Storage conditions

1. 1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Fig. 9 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

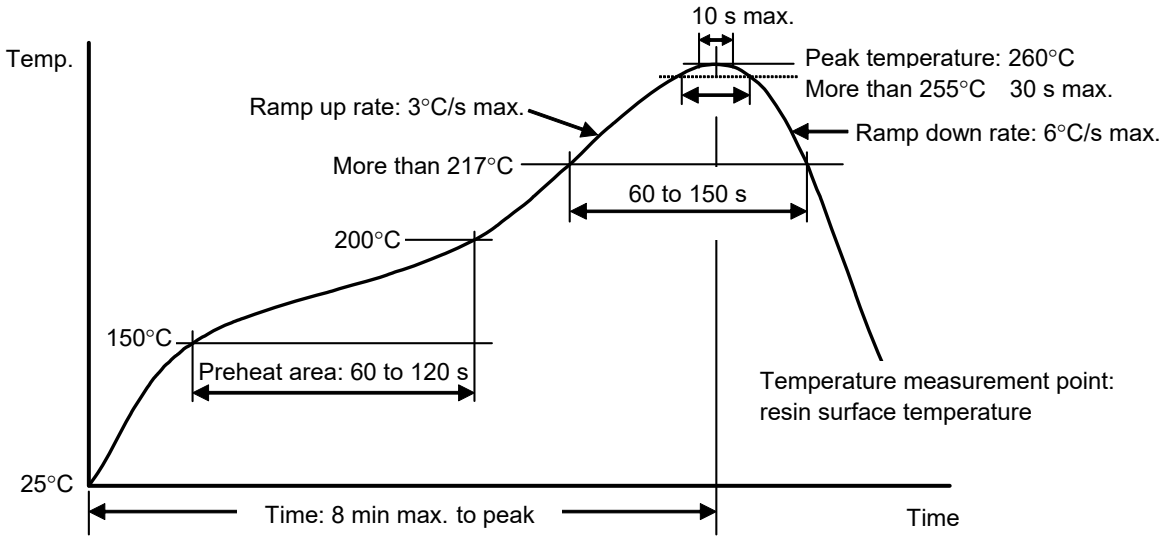


Fig. 9 Resistance to Soldering Heat Condition for Package (Reflow Method)

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1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.

1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1. 4 Prevent friction with other materials made with high polymer.

1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

1. 6 Avoid dealing with or storing products in an extremely arid environment.

2. “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

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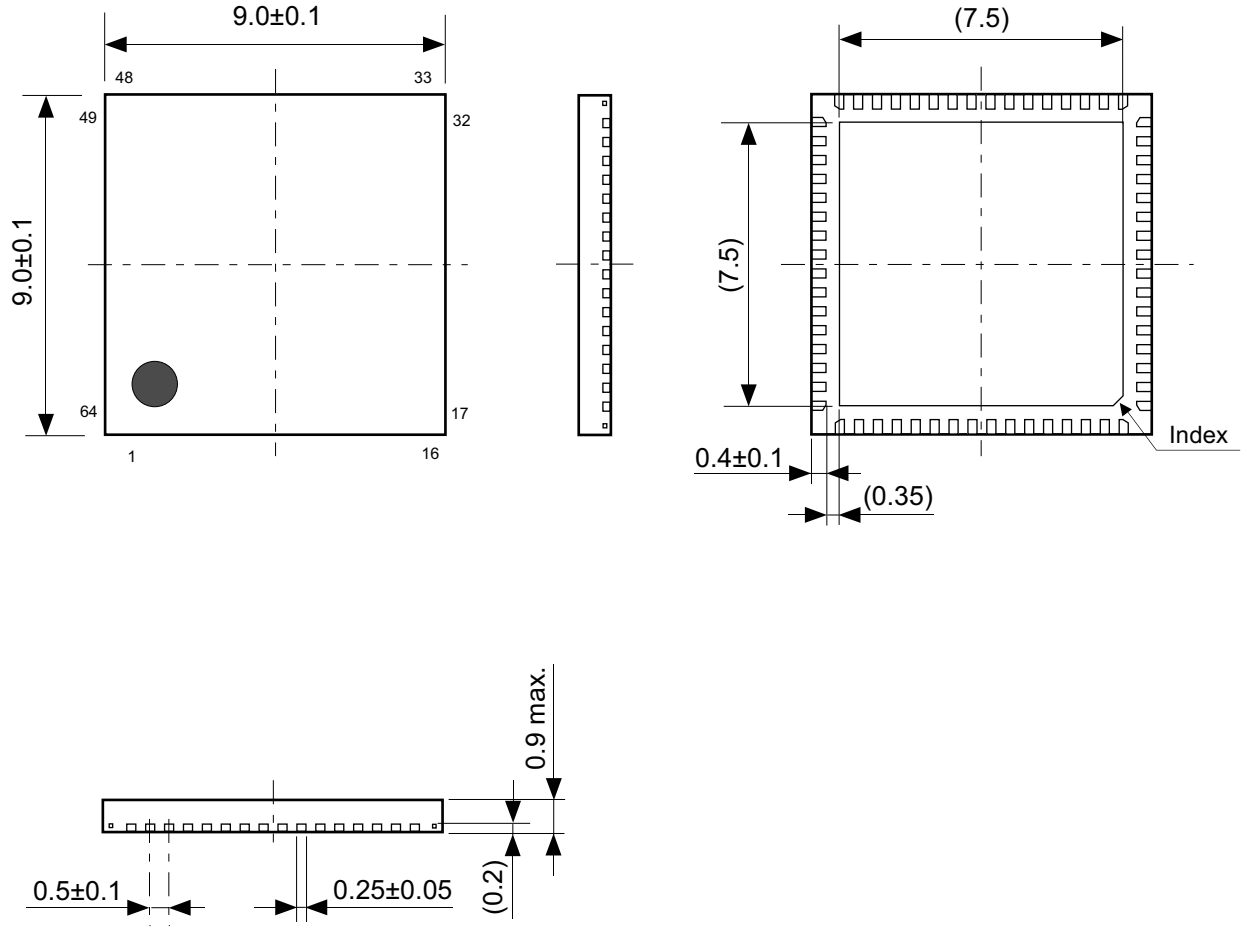
4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.



No. QN064-B-P-SD-2.0

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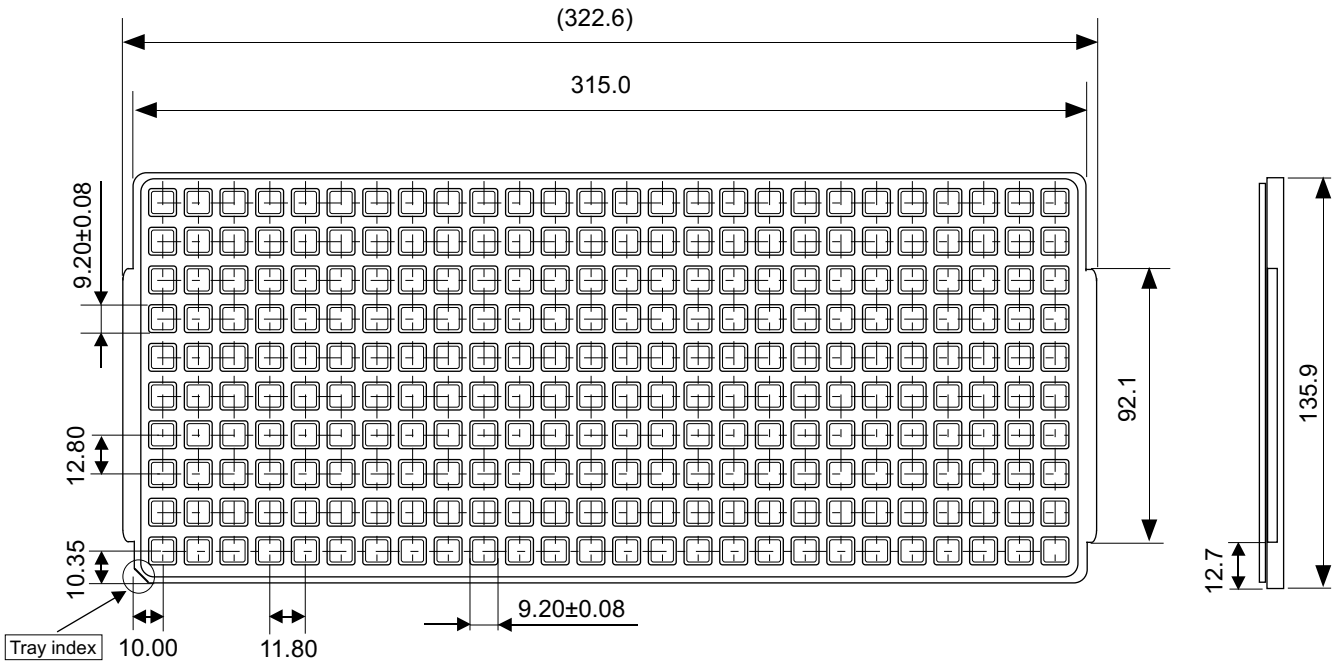
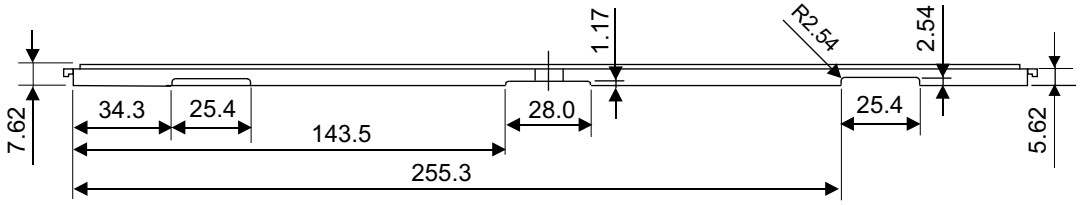
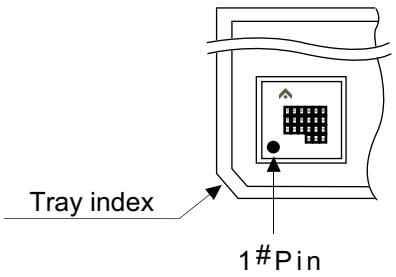
No.	QN064-B-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



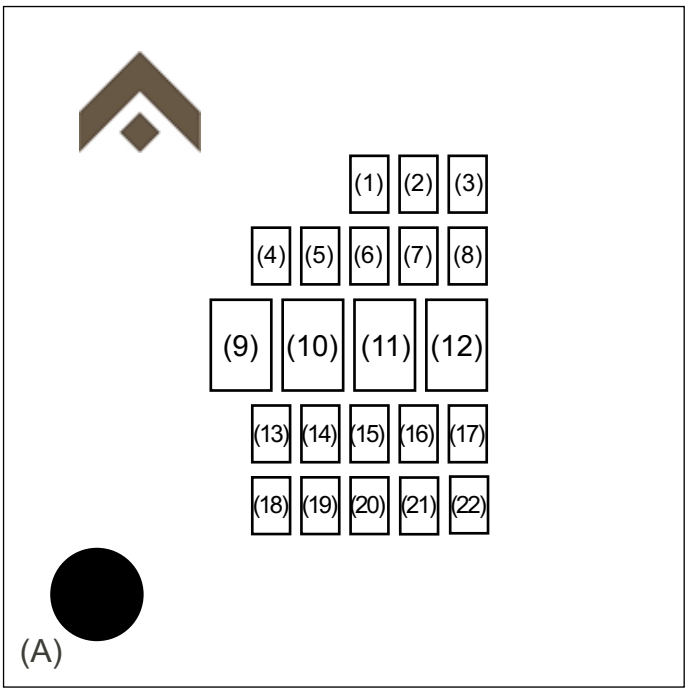


(Direction of IC in tray)



No. QFN9x9-B-T-SD-1.0

TITLE	QFN9x9-B-Tray		
No.	QFN9x9-B-T-SD-1.0		
ANGLE		QTY.	260
UNIT	mm		
ABLIC Inc.			



(1) : Year of assembly

(2) : Month of assembly

(3) : Week of assembly

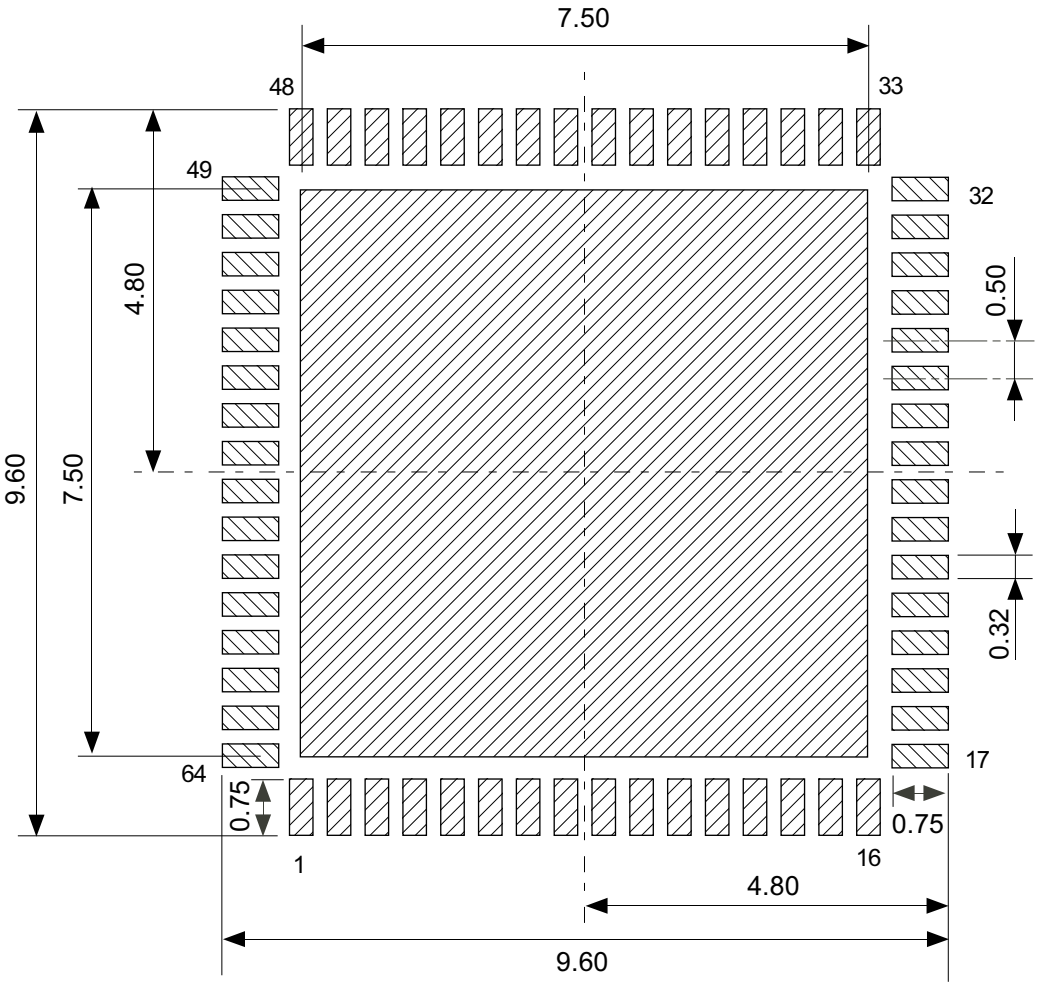
(4) to (12) : Product code

(13) to (22) : Quality control code

(A) : 1-pin mark

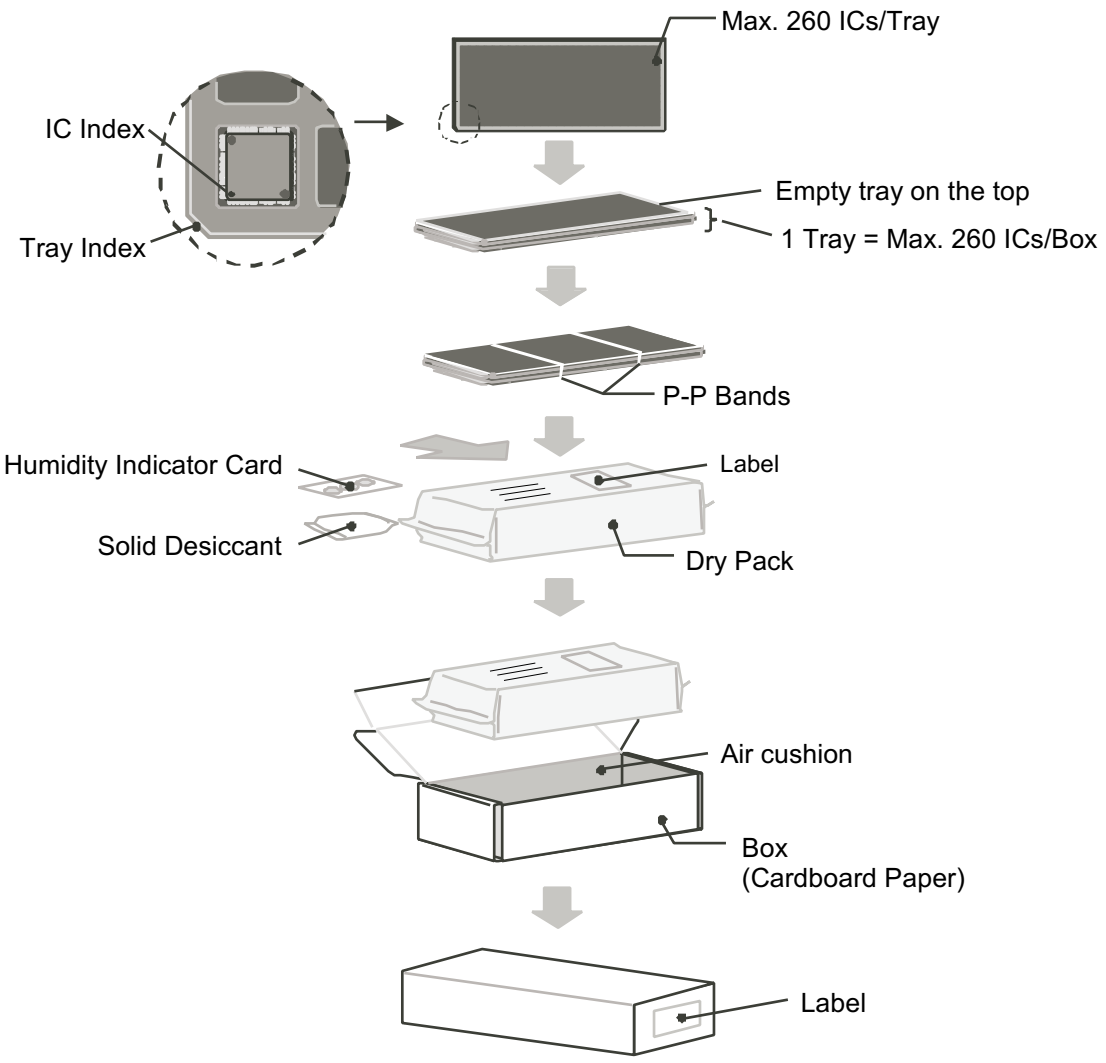
No. QN064-B-M-S4-1.0

TITLE	QFN64-B-Markings (S-UV5541)		
No.	QN064-B-M-S4-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



No. QN064-B-L-SD-2.0

TITLE	QFN64-B -Land Recommendation
No.	QN064-B-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. QN064-B-K-SD-2.0

TITLE	QFN64-B -Packing Procedure
No.	QN064-B-K-SD-2.0
ANGLE	
UNIT	
ABLIC Inc.	

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