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LOW CHARGE INJECTION 32-CHANNEL 8Ω HIGH-VOLTAGE ANALOG SWITCHES

Rev.1.0_00

The ABLIC S-UM6531E is a low charge injection 32-channel single-pole, double-throw (SPDT) high-voltage analog switch IC operated only by a single 5V for ultrasound imaging applications.
Users can select either Serial Digital Interface (SDI) or Bank Interface.
The S-UM6531E has the same packaging and pinout as the HDL6M06531B with improved Con/Coff and off isolation performance.

■ Functions

- 32-channel high-voltage SPDT analog switches with user-selectable SDI or Bank interface

■ Features

- 0V to ±100V analog signal voltage range allowing ±150V voltage overshoot
- 10kHz to 85MHz analog signal frequency range
- 2A peak analog signal current per channel
- 8Ω switch on-resistance
- 40kΩ bleed resistor on probe side
- 32-bit shift registers
- Low on/off-capacitance
- 15pC charge injection to 1000pF
- -75dB off-isolation at analog small-signal 5MHz
- -60dB switch crosstalk
- Selectable Serial Digital Interface (32-bit shift registers) or Bank Interface (1 bank of 32-channel)
- 1.8V to 5V CMOS logic interface
- Single +5V power supply (NO HIGH-VOLTAGE POWER SUPPLY required)
- Low power dissipation (static 5mW)
- Embedded thermal protection flag indicator
- Unique pin configuration for easy PCB traces
- RoHS compliant 64-lead 9x9mm QFN

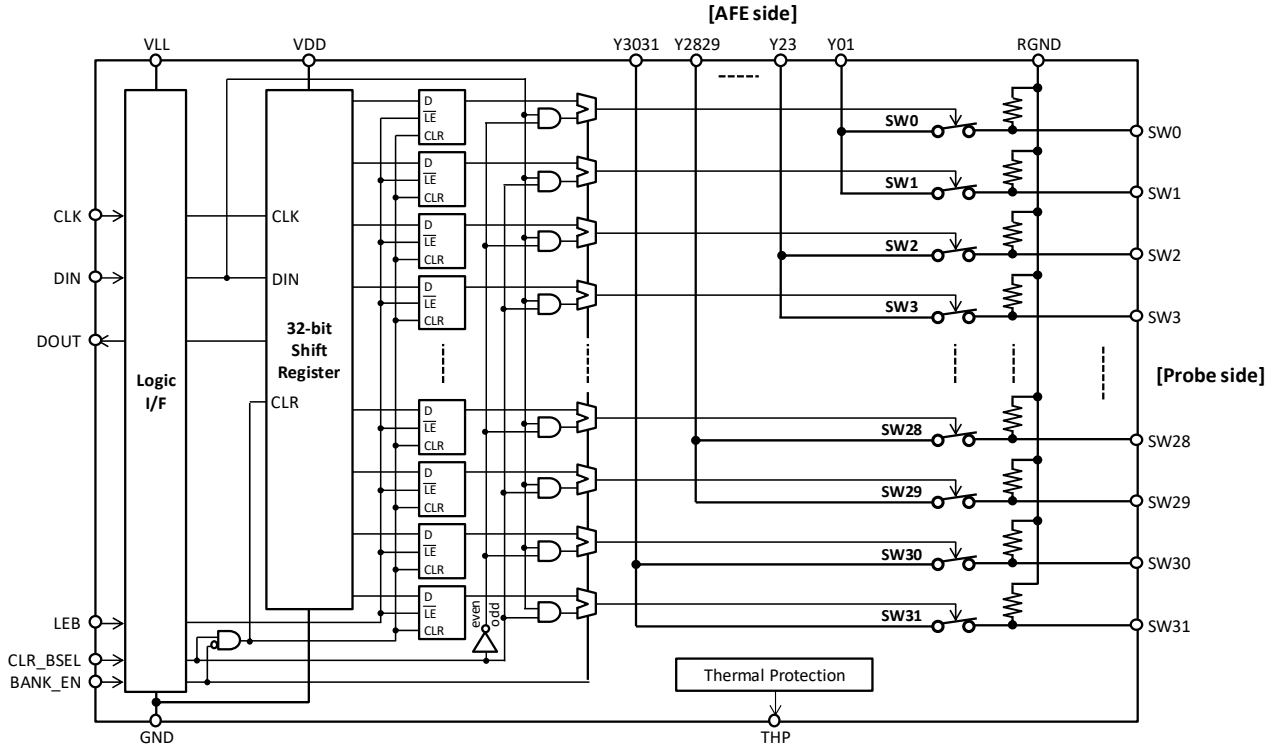

Figure 1 Block Diagram

■ Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Positive logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Logic input voltage	DIN, LEB, CLK, CLR_BSEL, BANK_EN	-0.4 to +7	V	
4	Logic output voltage	DOUT, THP	-0.4 to +7	V	
5	Analog signal range (steady state voltage)	V_{SIG}	-105 to +105	V	
6	Analog signal range (peak overshoot voltage)	V_{SIG_OS}	-150 to +150	V	Max. 500ns pulse width
7	Peak analog signal current per channel	I_{SW}	2.5	A	
8	Operating junction temperature	T_{Jop}	-20 to +150	°C	
9	Storage temperature	T_{STG}	-55 to +150	°C	
10	Maximum power dissipation	P_{Dmax}	4	W	

Remark Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

■ Operating Supply Voltages, Logic Levels, and Application Circuits

1. Operating supply voltages, temperature, and logic levels

Table 2 Operating Supply Voltages and Logic Levels

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V_{LL}	1.7	1.8 to 5	V_{DD}	V	
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	IC substrate voltage *1	V_{SUB}	-	0	-	V	
4	Operating free-air temperature	T_A	0	-	75	°C	
5	High-level logic input voltage	V_{IH}	$0.8V_{LL}$	-	V_{LL}	V	
6	Low-level logic input voltage	V_{IL}	0	-	$0.2V_{LL}$	V	
7	High-level logic output voltage	V_{oH}	$0.8V_{LL}$	-	-	V	I_{SOURCE} = 1mA
8	Low-level logic output voltage	V_{oL}	-	-	$0.2V_{LL}$	V	I_{SINK} = 1mA
9	Logic input high current *2	I_{IH}	-10	-	10	μA	DIN, LEB, CLK, CLR_BSEL, BANK_EN
10	Logic input low current	I_{IL}	-10	-	10	μA	
11	Logic input capacitance	C_{IN}	-	2	-	pF	
12	Set up time before LEB rises	t_{SD}	10	-	-	ns	
13	Time width of LEB	t_{WLEB}	12	-	-	ns	
14	Clock delay time to data out	t_{DO}	7	10	24	ns	
15	Time width of CLR_BSEL	t_{OLR}	12	-	-	ns	
16	Clock frequency	f_{CLK}	-	-	50	MHz	V_{LL}=1.8V
			-	-	80	MHz	V_{LL}=2.5V
			-	-	95	MHz	V_{LL}=3.3V
17	Clock rise and fall times	t_R, t_F	-	-	50	ns	
18	Setup time data to clock	t_{SU}	4	-	-	ns	
19	Hold time data from clock	t_{HLD}	4	-	-	ns	
20	Bank interface setup time	t_{SD_BNK}	100	-	-	ns	
21	BANKx minimum pulse width	t_{WBANK}	4	-	-	μs	

***1.** Thermal pad on the bottom of the package must be soldered to the ground.
***2.** BANK_EN has 100μA leakage at V_{LL}=5V due to 50kΩ internal pull-down resistor.

2. Power supply sequencing

No power supply sequencing is required even if V_{LL} is different from V_{DD}.
Please apply the V_{DD} voltage to the V_{LL} when operating with a single 5V.

■ Electrical Characteristics

1. DC characteristics

Table 3 DC Characteristics

V_{LL}=3.3V, V_{DD}=5V, LEB=0, BANK_EN=0/1, T_A=25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Analog signal range (steady state voltage)	V_{SIG}	-100	-	+100	V	
2	Analog signal range (peak overshoot voltage)	V_{SIG_OS}	-150	-	+150	V	Max. 500ns pulse width
3	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	μA	Quiescent current-1 All switches off
4	V_{DD} quiescent current	I_{DDQ}	-	1.5	-	mA	
5	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	μA	Quiescent current-2 All switches on
6	V_{DD} quiescent current	I_{DDQ}	-	1.5	-	mA	
7	V_{LL} dynamic current	I_{LL}	-	2	10	μA	Dynamic current All channels switching simultaneously at f_{SW}=50kHz
8	V_{DD} dynamic current	I_{DD}	-	3.4	4.6	mA	
9	DC offset switch off	V_{OS}	-	0	-	mV	
10	Small signal switch on-resistance	R_{ONS}	-	8	10	Ω	V_{SIG}=0.1Vpp to 5Vpp @5MHz, R_S=10Ω
11	Small signal switch on-resistance matching	ΔR_{ONS}	-	2	5	%	V_{SIG}=0V, I_{SIG}=5mA
12	Large signal switch on-resistance	R_{ONL}	-	8	-	Ω	V_{SIG}=20Vpp@5MHz, R_S=10Ω
13	Shunt resistance	R_{BLD}	30	40	50	kΩ	On probe side
14	Switch output peak current	I_{SW}	-	2	-	A	100ns pulse, 0.1% duty cycle

2. Thermal protection

Table 4 Thermal Protection Characteristics

V_{LL}=3.3V, V_{DD}=5V, LEB=0, BANK_EN=0/1, T_A=25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, V_{LL}=3.3V, I_{THP}=1mA
4	THP temperature threshold	T_{THP}	90	110	130	ºC	Thermal protection flag indicator by THP pin (open N-MOS drain, Low=THP activating)
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	ºC	

3. AC Characteristics

Table 5 AC Characteristics

V_{LL}=3.3V, V_{DD}=5V, LEB=0, BANK_EN=0/1, T_A=25°C, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	Turn-on time		t_{ON}	-	2	4	μs	
			t_{ON_BNK}	-	2	4	μs	
2	Turn-off time		t_{OFF}	-	2	4	μs	
			t_{OFF_BNK}	-	2	4	μs	
3	Output switching frequency		f_{SW}	-	-	50	kHz	Duty cycle=50%
4	Small signal frequency		f_{SIG}	0.01	-	85	MHz	C_L=220pF
5	Off isolation	small signal	$V_{ISO(RX)}$	-	-75	-	dB	f_{SIG}=5MHz, R_L=50Ω
		large signal	$V_{ISO(TX)}$	-	-65	-	dB	f_{SIG}=5MHz, R_L=50Ω
6	Crosstalk		V_{CT}	-	-60	-	dB	f_{SIG}=5MHz, R_L=50Ω
7	On capacitance (one SW ON, another SW OFF)	small signal	$C_{ON(RX)}$	-	33	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
		large signal	$C_{ON(TX)}$	-	33	-	pF	V_{SIG}=10Vpp, f_{SIG}=1MHz
8	Off capacitance SW_ to GND	small signal	$C_{OFF(SW\_RX)}$	-	20	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
9	Off capacitance Y_ to GND (both SW OFF)	small signal	$C_{OFF(Y\_RX)}$	-	25	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
		large signal	$C_{OFF(Y\_TX)}$	-	26	-	pF	V_{SIG}=10Vpp, f_{SIG}=1MHz
10	Output spike voltage (SW_)		$V_{SPK\_ON(SW)}$	-	40	-	mV	50Ω load @switch on
			$V_{SPK\_OFF(SW)}$	-	60	-	mV	50Ω load @switch off
11	Output spike voltage (Y_)		$V_{SPK\_ON(Y)}$	-	40	-	mV	50Ω load @switch on
			$V_{SPK\_OFF(Y)}$	-	60	-	mV	50Ω load @switch off
12	Charge injection		QC	-	15	-	pC	

■ Test Circuits

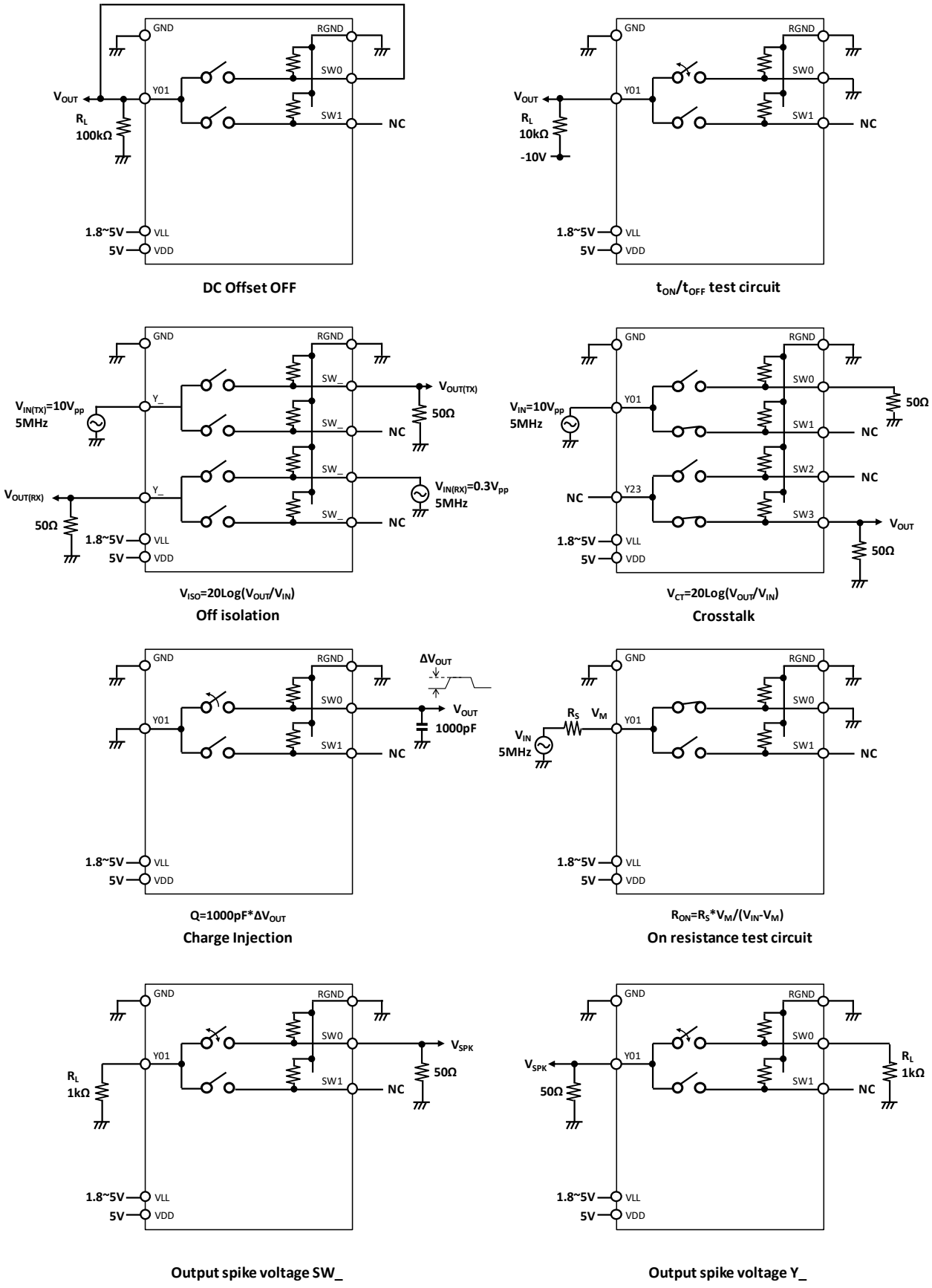

Figure 2 Test Circuits

■ Truth Table

Table 6 Truth Table

Logic Inputs								Analog Switch State				
LEB	CLR_BSEL	BANK_EN	DIN									
			D0	D1	···	D30	D31	SW0	SW1	···	SW30	SW31
L	L	L	L	-		-	-	OFF	-		-	-
L	L	L	H	-		-	-	ON	-		-	-
L	L	L	-	L		-	-	-	OFF		-	-
L	L	L	-	H		-	-	-	ON		-	-
L	L	L	-	-		-	-	-	-		-	-
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L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		L	-	-	-		OFF	-
L	L	L	-	-		H	-	-	-		ON	-
L	L	L	-	-		-	L	-	-		-	OFF
L	L	L	-	-		-	H	-	-		-	ON
H	L	L	X	X	X	X	X	Hold Previous State				
X	H	L	X	X	X	X	X	ALL SWs OFF				
X	L	H	L					ALL SWs OFF				
X	L	H	H					Even channel SWs ON, Odd channel SWs OFF				
X	H	H	L					ALL SWs OFF				
X	H	H	H					Odd channel SWs ON, Even channel SWs OFF				

■ Logic Timing

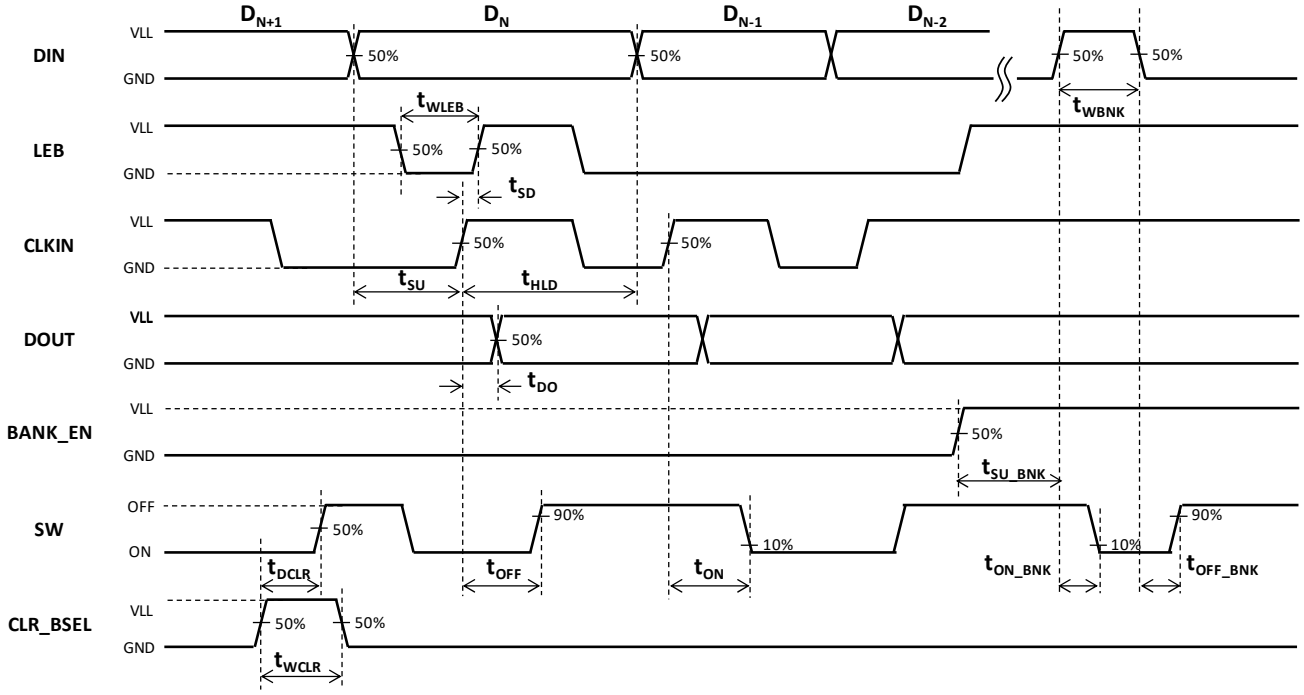

Figure 3 Logic Timing

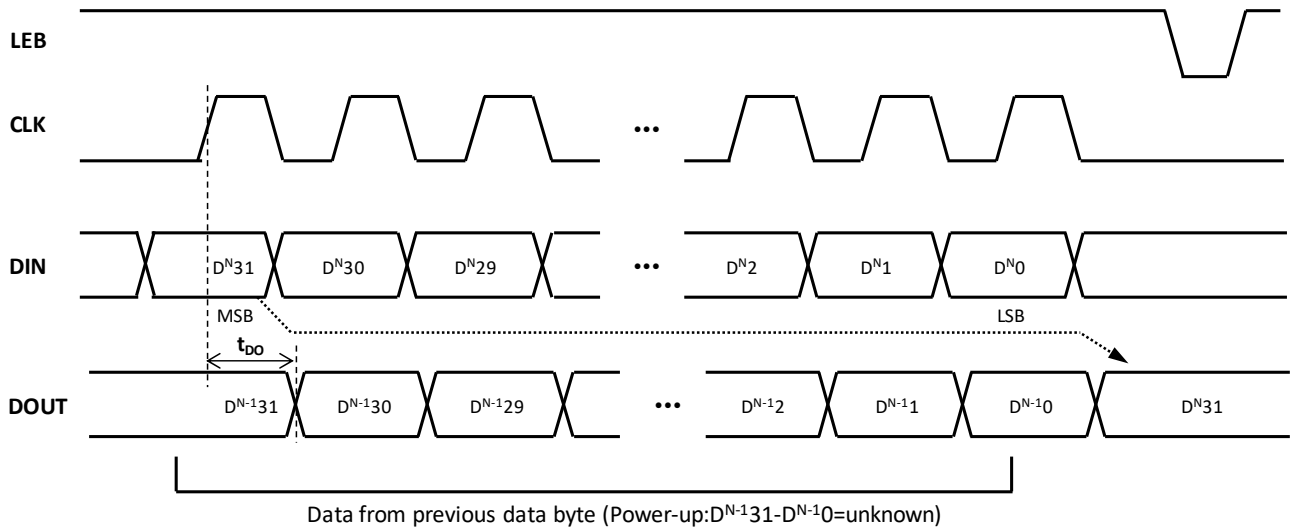

Figure 4 Latch Enable Interface Timing

■ Pin Configuration

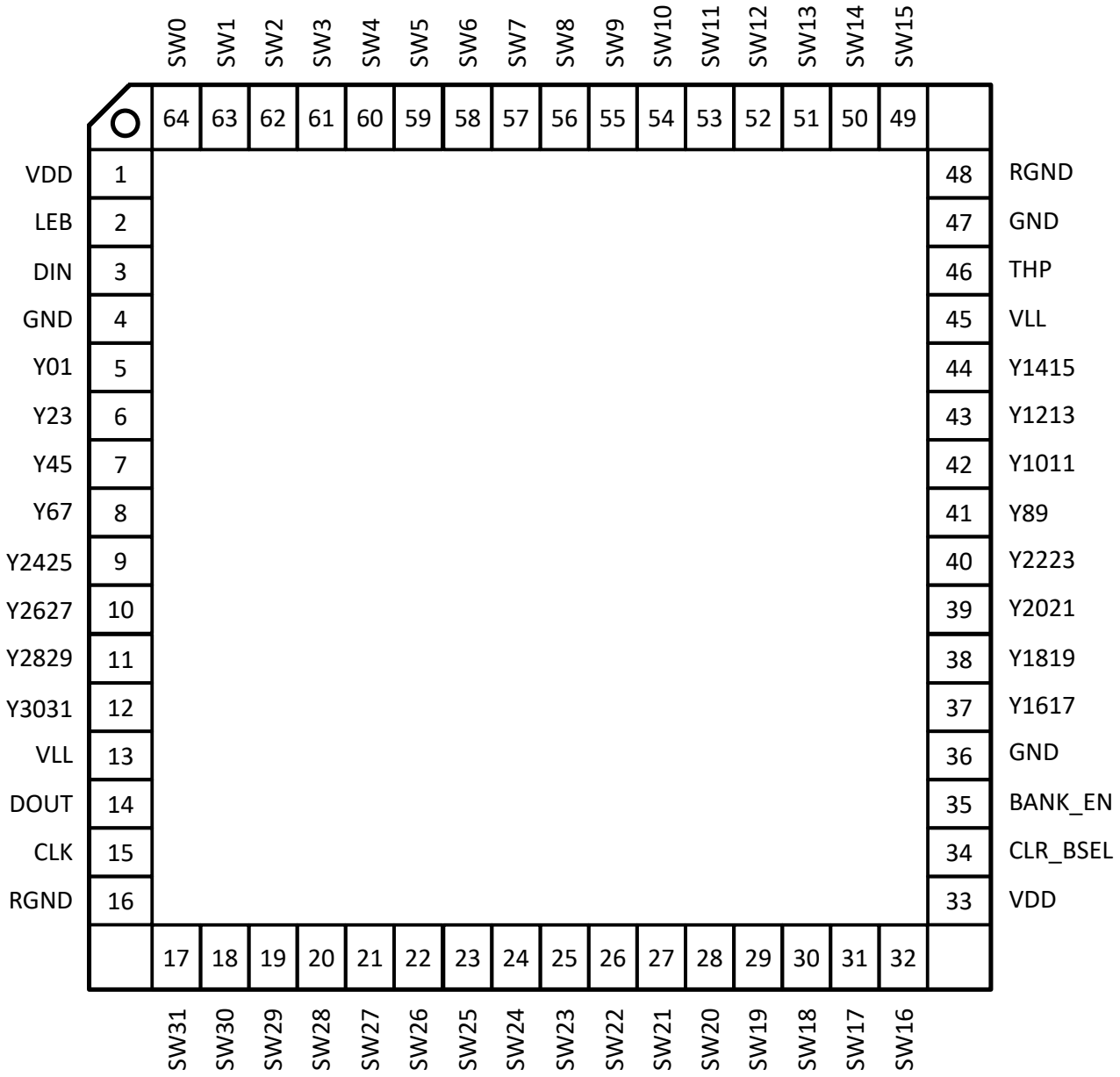

Figure 5 Pin Configuration

Table 7 Pin Configuration (1 / 2)

Pin#	Pin Name	I/O	Function
1	VDD	-	Positive low voltage power supply (+5V)
2	LEB	I	Active-Low latch enable input, Hi=Hold data, Low=Latch data input
3	DIN	I	Serial-Data (BANK_EN=0) / Bank-Data (BANK_EN=1) input
4	GND	-	Drive power ground (0V)
5	Y01	I/O	Analog switch terminal 0-1 (AFE side)
6	Y23	I/O	Analog switch terminal 2-3 (AFE side)
7	Y45	I/O	Analog switch terminal 4-5 (AFE side)
8	Y67	I/O	Analog switch terminal 6-7 (AFE side)
9	Y2425	I/O	Analog switch terminal 24-25 (AFE side)
10	Y2627	I/O	Analog switch terminal 26-27 (AFE side)
11	Y2829	I/O	Analog switch terminal 28-29 (AFE side)
12	Y3031	I/O	Analog switch terminal 30-31 (AFE side)
13	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
14	DOUT	O	Serial-Data output
15	CLK	I	Serial-Clock input
16	RGND	-	Bleed resistor ground (0V)
17	SW31	I/O	Analog switch terminal 31 (Probe side)
18	SW30	I/O	Analog switch terminal 30 (Probe side)
19	SW29	I/O	Analog switch terminal 29 (Probe side)
20	SW28	I/O	Analog switch terminal 28 (Probe side)
21	SW27	I/O	Analog switch terminal 27 (Probe side)
22	SW26	I/O	Analog switch terminal 26 (Probe side)
23	SW25	I/O	Analog switch terminal 25 (Probe side)
24	SW24	I/O	Analog switch terminal 24 (Probe side)
25	SW23	I/O	Analog switch terminal 23 (Probe side)
26	SW22	I/O	Analog switch terminal 22 (Probe side)
27	SW21	I/O	Analog switch terminal 21 (Probe side)
28	SW20	I/O	Analog switch terminal 20 (Probe side)
29	SW19	I/O	Analog switch terminal 19 (Probe side)
30	SW18	I/O	Analog switch terminal 18 (Probe side)
31	SW17	I/O	Analog switch terminal 17 (Probe side)
32	SW16	I/O	Analog switch terminal 16 (Probe side)

Table 7 Pin Configuration (2 / 2)

Pin#	Pin Name	I/O	Function
33	VDD	-	Positive low voltage power supply (+5V)
34	CLR_BSEL	I	Shift register and latch clear input (BANK_EN=0), Bank-switching selection, Low=Even channels, Hi=Odd channels (BANK_EN=1)
35	BANK_EN	I	Logic interface control, Hi=Bank interface, Low=Serial data interface
36	GND	-	Drive power ground (0V)
37	Y1617	I/O	Analog switch terminal 16-17 (AFE side)
38	Y1819	I/O	Analog switch terminal 18-19 (AFE side)
39	Y2021	I/O	Analog switch terminal 20-21 (AFE side)
40	Y2223	I/O	Analog switch terminal 22-23 (AFE side)
41	Y89	I/O	Analog switch terminal 8-9 (AFE side)
42	Y1011	I/O	Analog switch terminal 10-11 (AFE side)
43	Y1213	I/O	Analog switch terminal 12-13 (AFE side)
44	Y1415	I/O	Analog switch terminal 14-15 (AFE side)
45	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
46	THP	O	Thermal protection output flag, open N-MOS drain
47	GND	-	Drive power ground (0V)
48	RGND	-	Bleed resistor ground (0V)
49	SW15	I/O	Analog switch terminal 15 (Probe side)
50	SW14	I/O	Analog switch terminal 14 (Probe side)
51	SW13	I/O	Analog switch terminal 13 (Probe side)
52	SW12	I/O	Analog switch terminal 12 (Probe side)
53	SW11	I/O	Analog switch terminal 11 (Probe side)
54	SW10	I/O	Analog switch terminal 10 (Probe side)
55	SW9	I/O	Analog switch terminal 9 (Probe side)
56	SW8	I/O	Analog switch terminal 8 (Probe side)
57	SW7	I/O	Analog switch terminal 7 (Probe side)
58	SW6	I/O	Analog switch terminal 6 (Probe side)
59	SW5	I/O	Analog switch terminal 5 (Probe side)
60	SW4	I/O	Analog switch terminal 4 (Probe side)
61	SW3	I/O	Analog switch terminal 3 (Probe side)
62	SW2	I/O	Analog switch terminal 2 (Probe side)
63	SW1	I/O	Analog switch terminal 1 (Probe side)
64	SW0	I/O	Analog switch terminal 0 (Probe side)

■ Package

Table 8 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-64(0909)B	QN064-B-P-SD	QN064-B-T-SD	QN064-B-M-S1	QN064-B-L-SD	QN064-B-K-SD

■ Storage, Mounting

1. Storage conditions

1. 1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Figure 6 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

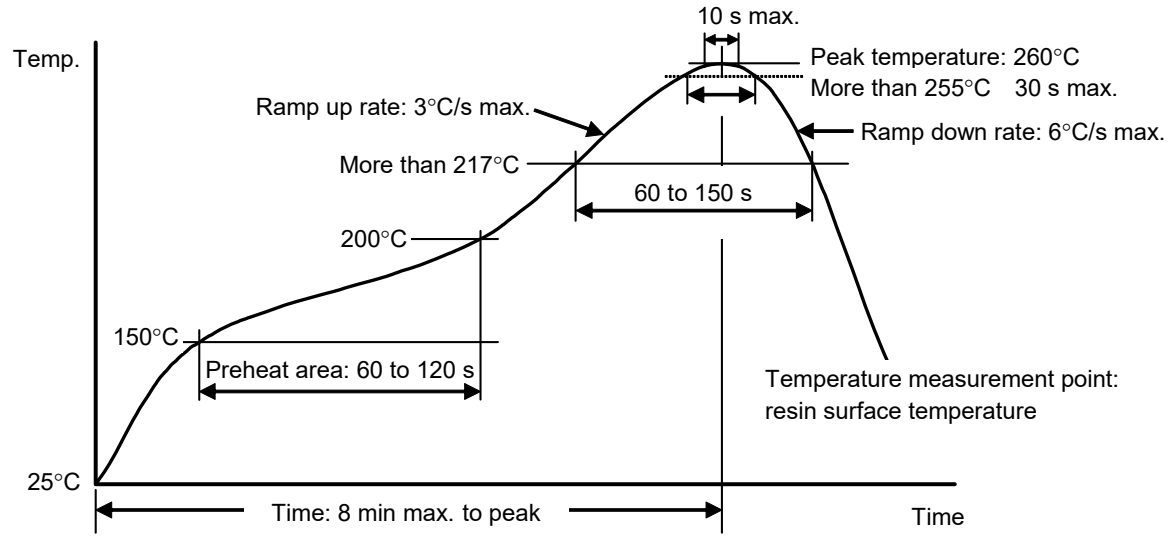

Figure 6 Resistance to Soldering Heat Condition for Package (Reflow Method)

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■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.

1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1. 4 Prevent friction with other materials made with high polymer.

1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

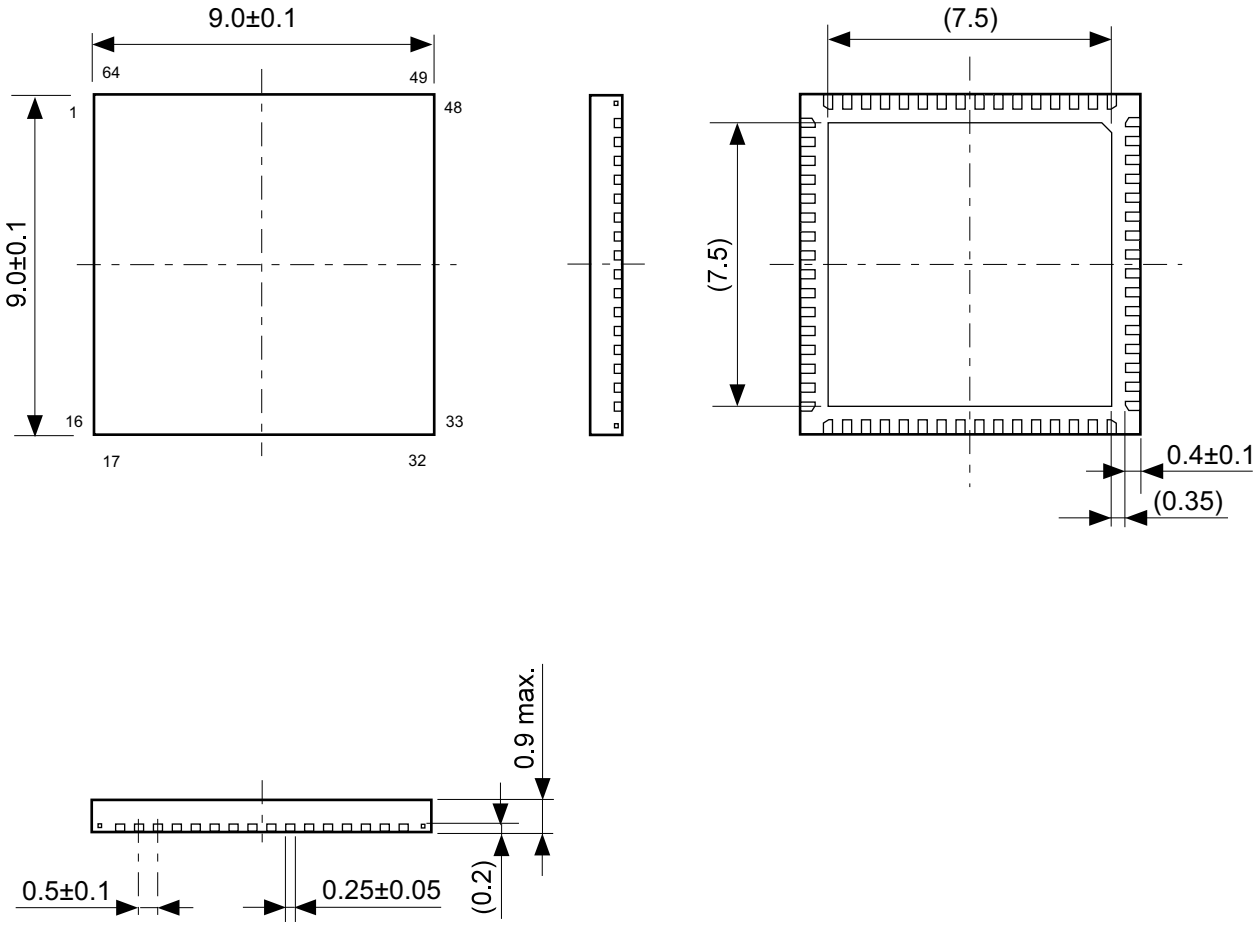
1. 6 Avoid dealing with or storing products in an extremely arid environment.

2. "Absolute maximum ratings" should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.



No. QN064-B-P-SD-1.0

TITLE	QFN64-B-PKG Dimensions
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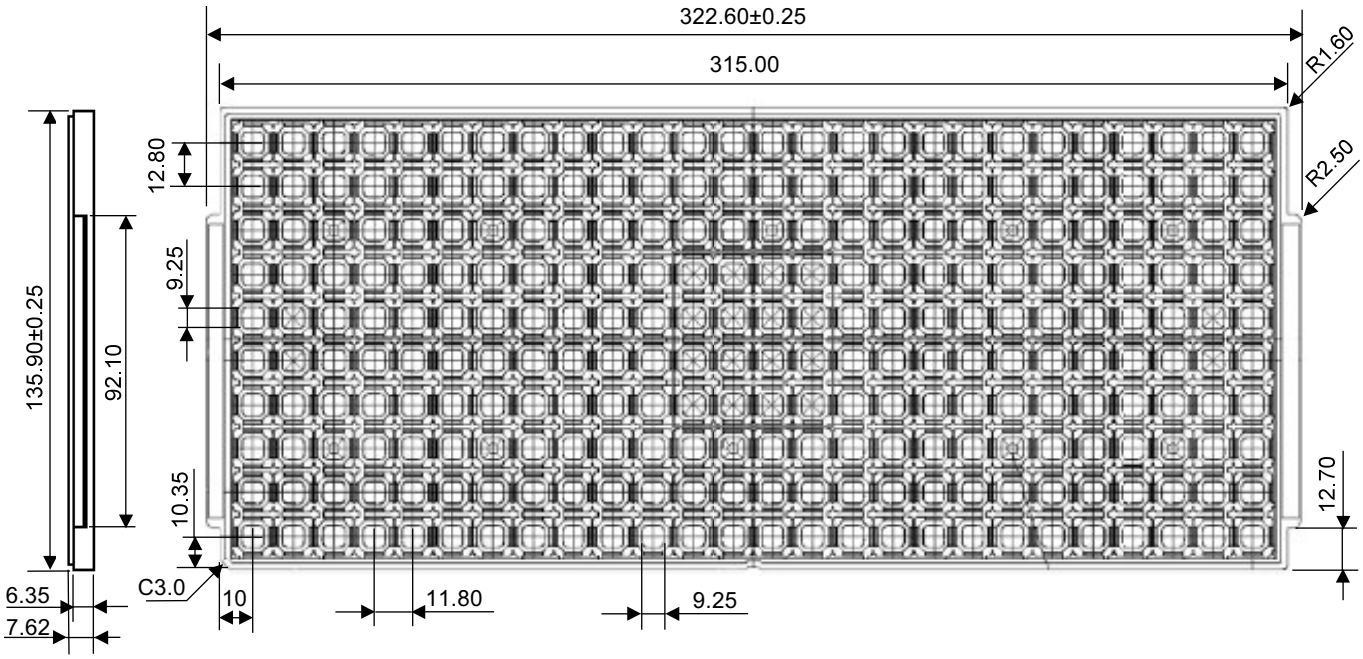
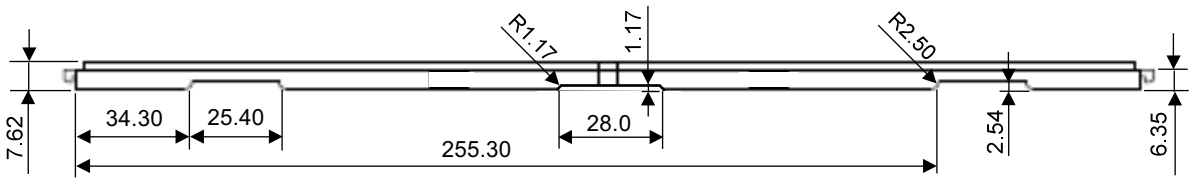
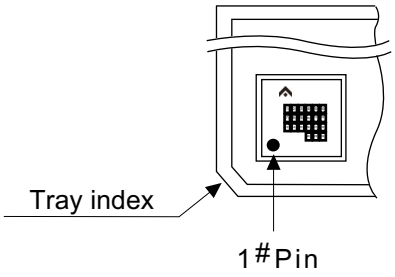
ANGLE	
UNIT	mm
ABLIC Inc.	



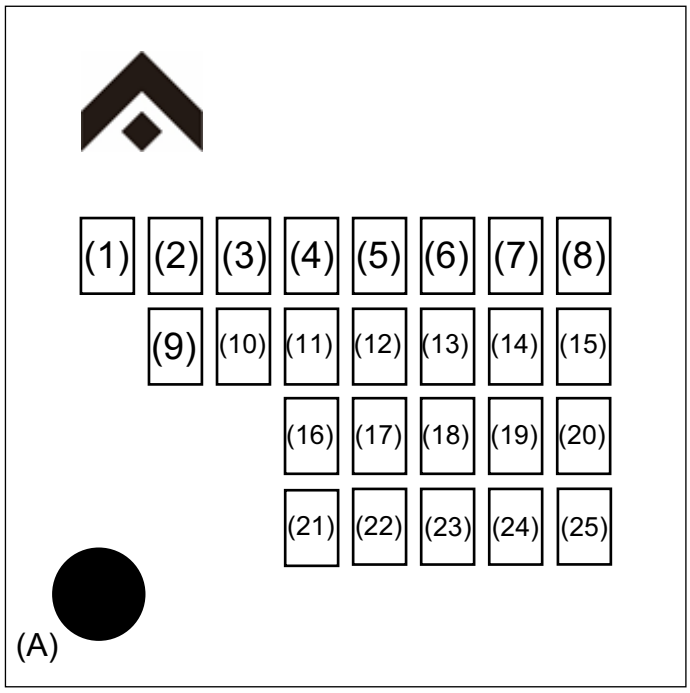


(Direction of IC in tray)



No. QN064-B-T-SD-1.0

TITLE	QFN64-B-Tray		
No.	QN064-B-T-SD-1.0		
ANGLE		QTY.	260
UNIT	mm		
ABLIC Inc.			



(1) to (10) : Product code

(11) , (12) : Quality control code

(13) : Year of assembly

(14) : Month of assembly

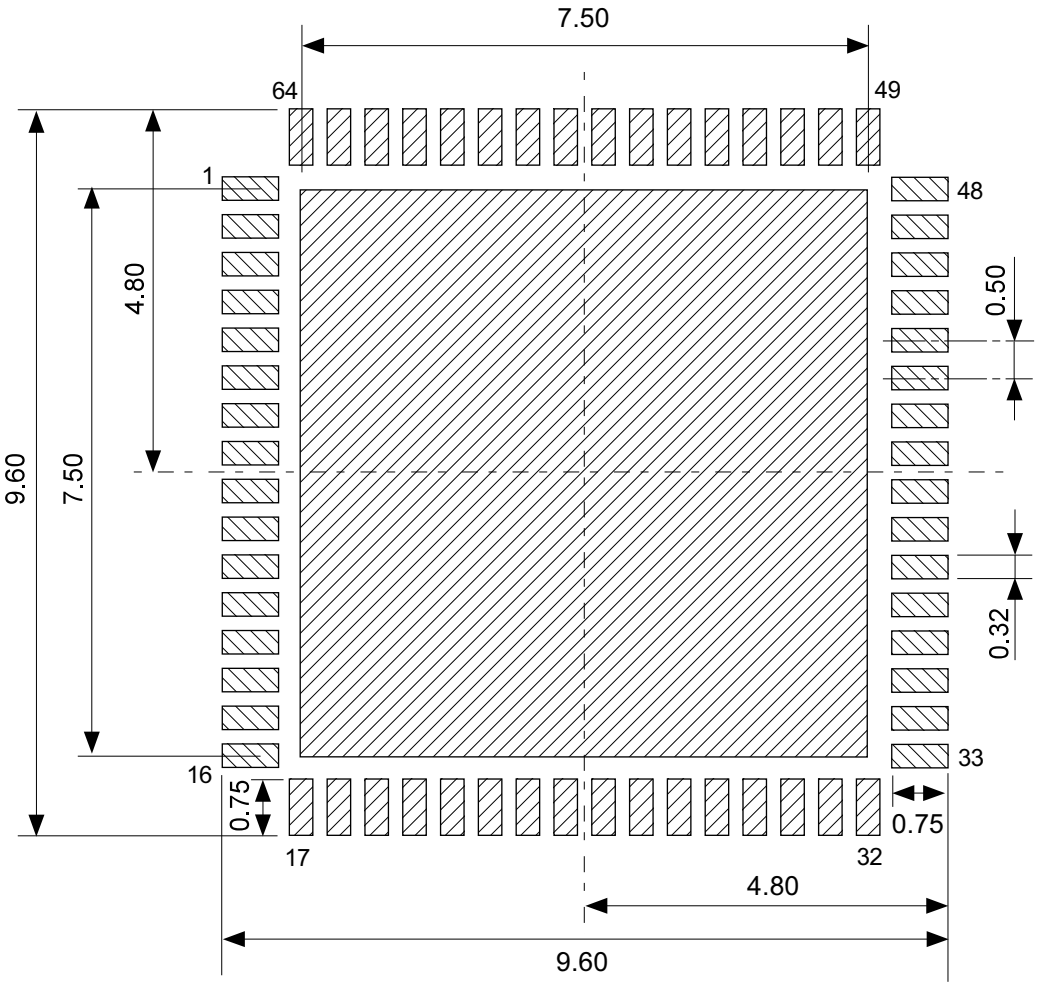
(15) : Week of assembly

(16) to (25) : Quality control code

(A) : 1-pin mark

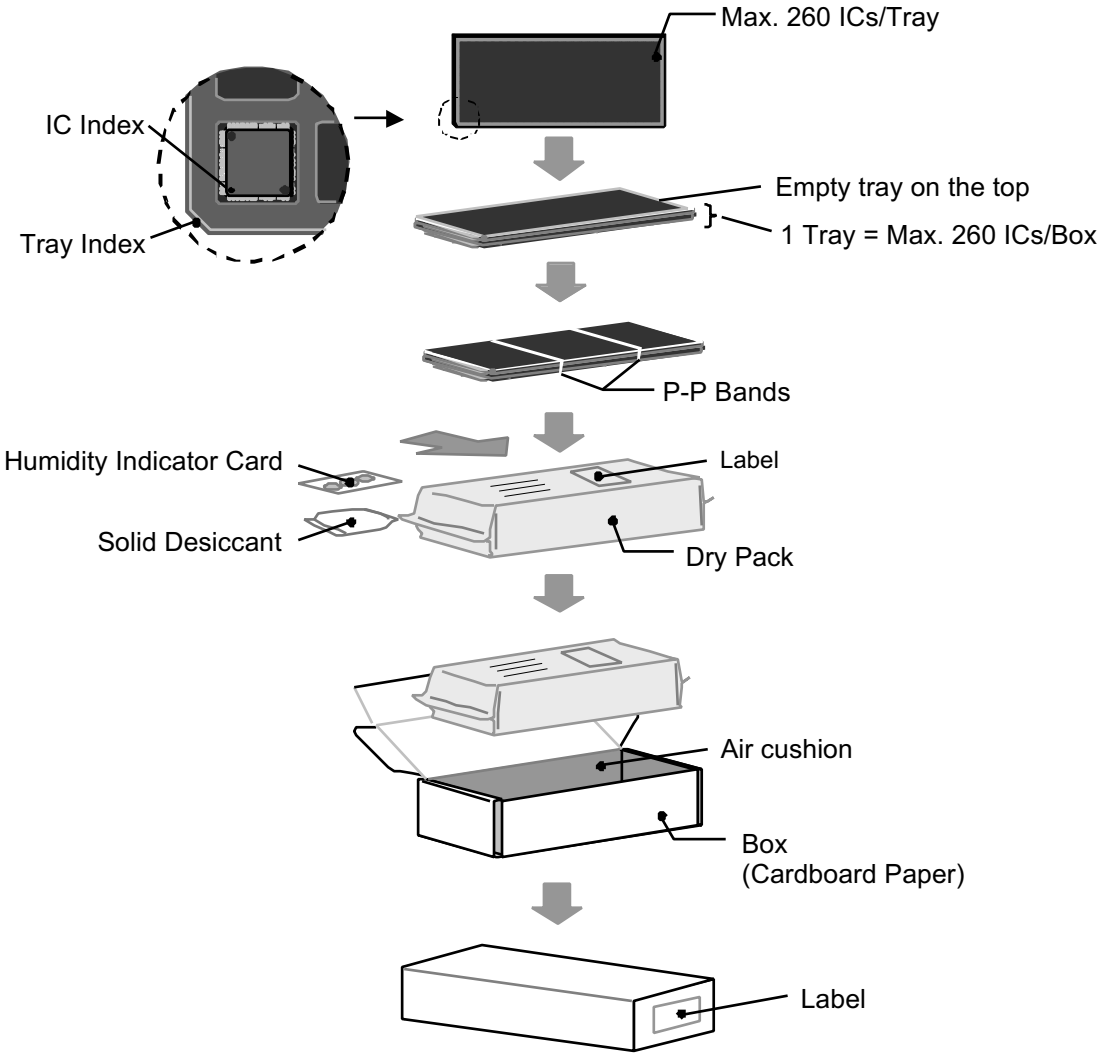
No. QN064-B-M-S1-1.0

TITLE	QFN64-B-Markings		
No.	QN064-B-M-S1-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



No. QN064-B-L-SD-1.0

TITLE	QFN64-B -Land Recommendation
No.	QN064-B-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



TITLE	QFN64-B -Packing Procedure
No.	QN064-B-K-SD-2.0
ANGLE	
UNIT	
ABLIC Inc.	

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