S-UM6524

LOW CHARGE INJECTION 32-CHANNEL 4 Ω HIGH-VOLTAGE ANALOG SWITCHES

Rev.1.0_00

The ABLIC S-UM6524 is a low charge injection 32-channel single-pole single-throw (SPST) high-voltage analog switch IC operated only by a single 5 V for ultrasound imaging applications. The S-UM6524 has ±100 V analog signal range allowing up to ±150 V voltage overshoot.

■ Function

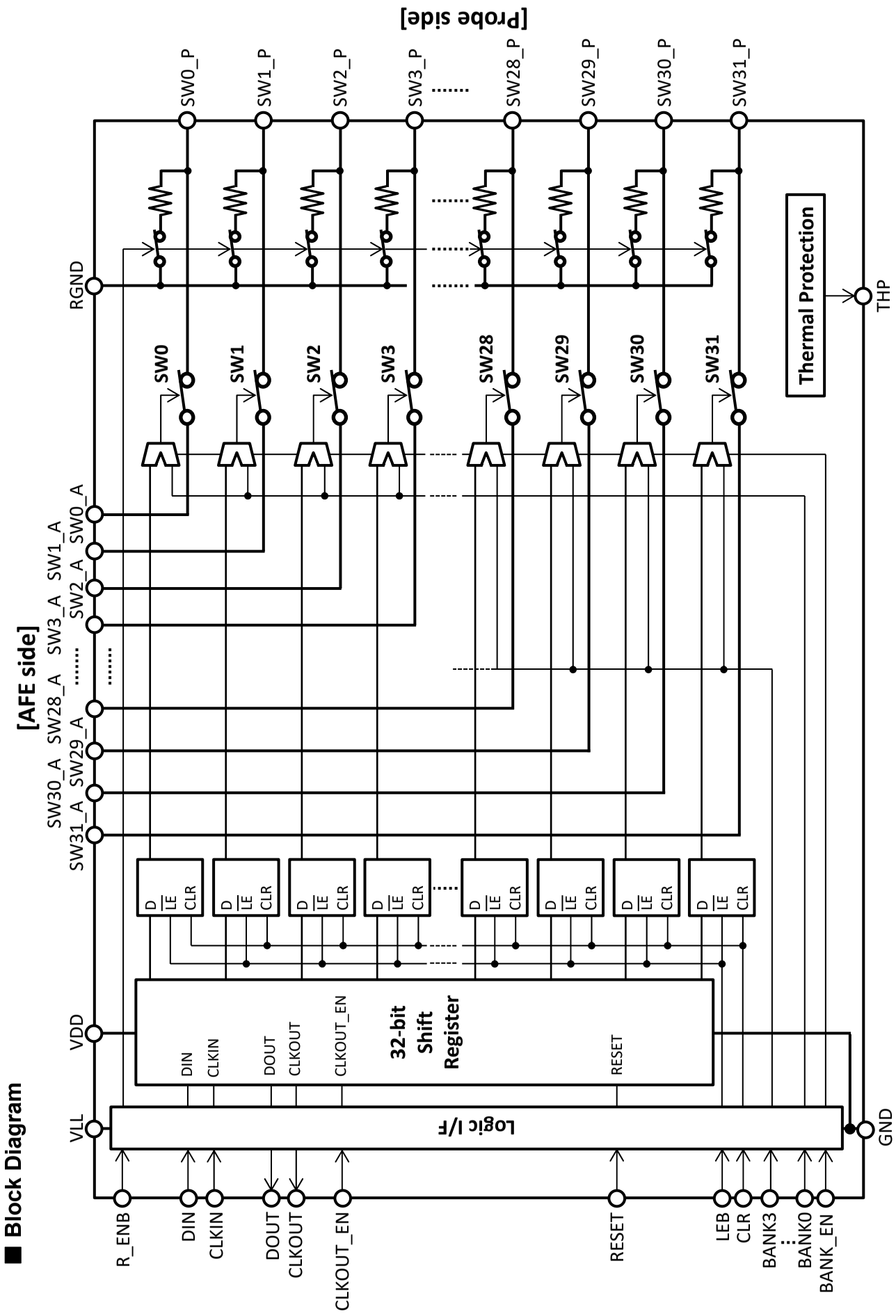
- 32-channel high-voltage SPST analog switches with user-selectable logic interface and bleed resistor

■ Features

- 0 V to ±100 V analog signal voltage range allowing up to ±150 V voltage overshoot
- 10 kHz to 75 MHz analog signal frequency range
- 2 A peak analog signal current per channel
- 4 Ω switch on-resistance
- Single +5 V power supply (NO HIGH-VOLTAGE POWER SUPPLY required)
- User-selectable Serial Digital Interface (32-bit shift registers) or Bank Interface (4 banks of 8-channel)
- User-selectable 40 kΩ bleed resistor on probe side
- Low on/off-capacitance
- 15 pC charge injection to 1000 pF
- -75 dB off-isolation at analog small-signal 5 MHz
- -60 dB switch crosstalk
- 1.8 V to 5 V CMOS logic interface
- Low power dissipation (static 5 mW)
- Embedded thermal protection with flag indicator
- RoHS compliant 13 × 13 mm BGA package

■ Contents

■ Block Diagram



■ Absolute Maximum Ratings

T_A = 25°C unless otherwise noted.

No.	Items	Symbol	Value	Unit	Condition
1	Positive logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Logic input voltage	DIN, CLKIN, RESET, CLR, LEB, BANK0, BANK1, BANK2, BANK3, BANK_EN, CLKOUT_EN, R_ENB	-0.4 to +7	V	
4	Logic output voltage	DOUT, CLKOUT, THP	-0.4 to +7	V	
5	Analog signal range (steady state voltage)	V_{SIG}	-105 to +105	V	
6	Analog signal range (peak overshoot voltage)	V_{SIG_OS}	-150 to +150	V	500 ns max. pulse width
7	Peak analog signal current per channel	I_{SW}	2	A	
8	Operating junction temperature	T_{Jop}	-20 to +150	°C	
9	Storage temperature	T_{STG}	-55 to +150	°C	
10	Maximum power dissipation	P_{Dmax}	4	W	

■ Operating Supply Voltages, Temperature, Logic Levels

T_A = 25°C unless otherwise noted.

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Condition
1	Logic supply voltage	V_{LL}	1.7	1.8 to 5	V_{DD}	V	
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	Operating free-air temperature	T_A	0	-	75	°C	
4	High-level logic input voltage	V_{IH}	0.8 × V_{LL}	-	V_{LL}	V	
5	Low-level logic input voltage	V_{IL}	0	-	0.2 × V_{LL}	V	
6	High-level logic output voltage	V_{OH}	0.8 × V_{LL}	-	-	V	I_{SOURCE} = 1 mA
7	Low-level logic output voltage	V_{OL}	-	-	0.2 × V_{LL}	V	I_{SINK} = 1 mA
8	Logic input high current *1)	I_{IH}	-10	-	10	µA	DIN, CLKIN, RESET, CLR, LEB, BANK0, BANK1, BANK2, BANK3, BANK_EN, CLKOUT_EN, R_ENB
9	Logic input low current	I_{IL}	-10	-	10	µA	
10	Logic input capacitance	C_{IN}	-	2	-	pF	
11	Clock frequency	f_{CLK}	-	-	50	MHz	CLKOUT_EN = 0, V_{LL} = 1.8 V
			-	-	80	MHz	CLKOUT_EN = 0, V_{LL} = 2.5 V
			-	-	95	MHz	CLKOUT_EN = 0, V_{LL} = 3.3 V
			-	-	60	MHz	CLKOUT_EN = 1, V_{LL} = 1.8 V
			-	-	85	MHz	CLKOUT_EN = 1, V_{LL} = 2.5 V
			-	-	130	MHz	CLKOUT_EN = 1, V_{LL} = 3.3 V
12	Clock rise and fall times	t_R, t_F	-	-	50	ns	
13	CLKIN to DOUT delay	t_{DO}	7	10	24	ns	
14	CLKOUT to DOUT delay	t_{DO1}	1.3	-	1.9	ns	
15	CLKIN to CLKOUT delay	t_{DCKO}	7	10	24	ns	
16	DIN to CLKIN setup time	t_{SU}	1	-	-	ns	
17	DIN to CLKIN hold time	t_{HD}	2	-	-	ns	
18	LEB setup time	t_{SLEB}	5	-	-	ns	
19	LEB low-pulse width	t_{WLEB}	12	-	-	ns	
20	CLR response time	t_{DCLR}	-	-	500	ns	
21	CLR high-pulse width	t_{WCLR}	12	-	-	ns	
22	Bank interface setup time	t_{SBNK}	100	-	-	ns	
23	Bank interface hold time	t_{HBNK}	1	-	-	ms	
24	BANKx minimum pulse width	t_{WBNK}	4	-	-	µs	
25	RESET response time	t_{DRST}	-	-	400	ns	
26	RESET high-pulse width	t_{WRST}	12	-	-	ns	

NOTE: *1) BANK_EN, CLKOUT_EN, and R_ENB have 100 µA leakage at V_{LL} = 5 V due to 50 kΩ internal pull-down resistor.

■ Power Supply Sequencing

No power supply sequencing is required even if V_{LL} is different from V_{DD}.
Please apply the V_{DD} voltage to the V_{LL} when operating with a single 5 V.

■ DC Characteristics

V_{LL} = 3.3 V, V_{DD} = 5 V, LEB = 0, T_A = 25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Unit	Conditions
			Min.	Typ.	Max.		
1	Analog signal range (steady state voltage)	V_{SIG}	-100	-	+100	V	
2	Analog signal range (peak overshoot voltage)	V_{SIG_OS}	-150	-	+150	V	500 ns max. pulse width
3	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	µA	Quiescent current-1 All switches off
4	V_{DD} quiescent current	I_{DDQ}	-	2.6	-	mA	
5	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	µA	Quiescent current-2 All switches on
6	V_{DD} quiescent current	I_{DDQ}	-	2.6	-	mA	
7	V_{LL} dynamic current	I_{LL}	-	2	10	µA	Dynamic current All channels switching simultaneously at f_{SW} = 50 kHz
8	V_{DD} dynamic current	I_{DD}	-	5.8	6.8	mA	
9	DC offset switch off	V_{OS}	-	0	-	mV	
10	Small signal switch on-resistance	R_{ONS}	-	4	6	Ω	V_{SIG} = 0.1 Vpp to 5 Vpp (5 MHz, R_S = 10 Ω)
11	Small signal switch on-resistance matching	ΔR_{ONS}	-	2	5	%	V_{SIG} = 0 V, I_{SIG} = 5 mA
12	Large signal switch on-resistance	R_{ONL}	-	4	-	Ω	V_{SIG} = 20 Vpp (5 MHz, R_S = 10 Ω)
13	Bleed resistance	R_{BLD}	30	40	50	kΩ	R_ENB = 0, probe side only
14	Switch output peak current	I_{SW}	-	2	-	A	100 ns pulse, 0.1% duty cycle

■ Thermal Protection Characteristics

V_{LL} = 3.3 V, V_{DD} = 5 V, LEB = 0, T_A = 25°C, unless otherwise specified.

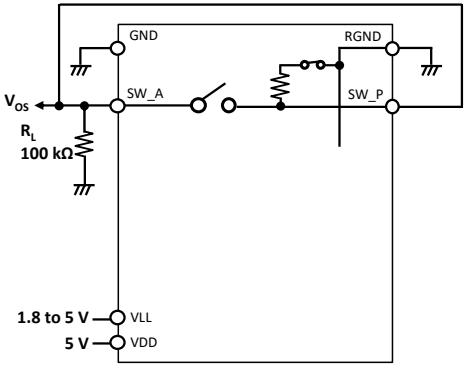
No.	Items	Symbol	Spec			Unit	Conditions
			Min.	Typ.	Max.		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, V_{LL} = 3.3 V, I_{THP} = 1 mA
4	THP temperature threshold	T_{THP}	90	110	130	ºC	Thermal protection flag indicator by THP pin (open N-MOS drain, Low = THP activating)
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	ºC	

■ AC Characteristics

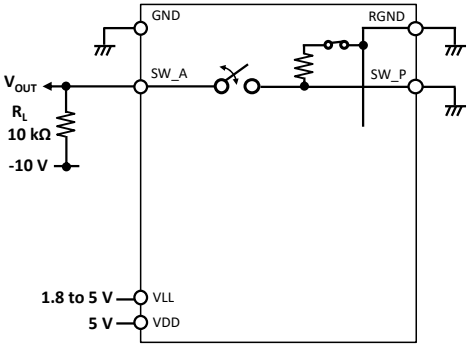
V_{LL} = 3.3V, V_{DD} = 5 V, LEB = 0, T_A = 25°C, unless otherwise specified.

No.	Items		Symbol	Spec			Unit	Conditions
				Min.	Typ.	Max.		
1	Turn-on time		t_{ON}	-	2	4	µs	BANK_EN = 0
			t_{ON_BNK}	-	2	4	µs	BANK_EN = 1
2	Turn-off time		t_{OFF}	-	2	4	µs	BANK_EN = 0
			t_{OFF_BNK}	-	2	4	µs	BANK_EN = 1
3	Output switching frequency		f_{SW}	-	-	50	kHz	Duty cycle = 50%
4	Small signal frequency		f_{SIG}	0.01	-	75	MHz	C_L = 220 pF
5	Off isolation	small signal	$V_{ISO(RX)}$	-	-75	-	dB	f_{SIG} = 5 MHz, R_L = 50 Ω
		large signal	$V_{ISO(TX)}$	-	-65	-	dB	f_{SIG} = 5 MHz, R_L = 50 Ω
6	Crosstalk		V_{CT}	-	-60	-	dB	f_{SIG} = 5 MHz, R_L = 50 Ω
7	On capacitance	small signal	$C_{ON(RX)}$	-	38	-	pF	V_{SIG} = 0 V, f_{SIG} = 1 MHz
		large signal	$C_{ON(TX)}$	-	45	-	pF	V_{SIG} = 10 Vpp, f_{SIG} = 1 MHz
8	Off capacitance SW_P to GND	small signal	$C_{OFF(SWP\_RX)}$	-	20	-	pF	V_{SIG} = 0 V, f_{SIG} = 1 MHz
9	Off capacitance SW_A to GND	small signal	$C_{OFF(SWA\_RX)}$	-	16	-	pF	V_{SIG} = 0 V, f_{SIG} = 1 MHz
		large signal	$C_{OFF(SWA\_TX)}$	-	33	-	pF	V_{SIG} = 10 Vpp, f_{SIG} = 1 MHz
10	Output spike voltage (SW_P)		$V_{SPK\_ON(SWP)}$	-	30	-	mV	50 Ω load (switch on)
			$V_{SPK\_OFF(SWP)}$	-	60	-	mV	50 Ω load (switch off)
11	Output spike voltage (SW_A)		$V_{SPK\_ON(SWA)}$	-	30	-	mV	50 Ω load (switch on)
			$V_{SPK\_OFF(SWA)}$	-	60	-	mV	50 Ω load (switch off)
12	Charge injection		QC	-	15	-	pC	

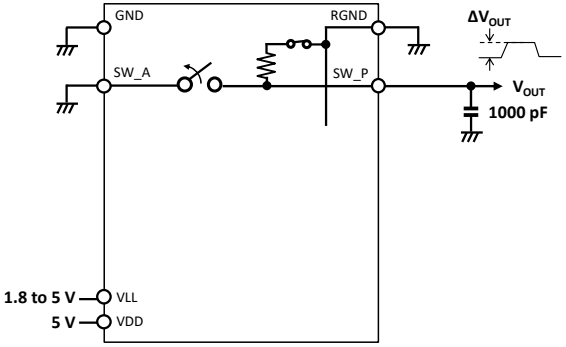
■ Test Circuits



DC Offset OFF

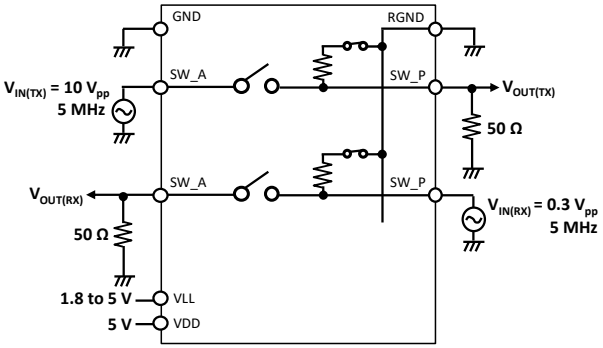


t_{ON}/t_{OFF} test circuit



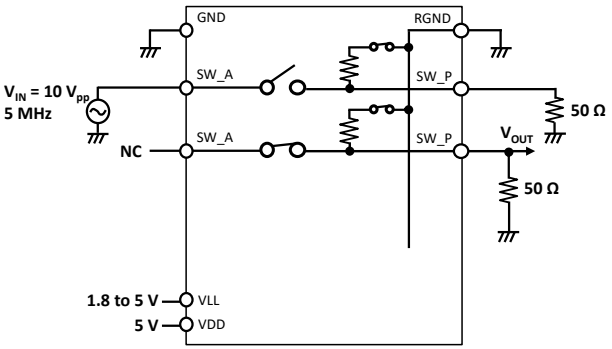
$Q = 1000\ pF \times \Delta V_{OUT}$

Charge Injection



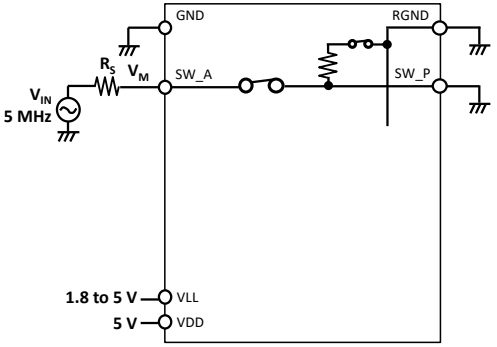
$V_{ISO} = 20Log(V_{OUT}/V_{IN})$

Off isolation



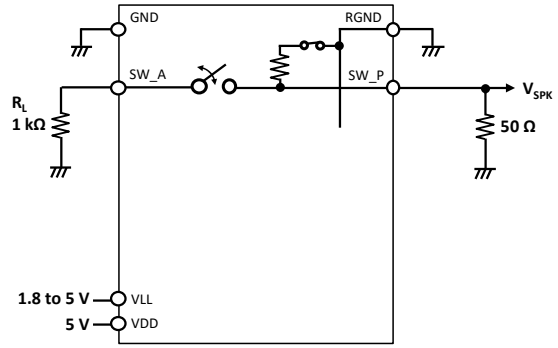
$V_{CT} = 20Log(V_{OUT}/V_{IN})$

Crosstalk

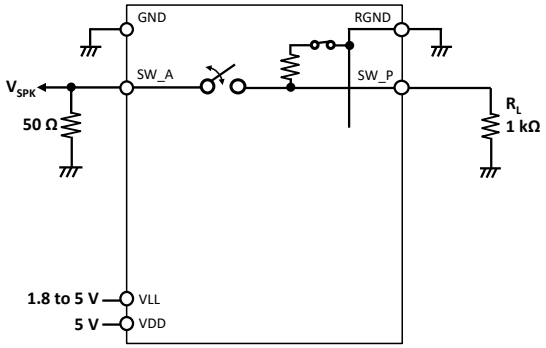


$R_{ON} = R_S \times V_M / (V_{IN} - V_M)$

On resistance test circuit



Output spike voltage SW_P

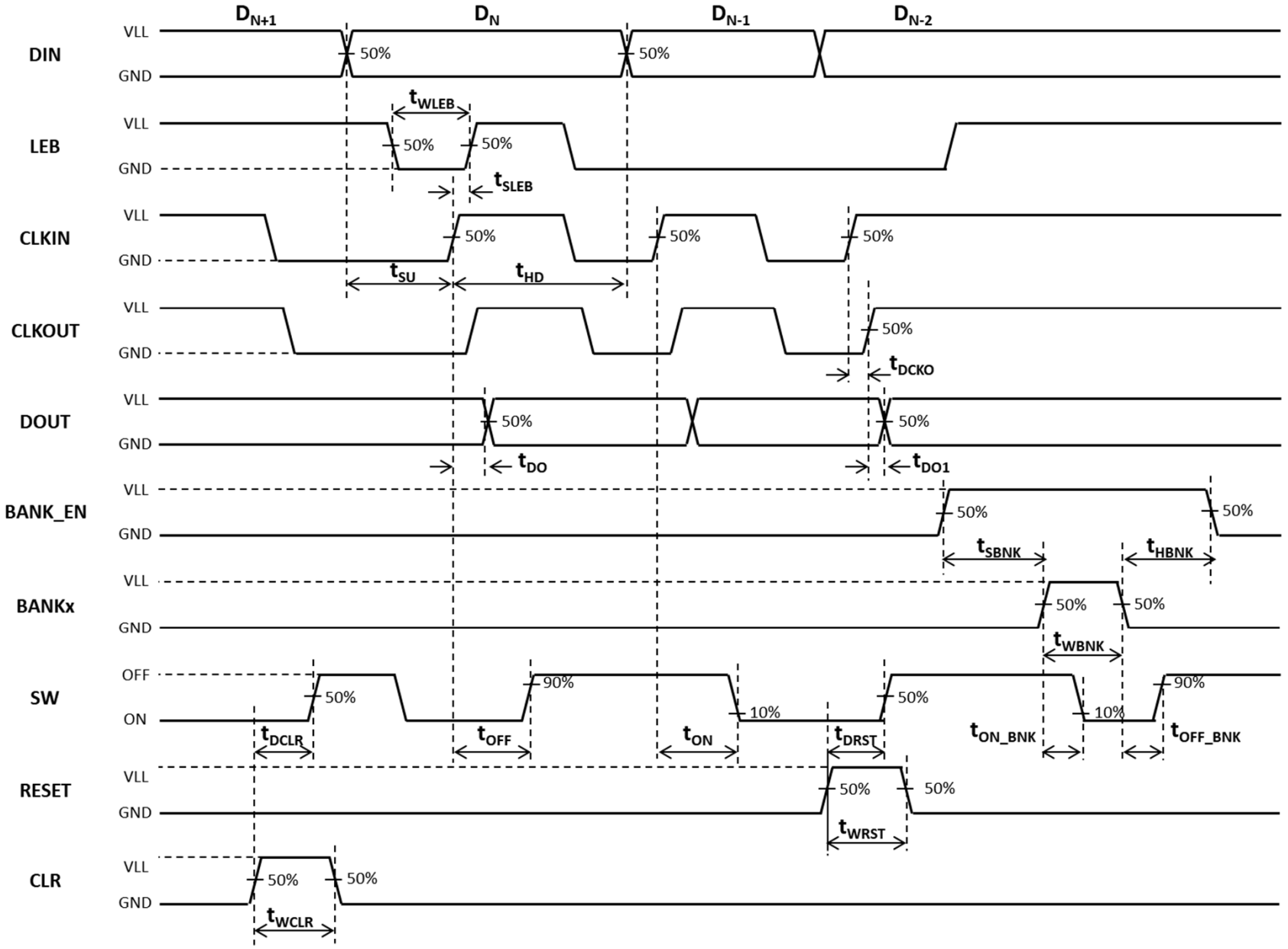


Output spike voltage SW_A

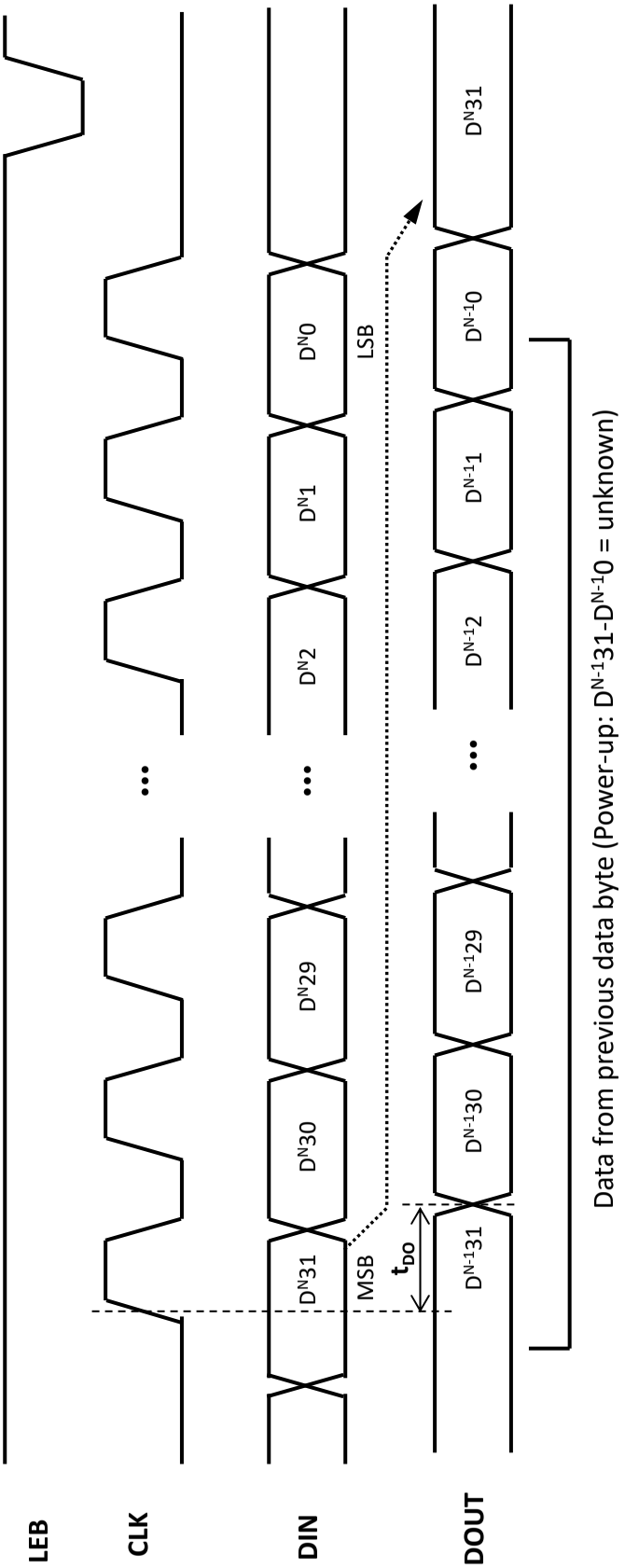
■ Truth Table

Logic Inputs																						Analog Switch State																	
RESET	LEB	CLR	BANK_EN	BANK0	BANK1	BANK2	BANK3	DIN																																
								D0	…	D7	D8	…	D15	D16	…	D23	D24	…	D31	SW0	…	SW7	SW8	…	SW15	SW16	…	SW23	SW24	…	SW31									
L	L	L	L	X	X	X	X	L		-	-		-	-		-	-		-	OFF		-	-		-	-		-	-		-							
L	L	L	L	X	X	X	X	H		-	-		-	-		-	-		-	ON		-	-		-	-		-	-		-							
L	L	L	L	X	X	X	X	-		L	-		-	-		-	-		-	-		OFF	-		-	-		-	-		-							
L	L	L	L	X	X	X	X	-		H	-		-	-		-	-		-	-		ON	-		-	-		-	-		-							
L	L	L	L	X	X	X	X	-		-	L		-	-		-	-		-	-		-	OFF		-	-		-	-		-							
L	L	L	L	X	X	X	X	-		-	H		-	-		-	-		-	-		-	ON		-	-		-	-		-							
L	L	L	L	X	X	X	X	-		-	-		L	-		-	-		-	-		-	-		OFF	-		-	-		-							
L	L	L	L	X	X	X	X	-	…	-	-	…	H	-	…	-	-	…	-	-	…	-	-	…	ON	-	…	-	-	…	-							
L	L	L	L	X	X	X	X	-		-	-		-	L		-	-		-	-		-	-		-	OFF		-	-		-							
L	L	L	L	X	X	X	X	-		-	-		-	H		-	-		-	-		-	-		-	ON		-	-		-							
L	L	L	L	X	X	X	X	-		-	-		-	-		L	-		-	-		-	-		-	-		OFF	-		-							
L	L	L	L	X	X	X	X	-		-	-		-	-		H	-		-	-		-	-		-	-		ON	-		-							
L	L	L	L	X	X	X	X	-		-	-		-	-		-	L		-	-		-	-		-	-		-	OFF		-							
L	L	L	L	X	X	X	X	-		-	-		-	-		-	H		-	-		-	-		-	-		-	ON		-							
L	L	L	L	X	X	X	X	-		-	-		-	-		-	-		L	-		-	-		-	-		-	-		OFF							
L	L	L	L	X	X	X	X	-		-	-		-	-		-	-		H	-		-	-		-	-		-	-		ON							
L	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Hold Previous State																			
L	X	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	ALL SWs OFF																			
H	H	L	L	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	Hold Previous State																			
H	L	L	L	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	ALL SWs OFF																			
X	X	X	H	**H**	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	**SW0 to SW7 ON**			SW8 to SW15 OFF			SW16 to SW23 OFF			SW24 to SW31 OFF										
X	X	X	H	L	**H**	L	L	X	X	X	X	X	X	X	X	X	X	X	X	SW0 to SW7 OFF			**SW8 to SW15 ON**			SW16 to SW23 OFF			SW24 to SW31 OFF										
X	X	X	H	L	L	**H**	L	X	X	X	X	X	X	X	X	X	X	X	X	SW0 to SW7 OFF			SW8 to SW15 OFF			**SW16 to SW23 ON**			SW24 to SW31 OFF										
X	X	X	H	L	L	L	**H**	X	X	X	X	X	X	X	X	X	X	X	X	SW0 to SW7 OFF			SW8 to SW15 OFF			SW16 to SW23 OFF			**SW24 to SW31 ON**										

■ Logic Timing



■ Latch Enable Interface Timing



■ Pin Description

Pin Name	I/O	Function
VLL	-	Positive voltage supply of low voltage interface (+1.8 V to +5 V)
VDD	-	Positive low voltage power supply (+5 V)
GND	-	Drive power ground (0 V)
RGND	-	Bleed resistor ground (0 V)
DIN	I	Serial-Data input
DOUT	O	Serial-Data output
CLKIN	I	Serial-Clock input
CLKOUT	O	Serial-Clock output
LEB	I	Active-Low latch enable input, Hi = Hold data, Low = Latch data input
BANK0	I	Bank-Data input 0 for SW0 to SW7, Hi = ON, Low = OFF
BANK1	I	Bank-Data input 1 for SW8 to SW15, Hi = ON, Low = OFF
BANK2	I	Bank-Data input 2 for SW16 to SW23, Hi = ON, Low = OFF
BANK3	I	Bank-Data input 3 for SW24 to SW31, Hi = ON, Low = OFF
RESET	I	Shift register reset input
CLR	I	Latch clear input
CLKOUT_EN	I	Clock out enable input, Hi = Clock out, Low = Disable (Low)
R_ENB	I	Bleed resistor enable input, Hi = Disable, Low = Enable
BANK_EN	I	Bank interface enable input, Hi = Bank-Data interface , Low = Serial-Data interface
THP	O	Thermal protection output flag, open N-MOS drain (Low = THP activating)
SWx_A	I/O	Analog switch terminal n (AFE side), Suffix “x” corresponds to channel number (x = 0 to 31)
SWx_P	I/O	Analog switch terminal n (Probe side), Suffix “x” corresponds to channel number (x = 0 to 31)
NC	-	No connection (Not internally connected)

■ Pin Configuration (Table)

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
A1	VLL	B1	VDD	C1	NC	D1	SW31_A	E1	NC	F1	NC	G1	SW29_A	H1	NC	J1	NC	K1	SW27_A
A2	DIN	B2	LEB	C2	NC	D2	NC	E2	SW30_A	F2	NC	G2	NC	H2	SW28_A	J2	NC	K2	NC
A3	CLKIN	B3	RESET	C3	NC	D3	SW31_P	E3	NC	F3	NC	G3	SW29_P	H3	NC	J3	NC	K3	SW27_P
A4	GND	B4	RGND	C4	NC	D4	NC	E4	SW30_P	F4	NC	G4	NC	H4	SW28_P	J4	NC	K4	NC
A5	NC	B5	NC	C5	NC	D5	NC	E5	NC	F5	NC	G5	NC	H5	NC	J5	NC	K5	NC
A6	NC	B6	SW0_A	C6	NC	D6	SW0_P	E6	NC	F6	NC	G6	-	H6	-	J6	-	K6	-
A7	SW1_A	B7	NC	C7	SW1_P	D7	NC	E7	NC	F7	-	G7	GND	H7	GND	J7	GND	K7	GND
A8	NC	B8	NC	C8	NC	D8	NC	E8	NC	F8	-	G8	GND	H8	GND	J8	GND	K8	GND
A9	NC	B9	SW2_A	C9	NC	D9	SW2_P	E9	NC	F9	-	G9	GND	H9	GND	J9	GND	K9	GND
A10	SW3_A	B10	NC	C10	SW3_P	D10	NC	E10	NC	F10	-	G10	GND	H10	GND	J10	GND	K10	GND
A11	NC	B11	NC	C11	NC	D11	NC	E11	NC	F11	-	G11	GND	H11	GND	J11	GND	K11	GND
A12	NC	B12	SW4_A	C12	NC	D12	SW4_P	E12	NC	F12	-	G12	GND	H12	GND	J12	GND	K12	GND
A13	SW5_A	B13	NC	C13	SW5_P	D13	NC	E13	NC	F13	-	G13	GND	H13	GND	J13	GND	K13	GND
A14	NC	B14	NC	C14	NC	D14	NC	E14	NC	F14	-	G14	-	H14	-	J14	-	K14	-
A15	NC	B15	SW6_A	C15	NC	D15	SW6_P	E15	NC	F15	NC	G15	NC	H15	NC	J15	NC	K15	NC
A16	SW7_A	B16	NC	C16	SW7_P	D16	NC	E16	NC	F16	SW8_P	G16	NC	H16	NC	J16	SW10_P	K16	NC
A17	NC	B17	NC	C17	NC	D17	NC	E17	NC	F17	NC	G17	SW9_P	H17	NC	J17	NC	K17	SW11_P
A18	VDD	B18	GND	C18	GND	D18	RGND	E18	NC	F18	SW8_A	G18	NC	H18	NC	J18	SW10_A	K18	NC
A19	THP	B19	VLL	C19	DOUT	D19	CLKOUT	E19	NC	F19	NC	G19	SW9_A	H19	NC	J19	NC	K19	SW11_A

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
L1	NC	M1	NC	N1	SW25_A	P1	NC	Q1	NC	R1	GND	S1	VDD3	T1	CLR	U1	BANK3
L2	SW26_A	M2	NC	N2	NC	P2	SW24_A	Q2	NC	R2	RGND	S2	CLKOUT_EN	T2	R_ENB	U2	BANK2
L3	NC	M3	NC	N3	SW25_P	P3	NC	Q3	NC	R3	NC	S3	NC	T3	NC	U3	NC
L4	SW26_P	M4	NC	N4	NC	P4	SW24_P	Q4	NC	R4	NC	S4	SW23_P	T4	NC	U4	SW23_A
L5	NC	M5	NC	N5	NC	P5	NC	Q5	NC	R5	SW22_P	S5	NC	T5	SW22_A	U5	NC
L6	-	M6	-	N6	-	P6	-	Q6	NC	R6	NC	S6	NC	T6	NC	U6	NC
L7	GND	M7	GND	N7	GND	P7	-	Q7	NC	R7	NC	S7	SW21_P	T7	NC	U7	SW21_A
L8	GND	M8	GND	N8	GND	P8	-	Q8	NC	R8	SW20_P	S8	NC	T8	SW20_A	U8	NC
L9	GND	M9	GND	N9	GND	P9	-	Q9	NC	R9	NC	S9	NC	T9	NC	U9	NC
L10	GND	M10	GND	N10	GND	P10	-	Q10	NC	R10	NC	S10	SW19_P	T10	NC	U10	SW19_A
L11	GND	M11	GND	N11	GND	P11	-	Q11	NC	R11	SW18_P	S11	NC	T11	SW18_A	U11	NC
L12	GND	M12	GND	N12	GND	P12	-	Q12	NC	R12	NC	S12	NC	T12	NC	U12	NC
L13	GND	M13	GND	N13	GND	P13	-	Q13	NC	R13	NC	S13	SW17_P	T13	NC	U13	SW17_A
L14	-	M14	-	N14	-	P14	-	Q14	NC	R14	SW16_P	S14	NC	T14	SW16_A	U14	NC
L15	NC	M15	NC	N15	NC	P15	NC	Q15	NC	R15	NC	S15	NC	T15	NC	U15	NC
L16	NC	M16	SW12_P	N16	NC	P16	NC	Q16	SW14_P	R16	NC	S16	NC	T16	GND	U16	GND
L17	NC	M17	NC	N17	SW13_P	P17	NC	Q17	NC	R17	SW15_P	S17	NC	T17	RGND	U17	BANK1
L18	NC	M18	SW12_A	N18	NC	P18	NC	Q18	SW14_A	R18	NC	S18	NC	T18	GND	U18	BANK0
L19	NC	M19	NC	N19	SW13_A	P19	NC	Q19	NC	R19	SW15_A	S19	NC	T19	VDD2	U19	BANK_EN

■ Pin Configuration (MAP)

TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U
1	VLL	VDD	NC	SW31_A	NC	NC	SW29_A	NC	NC	SW27_A	NC	NC	SW25_A	NC	NC	GND	VDD	CLR	BANK3
2	DIN	LEB	NC	NC	SW30_A	NC	NC	SW28_A	NC	NC	SW26_A	NC	NC	SW24_A	NC	RGND	CLKOUT_EN	R_ENB	BANK2
3	CLKIN	RESET	NC	SW31_P	NC	NC	SW29_P	NC	NC	SW27_P	NC	NC	SW25_P	NC	NC	NC	NC	NC	NC
4	GND	RGND	NC	NC	SW30_P	NC	NC	SW28_P	NC	NC	SW26_P	NC	NC	SW24_P	NC	NC	SW23_P	NC	SW23_A
5	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	SW22_P	NC	SW22_A	NC
6	NC	SW0_A	NC	SW0_P	NC	NC	–	–	–	–	–	–	–	–	NC	NC	NC	NC	NC
7	SW1_A	NC	SW1_P	NC	NC	–	GND	GND	GND	GND	GND	GND	GND	–	NC	NC	SW21_P	NC	SW21_A
8	NC	NC	NC	NC	NC	–	GND	GND	GND	GND	GND	GND	GND	–	NC	SW20_P	NC	SW20_A	NC
9	NC	SW2_A	NC	SW2_P	NC	–	GND	GND	GND	GND	GND	GND	GND	–	NC	NC	NC	NC	NC
10	SW3_A	NC	SW3_P	NC	NC	–	GND	GND	GND	GND	GND	GND	GND	–	NC	NC	SW19_P	NC	SW19_A
11	NC	NC	NC	NC	NC	–	GND	GND	GND	GND	GND	GND	GND	–	NC	SW18_P	NC	SW18_A	NC
12	NC	SW4_A	NC	SW4_P	NC	–	GND	GND	GND	GND	GND	GND	GND	–	NC	NC	NC	NC	NC
13	SW5_A	NC	SW5_P	NC	NC	–	GND	GND	GND	GND	GND	GND	GND	–	NC	NC	SW17_P	NC	SW17_A
14	NC	NC	NC	NC	NC	–	–	–	–	–	–	–	–	–	NC	SW16_P	NC	SW16_A	NC
15	NC	SW6_A	NC	SW6_P	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
16	SW7_A	NC	SW7_P	NC	NC	SW8_P	NC	NC	SW10_P	NC	NC	SW12_P	NC	NC	SW14_P	NC	NC	GND	GND
17	NC	NC	NC	NC	NC	NC	SW9_P	NC	NC	SW11_P	NC	NC	SW13_P	NC	NC	SW15_P	NC	RGND	BANK1
18	VDD	**GND**	GND	RGND	NC	SW8_A	NC	NC	SW10_A	NC	NC	SW12_A	NC	NC	SW14_A	NC	NC	GND	BANK0
19	THP	VLL	DOUT	CLKOUT	NC	NC	SW9_A	NC	NC	SW11_A	NC	NC	SW13_A	NC	NC	SW15_A	NC	VDD	BANK_EN

■ Package

Package Name	Dimension	Tray	Marking	Land	Packing
BGA-330(1313)A	RA330-A-P-S1	RA330-A-T-SD	RA330-A-M-SD	RA330-A-L-SD	RA330-A-K-SD

■ Storage, Mounting

1. Storage conditions

1. 1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Figure 1 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

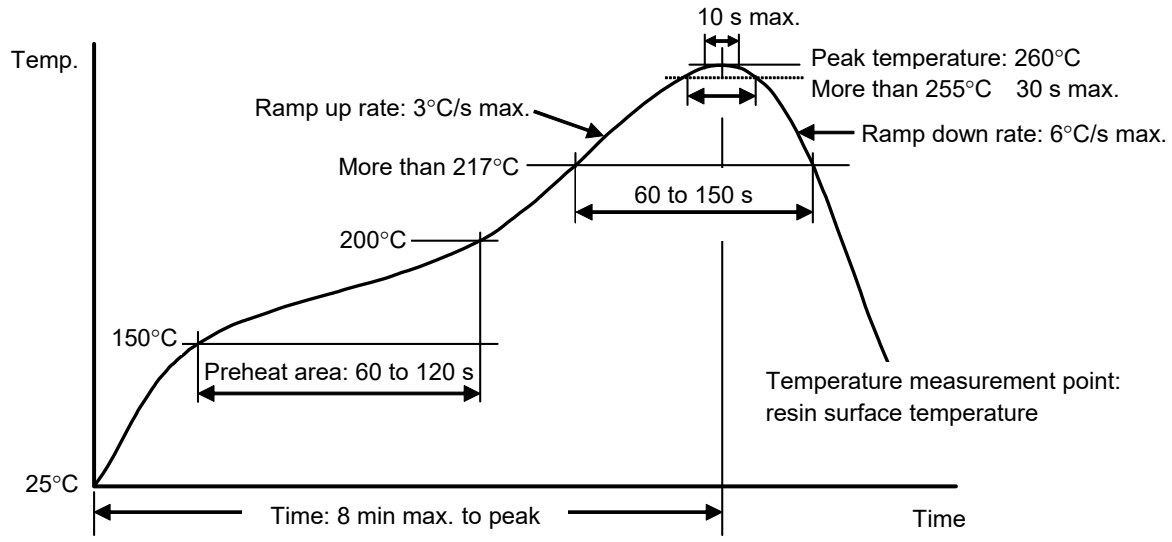


Figure 1 Resistance to Soldering Heat Condition for Package (Reflow Method)

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■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.

1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1. 4 Prevent friction with other materials made with high polymer.

1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

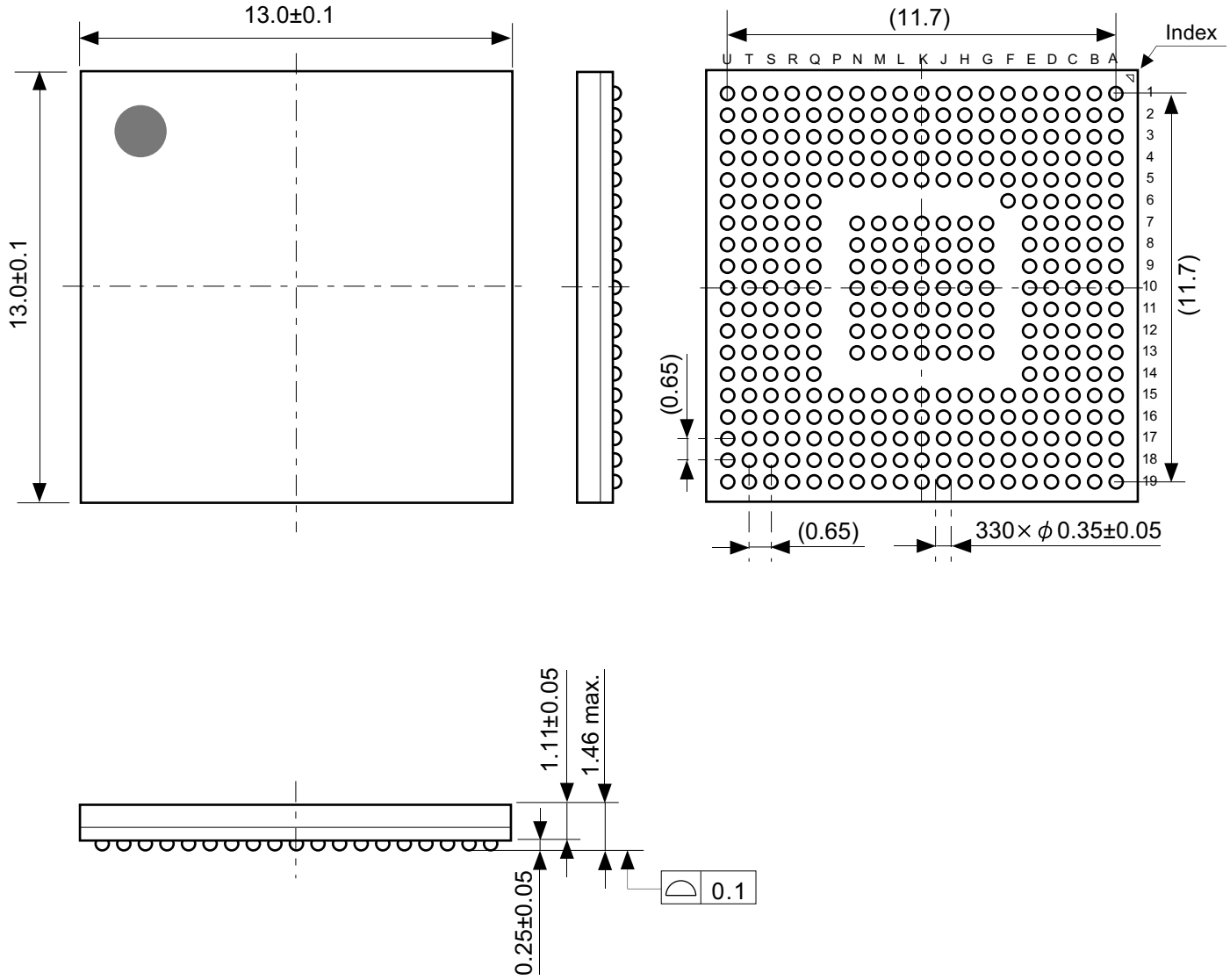
1. 6 Avoid dealing with or storing products in an extremely arid environment.

2. “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

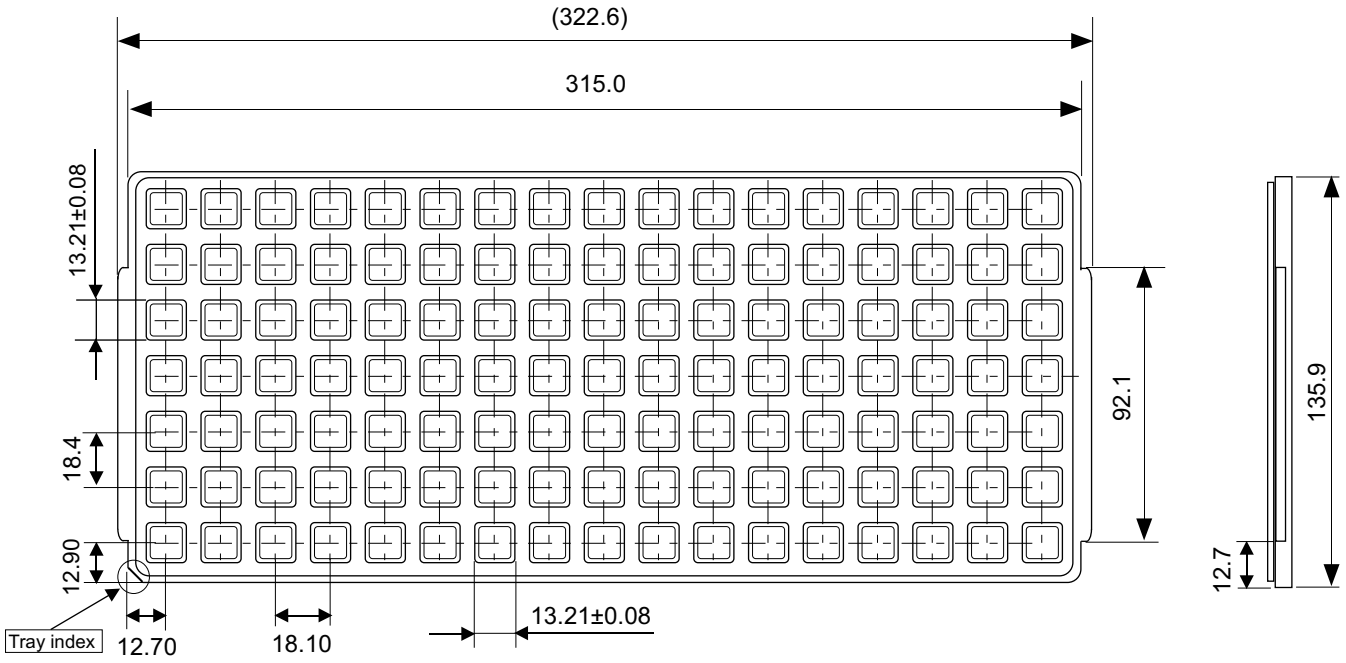
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

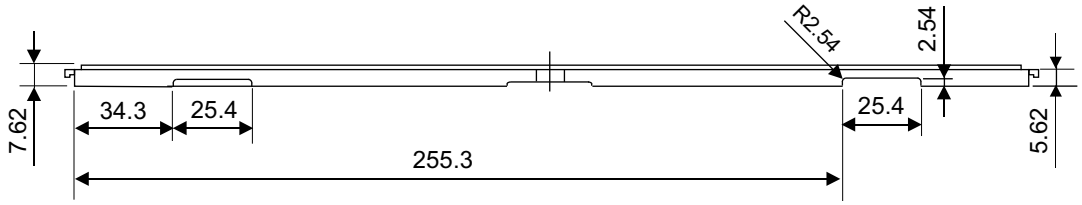


No. RA330-A-P-S1-1.0

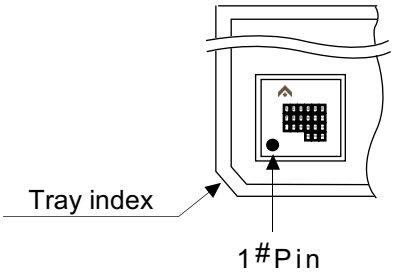
TITLE	BGA330-A-PKG Dimensions (S-UM6524)
No.	RA330-A-P-S1-1.0
ANGLE	
UNIT	mm

ABLIC Inc.





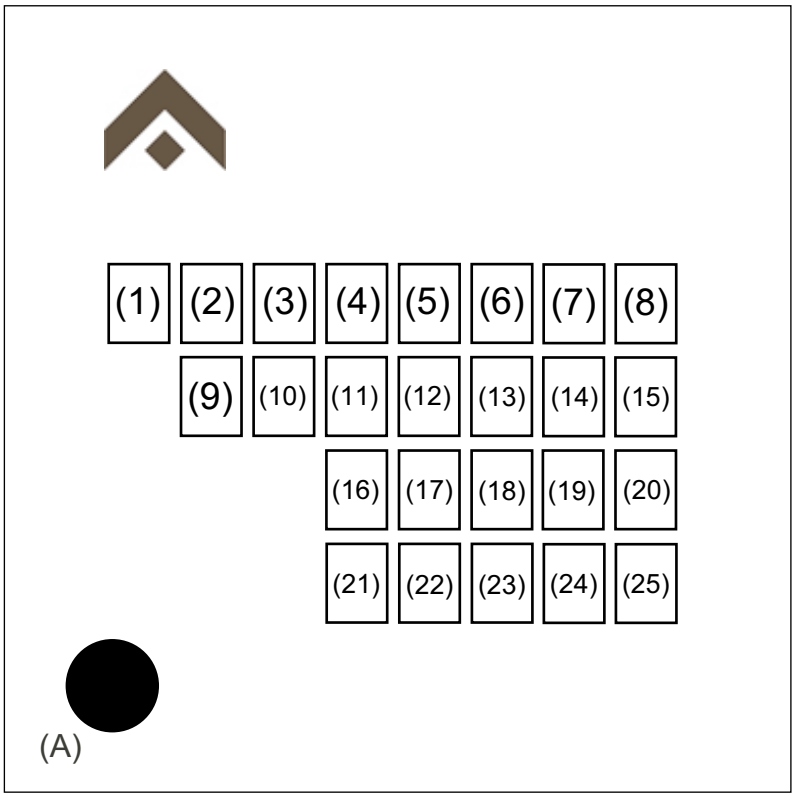
(Direction of IC in tray)



No. RA330-A-T-SD-3.0

TITLE	BGA330-A-Tray		
No.	RA330-A-T-SD-3.0		
ANGLE		QTY.	119
UNIT	mm		

ABLIC Inc.



(1) to (10) : Product code

(11) , (12) : Quality control code

(13) : Year of assembly

(14) : Month of assembly

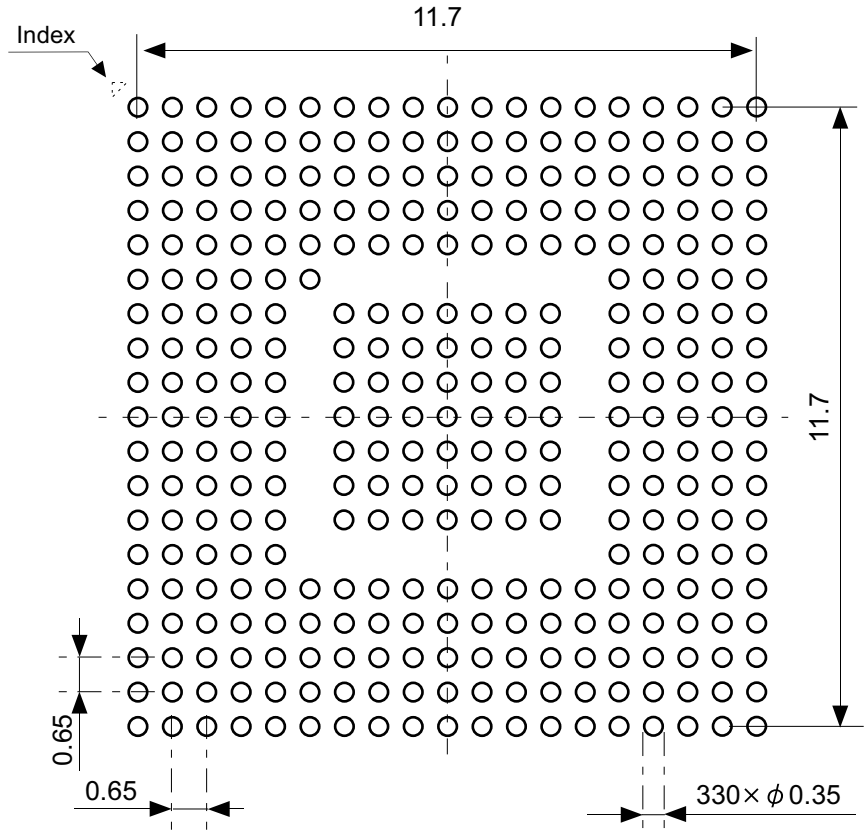
(15) : Week of assembly

(16) to (25) : Quality control code

(A) : 1-pin mark

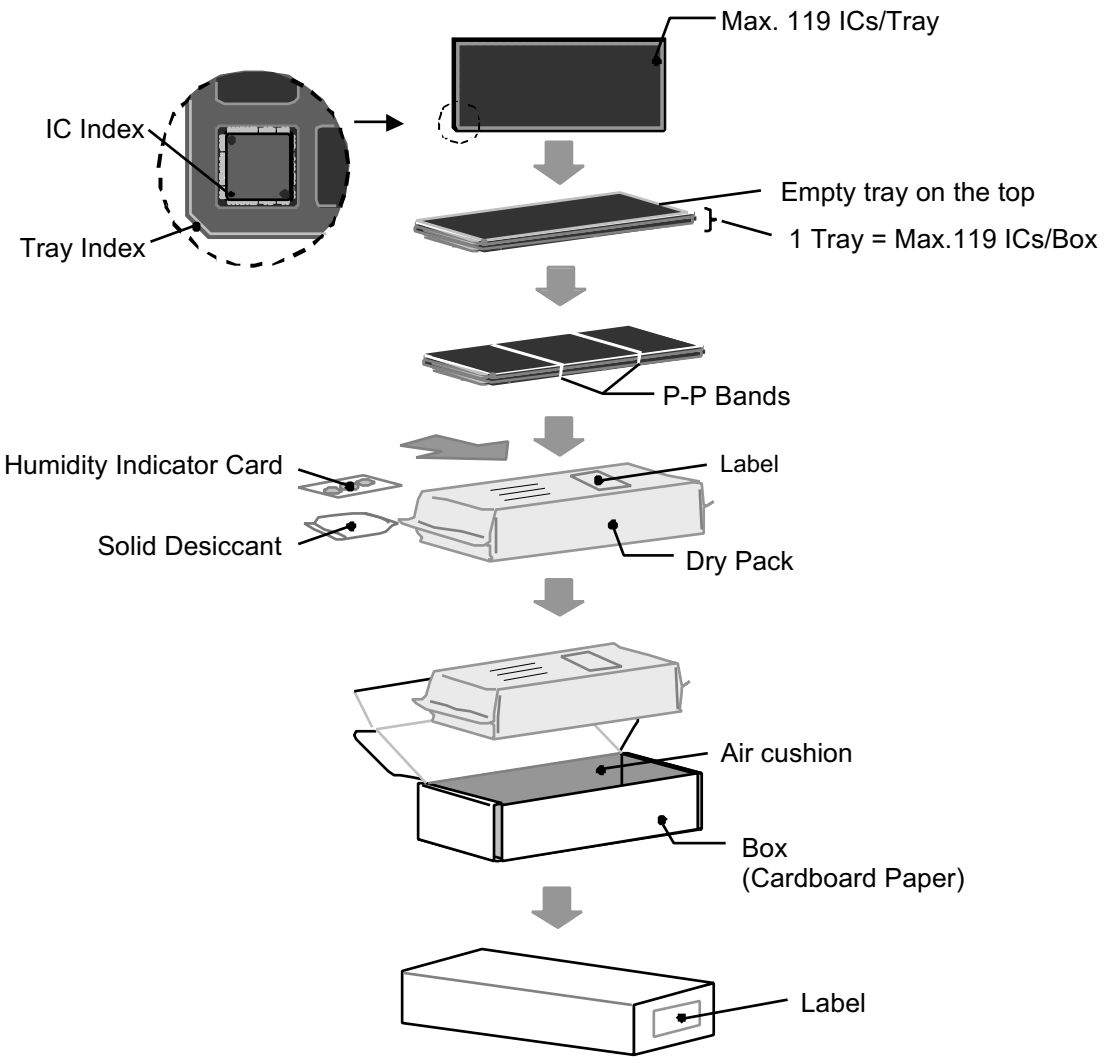
No. RA330-A-M-SD-1.0

TITLE	BGA330-A-Markings		
No.	RA330-A-M-SD-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



No. RA330-A-L-SD-2.0

TITLE	BGA330-A -Land Recommendation
No.	RA330-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



TITLE	BGA330-A -Packing Procedure
No.	RA330-A-K-SD-1.0
ANGLE	
UNIT	
ABLIC Inc.	

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2.4-2019.07