

The ABLIC S-UM6523 is a low charge injection 32-channel single-pole single-throw (SPST) high-voltage analog switch IC operated only by a single 5 V for ultrasound imaging applications. The S-UM6523 has  $\pm 100$  V analog signal range allowing up to  $\pm 150$  V voltage overshoot.

## ■ Function

- 32-channel high-voltage SPST analog switches with user-selectable logic interface and bleed resistor

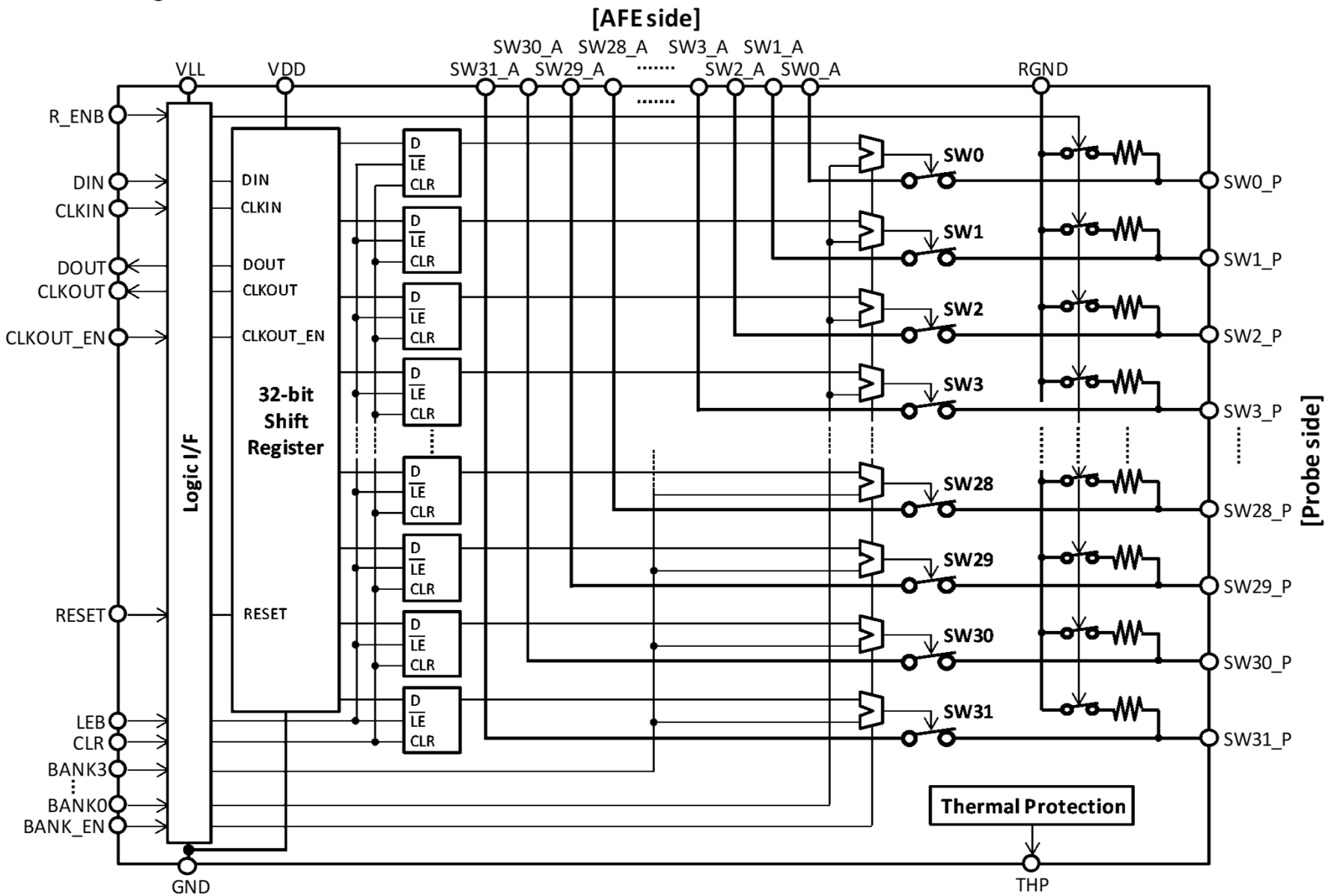
## ■ Features

- 0 V to  $\pm 100$  V analog signal voltage range allowing up to  $\pm 150$  V voltage overshoot
- 10 kHz to 70 MHz analog signal frequency range
- 2 A peak analog signal current per channel
- 8  $\Omega$  switch on-resistance
- Single +5 V power supply (NO HIGH-VOLTAGE POWER SUPPLY required)
- User-selectable Serial Digital Interface (32-bit shift registers) or Bank Interface (4 banks of 8-channel)
- User-selectable 40 k $\Omega$  bleed resistor on probe side
- Low on/off-capacitance
- 15 pC charge injection to 1000 pF
- -70 dB off-isolation at analog small-signal 5 MHz
- -60 dB switch crosstalk
- 1.8 V to 5 V CMOS logic interface
- Low power dissipation (static 5 mW)
- Embedded thermal protection with flag indicator
- RoHS compliant 9  $\times$  9 mm BGA package

■ **Contents**

Block Diagram.....	3
Absolute Maximum Ratings.....	4
Operating Supply Voltages, Temperature, Logic Levels.....	5
Power Supply Sequencing.....	5
DC Characteristics.....	6
Thermal Protection Characteristics.....	6
AC Characteristics.....	7
Test Circuits.....	8
Truth Table.....	9
Logic Timing.....	10
Latch Enable Interface Timing.....	11
Pin Description.....	12
Pin Configuration (Table).....	13
Pin Configuration (MAP).....	14
Package.....	15
Storage, Mounting.....	15
Important Notice.....	16
Cautions.....	17
Package outline, tray, marking, land recommendation and packing.....	18
Disclaimers (Handling Precautions).....	23

■ Block Diagram



■ **Absolute Maximum Ratings**

T<sub>A</sub> = 25°C unless otherwise noted.

No.	Item	Symbol	Value	Unit	Condition
1	Positive logic supply voltage	V <sub>LL</sub>	-0.4 to +7	V	
2	Positive supply voltage	V <sub>DD</sub>	-0.4 to +7	V	
3	Logic input voltage	DIN, CLKIN, RESET, CLR, LEB, BANK0, BANK1, BANK2, BANK3, BANK_EN, CLKOUT_EN, R_ENB	-0.4 to +7	V	
4	Logic output voltage	DOUT, CLKOUT, THP	-0.4 to +7	V	
5	Analog signal range (steady state voltage)	V <sub>SIG</sub>	-105 to +105	V	
6	Analog signal range (peak overshoot voltage)	V <sub>SIG_OS</sub>	-150 to +150	V	500 ns max. pulse width
7	Peak analog signal current per channel	I <sub>SW</sub>	2	A	
8	Operating junction temperature	T <sub>Jop</sub>	-20 to +150	°C	
9	Storage temperature	T <sub>STG</sub>	-55 to +150	°C	
10	Maximum power dissipation	P <sub>Dmax</sub>	4	W	

## ■ Operating Supply Voltages, Temperature, Logic Levels

$T_A = 25^\circ\text{C}$  unless otherwise noted.

No.	Item	Symbol	Min.	Typ.	Max.	Unit	Condition
1	Logic supply voltage	$V_{LL}$	1.7	1.8 to 5	$V_{DD}$	V	
2	Positive supply voltage	$V_{DD}$	4.75	5	5.25	V	
3	Operating free-air temperature	$T_A$	0	-	75	$^\circ\text{C}$	
4	High-level logic input voltage	$V_{IH}$	$0.8 \times V_{LL}$	-	$V_{LL}$	V	
5	Low-level logic input voltage	$V_{IL}$	0	-	$0.2 \times V_{LL}$	V	
6	High-level logic output voltage	$V_{OH}$	$0.8 \times V_{LL}$	-	-	V	$I_{SOURCE} = 1 \text{ mA}$
7	Low-level logic output voltage	$V_{OL}$	-	-	$0.2 \times V_{LL}$	V	$I_{SINK} = 1 \text{ mA}$
8	Logic input high current *1)	$I_{IH}$	-10	-	10	$\mu\text{A}$	DIN, CLKIN, RESET, CLR, LEB, BANK0, BANK1, BANK2, BANK3, BANK_EN, CLKOUT_EN, R_ENB
9	Logic input low current	$I_{IL}$	-10	-	10	$\mu\text{A}$	
10	Logic input capacitance	$C_{IN}$	-	2	-	pF	
11	Clock frequency	$f_{CLK}$	-	-	50	MHz	CLKOUT_EN = 0, $V_{LL} = 1.8 \text{ V}$
			-	-	80	MHz	CLKOUT_EN = 0, $V_{LL} = 2.5 \text{ V}$
			-	-	95	MHz	CLKOUT_EN = 0, $V_{LL} = 3.3 \text{ V}$
			-	-	60	MHz	CLKOUT_EN = 1, $V_{LL} = 1.8 \text{ V}$
			-	-	85	MHz	CLKOUT_EN = 1, $V_{LL} = 2.5 \text{ V}$
-	-	130	MHz	CLKOUT_EN = 1, $V_{LL} = 3.3 \text{ V}$			
12	Clock rise and fall times	$t_R, t_F$	-	-	50	ns	
13	CLKIN to DOUT delay	$t_{DO}$	7	10	24	ns	
14	CLKOUT to DOUT delay	$t_{DO1}$	1.3	-	1.9	ns	
15	CLKIN to CLKOUT delay	$t_{DCKO}$	7	10	24	ns	
16	DIN to CLKIN setup time	$t_{SU}$	1	-	-	ns	
17	DIN to CLKIN hold time	$t_{HD}$	2	-	-	ns	
18	LEB setup time	$t_{SLEB}$	5	-	-	ns	
19	LEB low-pulse width	$t_{WLEB}$	12	-	-	ns	
20	CLR response time	$t_{DCLR}$	-	-	500	ns	
21	CLR high-pulse width	$t_{WCLR}$	12	-	-	ns	
22	Bank interface setup time	$t_{SBNK}$	100	-	-	ns	
23	Bank interface hold time	$t_{HBNK}$	1	-	-	us	
24	BANKx minimum pulse width	$t_{WBNK}$	4	-	-	us	
25	RESET response time	$t_{DRST}$	-	-	400	ns	
26	RESET high-pulse width	$t_{WRST}$	12	-	-	ns	

NOTE: \*1) BANK\_EN, CLKOUT\_EN, and R\_ENB have 100  $\mu\text{A}$  leakage at  $V_{LL} = 5 \text{ V}$  due to 50 k $\Omega$  internal pull-down resistor.

## ■ Power Supply Sequencing

No power supply sequencing is required even if  $V_{LL}$  is different from  $V_{DD}$ .  
Please apply the  $V_{DD}$  voltage to the  $V_{LL}$  when operating with a single 5 V.

**■ DC Characteristics**

$V_{LL} = 3.3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ ,  $LEB = 0$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

No.	Item	Symbol	Spec			Unit	Condition
			Min.	Typ.	Max.		
1	Analog signal range (steady state voltage)	$V_{SIG}$	-100	-	+100	V	
2	Analog signal range (peak overshoot voltage)	$V_{SIG\_OS}$	-150	-	+150	V	500 ns max. pulse width
3	$V_{LL}$ quiescent current	$I_{LLQ}$	-	0.2	-	μA	Quiescent current-1 All switches off
4	$V_{DD}$ quiescent current	$I_{DDQ}$	-	2.6	-	mA	
5	$V_{LL}$ quiescent current	$I_{LLQ}$	-	0.2	-	μA	Quiescent current-2 All switches on
6	$V_{DD}$ quiescent current	$I_{DDQ}$	-	2.6	-	mA	
7	$V_{LL}$ dynamic current	$I_{LL}$	-	2	10	μA	Dynamic current All channels switching simultaneously at $f_{SW} = 50\text{ kHz}$
8	$V_{DD}$ dynamic current	$I_{DD}$	-	4.6	5.6	mA	
9	DC offset switch off	$V_{OS}$	-	0	-	mV	
10	Small signal switch on-resistance	$R_{ONS}$	-	8	10	Ω	$V_{SIG} = 0.1\text{ Vpp}$ to $5\text{ Vpp}$ (5 MHz, $R_S = 10\text{ Ω}$ )
11	Small signal switch on-resistance matching	$\Delta R_{ONS}$	-	2	5	%	$V_{SIG} = 0\text{ V}$ , $I_{SIG} = 5\text{ mA}$
12	Large signal switch on-resistance	$R_{ONL}$	-	8	-	Ω	$V_{SIG} = 20\text{ Vpp}$ (5 MHz, $R_S = 10\text{ Ω}$ )
13	Bleed resistance	$R_{BLD}$	30	40	50	kΩ	$R\_ENB = 0$ , probe side only
14	Switch output peak current	$I_{SW}$	-	2	-	A	100 ns pulse, 0.1% duty cycle

**■ Thermal Protection Characteristics**

$V_{LL} = 3.3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ ,  $LEB = 0$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

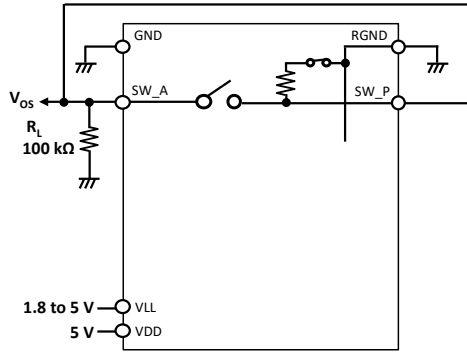
No.	Item	Symbol	Spec			Unit	Condition
			Min.	Typ.	Max.		
1	THP pull-up voltage	$V_{PUTHP}$	-	-	5.25	V	Open drain
2	THP output current	$I_{THP}$	-	1.0	-	mA	-
3	THP output low voltage	$V_{OLTHP}$	-	-	0.5	V	THP active, $V_{LL} = 3.3\text{ V}$ , $I_{THP} = 1\text{ mA}$
4	THP temperature threshold	$T_{THP}$	90	110	130	°C	Thermal protection flag indicator by THP pin (open N-MOS drain, Low = THP activating)
5	THP reset hysteresis	$T_{HYSTHP}$	-	10	-	°C	

## ■ AC Characteristics

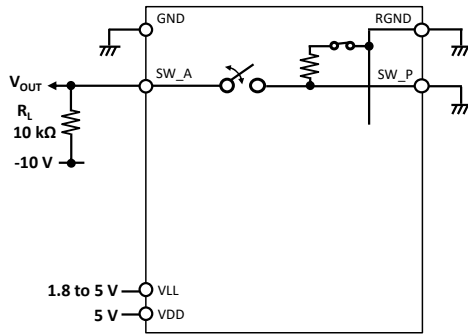
$V_{LL} = 3.3V$ ,  $V_{DD} = 5V$ ,  $LEB = 0$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

No.	Item	Symbol	Spec			Unit	Condition	
			Min.	Typ.	Max.			
1	Turn-on time	$t_{ON}$	-	2	4	$\mu s$	BANK_EN = 0	
		$t_{ON\_BNK}$	-	2	4	$\mu s$	BANK_EN = 1	
2	Turn-off time	$t_{OFF}$	-	2	4	$\mu s$	BANK_EN = 0	
		$t_{OFF\_BNK}$	-	2	4	$\mu s$	BANK_EN = 1	
3	Output switching frequency	$f_{SW}$	-	-	50	kHz	Duty cycle = 50%	
4	Small signal frequency	$f_{SIG}$	0.01	-	70	MHz	$C_L = 220 pF$	
5	Off isolation	small signal	$V_{ISO(RX)}$	-	-70	-	dB	$f_{SIG} = 5 MHz$ , $R_L = 50 \Omega$
		large signal	$V_{ISO(TX)}$	-	-65	-	dB	$f_{SIG} = 5 MHz$ , $R_L = 50 \Omega$
6	Crosstalk	$V_{CT}$	-	-60	-	dB	$f_{SIG} = 5 MHz$ , $R_L = 50 \Omega$	
7	On capacitance	small signal	$C_{ON(RX)}$	-	23	-	pF	$V_{SIG} = 0V$ , $f_{SIG} = 1 MHz$
		large signal	$C_{ON(TX)}$	-	19	-	pF	$V_{SIG} = 10V_{pp}$ , $f_{SIG} = 1 MHz$
8	Off capacitance SW_P to GND	small signal	$C_{OFF(SWP\_RX)}$	-	16	-	pF	$V_{SIG} = 0V$ , $f_{SIG} = 1 MHz$
9	Off capacitance SW_A to GND	small signal	$C_{OFF(SWA\_RX)}$	-	13	-	pF	$V_{SIG} = 0V$ , $f_{SIG} = 1 MHz$
		large signal	$C_{OFF(SWA\_TX)}$	-	10	-	pF	$V_{SIG} = 10V_{pp}$ , $f_{SIG} = 1 MHz$
10	Output spike voltage (SW_P)		$V_{SPK\_ON(SWP)}$	-	30	-	mV	50 Ω load (switch on)
			$V_{SPK\_OFF(SWP)}$	-	60	-	mV	50 Ω load (switch off)
11	Output spike voltage (SW_A)		$V_{SPK\_ON(SWA)}$	-	30	-	mV	50 Ω load (switch on)
			$V_{SPK\_OFF(SWA)}$	-	60	-	mV	50 Ω load (switch off)
12	Charge injection	QC	-	15	-	pC		

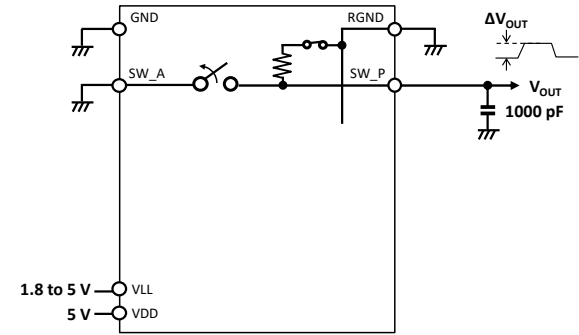
### Test Circuits



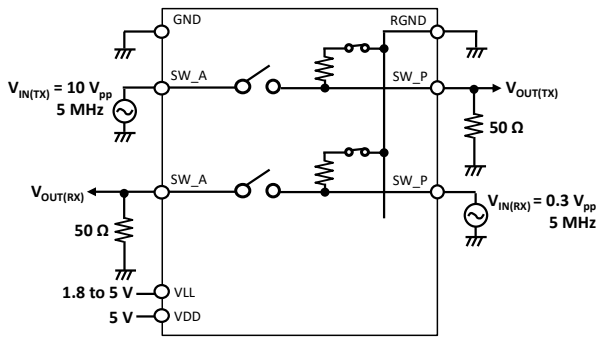
DC Offset OFF



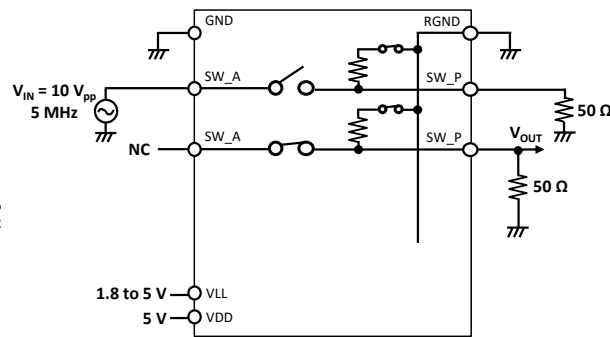
$t_{ON}/t_{OFF}$  test circuit



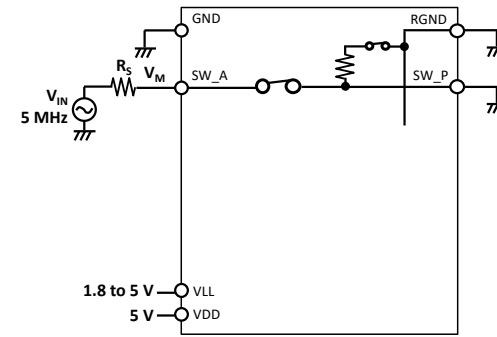
$Q = 1000 \text{ pF} \times \Delta V_{OUT}$   
Charge Injection



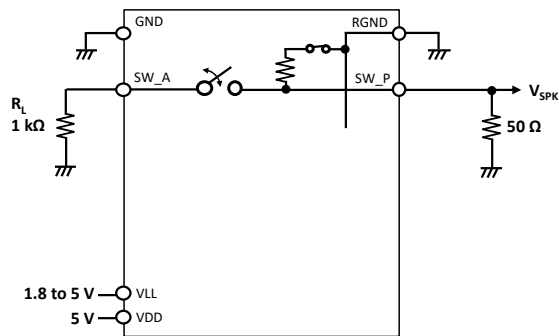
$V_{ISO} = 20 \text{Log}(V_{OUT}/V_{IN})$   
Off isolation



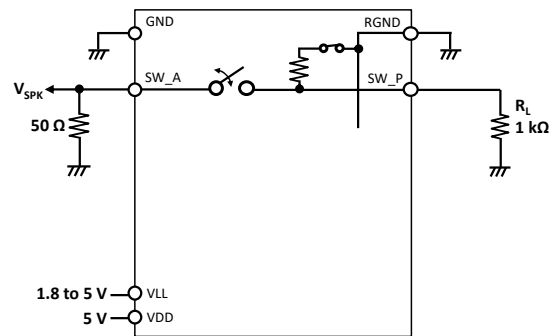
$V_{CT} = 20 \text{Log}(V_{OUT}/V_{IN})$   
Crosstalk



$R_{ON} = R_S \times V_M / (V_{IN} - V_M)$   
On resistance test circuit



Output spike voltage SW\_P

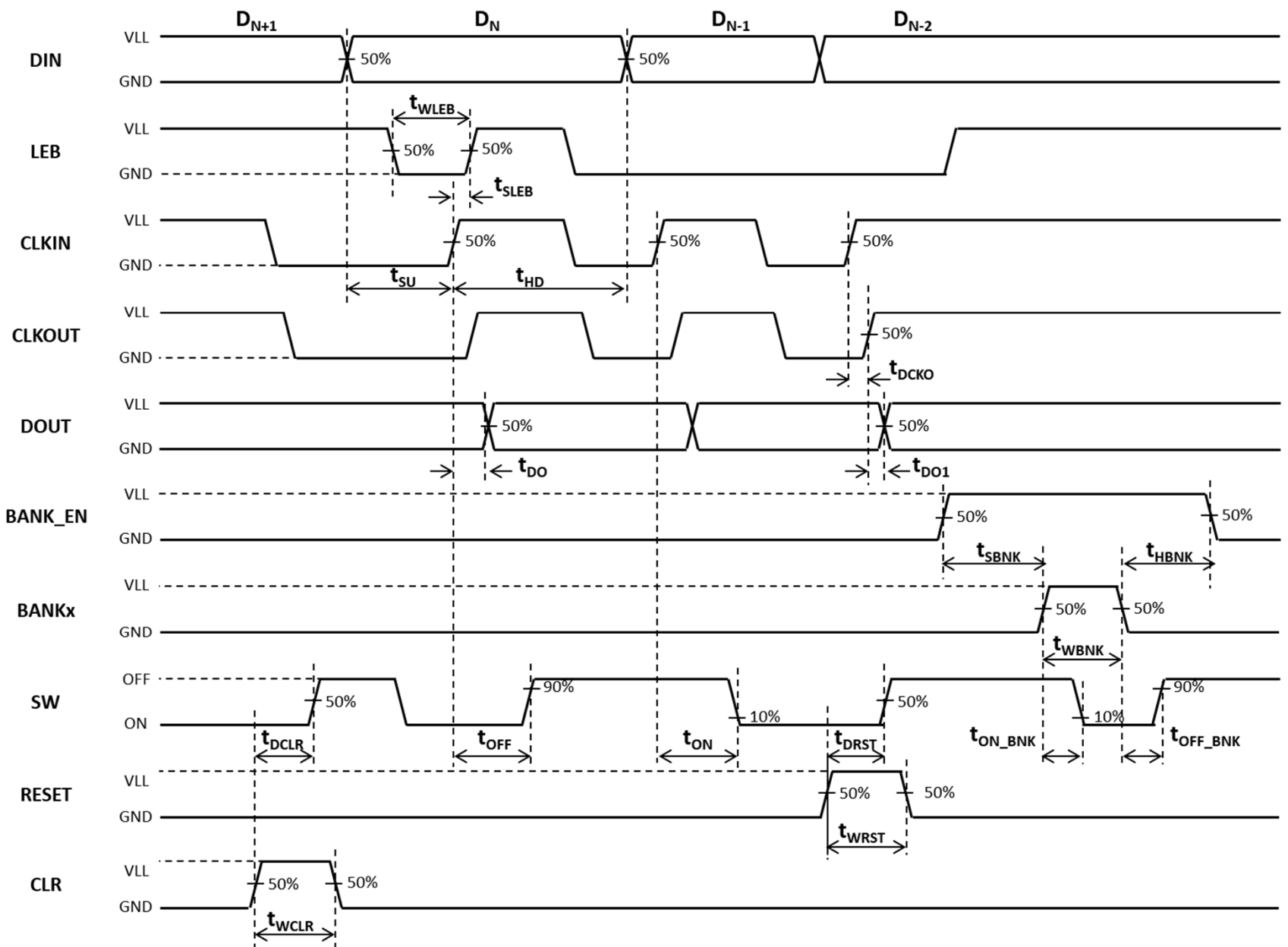


Output spike voltage SW\_A

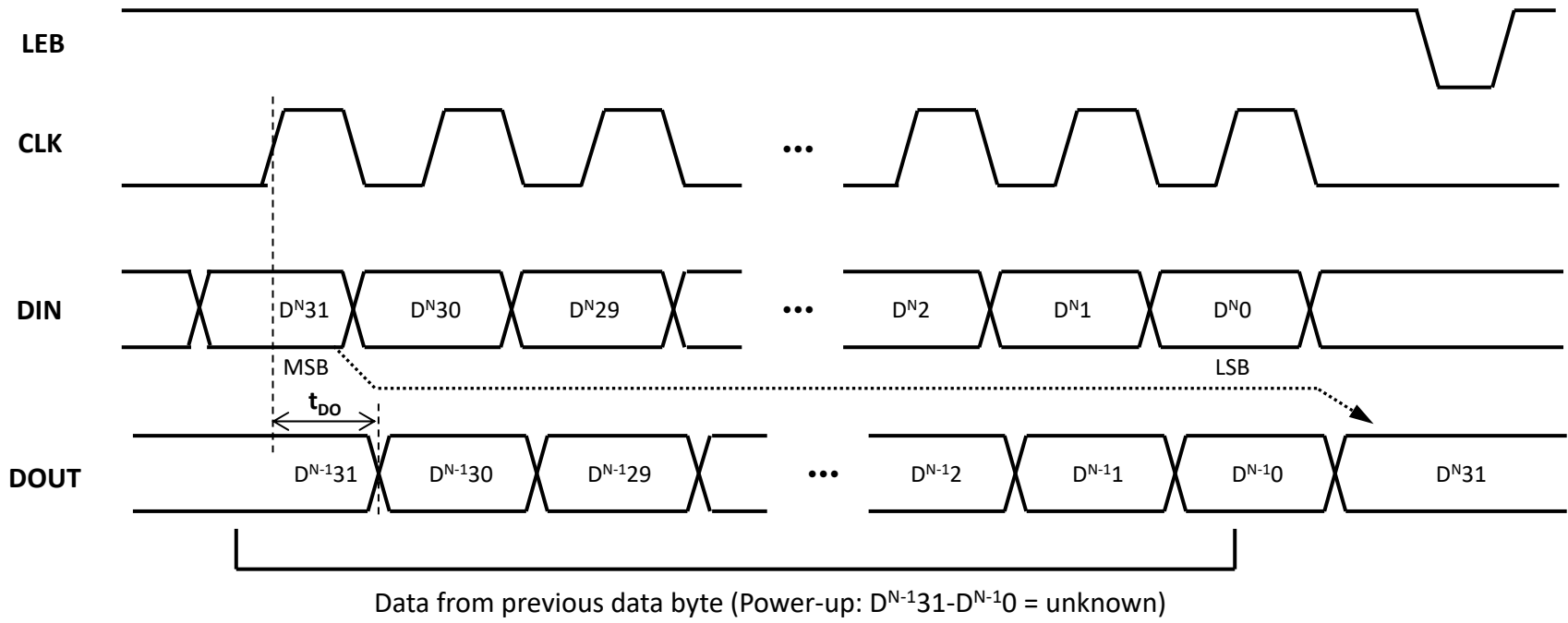




Logic Timing



### ■ Latch Enable Interface Timing



■ Pin Description

Pin Name	I/O	Function
VLL	-	Positive voltage supply of low voltage interface (+1.8 V to +5 V)
VDD	-	Positive low voltage power supply (+5 V)
GND	-	Drive power ground (0 V)
RGND	-	Bleed resistor ground (0 V)
DIN	I	Serial-Data input
DOUT	O	Serial-Data output
CLKIN	I	Serial-Clock input
CLKOUT	O	Serial-Clock output
LEB	I	Active-Low latch enable input, Hi = Hold data, Low = Latch data input
BANK0	I	Bank-Data input 0 for SW0 to SW7, Hi = ON, Low = OFF
BANK1	I	Bank-Data input 1 for SW8 to SW15, Hi = ON, Low = OFF
BANK2	I	Bank-Data input 2 for SW16 to SW23, Hi = ON, Low = OFF
BANK3	I	Bank-Data input 3 for SW24 to SW31, Hi = ON, Low = OFF
RESET	I	Shift register reset input
CLR	I	Latch clear input
CLKOUT_EN	I	Clock out enable input, Hi = Clock out, Low = Disable (Low)
R_ENB	I	Bleed resistor enable input, Hi = Disable, Low = Enable
BANK_EN	I	Bank interface enable input, Hi = Bank-Data interface , Low = Serial-Data interface
THP	O	Thermal protection output flag, open N-MOS drain (Low = THP activating)
SWx_A	I/O	Analog switch terminal n (AFE side), Suffix “x” corresponds to channel number (x = 0 to 31)
SWx_P	I/O	Analog switch terminal n (Probe side), Suffix “x” corresponds to channel number (x = 0 to 31)
NC	-	No connection (Not internally connected)

## ■ Pin Configuration (Table)

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
A1	DIN	B1	CLKIN	C1	VLL	D1	NC	E1	SW30_A	F1	NC	G1	SW28_A
A2	LEB	B2	RESET	C2	VDD	D2	SW31_A	E2	NC	F2	SW29_A	G2	NC
A3	GND	B3	GND	C3	RGND	D3	NC	E3	SW30_P	F3	NC	G3	SW27_P
A4	NC	B4	SW0_A	C4	NC	D4	SW0_P	E4	NC	F4	SW29_P	G4	NC
A5	SW1_A	B5	NC	C5	SW1_P	D5	GND	E5	SW31_P	F5	GND	G5	SW28_P
A6	NC	B6	SW2_A	C6	NC	D6	SW2_P	E6	GND	F6	GND	G6	GND
A7	SW3_A	B7	NC	C7	SW3_P	D7	GND	E7	GND	F7	GND	G7	GND
A8	NC	B8	SW4_A	C8	NC	D8	SW4_P	E8	GND	F8	GND	G8	GND
A9	SW5_A	B9	NC	C9	SW5_P	D9	GND	E9	SW9_P	F9	GND	G9	SW12_P
A10	NC	B10	SW6_A	C10	NC	D10	SW6_P	E10	NC	F10	SW10_P	G10	NC
A11	SW7_A	B11	NC	C11	SW7_P	D11	NC	E11	SW8_P	F11	NC	G11	SW11_P
A12	RGND	B12	DOUT	C12	GND	D12	SW8_A	E12	NC	F12	SW10_A	G12	NC
A13	THP	B13	VDD	C13	CLKOUT	D13	NC	E13	SW9_A	F13	NC	G13	SW11_A

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
H1	NC	J1	SW26_A	K1	NC	L1	SW24_A	M1	VDD	N1	CLR
H2	SW27_A	J2	NC	K2	SW25_A	L2	GND	M2	BANK3	N2	R_ENB
H3	NC	J3	SW24_P	K3	NC	L3	CLKOUT_EN	M3	RGND	N3	BANK2
H4	SW26_P	J4	NC	K4	SW23_P	L4	NC	M4	SW23_A	N4	NC
H5	GND	J5	SW25_P	K5	GND	L5	SW22_P	M5	NC	N5	SW22_A
H6	GND	J6	GND	K6	SW21_P	L6	NC	M6	SW21_A	N6	NC
H7	GND	J7	GND	K7	GND	L7	SW20_P	M7	NC	N7	SW20_A
H8	GND	J8	GND	K8	SW19_P	L8	NC	M8	SW19_A	N8	NC
H9	GND	J9	SW15_P	K9	GND	L9	SW18_P	M9	NC	N9	SW18_A
H10	SW13_P	J10	NC	K10	SW17_P	L10	NC	M10	SW17_A	N10	NC
H11	NC	J11	SW14_P	K11	NC	L11	SW16_P	M11	GND	N11	SW16_A
H12	SW12_A	J12	NC	K12	SW14_A	L12	RGND	M12	BANK0	N12	BANK1
H13	NC	J13	SW13_A	K13	NC	L13	SW15_A	M13	VDD	N13	BANK_EN

**TOP VIEW**

	A	B	C	D	E	F	G	H	J	K	L	M	N
1	DIN	CLKIN	VLL	NC	SW30_A	NC	SW28_A	NC	SW26_A	NC	SW24_A	VDD	CLR
2	LEB	RESET	VDD	SW31_A	NC	SW29_A	NC	SW27_A	NC	SW25_A	GND	BANK3	R_ENB
3	GND	GND	RGND	NC	SW30_P	NC	SW27_P	NC	SW24_P	NC	CLKOUT_EN	RGND	BANK2
4	NC	SW0_A	NC	SW0_P	NC	SW29_P	NC	SW26_P	NC	SW23_P	NC	SW23_A	NC
5	SW1_A	NC	SW1_P	GND	SW31_P	GND	SW28_P	GND	SW25_P	GND	SW22_P	NC	SW22_A
6	NC	SW2_A	NC	SW2_P	GND	GND	GND	GND	GND	SW21_P	NC	SW21_A	NC
7	SW3_A	NC	SW3_P	GND	GND	GND	GND	GND	GND	GND	SW20_P	NC	SW20_A
8	NC	SW4_A	NC	SW4_P	GND	GND	GND	GND	GND	SW19_P	NC	SW19_A	NC
9	SW5_A	NC	SW5_P	GND	SW9_P	GND	SW12_P	GND	SW15_P	GND	SW18_P	NC	SW18_A
10	NC	SW6_A	NC	SW6_P	NC	SW10_P	NC	SW13_P	NC	SW17_P	NC	SW17_A	NC
11	SW7_A	NC	SW7_P	NC	SW8_P	NC	SW11_P	NC	SW14_P	NC	SW16_P	GND	SW16_A
12	RGND	DOUT	GND	SW8_A	NC	SW10_A	NC	SW12_A	NC	SW14_A	RGND	BANK0	BANK1
13	THP	VDD	CLKOUT	NC	SW9_A	NC	SW11_A	NC	SW13_A	NC	SW15_A	VDD	BANK_EN

■ **Pin Configuration (MAP)**

■ Package

Package Name	Dimension	Tray	Marking	Land	Packing
BGA-169(0909)A	RA169-A-P-S1	RA169-A-T-SD	RA169-A-M-SD	RA169-A-L-SD	RA169-A-K-SD

■ Storage, Mounting

1. Storage conditions

- 1.1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.
- 1.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering. It is necessary to check the package surface temperature (resin) before setting the temperature profile. **Figure 1** shows the resistance to soldering heat condition for package (Reflow method). Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

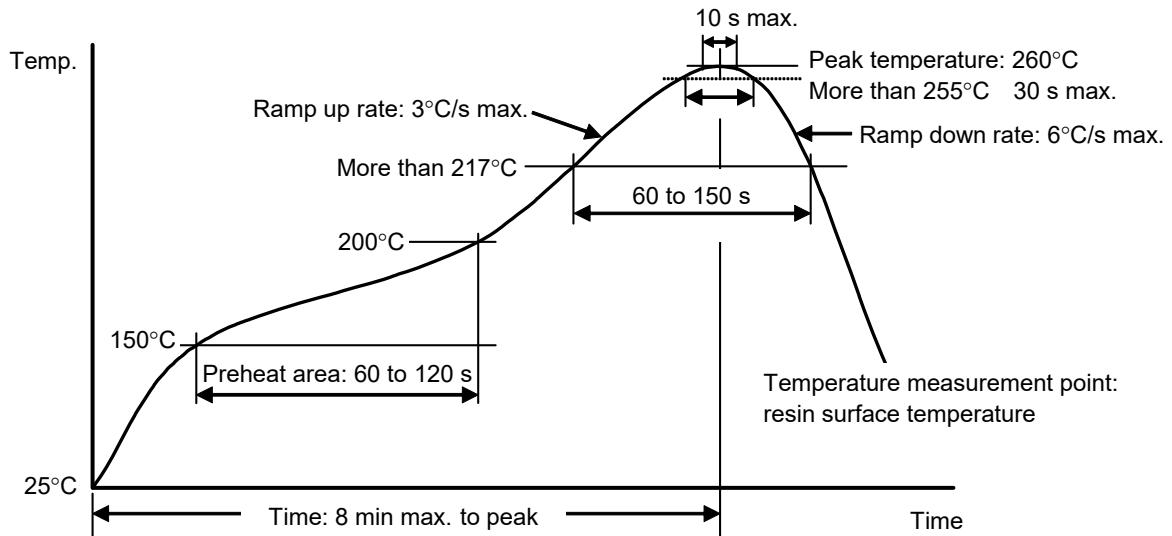


Figure 1 Resistance to Soldering Heat Condition for Package (Reflow Method)

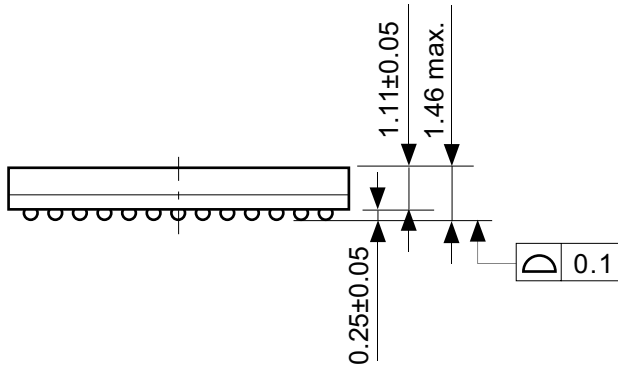
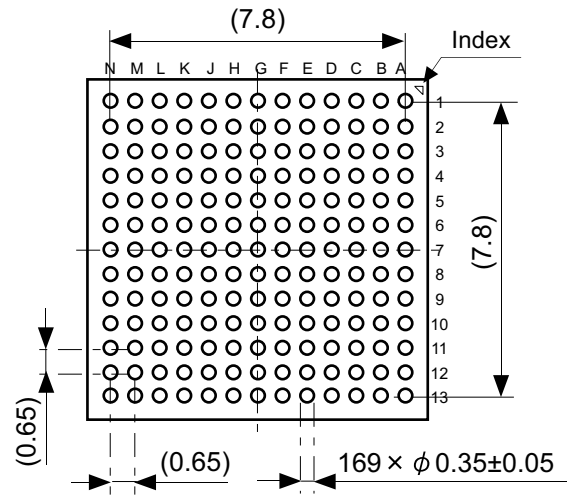
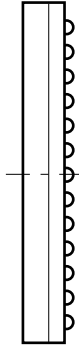
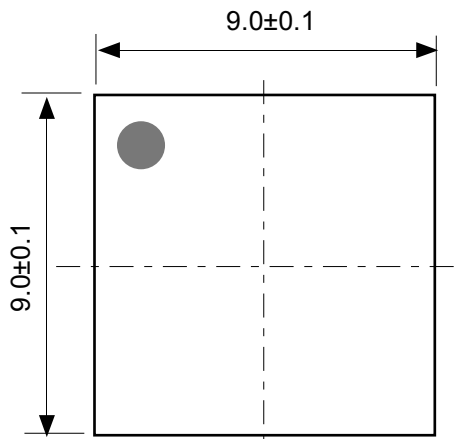
■ **Important Notice**

1. ABLIC Inc. warrants performance of its hardware products (hereinafter called “products”) to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent ABLIC Inc. needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.
2. Should any claim be made within one month of product delivery about products’ failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before such claim shall not be counted for such response.
3. ABLIC Inc. assumes no obligation or any way of compensation should any fault about customer products and applications using ABLIC Inc. products be found in marketplace. Only in such a case fault of ABLIC Inc. is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.
4. ABLIC Inc. reserves the right to make changes to the Product Specification at any time and to discontinue mass production of the relevant products without notice. Customers are advised before placing orders to confirm that the Product Specification of inquiry is the latest version and that the relevant product is currently on mass production status.
5. In no event shall ABLIC Inc. be liable for any damage that may result from an accident or any other cause during operation of the user’s units according to the Product Specification. ABLIC Inc. assumes no responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in the Product Specification.
6. No license is granted by the Product Specification under any patents or other rights of any third party or ABLIC Inc.
7. The Product Specification may not be reproduced or duplicated, in any form, in whole or in part, without the expressed written permission of ABLIC Inc.
8. Resale of ABLIC Inc. products with statements different from or beyond the parameters described in the Product Specification voids all express and any implied warranties for the products, and is an unfair and deceptive business practice. ABLIC Inc. is not responsible or liable for any such statements.
9. Products (technologies) described in the Product Specification are not to be provided to any party whose purpose in their application will hinder maintenance of international peace and safety nor are they to be applied to that purpose by their direct purchasers or any third party. When exporting those products (technologies), the necessary procedures are to be taken in accordance with related laws and regulations.



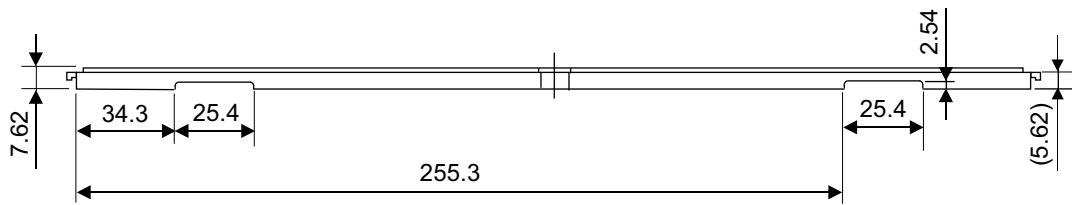
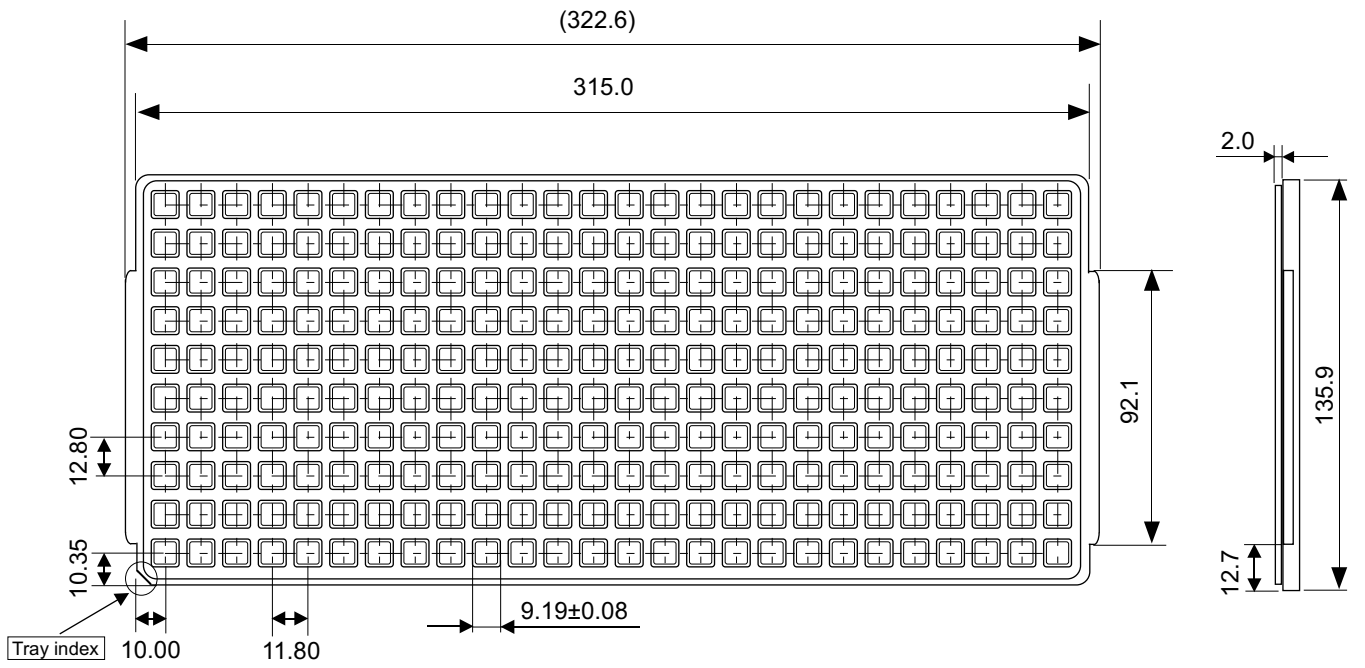
**■ Cautions**

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).
  - 1.1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.
  - 1.2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.
  - 1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.
  - 1.4 Prevent friction with other materials made with high polymer.
  - 1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.
  - 1.6 Avoid dealing with or storing products in an extremely arid environment.
2. "Absolute maximum ratings" should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.
3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)
4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

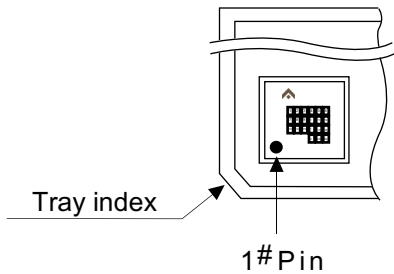


No. RA169-A-P-S1-1.0

TITLE	BGA169-A-PKG Dimensions (S-UM6523)
No.	RA169-A-P-S1-1.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

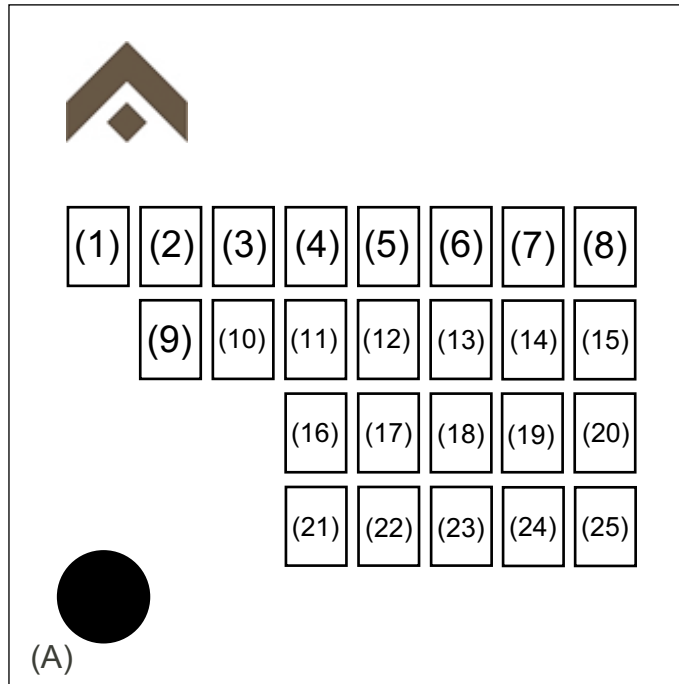


( Direction of IC in tray )



No. RA169-A-T-SD-1.0

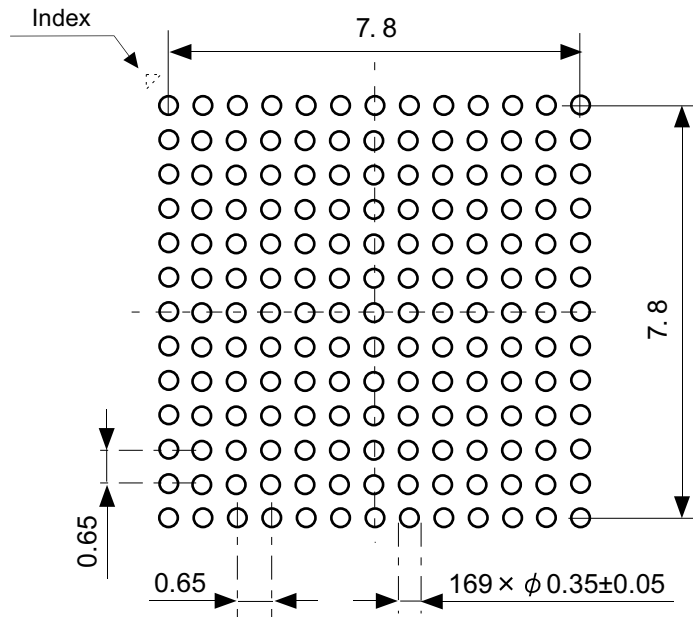
TITLE	BGA169-A-Tray		
No.	RA169-A-T-SD-1.0		
ANGLE		QTY.	260
UNIT	mm		
<b>ABLIC Inc.</b>			



- (1) to (10) : Product code
- (11) , (12) : Quality control code
- (13) : Year of assembly
- (14) : Month of assembly
- (15) : Week of assembly
- (16) to (25) : Quality control code
- (A) : 1-pin mark

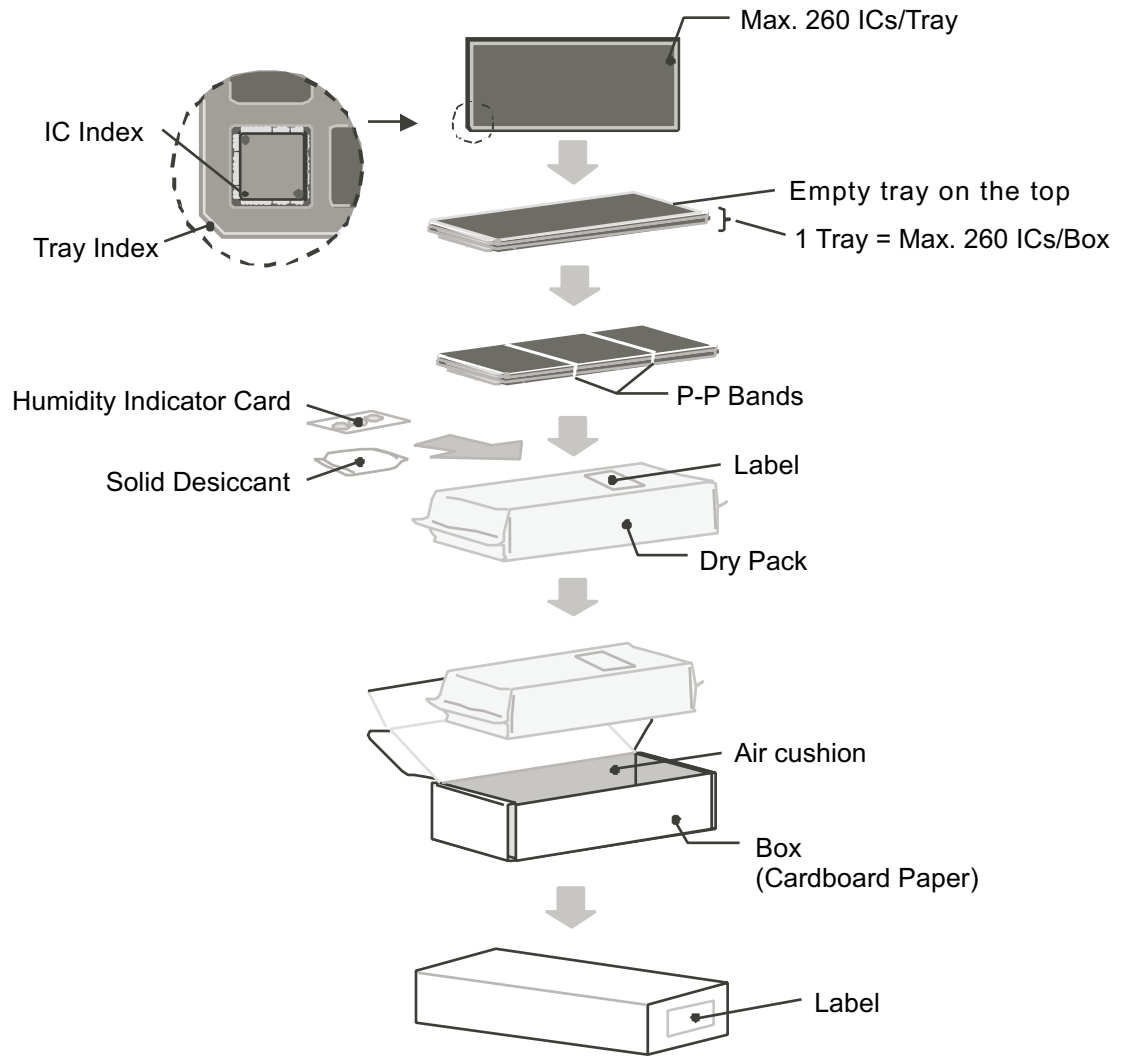
No. RA169-A-M-SD-1.0

TITLE	BGA169-A-Markings		
No.	RA169A-M-SD-1.0		
ANGLE			
UNIT		TYPE	LASER
<b>ABLIC Inc.</b>			



No. RA169-A-L-SD-1.0

TITLE	BGA169-A -Land Recommendation
No.	RA169-A-L-SD-1.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



TITLE	BGA169-A -Packing Procedure
No.	RA169-A-K-SD-1.0
ANGLE	
UNIT	
<b>ABLIC Inc.</b>	

## Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.  
The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07