S-US55D2

OCTAL DAC WITH DIFFERENTIAL OUTPUTS AND 2-BIT PER CHANNEL CMOS OUTPUT PATTERN GENERATORS FOR ULTRASOUND TRANSMITTER

Rev.1.2_00

The ABLIC S-US55D2 is an octal, 12-bit, 200MSPS, Digital-to-Analog Converter (DAC) with analog differential outputs and 2-bit per channel CMOS output pattern generators. It is designed for an ultrasound linear amplifier with 3-level pulser (3LP). Each channel has a 12bit x 4096 DAC pattern memory and a 128Byte 3LP pattern memory. The S-US55D2 is suitable as the input signal pattern generator to the S-UM55L2 ultrasound transmitter.

■ Function

- Octal DAC with differential outputs and 2-bit per channel CMOS output pattern generators for an ultrasound transmitter

■ Features

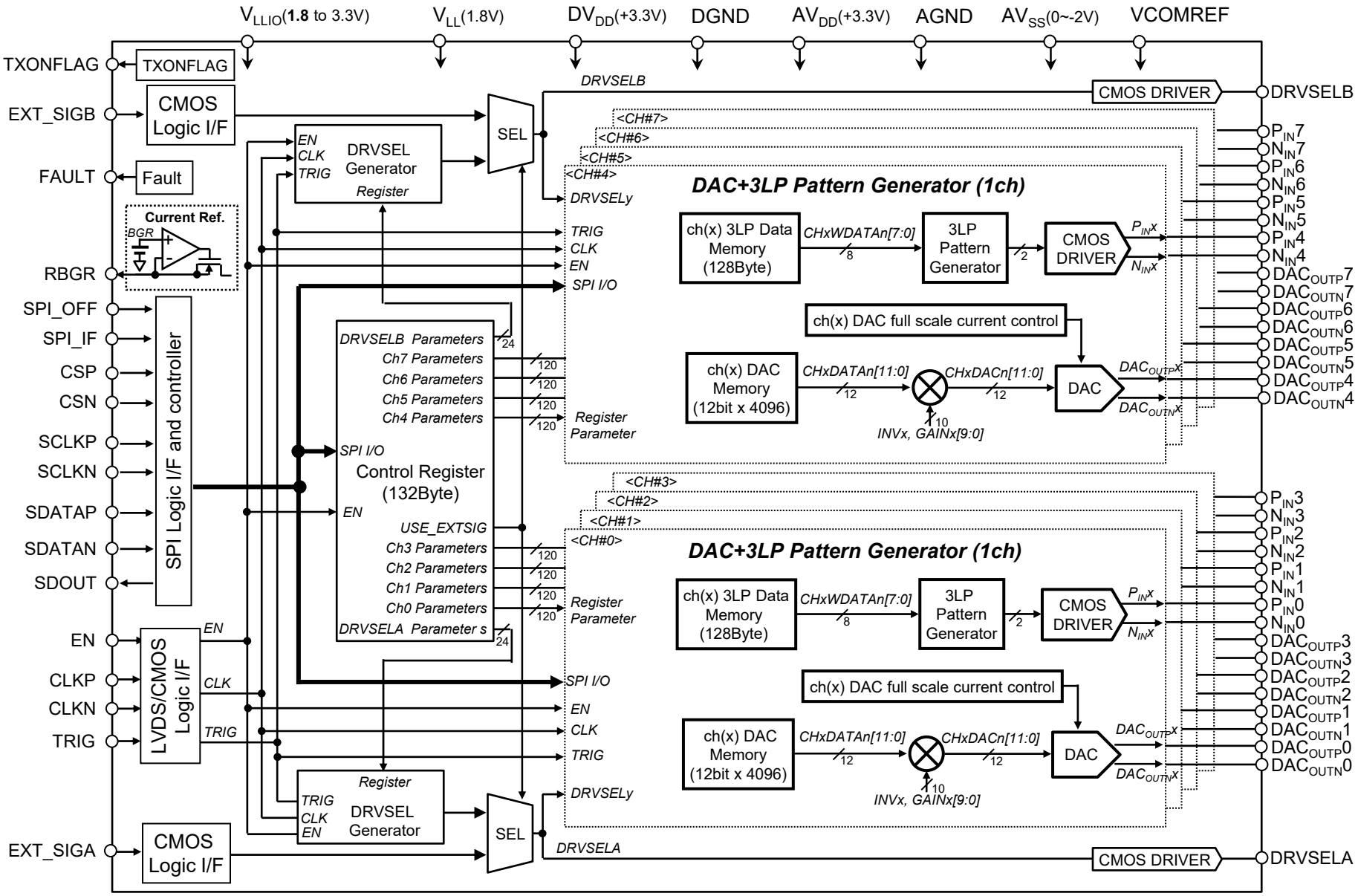
<DAC>
- On-chip 12bit x4096 pattern Memory for each DAC
- 0.16µs to 40.96µs programmable delay time with 5ns resolution from TRIG signal
- 200MSPS sampling rate
- Both current output mode and voltage output mode are available.
- 14Ω/2Ω output impedance are selectable at voltage output mode.
- 1.28mA ~ 10.24mA selectable full-scale current @Current output mode
- 0.074V~0.592V (0.083V~0.664V) selectable full-scale voltage @voltage output mode

<3LP pattern generator>
- On-chip 128Byte pattern Memory for each 3LP pattern generator
- 0.16µs to 40.96µs programmable delay time with 5ns resolution from TRIG signal

<Others>
- Serial Peripheral Interface (SPI) for access to Memory and Register.
- 1.8V to 3.3V CMOS control logic interface
- Latch-up free, low crosstalk by SOI CMOS technology
- 68-lead 10x10mm QFN package (RoHS compliant)

■ Contents

■ Block Diagram



■ Absolute Maximum Ratings

T_a=25°C unless otherwise noted.

No.	Items	Symbol	Value	Units	Condition
1	Logic I/F voltage	V_{LLIO}	-0.4 to +4	V	
2	Logic supply voltage	V_{LL}	-0.4 to +2.3	V	
3	Positive supply voltage for DAC	AV_{DD}	-0.4 to +7	V	
4	Negative supply voltage for DAC	AV_{SS}	-7 to +0.4	V	
5	Positive to Negative voltage rail	AV_{DD} - AV_{SS}	-0.4 to +7	V	
6	LVDS Positive supply voltage	DV_{DD}	-0.4 to +7	V	
7	DAC outputs (x=0~7)	I_{DACP}x, I_{DACN}x	-0.4 to +7	V	
8	RBGR output voltage	RBGR	-0.4 to +7	V	
9	VCOMREF input voltage	VCOMREF	AV_{SS} to AV_{DD}	V	
10	Logic output voltage (x=0~7)	P_{IN}x, N_{IN}x, DRVSELA, DRVSELB, SDOUT, FAULT	-0.4 to +7	V	
11	Logic input voltages	CLKP, CLKN, TRIG, SPI_OFF, EN, EXT_SIGA, EXT_SIGB, CSP, CSN, SCLKP, SCLKN, SDATAP, SDATAN	-0.4 to +7	V	
12	Operating junction temperature	T_{Jop}	-20 to +125	°C	
13	Storage temperature	T_{STG}	-55 to +150	°C	
14	Maximum power dissipation	P_{Dmax}	4	W	

NOTE: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

■ Operating Supply Voltage and Temperature

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic I/F voltage	V_{LLIO}	1.71	1.8 to 3.3	3.6	V	
2	Logic supply voltage ※1	V_{LL}	1.71	1.8	1.89	V	
3	LVDS Positive supply voltage	DV_{DD}	3.0	3.3	3.6	V	
4	DAC Positive supply voltage	AV_{DD}	3.0	3.3	3.6	V	
5	DAC Negative supply voltage	AV_{SS}	-2		0	V	
6	GND for LOGIC	DGND	-	0	-	V	
7	GND for DAC	AGND	-	0	-	V	
8	IC substrate voltage *	V_{SUB}	-	0	-	V	
9	DAC common voltage reference (Voltage output mode only)	VCOMREF	AV_{SS} +1.1		AV_{DD} -2	V	Register parameter OUTIFSEL[1:0]=10
			AV_{SS} +1.2		AV_{DD} -2	V	Register parameter OUTIFSEL[1:0]=11
10	Operating free-air Temperature	T_a	0		75	°C	

NOTE: * The package exposed pad internally connected to the chip substrate must be soldered to the ground.

※1. Be sure to power on VLL last

■ LVDS Differential Logic Inputs

CLKP/CLKN, CSP/CSN, SCLKP/SCLKN, SDATAP/SDATAN

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level input voltage	V_{IH}	1.265	-	-	V	V_{IHCMR}(Typ)+V_{DIFF}(Min)/2
2	Low-level input voltage	V_{IL}	-	-	1.135	V	V_{IHCMR}(Typ)-V_{DIFF}(Min)/2
3	Differential input voltage range	$V_{DIFF(range)}$	0.13	0.35	0.49	±V	Same as voltage swing
4	Differential input voltage peak to peak swing	$V_{DIFF(p-p)}$	0.26	0.7	0.98	V_{pp}	Differential peak-to-peak absolute voltage swing
5	Input common mode voltage	V_{IHCMR}	0.84	1.2	1.56	V	
6	High-level input current	I_{IH}	-	-	5.8	mA	
7	Low-level input current	I_{IL}	-	-	5.8	mA	
8	Input rise/fall time	t_r , t_f	-	-	600	ps	20% to 80% of V_{DIFF}
9	Input clock frequency (Tx)	f_{CLK}	-	-	200	MHz	CLKP/CLKN T_{CLK}=1/f_{CLK}
	Input clock frequency (SPI)	f_{SCLK}	-	-	100	MHz	SCLKP/SCLKN (Write mode), T_{SCLK}=1/f_{SCLK}
			-	-	50	MHz	SCLKP/SCLKN (Read mode)
10	Clock duty cycle	D_{CLK}, D_{SCLK}	45	50	55	%	
11	SDATA setup time	t_{SU_SDATA}	2.5			ns	SDATA to SCLK rise
12	SDATA hold time	t_{HLD_SDATA}	2.5			ns	SDATA to SCLK rise
13	CS setup time	t_{SU_CS}	2.5			ns	CS to SCLK rise
14	CS hold time	t_{HLD_CS}	2.5			ns	CS to SCLK rise
15	CS width	t_{W_CS}	$1042T_{SCLK}$			ns	Write to 3LP Memory (128byte)
			$49170T_{SCLK}$			ns	Write to DAC Memory (6144Byte)
			$1074T_{SCLK}$			ns	Write to All Control Register (132Byte)
			$114T_{SCLK}$			ns	Write to common Register (12Byte)
			$138T_{SCLK}$			ns	Write to ch(x) Register (15Byte), x=0~7
			$1042T_{SCLK}$			ns	Read from 3LP Memory (128byte)
			$49170T_{SCLK}$			ns	Read from DAC Memory (6144Byte)
			$1074T_{SCLK}$			ns	Read from All control Register (132Byte)
			$34T_{SCLK}$			ns	Read CRC & Calculated CRC data (2Byte)
			$66T_{SCLK}$			ns	Read from Error Register (6Byte)

NOTE: External termination resister (100Ω) is necessary for LVDS I/F differential inputs.

■ CMOS Logic Inputs & Outputs

EN, TRIG, SPI_OFF, EXT_SIGA, EXT_SIGB, SDOUT, DRVSELA, DRVSELB, PINx/NINx (x=0~7), CSP/CSN *2, SCLKP/SCLKN *2, SDATAP/SDATAN *2

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level logic input voltage	V_{IH}	$0.8V_{LLIO}$	-	V_{LLIO}	V	
2	Low-level logic input voltage	V_{IL}	0	-	$0.2V_{LLIO}$	V	
3	Logic input capacitance	C_{IN}	-	3	-	pF	
4	Logic input high current	I_{IH}	-10	-	10	μA	
5	Logic input low current *1	I_{IL}	-10	-	10	μA	
6	Input rise/fall time	t_r , t_f	-	-	2.0	ns	10~90% of signal
7	TRIG fall to clock rise setup time	$t_{SU\_TRFtoCKR}$	1.4	-	-	ns	
8	TRIG fall to clock rise hold time	$t_{HLD\_TRFtoCKR}$	1.4	-	-	ns	
9	TRIG width	t_{W_TRIG}	$6T_{CLK}$	-	-	ns	
10	High-level logic output voltage	V_{OH}	$0.8V_{LLIO}$	-	V_{LLIO}	V	SDOUT, PINx/NINx(x=0~7), DRVSELA, DRVSELB
11	Low-level logic output voltage	V_{OL}	0	-	$0.2V_{LLIO}$	V	
12	Logic output off leak current	$I_{OFFLEAK}$	-10	-	10	μA	SDOUT HiZ output
13	SDOUT propagation delay	t_{D_SDOUT}	10	13	17	ns	V_{LLIO}=3.3V
			12	15	19	ns	V_{LLIO}=2.5V
			14	18	23	ns	V_{LLIO}=1.8V

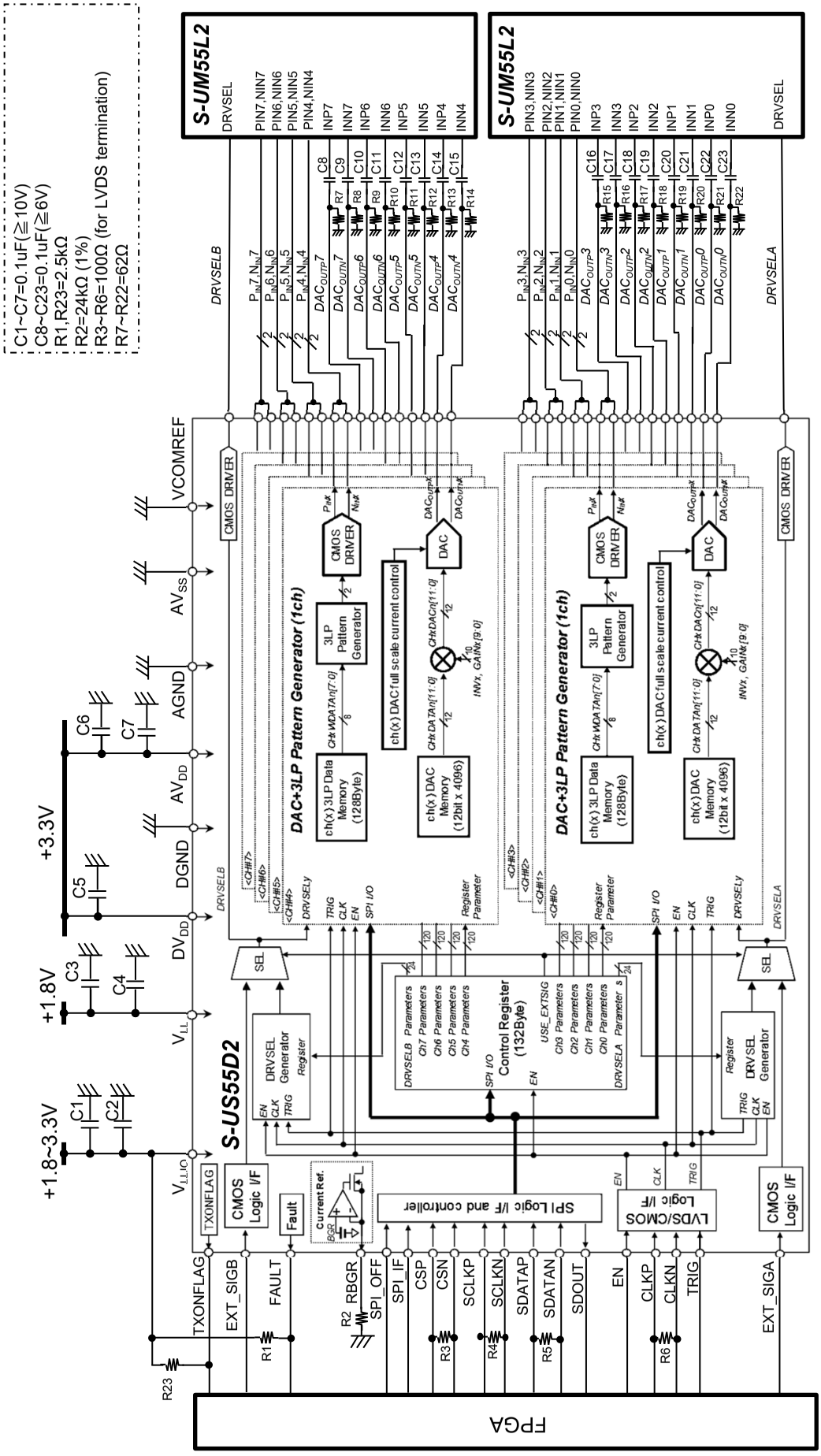
Remark:
*1) EN has 50μA leakage at V_{LLIO}=2.5V due to 50kΩ internal pull-up resistor.
*2) Single-ended CMOS interface is also available for SPI pins of CSP/N, SCLKP/N and SDATAP/N by setting SPI-IF to “Hi”. When SPI-IF is set to “Hi”, SPI CMOS inputs must be connected to P-terminals of SPI pins (CSP, SCLKP and SDATAP) and N-terminals of SPI pins (CSN, SCLKN and SDATAN) are need to be open.
(As for the N-terminals of SPI pins (CSN, SCLKN and SDATAN), half of V_{LLIO} (V_{LLIO}/2) is biased internally .)

■ Open Drain Outputs

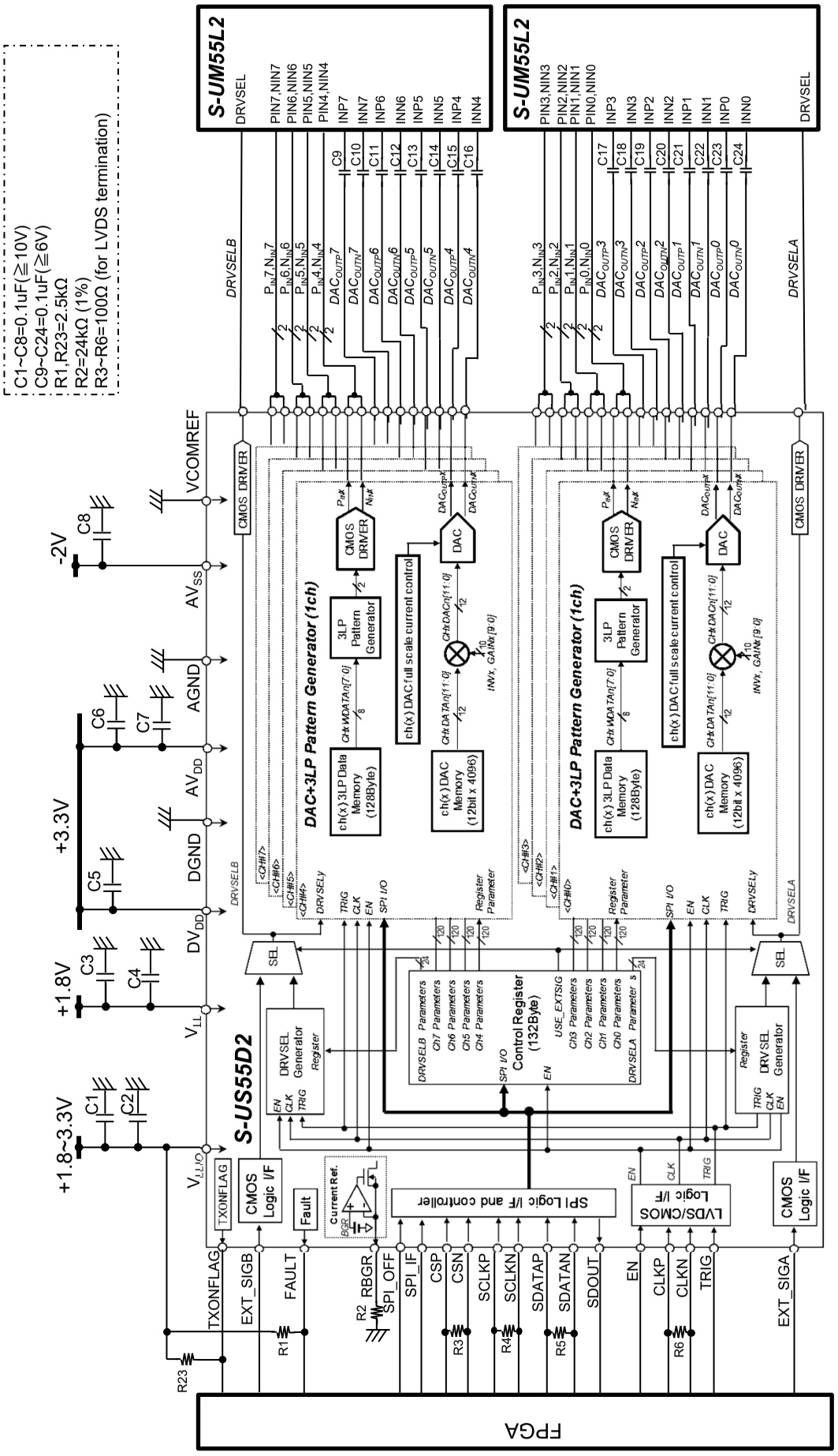
FAULT, TXONFLAG

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Pull-up voltage	$V_{PUFAULT}$	-	-	V_{LLIO}	V	Connected to V_{LLIO} with external pull-up resistor (R1, shown in page 9)
2	Output low voltage	$V_{OLFAULT}$	-	-	0.5	V	Open drain MOS is Active. V_{LLIO}=2.5V External pull-up resistor (R1) =2.5kΩ
3	Output current	I_{FAULT}	-	1.0	-	mA	
4	Off leakage current	$I_{OFFLEAK}$	-10	-	10	µA	Open drain MOS is disabled. (HiZ)

■ Typical Application Circuit (current output)



■ Typical Application Circuit (voltage output)



■ Operating Supply Currents (1)

V_{LLIO}=2.5V, V_{LL}=1.8V, DV_{DD}=AV_{DD}=3.3V, AV_{SS}=-2V, T_A=25˚C, CLKP/CLKN=200MHz,
PINx/NINx(x=0~7) load = 10pF, unless otherwise specified.

No	Items		Symbol	Min	Typ	Max	Units	Condition
1	V_{LLIO} current		I_{LLIOQD}	-	0.06	-	mA	Quiescent current-1 Quiescent current at chip is disabled. EN="1"(Disable) CLKP/CLKN is stopped.
2	V_{LL} current		I_{LLQD}	-	0.11	-	mA	
3	DV_{DD} current	SPI_OFF="1",SPI_IF="0/1"	I_{DDDQD}	-	0.7	-	mA	
		SPI_OFF="0",SPI_IF="1"		-	1.3	-	mA	
		SPI_OFF="0",SPI_IF="0"		-	6.3	-	mA	
4	AV_{DD} current		I_{ADDQD}	-	2.8	-	mA	
5	AV_{SS} current		I_{ASSQD}	-	0.65	-	mA	
6	V_{LLIO} current		$I_{LLIOQE1}$	-	0.1	-	mA	Quiescent current-2 Quiescent current at chip is enable and all DAC is bias-off, Both DAC and 3LP-PG are not operated. EN="0"(Enable) CLKP/CLKN is activated (200MHz) DACTXCHx="0" (x=0~7) TLPTXCHx="0" (x=0~7) PWRSAVE="1"
7	V_{LL} current		I_{LLQE1}	-	22.3	-	mA	
8	DV_{DD} current	SPI_OFF="1",SPI_IF="0/1"	I_{DDDQE1}	-	3.2	-	mA	
		SPI_OFF="0",SPI_IF="1"		-	3.8	-	mA	
		SPI_OFF="0",SPI_IF="0"		-	8.6	-	mA	
9	AV_{DD} current		I_{ADDQE1}	-	2.9	-	mA	
10	AV_{SS} current		I_{ASSQE1}	-	0.65	-	mA	
11	V_{LLIO} current		$I_{LLIOQE2}$	-	0.1	-	mA	Quiescent current-3 Quiescent current at chip is enable and all DAC is bias-on, Both DAC and 3LP-PG are not operated. EN="0"(Enable) CLKP/CLKN is activated (200MHz) DACTXCHx="0" (x=0~7) TLPTXCHx="0" (x=0~7) PWRSAVE="0"
12	V_{LL} current		I_{LLQE2}	-	22.3	-	mA	
13	DV_{DD} current	SPI_OFF="1",SPI_IF="0/1"	I_{DDDQE2}	-	3.2	-	mA	
		SPI_OFF="0",SPI_IF="1"		-	3.8	-	mA	
		SPI_OFF="0",SPI_IF="0"		-	8.6	-	mA	
14	AV_{DD} current	ICSELx[2:0] ="111"	I_{ADDQE2}	-	88	-	mA	
		ICSELx[2:0] ="000"		-	14	-	mA	
15	AV_{SS} current		I_{ASSQE2}	-	0.65	-	mA	

■ Operating Supply Currents (2)

V_{LLIO}=2.5V, V_{LL}=1.8V, DV_{DD}=AV_{DD}=3.3V, AV_{SS}=-2V, T_A=25˚C, CLKP/CLKN=200MHz, unless otherwise specified.

No	Items		Symbol	Min	Typ	Max	Units	Condition
16	V_{LLIO} current		$I_{LLIODAC1}$	-	0.1	-	mA	DAC operating current -1 Operating current with current DAC. EN="0"(Enable) DRVSELA/B ="1" (DAC is selected) DAC output load = 50Ω//2pF All channel active CW 5MHz sin wave outputs OUTIFSEL[1:0]="00" (Current output mode) DACTXCHx="1" (x=0~7)
17	V_{LL} current		I_{LLDAC1}	-	229	-	mA	
18	DV_{DD} current	SPI_OFF="1",SPI_IF="0/1"	$I_{DDDDAC1}$	-	3.2	-	mA	
		SPI_OFF="0",SPI_IF="1"		-	3.8	-	mA	
		SPI_OFF="0",SPI_IF="0"		-	8.6	-	mA	
19	AV_{DD} current	ICSELx[2:0] ="111"	$I_{ADDDAC1}$	-	229	-	mA	
		ICSELx[2:0] ="000"		-	156	-	mA	
20	AV_{SS} current		$I_{ASSDAC1}$	-	0.65	-	mA	
21	V_{LLIO} current		$I_{LLIODAC2}$	-	0.1	-	mA	DAC operating current -2 Operating current with voltage DAC (Ro=14Ω). EN="0"(Enable) DRVSELA/B ="1" (DAC is selected) DAC output load = 500Ω//2pF All channel active CW 5MHz sin wave outputs OUTIFSEL[1:0]="10" (Voltage mode Ro=14Ω) DACTXCHx="1" (x=0~7)
22	V_{LL} current		I_{LLDAC2}	-	229	-	mA	
23	DV_{DD} current	SPI_OFF="1",SPI_IF="0/1"	$I_{DDDDAC2}$	-	3.2	-	mA	
		SPI_OFF="0",SPI_IF="1"		-	3.8	-	mA	
		SPI_OFF="0",SPI_IF="0"		-	8.6	-	mA	
24	AV_{DD} current	ICSELx[2:0] ="111"	$I_{ADDDAC2}$	-	206	-	mA	
		ICSELx[2:0] ="000"		-	183	-	mA	
25	AV_{SS} current	ICSELx[2:0] ="111"	$I_{ASSDAC2}$	-	62	-	mA	
		ICSELx[2:0] ="000"		-	40	-	mA	
26	V_{LLIO} current		$I_{LLIODAC3}$	-	0.1	-	mA	DAC operating current -3 Operating current with voltage DAC (Ro=2Ω). EN="0"(Enable) DRVSELA/B ="1" (DAC is selected) DAC output load= 500Ω//2pF All channel active CW 5MHz sin wave outputs OUTIFSEL[1:0]="11" (Voltage mode Ro=2Ω) DACTXCHx="1" (x=0~7)
27	V_{LL} current		I_{LLDAC3}	-	229	-	mA	
28	DV_{DD} current	SPI_OFF="1",SPI_IF="0/1"	$I_{DDDDAC3}$	-	3.2	-	mA	
		SPI_OFF="0",SPI_IF="1"		-	3.8	-	mA	
		SPI_OFF="0",SPI_IF="0"		-	8.6	-	mA	
29	AV_{DD} current	ICSELx[2:0] ="111"	$I_{ADDDAC3}$	-	310	-	mA	
		ICSELx[2:0] ="000"		-	287	-	mA	
30	AV_{SS} current	ICSELx[2:0] ="111"	$I_{ASSDAC3}$	-	163	-	mA	
		ICSELx[2:0] ="000"		-	140	-	mA	

■ Operating Supply Currents (3)

V_{LLIO}=2.5V, V_{LL}=1.8V, DV_{DD}=AV_{DD}=3.3V, AV_{SS}=-2V, T_A=25°C, CLKP/CLKN=200MHz, PINx/NINx(x=0~7) load = 10pF, unless otherwise specified.

No	Items		Symbol	Min	Typ	Max	Units	Condition
1	V_{LLIO} current		$I_{LLIO3LP1}$	-	4.0	-	mA	3LP Pattern Generator operating current-1 Operating current with 3LP Pattern Generator at DAC is bias-off, EN="0"(Enable) DRVSELA/B ="0" (3LP DATA is selected) All channel active, CW 5MHz BIP wave outputs DACTXCHx="0" (x=0~7) TLPTXCHx="1" (x=0~7) PWRSAVE="1"
2	V_{LL} current		I_{LL3LP1}	-	24	-	mA	
3	DV_{DD} current	SPI_OFF="1",SPI_IF="0/1"	$I_{DDD3LP1}$	-	3.2	-	mA	
		SPI_OFF="0",SPI_IF="1"		-	3.8	-	mA	
		SPI_OFF="0",SPI_IF="0"		-	8.6	-	mA	
4	AV_{DD} current		$I_{ADD3LP1}$	-	3.0	-	mA	
5	AV_{SS} current		$I_{ASS3LP1}$	-	0.65	-	mA	
6	V_{LLIO} current		$I_{LLIO3LP2}$	-	4.0	-	mA	3LP Pattern Generator operating current-2 Operating current with 3LP Pattern Generator at current DAC is bias-on, EN="0"(Enable) DRVSELA/B ="0" (3LP DATA is selected) All channel active, CW 5MHz BIP wave outputs OUTIFSEL[1:0]="00" (Current output mode) DACTXCHx="0/1" (x=0~7) TLPTXCHx="1" (x=0~7) PWRSAVE="0"
7	V_{LL} current		I_{LL3LP2}	-	24	-	mA	
8	DV_{DD} current	SPI_OFF="1",SPI_IF="0/1"	$I_{DDD3LP2}$	-	3.2	-	mA	
		SPI_OFF="0",SPI_IF="1"		-	3.8	-	mA	
		SPI_OFF="0",SPI_IF="0"		-	8.6	-	mA	
9	AV_{DD} current	ICSELx[2:0] ="111"	$I_{ADD3LP2}$	-	88	-	mA	
		ICSELx[2:0] ="000"		-	14	-	mA	
10	AV_{SS} current		$I_{ASS3LP2}$	-	0.65	-	mA	
11	V_{LLIO} current		$I_{LLIO3LP3}$	-	4.0	-	mA	3LP Pattern Generator operating current-3 Operating current with 3LP Pattern Generator at voltage DAC is bias-on, EN="0"(Enable) DRVSELA/B ="0" (3LP DATA is selected) All channel active, CW 5MHz BIP wave outputs OUTIFSEL[1:0]="10" (Voltage output mode Ro=14Ω) DACTXCHx="0/1" (x=0~7) TLPTXCHx="1" (x=0~7) PWRSAVE="0"
12	V_{LL} current		I_{LL3LP3}	-	24	-	mA	
13	DV_{DD} current	SPI_OFF="1",SPI_IF="0/1"	$I_{DDD3LP3}$	-	3.2	-	mA	
		SPI_OFF="0",SPI_IF="1"		-	3.8	-	mA	
		SPI_OFF="0",SPI_IF="0"		-	8.6	-	mA	
14	AV_{DD} current	ICSELx[2:0] ="111"	$I_{ADD3LP3}$	-	64	-	mA	
		ICSELx[2:0] ="000"		-	41	-	mA	
15	AV_{SS} current	ICSELx[2:0] ="111"	$I_{ASS3LP3}$	-	62	-	mA	
		ICSELx[2:0] ="000"		-	40	-	mA	

■ Static Characteristics

V_{LLIO}=2.5V, V_{LL}=2.5V, DV_{DD}=AV_{DD}=3.3V, T_A=25˚C, CLKP/CLKN=200MHz, unless otherwise specified.

No	Items	Symbol	Min	Typ	Max	Unit	Note
1	DAC Resolution			12		bits	
2	DAC Differential Nonlinearity	DNLx	-2	+/-1	2	LSB	Differential Non-linearity of DAC differential outputs
3	DAC Integral Nonlinearity	INLx	-3.5	+/-1	3.5	LSB	Integral Non-linearity of DAC differential outputs
4	DAC Full-scale output current (Current output mode)	I_{FS}x	1.28		10.24	mA	Register OUTIFSEL[1:0]="00"
5	DAC Full-scale output voltage (Voltage output mode)	V_{FS}x	0.077		0.592	V	No load, Register OUTIFSEL[1:0]="10" (Ro=14Ω)
			0.083		0.664		No load, Register OUTIFSEL[1:0]="11" (Ro=2Ω)
6	DAC digital gain	G_Dx	-1		1	V/V	programable with register GAINx[9:0] and INVx, except for 0, step=1/1024
7	DAC differential current offset error (Current output mode)	I_{OFS}x	-0.8		+0.8	LSB	Without adjustment
				+/-0.375		LSB	Adjusted with Register OFSADJx[6:0]
8	DAC differential voltage offset error (Voltage output mode)	V_{OFS}x	-5		+5	LSB	Without adjustment, ICSEL[2:0]="111" (V_{FS}x is max)
				+/-0.375		LSB	Adjusted with Register OFSADJx[6:0], ICSEL[2:0]="111"
9	DAC Gain error	G_{ERROR}x	-4	+/-1	+4	%	Without adjustment
				+/-0.06			Adjusted with Register GAINADJx[6:0]
10	DAC ch to ch Gain matching	ΔG_{CH-CH}	+0.6	+/-0.1	-0.6	%	Without adjustment
11	DAC output impedance (Voltage output mode only)	Ro	100M			Ω	DAC is disabled
				18			DAC is active, OUTIFSEL[1:0]="10"
				3.5			DAC is active, OUTIFSEL[1:0]="11"
12	DAC output common voltage error	V_{OFS_COM}	-10		10	mV	Voltage output only (OUTIFSEL[1:0]="10" or "11")
13	Internal BGR reference voltage	V_{BGR}		1.207		V	

■ Dynamic Characteristics

V_{LLIO}=2.5V, V_{LL}=1.8V, DV_{DD}=AV_{DD}=3.3V, V_{SS}=-2V, T_A=25˚C, CLKP/CLKN=200MHz, ICSELx[2:0]=111, VCOMREF=0V, unless otherwise specified.

No.	Items	Symbol	Min	Typ	Max	Unit	Note
1	DAC Spurious Free Dynamic Range	SFDR	49	55		dBc	f_{CLK}= 200MHz, ICSELx[2:0]=111, Current output, 5MHz
2	DAC output noise (load noise is included, @5MHz)	No		2		nv/rtHz	Current output (OUTIFSEL[1:0]="00"), load=50Ω//2pF
				4.5			Voltage output (OUTIFSEL[1:0]="10"), load=500Ω//2pF
				6			Voltage output (OUTIFSEL[1:0]="11"), load=500Ω//2pF
3	DAC differential output voltage	DR_{VOUT}		1.03		Vpp	Current output (OUTIFSEL[1:0]="00") load=50Ω//2pF
				1.15			Voltage output (OUTIFSEL[1:0]="10") load=500Ω//2pF
				1.33			Voltage output (OUTIFSEL[1:0]="11") load=500Ω//2pF
4	DAC output propagation delay (From programmed delay clock rise)	t_{PD_DAC}		14		ns	Current output (OUTIFSEL[1:0]="00") load=50Ω//2pF
				16			Voltage output (OUTIFSEL[1:0]="10") load=500Ω//2pF
				17.5			Voltage output (OUTIFSEL[1:0]="11") load=500Ω//2pF
5	DAC output rise/fall time (full-scale swing, 10%-90%)	t_{RF_DAC}		3		ns	Current output (OUTIFSEL[1:0]="00") load=50Ω//2pF
				8			Voltage output (OUTIFSEL[1:0]="10") load=500Ω//2pF
				5.5			Voltage output (OUTIFSEL[1:0]="11") load=500Ω//2pF
6	DAC output current settling time (full-scale step, settling to <+/-0.1%)	t_{SET_DAC}		9		ns	Current output (OUTIFSEL[1:0]="00") load=50Ω//2pF
				22			Voltage output (OUTIFSEL[1:0]="10") load=500Ω//2pF
				26			Voltage output (OUTIFSEL[1:0]="11") load=500Ω//2pF
7	3LP Data output propagation delay	t_{PD_3LP}		11		ns	From programmed delay clock rise edge
8	3LP Data output rise/fall time	t_{RF_3LP}		1	2	ns	load = 10pF
9	DRVSEL output propagation delay	t_{PD_DRVSEL}		12		ns	From programmed wait clock rise edge
10	DRVSEL output rise/fall time	t_{RF_DRVSEL}		1	2	ns	load = 10pF

■ Tx Pattern Width and Delay Digital Control Table

Clock frequency = 200MHz (T_{CLK}=5ns)

No	Items	Symbol	Min	Typ	Max	Unit	Note
1	DRVSELy(y=A,B) wait time from TRIG fall edge	$T_{WAIT\_DRVSELy}$	0.16		40.955	μs	$T_{WAIT\_DRVSELy} = T_{CLK}$*(32*WAITy + 31) WAITy(=0~255) is decimal number of WAITy[7:0]
2	DRVSELy(y=A,B) wait time step	ΔT_{WAIT_DRVSEL}		0.16		μs	$\Delta T_{WAIT\_DRVSEL} = 32*T_{CLK}$
3	DRVSELy(y=A,B) “high” period	$T_{WIDTH\_DRVSELy}$	0			ms	If WIDTHy[15:0]= all high, Hi state is kept until next Trig rise edge or it is reset by “EN”. Else, $T_{WIDTH\_DRVSELy}$(=0~10.48544ms) = 32*T_{CLK}*WIDTHy WIDTHy(=0~65534) is decimal number of WIDTHy[15:0]
4	DRVSELy(y=A,B) “high” period step	ΔT_{WIDTH_DRVSEL}		0.16		μs	$\Delta T_{WIDTH\_DRVSEL} = 32*T_{CLK}$
5	DRVSELy(y=A,B) L to H settling	T_{PON_DRV}			3.2	μs	During 640 clock cycle (3.2us) from DRVSEL rise/fall edge. DAC/3LP output for Tx is not allowed.
6	DRVSELy(y=A,B) H to L settling	T_{POFF_DRV}			3.205	μs	
7	DAC clock rate	$f_{DAC\text{-}CLK}$			200	Mbps	
8	Initial wait time for DAC/3LP data output from TRIG fall edge	T_{INIT}		0.16		μs	$\Delta T_{INIT} = 32*T_{CLK}$
9	CHx(x=0~7) delay range of DAC output from TRIG fall edge	T_{DL_CHxDAC}	0.16		41.115	μs	T_{DL_CHxDAC}=(32+DAC_DLx)*T_{CLK} DAC_DLx(=0~8191※1) is a decimal number of DAC_DLx [12:0]
10	CHx delay delta resolution of DAC output (x=0~7)	ΔT_{DL_CHxDAC}		5		ns	$\Delta T_{DL\_CHxDAC}=T_{CLK}$
11	Ch#x(x=0~7) Tx pulse width of 3LP	$T_{CHxWIDTHn}$	10		325	ns	$T_{CHxWIDTHn}$ [ns] = T_{CLK} * (CHxWIDTHn + 2) CHxWIDTHn(=0~63) is decimal number of CHxWIDTHn[5:0] in memory #n, n=0~127
12	Tx pulse width resolution of 3LP	$\Delta T_{CHxWIDTHn}$		5		ns	$\Delta T_{CHxWIDTHn} =T_{CLK}$
13	CHx(x=0~7) delay range of 3LP Tx output from TRIG fall edge	T_{DL_CHx3LP}	0.16		41.115	μs	T_{DL_CHx3LP}=(32+TLP_DLx)*T_{CLK} TLP_DLx(=0~8191) is a decimal number of TLP_DLx [12:0]
14	CHx(x=0~7) delay delta resolution of TLP output	ΔT_{DL_CHx3LP}		5		ns	$\Delta T_{DL\_CHx3LP}=T_{CLK}$

※1 . In case of USE_EXTSIG=0 , DAC_DLx=0~639(decimal number) cannot be used due to restrictions with DRVSEL.

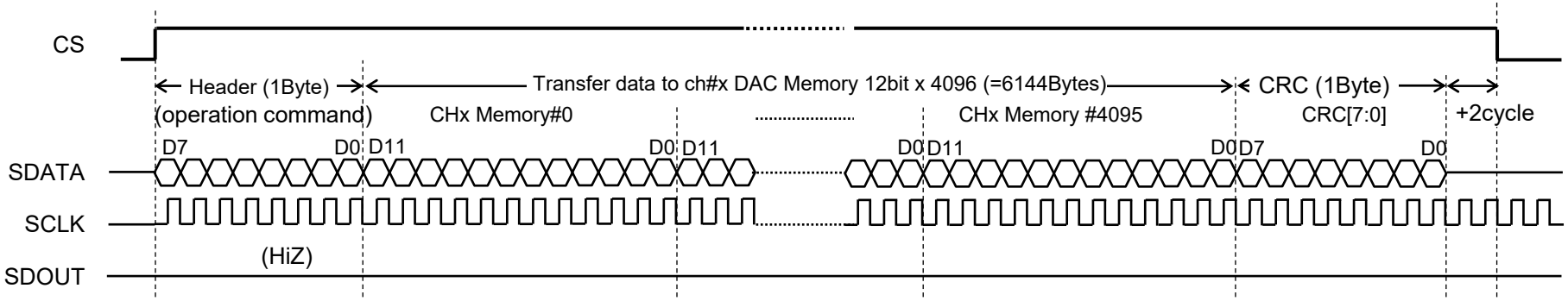
■ SPI Header Configuration

SDATA Control Header (First 1Byte of SDATA)								SPI operation
D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)	
0	*	*	*	*	*	*	*	Hold
1	0	0	0	0	0	0	0	Write to all-channel 3LP Memory at the same time (128Byte)
		0	0	1	0	0	0	Write to CH0 3LP Memory (128Byte)
					0	0	1	Write to CH1 3LP Memory (128Byte)
					0	1	0	Write to CH2 3LP Memory (128Byte)
					0	1	1	Write to CH3 3LP Memory (128Byte)
					1	0	0	Write to CH4 3LP Memory (128Byte)
					1	0	1	Write to CH5 3LP Memory (128Byte)
					1	1	0	Write to CH6 3LP Memory (128Byte)
					1	1	1	Write to CH7 3LP Memory (128Byte)
		0	1	0	0	0	0	Write to all-channel DAC Memory at the same time (6144Byte)
		0	1	1	0	0	0	Write to CH0 DAC Memory (6144Byte)
					0	0	1	Write to CH1 DAC Memory (6144Byte)
					0	1	0	Write to CH2 DAC Memory (6144Byte)
					0	1	1	Write to CH3 DAC Memory (6144Byte)
					1	0	0	Write to CH4 DAC Memory (6144Byte)
					1	0	1	Write to CH5 DAC Memory (6144Byte)
					1	1	0	Write to CH6 DAC Memory (6144Byte)
					1	1	1	Write to CH7 DAC Memory (6144Byte)
		1	0	0	0	0	0	Write to Register 132Byte(#0~#131)
					1	0	0	Write to Register 12Byte(#0~#11)
		1	0	1	0	0	0	Write to Register 15Byte(#12~#26)
					0	0	1	Write to Register 15Byte(#27~#41)
					0	1	0	Write to Register 15Byte(#42~#56)
					0	1	1	Write to Register 15Byte(#57~#71)
					1	0	0	Write to Register 15Byte(#72~#86)
					1	0	1	Write to Register 15Byte(#87~#101)
					1	1	0	Write to Register 15Byte(#102~#116)
					1	1	1	Write to Register 15Byte(#117~#131)
		1	1	*	*	*	*	Don't use
1	1	0	0	0	0	0	0	Don't use
		0	0	1	0	0	0	Read from CH0 3LP Memory (128Byte)
					0	0	1	Read from CH1 3LP Memory (128Byte)
					0	1	0	Read from CH2 3LP Memory (128Byte)
					0	1	1	Read from CH3 3LP Memory (128Byte)
					1	0	0	Read from CH4 3LP Memory (128Byte)
					1	0	1	Read from CH5 3LP Memory (128Byte)
					1	1	0	Read from CH6 3LP Memory (128Byte)
					1	1	1	Read from CH7 3LP Memory (128Byte)
		0	1	0	*	*	*	Don't use
		0	1	1	0	0	0	Read from CH0 DAC Memory (6144Byte)
					0	0	1	Read from CH1 DAC Memory (6144Byte)
					0	1	0	Read from CH2 DAC Memory (6144Byte)
					0	1	1	Read from CH3 DAC Memory (6144Byte)
					1	0	0	Read from CH4 DAC Memory (6144Byte)
					1	0	1	Read from CH5 DAC Memory (6144Byte)
					1	1	0	Read from CH6 DAC Memory (6144Byte)
					1	1	1	Read from CH7 DAC Memory (6144Byte)
		1	0	0	*	*	*	Read from Register 132Byte(#0~#131)
		1	0	1	*	*	*	Don't use
		1	1	0	*	*	*	Read from CRC[7:0] & CAL_CRC[7:0] (2Byte)
		1	1	1	*	*	*	Read from ERROR[47:0] (6byte)

Note: Control Headers which don't listed in the above table are prohibited.

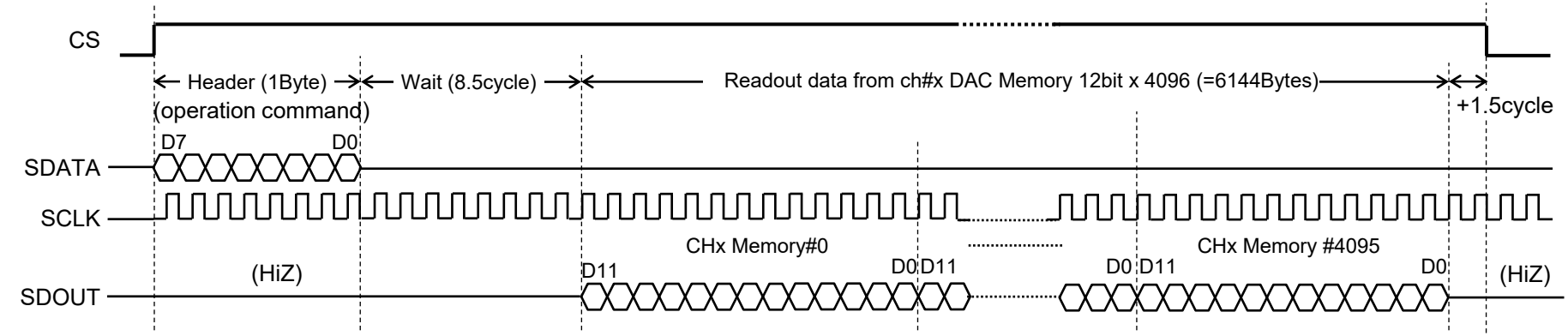
■ Access to DAC Memory with SPI

◆ Write to ch#x DAC Memory



Note:
In “WRITE” operation with SPI, internal logic circuit also calculates the CRC ,and writes it to internal Register CAL_CRC[7:0]. If CAL_CRC[7:0] unmatched transferred CRC data (CRC[7:0]), corresponding ERROR bit is set to “1” and FAULT is reported until ERROR bit is cleared.

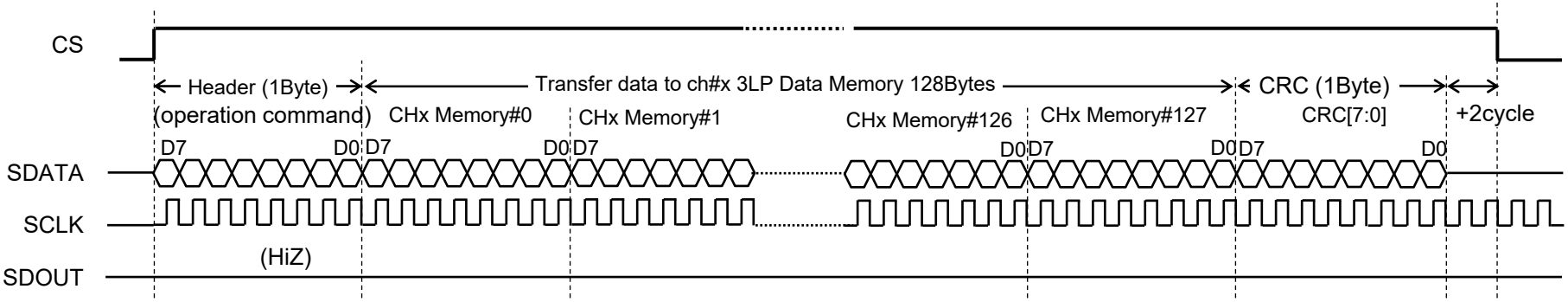
◆ Read from ch#x DAC Memory



Note:
In case of “READ” operation, SDATA inputs except for Header are ignored. (CRC error detection is disabled)

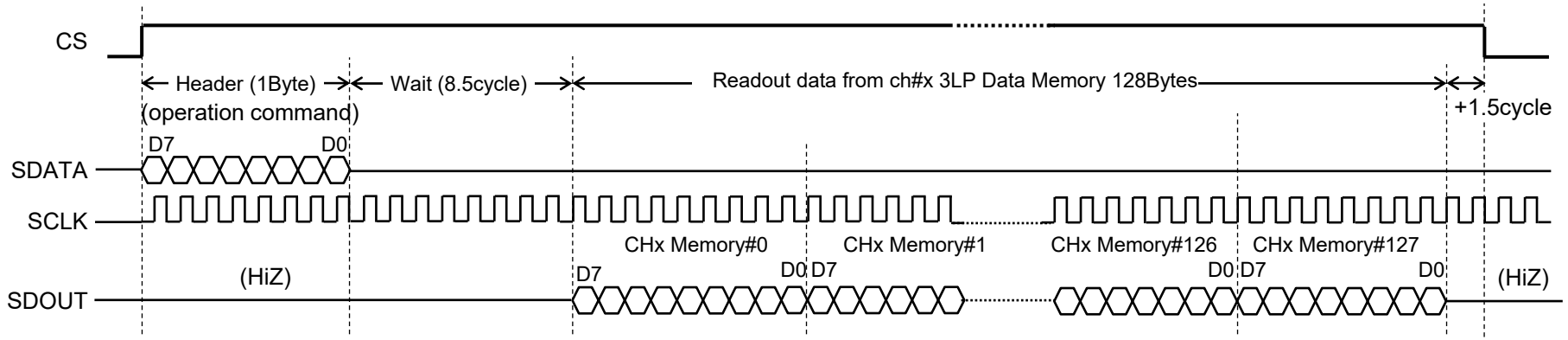
■ Access to 3LP Data Memory with SPI

◆ Write to ch#x 3LP Data Memory



Note:
In “WRITE” operation with SPI, internal logic circuit also calculates the CRC ,and writes it to internal Register CAL_CRC[7:0]. If CAL_CRC[7:0] unmatched transferred CRC data (CRC[7:0]), corresponding ERROR bit is set to “1” and FAULT is reported until ERROR bit is cleared.

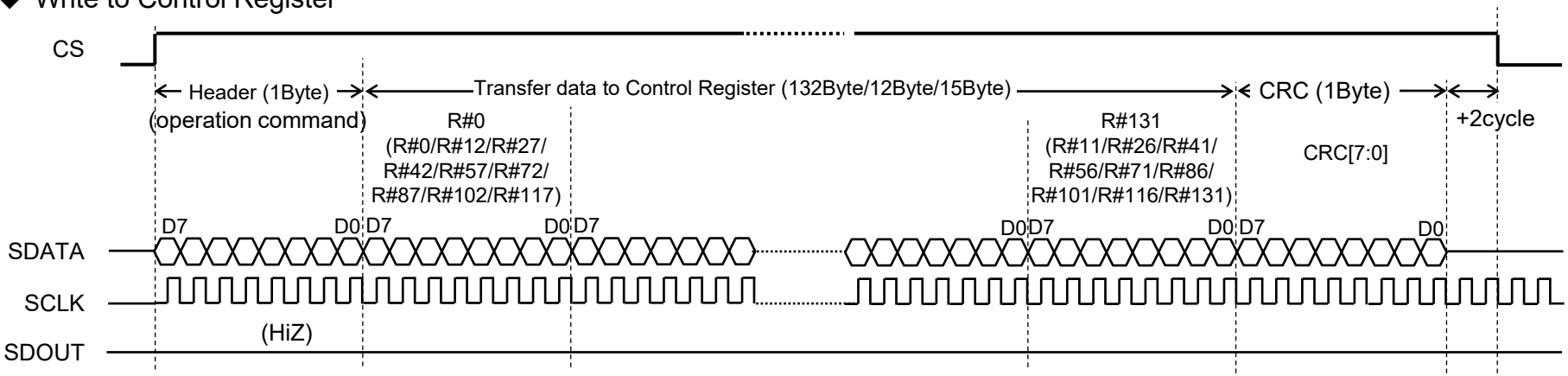
◆ Read from ch#x 3LP Data Memory



Note:
In case of “READ” operation, SDATA inputs except for Header are ignored. (CRC error detection is disabled)

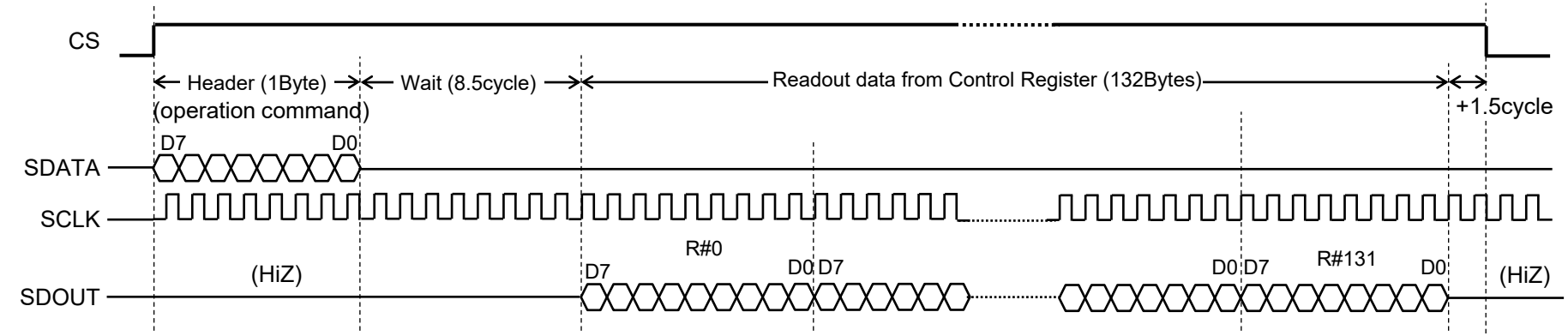
■ Access to Control Register with SPI

◆ Write to Control Register



Note:
In “WRITE” operation with SPI, internal logic circuit also calculates the CRC ,and writes it to internal Register CAL_CRC[7:0]. If CAL_CRC[7:0] unmatched transferred CRC data (CRC[7:0]), corresponding ERROR bit is set to “1” and FAULT is reported until ERROR bit is cleared.

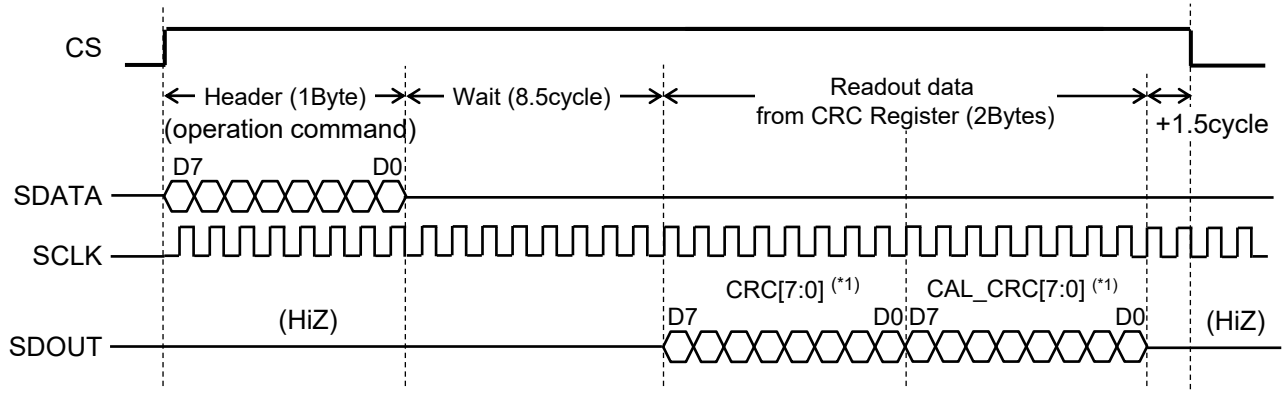
◆ Read from control Register



Note:
In case of “READ” operation, SDATA inputs except for Header are ignored. (CRC error detection is disabled)

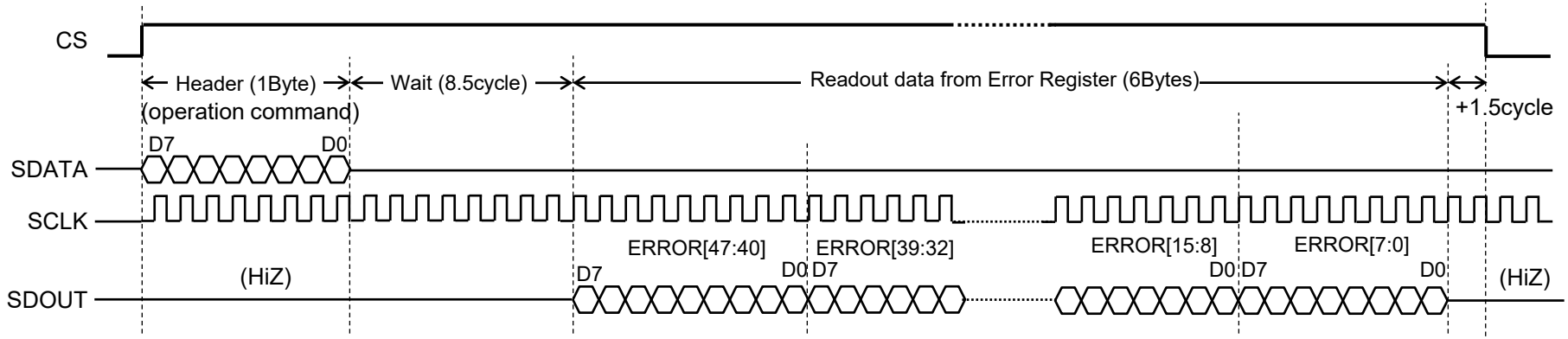
■ Access to CRC & ERROR Register with SPI

◆ Read from CRC Register



Note:
*1: CRC[7:0] and CALCRC[7:0] is the received CRC data and its calculated CRC data in previous “WRITE” operation.

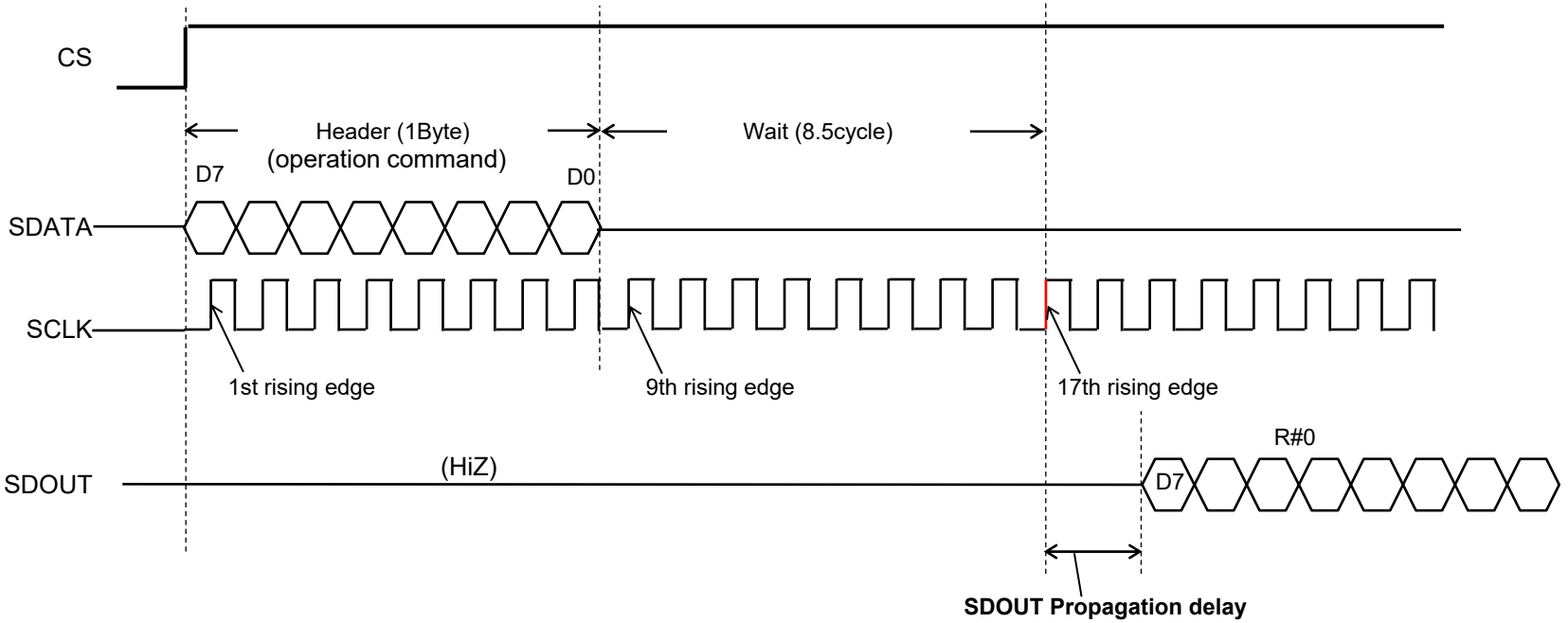
◆ Read from control Register



■ Definition of SDOUT Propagation Delay

The SDOUT propagation delay is defined as the time from the 17th rising edge of SCLK until the data comes out of SDOUT. (Independent of SCLK rate.)

◆ Read from Register and Memory



■ Operation Mode

◆ Operation mode

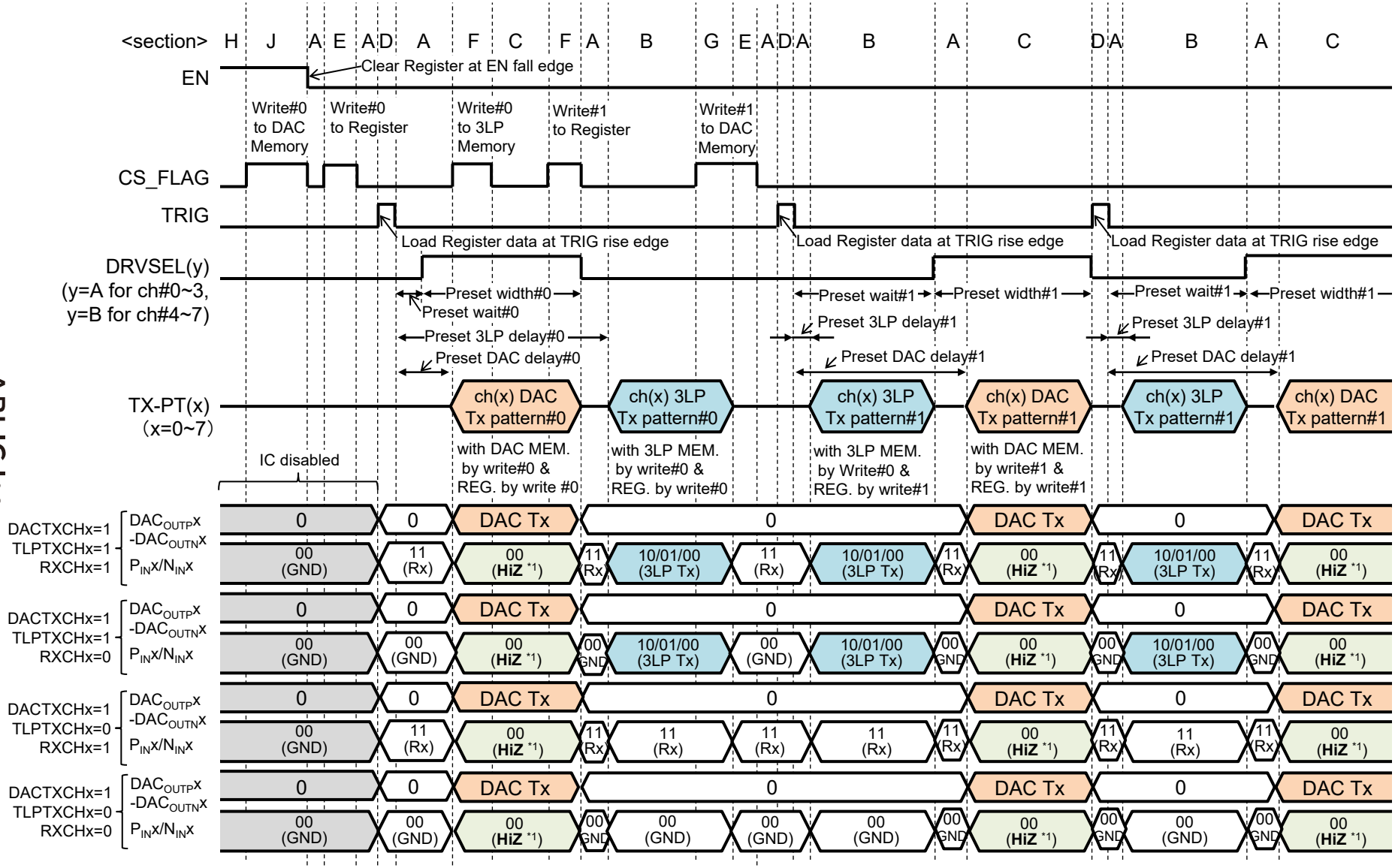
section	EN	CS_FLAG	TRIG	Tx-pattern	DRV_SEL(y)	Access to Ch(x) DAC Memory		Access to Ch(x) 3LP Memory		Access to Register (control)		Ch(x) DAC	Ch(x) 3LP Data		Operation mode
						Write	Read	Write	Read	Write	Read	Tx	Tx	Rx	
A	0	0	0	none	*	×	×	×	×	×	×	×	×	○(*1)	Rx(TRSW control with 3LP data)
B				Gen.	0	×	×	×	×	×	×	×	○(*1)	×	3LP Tx
C				Gen.	1	×	×	×	×	×	×	○(*1)	×	×	DAC Tx
D	0	0	1	none	*	×	×	×	×	×	×	×	×	×	Reset by TRIG
E	0	1	0	none	*	○	○	○	○	○	○	×	×	○(*1)	Access to Memory or Register during Rx
F				Gen.	0	○	○	×(*2)	○	○	○	×	○(*1)	×	Access to Memory or Register during 3LP Tx
G				Gen.	1	×(*2)	×(*2)	○	○	○	○	○(*1)	×	×	Access to Memory or Register during DAC Tx
-	0	1	1	none	*	○	○	○	○	○	○	×	×	×	Error[6] condition, N/A (*3)
H	1	0	*	none	0	×	×	×	×	×	×	×	×	×	Chip disabled
J	1	1	0	none	0	○	○	○	○	×(*4)	○	×	×	×	Access to Memory or Register during chip disabled
-	1	1	1	none	0	○	○	○	○	○	○	×	×	×	Error[6] condition, N/A (*3)

○ : available, × : not available, $CS\_FLAG = CS \bullet \overline{SPI\_OFF}$

SPI_OFF is the bias control of LVDS Receiver in SPI for power saving. (0:bias on, 1:bias-off)
Suffix x (=0~7) corresponds to channel number, and Suffix y (=A/B) corresponds to the number of DRV_SEL.
DRV_SELA(or DRV_SELB) controls the ch0~3 (or ch4~7) operation.

*1 : Register parameter DACTXCHx, TLPTXCHx or RXCHx is necessary to be set “1”.
*2 : If CH(x) DAC Memory is accessed during CH(x) DAC Tx operation or CH(x) 3LP Memory is accessed during CH(x) 3LP Tx operation, ERROR[4] or ERROR[5] is set to “1” and Tx operation is stopped.
*3 : “1” state of TRIG signal during CS_FLAG=‘1’ is the error operation, so Tx operation is reset and its TRIG “1” is ignored.
*4 : Register parameters are reset by fall edge of “EN”.

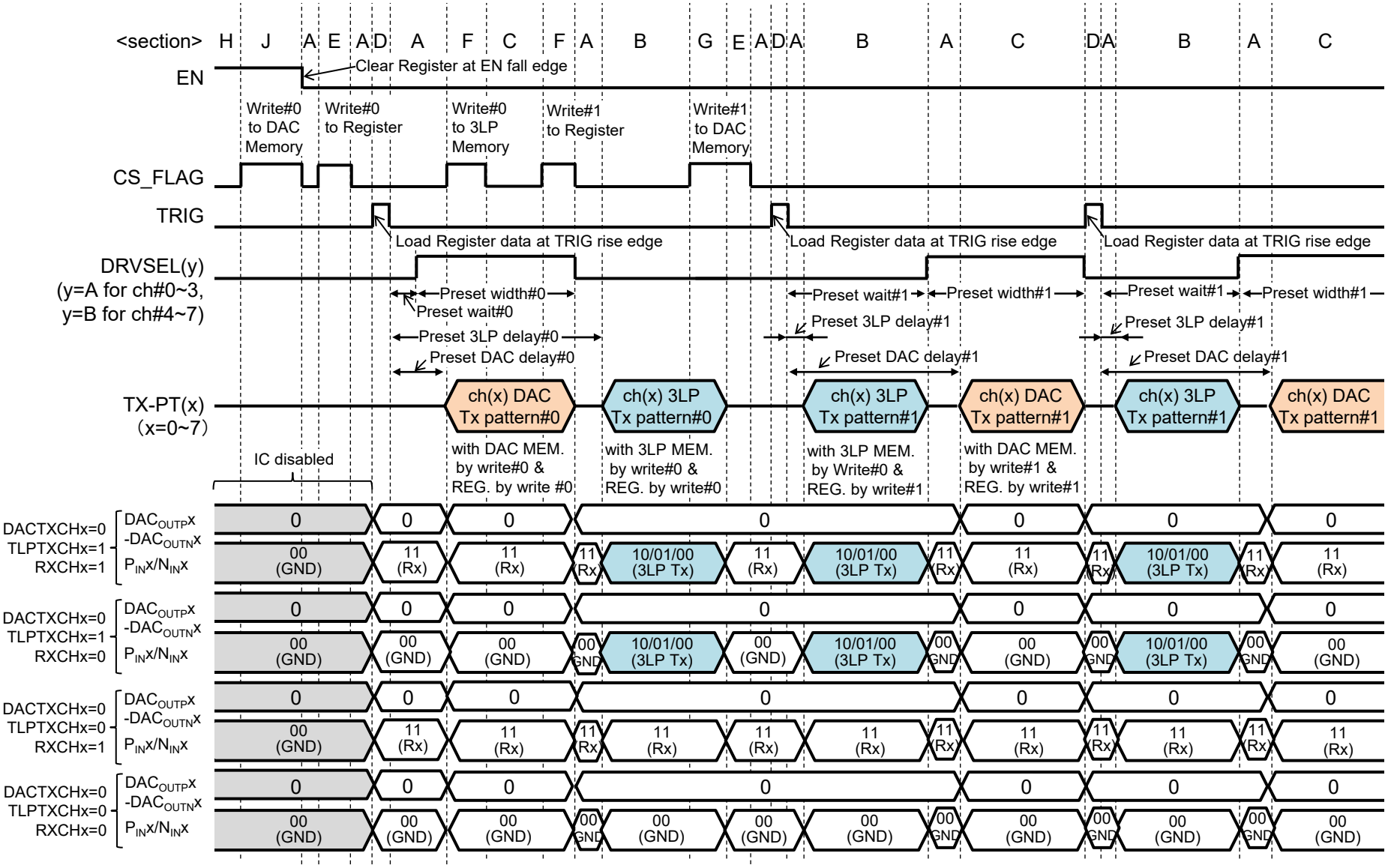
■ Operation Sequence Example



2bit output code of $P_{IN}x/N_{IN}x$ corresponds to 3LP input code of “S-UM55L2”.

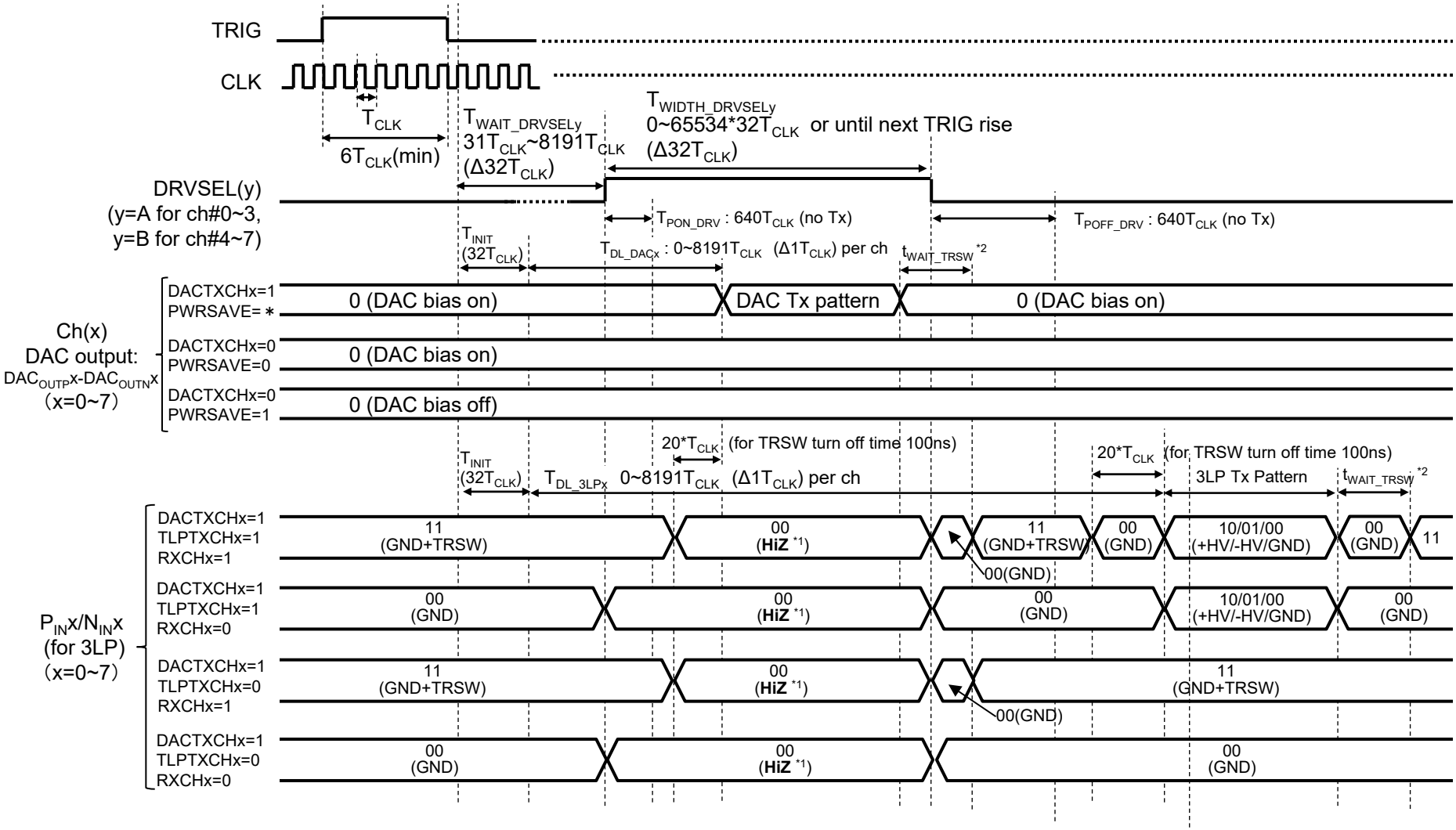
*1: In 3LP Tx driver of “S-UM55L2”, “HiZ” operation is assigned to “00” inputs during DRVSEL =1.

■ Operation Sequence Example (continuation)



2bit output code of $P_{IN}x/N_{IN}x$ corresponds to 3LP input code of “S-UM55L2”.
*1: In 3LP Tx driver of “S-UM55L2”, “HiZ” operation is assigned to “00” inputs during DRVSEL =1.

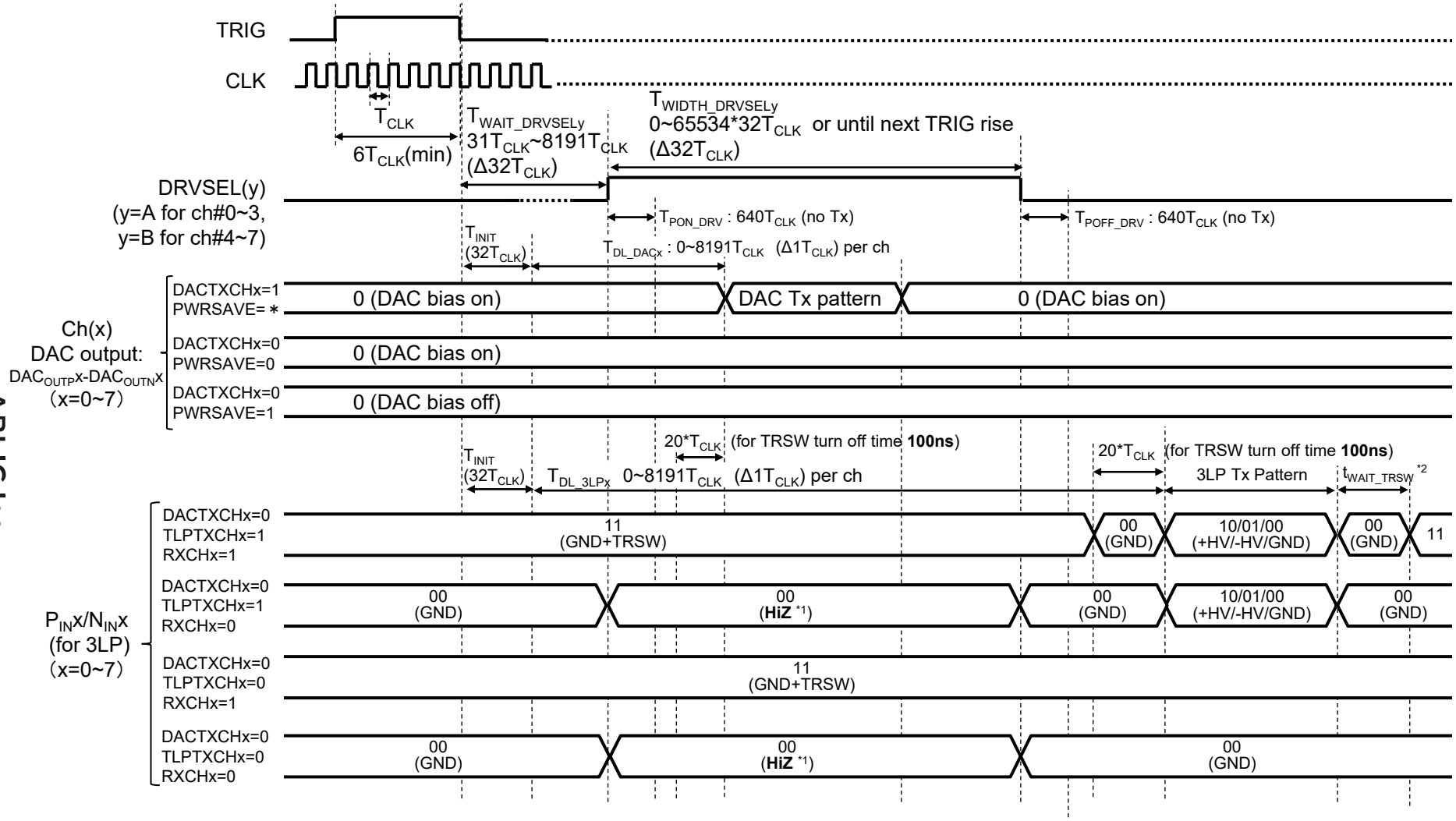
■ Tx Pattern Generation Timing Chart



***1: In S-UM55L2, 3LP driver outputs "HiZ" state during DRVSELy is "Hi" except both PINX and NINx is "Hi".**

*2: t_{WAIT_TRSW} (0/80/120/160/200/240/280/320T_{CLK}) is adjustable clamp time after transmission (per channel).

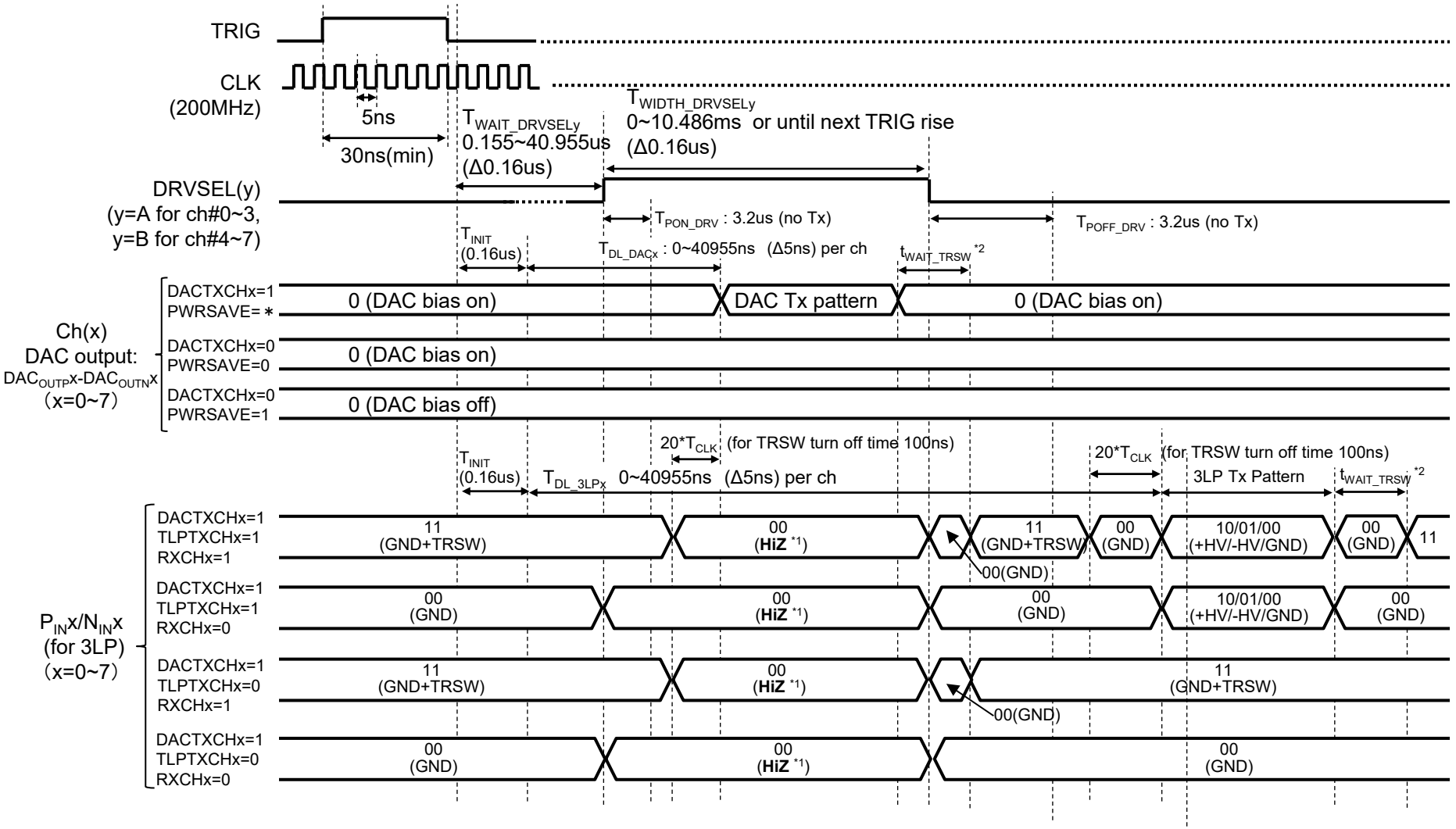
■ Tx Pattern Generation Timing Chart (continuation)



***1: In S-UM55L2, 3LP driver outputs "HiZ" state during DRVSELy is "Hi" except both PINX and NINx is "Hi".**

*2: t_{WAIT_TRSW} (0/80/120/160/200/240/280/320T_{CLK}) is adjustable clamp time after transmission (per channel).

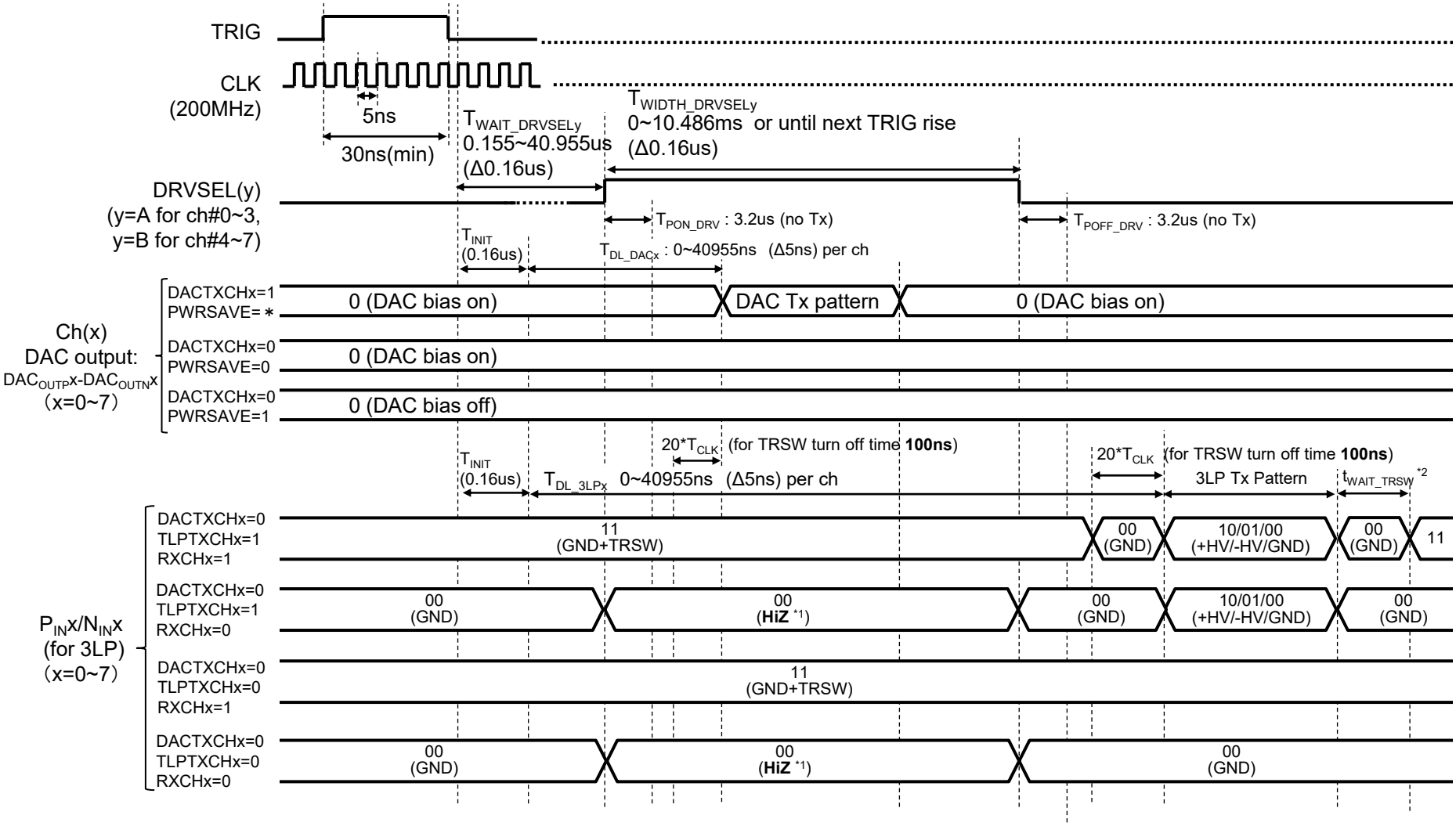
■ Tx Pattern Generation Timing Chart when use 200MHz CLK (1/2)



***1: In S-UM55L2, 3LP driver outputs "HiZ" state during DRVSELy is "Hi" except both PINX and NINx is "Hi".**

*2: t_{WAIT_TRSW} (0ns/400ns/600ns/800ns/1µs/1.2µs/1.4µs/1.6µs) is adjustable clamp time after transmission (per channel).

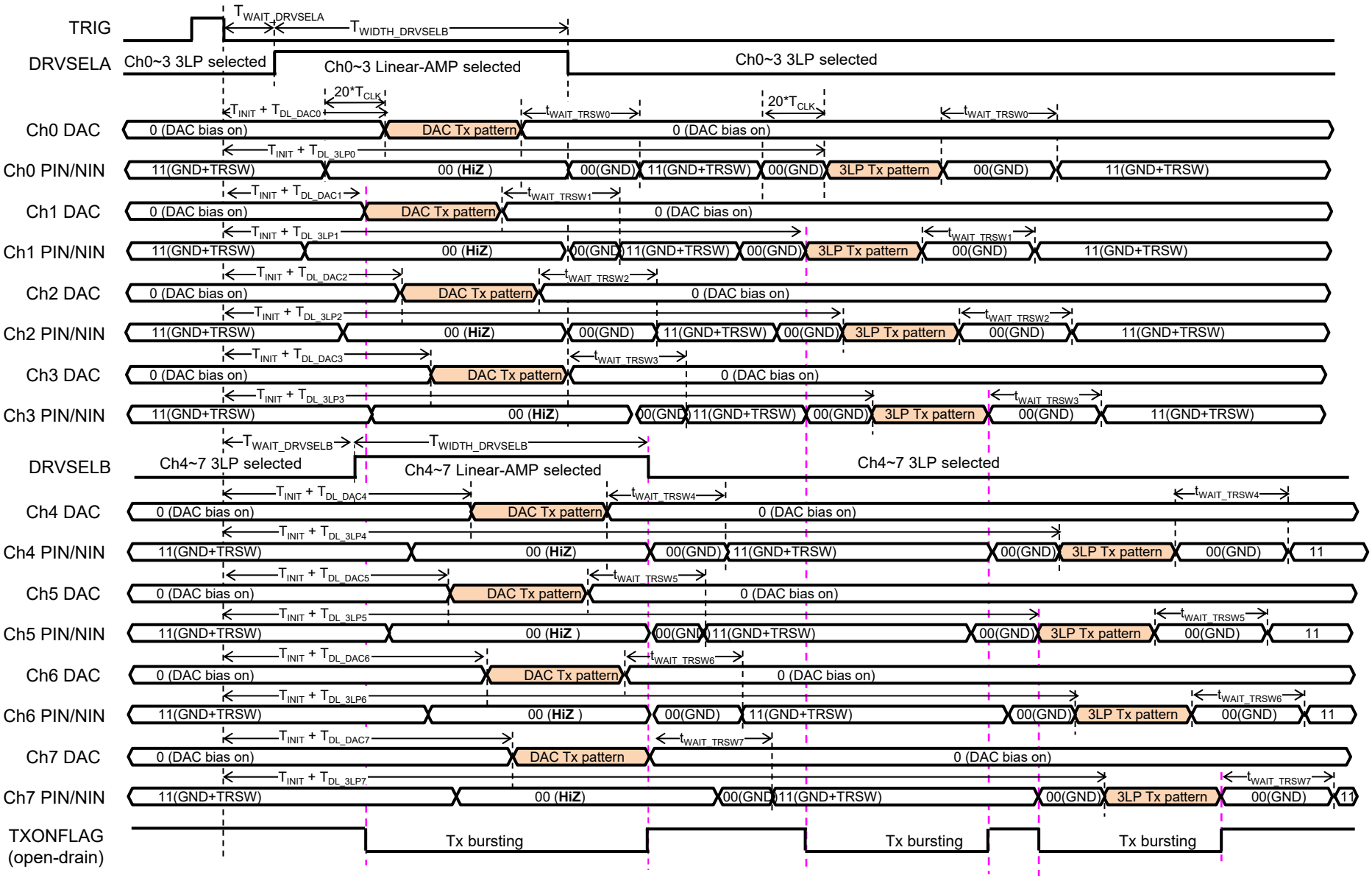
■ Tx Pattern Generation Timing Chart when use 200MHz CLK (2/2)



***1: In S-UM55L2, 3LP driver outputs "HiZ" state during DRVSELy is "Hi" except both PINX and NINx is "Hi".**

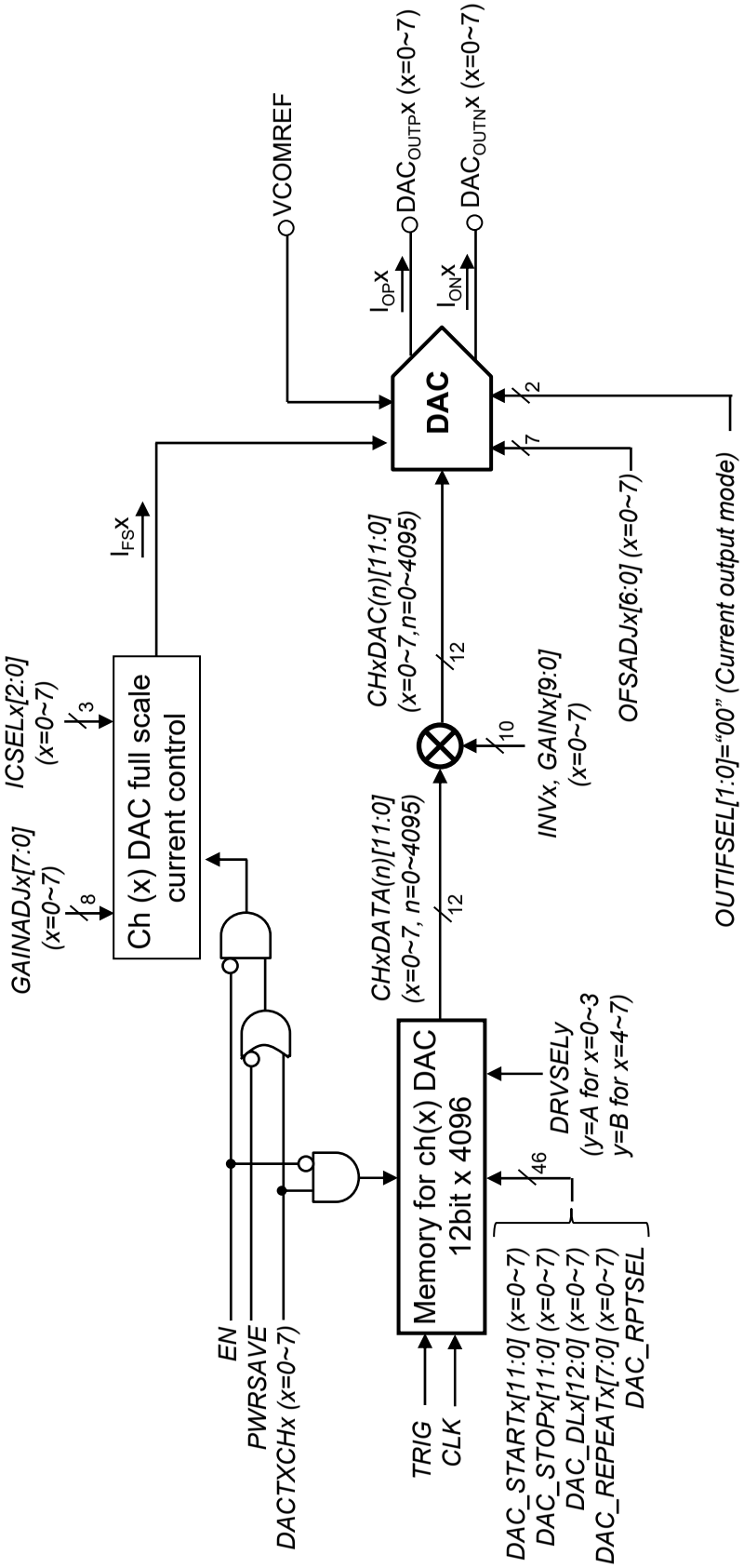
*2: t_{WAIT_TRSW} (0ns/400ns/600ns/800ns/1μs/1.2μs/1.4μs/1.6μs) is adjustable clamp time after transmission (per channel).

■ Tx Timing chart on “TXONFLAG”



Note: TXONFLAG is newly added open-drain indicator which is “OR” of each channel Tx bursting time.

■ DAC Block Diagram (Current Output mode)



■ DAC Equations & Parameter Definitions (Current mode)

◆ DAC Equations

$I_{OP}x$ [mA]=$I_{FS}x$*(2048 + CHxDAC(n))/4096 + $I_{FS}x$*(1-OFSADJx[6])*3*OFSADJx/16384

$I_{ON}x$ [mA]=$I_{FS}x$*(2048 – CHxDAC(n))/4096 + $I_{FS}x$*OFSADJx[6]*3*OFSADJx/16384

$I_{OP}x$ - $I_{ON}x$ [mA] = 2*$I_{FS}x$*CHxDAC(n)/4096 + $I_{FS}x$*(1-2*OFSADJx[6])*3*OFSADJx/16384

$I_{FS}x$ [mA]=1.28*G_{ADJ}*(ICSELx+1)

G_{ADJ} =1+(6.25e-4)*(1-2*GAINADJx[7])*GAINADJx

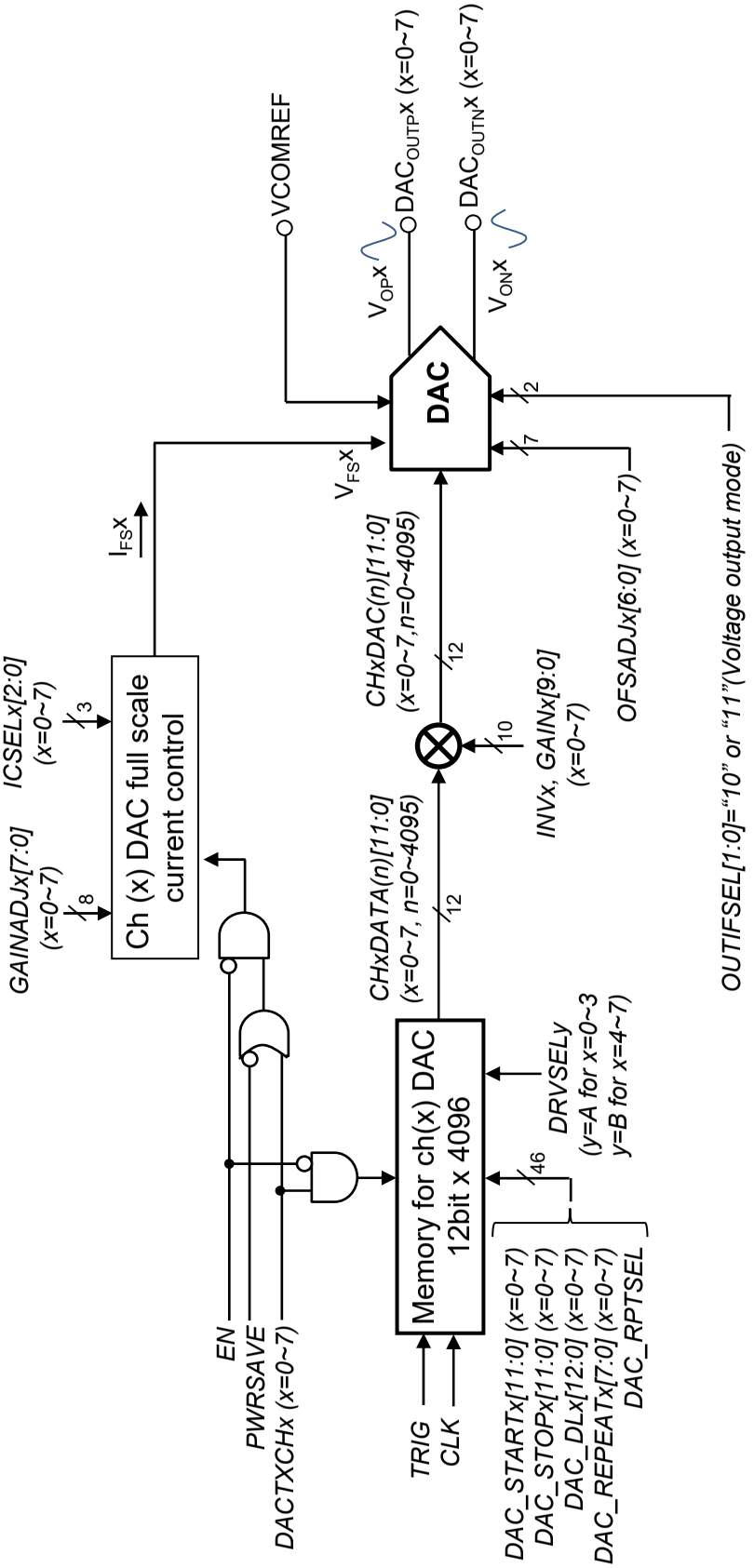
CHxDAC(n)=$G_D x$*CHxDATA(n)

$G_D x$ [V/V]=(1-2*INVX)*(GAINx+1)/1024

◆ Parameter Definitions

$I_{OP}x$ [mA]: ch(x) DAC positive side output current from AV_{DD}
$I_{ON}x$ [mA]: ch(x) DAC negative side output current from AV_{DD}
$I_{OP}x$ - $I_{ON}x$ [mA]: ch(x) DAC differential output current
$I_{FS}x$ [mA]: Selectable DAC full scale current (=1.2875mA~10.3mA, step=1.2875mA=25600*V_{BGR}/R_{BGR} at G_{ADJ}=1 ）
ICSELx(=0~7) : decimal number of 3bit full-scale current selector ICSELx[2:0]
G_{ADJ} [V/V]: Gain adjustment coefficient for DAC unit current compensation (=0.9603 ~1.0397, step=3.125e-4)
GAINADJx[7] (=0/1) : polarity bit of gain compensation data for ch(x) differential DAC output (0=positive, 1=negative)
GAINADJx(=0~127) : decimal number of gain compensation data for ch (x) differential DAC except for MSB (GAINADJ[6:0]).
CHxDAC(n) (=-2047~2047) : decimal number of 12bit DAC inputs CHxDAC(n) [11:0] , MSB is polarity bit
CHxDATA(n) (=-2047~2047) : decimal number of 12bit data CHxDATA(n) [11:0] form ch(x) DAC Memory(#n), MSB is polarity bit.
$G_D x$ [V/V]: Selectable digital gain for DAC (=-1~1 except for 0, step=1/1024)
INVx (=0/1) : Inversion control of DAC/3LP output polarity. (0=Normal, 1=Inversion)
GAINx (=0~1023) is decimal number of GAINx[9:0]
OFSADJx[6] (=0/1) : polarity bit of offset compensation data for differential DAC output (0=positive, 1=negative),
OFSADJx (=0~63) : decimal number of offset compensation data for ch (x) differential DAC except for MSB (OFSADJx[5:0]).

■ DAC Block Diagram (Voltage Output mode)



■ DAC Equations & Parameter Definitions (Voltage mode)

◆ DAC Equations

$V_{OP}x$ [V]=$V_{FS}x$*{ +CHxDAC(n)/4096 + (1-OFSADJx[6])* 3* OFSADJx/16384} + VCOMREF

$V_{ON}x$ [V]=$V_{FS}x$*{ –CHxDAC(n)/4096 + OFSADJx[6]* 3* OFSADJx/16384} + VCOMREF

$V_{OP}x$ - $V_{ON}x$ [V] = $V_{FS}x$*{2*CHxDAC(n)/4096 + (1-2*OFSADJx[6])* 3* OFSADJx/16384}

$V_{FS}x$ [V] =0.074*G_{ADJ}*(ICSELx+1) @OUTIFSEL[1:0]="10"

=0.083*G_{ADJ}*(ICSELx+1) @OUTIFSEL[1:0]="11"

G_{ADJ} =1+(6.25e-4)*(1-2*GAINADJx[7])*GAINADJx

CHxDAC(n)=G_Dx*CHxDATA(n)

G_Dx [V/V]=(1-2*INVX)*(GAINx+1)/1024

◆ Parameter Definitions

$V_{OP}x$ [V]: ch(x) DAC positive side output voltage

$V_{ON}x$ [V]: ch(x) DAC negative side output voltage

$V_{OP}x$ - $V_{ON}x$ [V]: ch(x) DAC differential output voltage

$V_{FS}x$ [mA]: Selectable DAC full scale voltage

= 0.077V~0.616V, step=0.077V @ G_{ADJ}=1 , OUTIFSEL='10'

= 0.083V~0.664V, step=0.083V @ G_{ADJ}=1 , OUTIFSEL='11'

ICSELx(=0~7) : decimal number of 3bit full-scale current selector ICSELx[2:0]

G_{ADJ} [V/V]: Gain adjustment coefficient for DAC unit current compensation (=0.9603 ~1.0397, step=3.125e-4)

GAINADJx[7] (=0/1) : polarity bit of gain compensation data for ch(x) differential DAC output (0=positive, 1=negative)

GAINADJx(=0~127) : decimal number of gain compensation data for ch (x) differential DAC except for MSB (GAINADJ[6:0]).

CHxDAC(n) (=-2047~2047) : decimal number of 12bit DAC inputs CHxDAC(n) [11:0] , MSB is polarity bit

CHxDATA(n) (=-2047~2047) : decimal number of 12bit data CHxDATA(n) [11:0] form ch(x) DAC Memory(#n), MSB is polarity bit.

G_Dx [V/V]: Selectable digital gain for DAC (=-1~1 except for 0, step=1/1024)

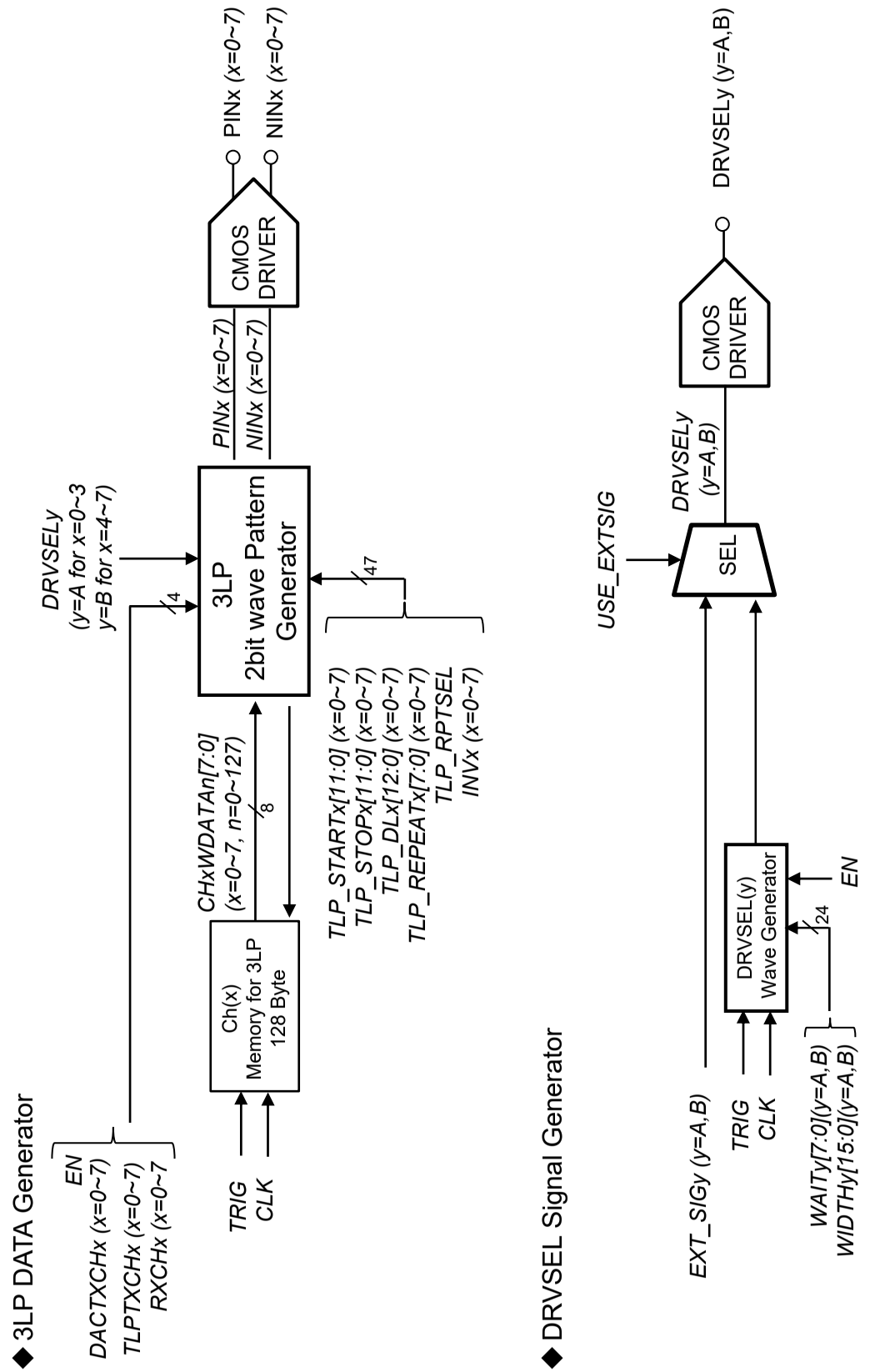
INVx (=0/1) : Inversion control of DAC/3LP output polarity. (0=Normal, 1=Inversion)

GAINx (=0~1023) is decimal number of GAINx[9:0]

OFSADJx[6] (=0/1) : polarity bit of offset compensation data for differential DAC output (0=positive, 1=negative),

OFSADJx (=0~63) : decimal number of offset compensation data for ch (x) differential DAC except for MSB (OFSADJx[5:0]).

■ 3LP DATA & DRVSEL Generator Block Diagram



■ DAC Memory MAP

Ch#x (x=0~7) DAC_MEM.#	D11 (MSB)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	Default	W/R
0	CHxDATA0[11:0]												-	W/R
1	CHxDATA1[11:0]												-	W/R
2	CHxDATA2[11:0]												-	W/R
3	CHxDATA3[11:0]												-	W/R
:	:												:	:
n	CHxDATAn[11:0]												-	W/R
:	:												:	:
4092	CHxDATA4092[11:0]												-	W/R
4093	CHxDATA4093[11:0]												-	W/R
4094	CHxDATA4094[11:0]												-	W/R
4095	CHxDATA4095[11:0]												-	W/R

In CH#x DAC Memory Map, each 12bit code CHxDATAn[11:0] corresponds to read-out data (CHxDATAn) in 1 clock cycle from CH#x DAC Memory#n.
Suffix “x” corresponds to channel number (x=0~7)
Suffix “n” corresponds to Memory number of 12bit code (n=0~4095)
CHxDATAn(=-2047~2047) is a decimal value of CHxDATAn[11:0].
Where, CHxDATAn[11] is polarity bit (0:+, 1: -) and decimal number of CHxDATAn[10:0](=0~2047) expresses the absolute value.
Note: Memory for DAC has no reset sequence.

■ 3LP Data Memory MAP

CH#x (x=0~7) 3LP_MEM.#	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Default	W/R
0	CHxCODE0[1:0]		CHxWIDTH0[5:0]						00000000	W/R
1	CHxCODE1[1:0]		CHxWIDTH1[5:0]						00000000	W/R
2	CHxCODE2[1:0]		CHxWIDTH2[5:0]						00000000	W/R
3	CHxCODE3[1:0]		CHxWIDTH3[5:0]						00000000	W/R
:	:		:						:	:
n	CHxCODEn[1:0]		CHxWIDTHn[5:0]						00000000	W/R
:	:		:						:	:
124	CHxCODE124[1:0]		CHxWIDTH124[5:0]						00000000	W/R
125	CHxCODE125[1:0]		CHxWIDTH125[5:0]						00000000	W/R
126	CHxCODE126[1:0]		CHxWIDTH126[5:0]						00000000	W/R
127	CHxCODE127[1:0]		CHxWIDTH127[5:0]						00000000	W/R

In CH#x 3LP DATA Memory Map, each 1-byte code consists of upper 2-bit CHxCODEn[1:0] and lower 6-bit CHxWIDTHn[5:0].
Suffix “x” corresponds to channel number (x=0~7)
Suffix “n” corresponds to 1-byte Memory number (n=0~127)
CHxCODEn[1:0] stands for an output state for 3LP Tx burst as shown in Truth Table.
CHxWIDTHn[5:0] expresses the pulse width (T_{WIDTH}) which is calculated as follows.

$$T_{CHxWIDTHn}\ [ns] = T_{CLK} * (CHxWIDTHn + 2)$$

Where, T_{CLK} is the CLKP/CLKN clock period and CHxWIDTHn(=0~63) is decimal number of CHxWIDTHn[5:0].
In case of 200MHz clock
T_{CLK} = 5ns and $T_{CHxWIDTHn}$ [ns] is 10ns ~ 325ns (5ns step)
Memory for 3LP data is reset by power-on transition of VLL.

■ Register Function (1)

Register Parameter		Function
PDSEL[1:0]	Common	DAC OUTPUT pull-down control during DAC bias-off 00: Open, 01: Not used, 10: pull-down to GND with 100Ω, 11: pull-down to VCOMREF with 40kΩ
OUTIFSEL[1:0]	Common	DAC OUTPUT mode Selection 00: current output, 01: Not available, 10: voltage output (Ro=14Ω), 11: voltage output (Ro=2Ω)
USE_EXTSIG	Common	0: use internal signal for DRVSELA/B, 1: use external signal as DRVSELA/B
PWRSAVE	Common	0: DAC bias is on at disable state, 1: DAC bias is off at disable state
DAC_RPTSEL	Common	Multiplying factor selection for DAC_REPEATx[7:0] / TLP_REPEATx[7:0] (0=1, 1=16)
TLP_RPTSEL	Common	Multiplying factor selection for DAC_REPEATx[7:0] / TLP_REPEATx[7:0] (0=1, 1=16)
DACTXCHx (x=0~7)	/channel	Enable/Disable control of DAC Outputs (DACOUTPx/DACOUTNx at CHx) (0:disabled, 1:enable) In case of PWRSAVE="1", ch(x) DAC is also bias-off at DACTXCHx="0"
TLPTXCHx (x=0~7)	/channel	Enable/Disable control for 3LP Tx operation at CHx (0: PINx,NINx ="0,0" , 1: PINx,NINx ="0,0" or "1,0" or "0,1" during Tx operation)
RXCHx (x=0~7)	/channel	Enable/Disable control for Rx operation (TRSW of TLP ON/Off) at CHx (0: PINx,NINx ="0,0" , 1: PINx,NINx ="1,1" during Rx operation)
WAITy[7:0] (y=A/B)	/4channel	DRVSELy wait time from TRIG fall : $32*T_{CLK}$*WAITy+$31*T_{CLK}$, WAITy(=0~255) is decimal number of WAITy[7:0]
WIDTHy[15:0] (y=A/B)	/4channel	DRVSELy Hi duration time ($T_{WIDTH\_DRVSEL}y$) WIDTHy[15:0]= 1111111111111111 : keep Hi until next Trig rise edge or reset with "EN" else $T_{WIDTH\_DRVSEL}y = 32*T_{CLK}$*WIDTHy, WIDTHy(=0~65535) is decimal number of WIDTHy[15:0]

Note: Register parameter hatched by brown color is latched to F/F with TRIG rise edge.

■ Register Function (2)

Register Parameter		Function
DAC_STARTx[11:0] (x=0~7)	/channel	Start address (0~4095) of the DAC Memory
DAC_STOPx[11:0] (x=0~7)	/channel	Stop address (0~4095) of the DAC Memory
DAC_REPEATx[7:0]	/channel	Repeat counts control of DAC Tx waveform pattern generation for ch(x) (x=0~7) DACx_REPEAT(=0~255) is decimal number of DAC_REPEATx[7:0] DACx_REPEAT=0, Repeat counts=1 DACx_REPEAT=1~254, Repeat counts=1*DAC_REPEATx or 16*DAC_REPEATx (Multiplying factor (1 or 16) is selectable with DAC_RPTSEL) DACx_REPEAT=255, Repeat counts = continuous wave (CW) CW is stopped by next TRIG rise edge or SPI access
DAC_DLx[12:0] (x=0~7)	/channel	Chx Tx delay from TRIG fall edge : $32*T_{CLK} + T_{CLK}$*DAC_DLx, (DAC_DLx = 0~8191) ※1
ICSELx[2:0] (x=0~7)	/channel	DAC unit current (I_C) , I_C(=0.3125~2.5) [uA] = 0.3125*(1+ICSELx) ICSELx(=0~7) is decimal number of ICSELx[2:0]
GAINx[9:0] (x=0~7)	/channel	DAC Digital Gain Control at CHx (G_{DIG}x), G_{DIG}x(=1/1024~1) = (1+GAINx)/1024 GAINx(=0~1023) is decimal number of GAINx[9:0]
ACT_GAINADJx (x=0~7)	/channel	Option for GAINADJx[7:0] (0: Register GAINADJx[7:0] is not available, 1: Register GAINADJx[7:0] is available)
GAINADJx[7:0] (x=0~7)	/channel	DAC gain adjustment coefficient (G_{ADJ}): 0.9206 ~1.0794 (step=6.25e-4) G_{ADJ} = 1+(1-2*GAINADJx[7])*(6.25e-4)*GAINADJx GAINADJx[7](=0/1) is polarity bit, GAINADJx(=0~127) is decimal number of GAINADJx[6:0]
ACT_OFSADJx (x=0~7)	/channel	Option for OFSADJx[6:0] (0: Register OFSADJx[6:0] is not available, 1: Register OFSADJx[6:0] is available)
OFSADJx[6:0] (x=0~7)	/channel	DAC differential current offset (ΔI_{DACP}x-I_{DACN}x) adjustment : -63*I_C/4 ~ +63*I_C/4, step=I_C/4 OFSADJx[6] =0: OFSADJx*I_C/4 is added to I_{DACP}x. , OFSADJx[6] =1: OFSADJx*I_C/4 is added to I_{DACN}x. OFSADJx(=0~63) is decimal number of OFSADJx[5:0]

Note: Register parameter hatched by brown color is latched to F/F with TRIG rise edge.

※1 . In case of USE_EXTSIG=0 , DAC_DLx=0~639(decimal number) cannot be used due to restrictions with DRVSEL.

■ Register Function (3)

Register Parameter		Function
TLP_STARTx[6:0] (x=0~7)	/channel	Start address (0~127) of the 3LP Memory
TLP_STOPx[6:0] (x=0~7)	/channel	Stop address (0~127) of the 3LP Memory
TLP_REPEATx[7:0]	/channel	Repeat counts control of Tx waveform pattern generation for ch(x) (x=0~7) TLP_REPEATx(=0~255) is decimal number of TLP_REPEATx[7:0] TLP_REPEATx=0 : Repeat counts=1 TLP_REPEATx=1~254 : Repeat counts=1*TLP_REPEATx or 16*TLP_REPEATx (Multiplying factor (1 or 16) is selectable with TLP_RPTSEL.) TLP_REPEATx=255 : Repeat counts = continuous wave (CW) CW is stopped by next TRIG rise edge or SPI access
TLP_DLx[12:0] (x=0~7)	/channel	Chx Tx delay from TRIG fall edge : $32*T_{CLK} + T_{CLK}*TLP\_DLx$, (TLP_DLx = 0~8191)
INVx	/channel	Polarity inversion of generating DAC/3LP Tx waveform pattern (0:Normal, 1: Inversion)
TRSW_WAITx[2:0]	/channel	clamp (TRSW-On wait) time after transmission "000"=0,"001"=80*T_{CLK}, "010"=120*T_{CLK}, "011"=160*T_{CLK}, "100"=200*T_{CLK}, "101"=240*Tclk, "110"=280*T_{CLK}, "111"=320*T_{CLK}

Note: Register parameter hatched by brown color is latched to F/F with TRIG rise edge.

■ Control Register Map (1)

Function	REG.#	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Default	W/R
Common setting	0	PDSEL[1:0]		OUTIFSEL[1:0]		USE_EXTSIG	PWRSAVE	DAC_RPTSEL	TLP_RPTSEL	00000000	W/R
Active ch selection	1	DACTXCH0	DACTXCH1	DACTXCH2	DACTXCH3	DACTXCH4	DACTXCH5	DACTXCH6	DACTXCH7	00000000	W/R
	2	TLPTXCH0	TLPTXCH1	TLPTXCH2	TLPTXCH3	TLPTXCH4	TLPTXCH5	TLPTXCH6	TLPTXCH7	00000000	W/R
	3	RXCH0	RXCH1	RXCH2	RXCH3	RXCH4	RXCH5	RXCH6	RXCH7	00000000	W/R
Reserved	4	RESERVEDC[15:8]								00000000	W/R
	5	RESERVEDC[7:0]								00000000	W/R
DRVSEL#A Setting	6	WAITA[7:0]								00000000	W/R
	7	WIDTHA[15:8]								00000000	W/R
	8	WIDTHA[7:0]								00000000	W/R
DRVSEL#B Setting	9	WAITB[7:0]								00000000	W/R
	10	WIDTHB[15:8]								00000000	W/R
	11	WIDTHB[7:0]								00000000	W/R

Note: Register parameter hatched by brown is re-latched into F/F with TRIG rise edge.

■ Control Register Map (2)

Function	REG.#	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Default	W/R
Ch#0 DAC Setting	12	DAC_START0[11:4]								00000000	W/R
	13	DAC_START0[3:0]				DAC_STOP0[11:8]				00000000	W/R
	14	DAC_STOP0[7:0]								00000000	W/R
	15	DAC_REPEAT0[7:0]								00000000	W/R
	16	DAC_DL0[12:5]								00000000	W/R
	17	DAC_DL0[4:0]					ICSEL0[2:0]			00000000	W/R
	18	ACT_GAINADJ0	TRSW_WAIT0[2:0]			RESERVED0[5:4]		GAIN0[9:8]		00000000	W/R
	19	GAIN0[7:0]								00000000	W/R
	20	GAIN_ADJ0[7:0]								00000000	W/R
	21	ACT_OFSADJ0	OFS_ADJ0[6:0]							00000000	W/R
Ch#0 3LP Data Setting	22	RESERVED0[3]	TLP_START0[6:0]							00000000	W/R
	23	RESERVED0[2]	TLP_STOP0[6:0]							00000000	W/R
	24	TLP_REPEAT0[7:0]								00000000	W/R
	25	TLP_DL0[12:5]								00000000	W/R
	26	TLP_DL0[4:0]					RESERVED0[1:0]		INV0	00000000	W/R
Ch#1 DAC Setting	27	DAC_START1[11:4]								00000000	W/R
	28	DAC_START1[3:0]				DAC_STOP1[11:8]				00000000	W/R
	29	DAC_STOP1[7:0]								00000000	W/R
	30	DAC_REPEAT1[7:0]								00000000	W/R
	31	DAC_DL1[12:5]								00000000	W/R
	32	DAC_DL1[4:0]					ICSEL1[2:0]			00000000	W/R
	33	ACT_GAINADJ1	TRSW_WAIT1[2:0]			RESERVED1[5:4]		GAIN1[9:8]		00000000	W/R
	34	GAIN1[7:0]								00000000	W/R
	35	GAIN_ADJ1[7:0]								00000000	W/R
	36	ACT_OFSADJ1	OFS_ADJ1[6:0]							00000000	W/R
Ch#1 3LP Data Setting	37	RESERVED1[3]	TLP_START1[6:0]							00000000	W/R
	38	RESERVED1[2]	TLP_STOP1[6:0]							00000000	W/R
	39	TLP_REPEAT1[7:0]								00000000	W/R
	40	TLP_DL1[12:5]								00000000	W/R
	41	TLP_DL1[4:0]					RESERVED1[1:0]		INV1	00000000	W/R

Note: Register parameter hatched by brown is re-latched into F/F with TRIG rise edge.

■ Control Register Map (3)

Function	REG.#	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Default	W/R
Ch#2 DAC Setting	42	DAC_START2[11:4]								00000000	W/R
	43	DAC_START2[3:0]				DAC_STOP2[11:8]				00000000	W/R
	44	DAC_STOP2[7:0]								00000000	W/R
	45	DAC_REPEAT2[7:0]								00000000	W/R
	46	DAC_DL2[12:5]								00000000	W/R
	47	DAC_DL2[4:0]					ICSEL2[2:0]			00000000	W/R
	48	ACT_GAINADJ2	TRSW_WAIT2[2:0]			RESERVED2[5:4]		GAIN2[9:8]		00000000	W/R
	49	GAIN2[7:0]								00000000	W/R
	50	GAIN_ADJ2[7:0]								00000000	W/R
	51	ACT_OFSADJ2	OFS_ADJ2[6:0]							00000000	W/R
Ch#2 3LP Data Setting	52	RESERVED2[3]	TLP_START2[6:0]							00000000	W/R
	53	RESERVED2[2]	TLP_STOP2[6:0]							00000000	W/R
	54	TLP_REPEAT2[7:0]								00000000	W/R
	55	TLP_DL2[12:5]								00000000	W/R
	56	TLP_DL2[4:0]					RESERVED2[1:0]		INV2	00000000	W/R
Ch#3 DAC Setting	57	DAC_START3[11:4]								00000000	W/R
	58	DAC_START3[3:0]				DAC_STOP3[11:8]				00000000	W/R
	59	DAC_STOP3[7:0]								00000000	W/R
	60	DAC_REPEAT3[7:0]								00000000	W/R
	61	DAC_DL3[12:5]								00000000	W/R
	62	DAC_DL3[4:0]					ICSEL3[2:0]			00000000	W/R
	63	ACT_GAINADJ3	TRSW_WAIT3[2:0]			RESERVED3[5:4]		GAIN3[9:8]		00000000	W/R
	64	GAIN3[7:0]								00000000	W/R
	65	GAIN_ADJ3[7:0]								00000000	W/R
	66	ACT_OFSADJ3	OFS_ADJ3[6:0]							00000000	W/R
Ch#3 3LP Data Setting	67	RESERVED3[3]	TLP_START3[6:0]							00000000	W/R
	68	RESERVED3[2]	TLP_STOP3[6:0]							00000000	W/R
	69	TLP_REPEAT3[7:0]								00000000	W/R
	70	TLP_DL3[12:5]								00000000	W/R
	71	TLP_DL3[4:0]					RESERVED3[1:0]		INV3	00000000	W/R

Note: Register parameter hatched by brown is re-latched into F/F with TRIG rise edge.

■ Control Register Map (4)

Function	REG.#	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Default	W/R
Ch#4 DAC Setting	72	DAC_START4[11:4]								00000000	W/R
	73	DAC_START4[3:0]				DAC_STOP4[11:8]				00000000	W/R
	74	DAC_STOP4[7:0]								00000000	W/R
	75	DAC_REPEAT4[7:0]								00000000	W/R
	76	DAC_DL4[12:5]								00000000	W/R
	77	DAC_DL4[4:0]					ICSEL4[2:0]			00000000	W/R
	78	ACT_GAINADJ4	TRSW_WAIT4[2:0]			RESERVED4[5:4]		GAIN4[9:8]		00000000	W/R
	79	GAIN4[7:0]								00000000	W/R
	80	GAIN_ADJ4[7:0]								00000000	W/R
	81	ACT_OFSADJ4	OFS_ADJ4[6:0]							00000000	W/R
Ch#4 3LP Data Setting	82	RESERVED4[3]	TLP_START4[6:0]							00000000	W/R
	83	RESERVED4[2]	TLP_STOP4[6:0]							00000000	W/R
	84	TLP_REPEAT4[7:0]								00000000	W/R
	85	TLP_DL4[12:5]								00000000	W/R
	86	TLP_DL4[4:0]					RESERVED4[1:0]		INV4	00000000	W/R
Ch#5 DAC Setting	87	DAC_START5[11:4]								00000000	W/R
	88	DAC_START5[3:0]				DAC_STOP5[11:8]				00000000	W/R
	89	DAC_STOP5[7:0]								00000000	W/R
	90	DAC_REPEAT5[7:0]								00000000	W/R
	91	DAC_DL5[12:5]								00000000	W/R
	92	DAC_DL5[4:0]					ICSEL5[2:0]			00000000	W/R
	93	ACT_GAINADJ5	TRSW_WAIT5[2:0]			RESERVED5[5:4]		GAIN5[9:8]		00000000	W/R
	94	GAIN5[7:0]								00000000	W/R
	95	GAIN_ADJ5[7:0]								00000000	W/R
	96	ACT_OFSADJ5	OFS_ADJ5[6:0]							00000000	W/R
Ch#5 3LP Data Setting	97	RESERVED5[3]	TLP_START5[6:0]							00000000	W/R
	98	RESERVED5[2]	TLP_STOP5[6:0]							00000000	W/R
	99	TLP_REPEAT5[7:0]								00000000	W/R
	100	TLP_DL5[12:5]								00000000	W/R
	101	TLP_DL5[4:0]					RESERVED5[1:0]		INV5	00000000	W/R

Note: Register parameter hatched by brown is re-latched into F/F with TRIG rise edge.

■ Control Register Map (5)

Function	REG.#	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Default	W/R
Ch#6 DAC Setting	102	DAC_START6[11:4]								00000000	W/R
	103	DAC_START6[3:0]				DAC_STOP6[11:8]				00000000	W/R
	104	DAC_STOP6[7:0]								00000000	W/R
	105	DAC_REPEAT6[7:0]								00000000	W/R
	106	DAC_DL6[12:5]								00000000	W/R
	107	DAC_DL6[4:0]					ICSEL6[2:0]			00000000	W/R
	108	ACT_GAINADJ6	TRSW_WAIT6[2:0]			RESERVED6[5:4]		GAIN6[9:8]		00000000	W/R
	109	GAIN6[7:0]								00000000	W/R
	110	GAIN_ADJ6[7:0]								00000000	W/R
	111	ACT_OFSADJ6	OFS_ADJ6[6:0]							00000000	W/R
Ch#6 3LP Data Setting	112	RESERVED6[3]	TLP_START6[6:0]							00000000	W/R
	113	RESERVED6[2]	TLP_STOP6[6:0]							00000000	W/R
	114	TLP_REPEAT6[7:0]								00000000	W/R
	115	TLP_DL6[12:5]								00000000	W/R
	116	TLP_DL6[4:0]					RESERVED6[1:0]		INV6	00000000	W/R
Ch#7 DAC Setting	117	DAC_START7[11:4]								00000000	W/R
	118	DAC_START7[3:0]				DAC_STOP7[11:8]				00000000	W/R
	119	DAC_STOP7[7:0]								00000000	W/R
	120	DAC_REPEAT7[7:0]								00000000	W/R
	121	DAC_DL7[12:5]								00000000	W/R
	122	DAC_DL7[4:0]					ICSEL7[2:0]			00000000	W/R
	123	ACT_GAINADJ7	TRSW_WAIT7[2:0]			RESERVED7[5:4]		GAIN7[9:8]		00000000	W/R
	124	GAIN7[7:0]								00000000	W/R
	125	GAIN_ADJ7[7:0]								00000000	W/R
	126	ACT_OFSADJ7	OFS_ADJ7[6:0]							00000000	W/R
Ch#7 3LP Data Setting	127	RESERVED7[3]	TLP_START7[6:0]							00000000	W/R
	128	RESERVED7[2]	TLP_STOP7[6:0]							00000000	W/R
	129	TLP_REPEAT7[7:0]								00000000	W/R
	130	TLP_DL7[12:5]								00000000	W/R
	131	TLP_DL7[4:0]					RESERVED7[1:0]		INV7	00000000	W/R

Note: Register parameter hatched by brown is re-latched into F/F with TRIG rise edge.

■ CRC & Error Register function (1)

Register parameter	Function
CRC[7:0]	Transferred 8bit CRC Data in last SPI Write operation CRC initial value = 00000000 CRC polynomial equation is $X^8+X^5+X^4+1$
CAL_CRC[7:0]	Calculated CRC values with transferred SDATA in last SPI Write operation
ERROR[47:40]	Memory address error for ch#x (x=0~7) 3LP data. (Start and Stop address is same when “TRIG” becomes high.) If Error has occurred in ch(x), Register bit ERROR[8x+40] is set to “1” and “FAULT” pin becomes to “0” until ERROR[8x+40] is cleared. Error[8x+40] is cleared with “EN” fall edge or setting Memory address for ch#x 3LP data properly.
ERROR[39:32]	Memory address error for ch#x (x=0~7) DAC. (Start and Stop address is same when “TRIG” becomes high.) If Error has occurred in ch(x), Register bit ERROR[8x+32] is set to “1” and “FAULT” pin becomes to “0” until ERROR[8x+32] is cleared. Error[8x+32] is cleared with “EN” fall edge or setting Memory address for ch#x DAC properly.
ERROR[31:24]	SPI transfer error (CRC un-match) has occurred during Write to memory for ch#x (x=0~7) 3LP data. If Error has occurred in ch(x), Register bit ERROR[8x+24] is set to “1” and “FAULT” pin becomes to “0” until ERROR[8x+24] is cleared. Error[8x+24] is cleared when the DATA for ch#x 3LP is transferred to memory normally.
ERROR[23:16]	SPI transfer error (CRC un-match) has occurred during Write to memory for ch#x (x=0~7) DAC data. If Error has occurred in ch(x), Register bit ERROR[8x+16] is set to “1” and “FAULT” pin becomes to “0” until ERROR[8x+16] is cleared. Error[8x+16] is cleared when the DATA for ch#x DAC is transferred to memory normally.
ERROR[15:8]	SPI transfer error (CRC un-match) has occurred during Write to Register on ch#x (x=0~7). If Error has occurred in ch(x), Register bit ERROR[8x+8] is set to “1” and “FAULT” pin becomes to “0” until ERROR[8x+8] is cleared. Error[8x+8] is cleared with “EN” fall edge or re-transferring the data to ch#x Register normally.

■ CRC & Error Register function (2)

Register parameter	Function
ERROR[7]	SPI transfer error (CRC un-match) has occurred during Write to Register#0~#11. If Error has occurred, Register bit ERROR[7] is set to “1” and “FAULT” pin becomes to “0” until ERROR[7] is cleared. Error[7] is cleared with “EN” fall edge or re-transferring the data to Register#0~#6 normally.
ERROR[6]	TRIG “hi” has occurred during SPI operation. If Error has occurred, Register bit ERROR[6] is set to “1” until it is cleared. Error[6] is cleared with “EN” fall edge.
ERROR[5]	Access to ch#x (x=0~7) 3LP memory has occurred during ch#x (x=0~7) 3LP Tx data is output. If Error has occurred, Register bit ERROR[5] is set to “1” until cleared. Error[5] is cleared with “EN” fall edge.
ERROR[4]	Access to ch#x (x=0~7) DAC memory has occurred during ch#x (x=0~7) DAC Tx operation. If Error has occurred, Register bit ERROR[4] is set to “1” until cleared. Error[4] is cleared with “EN” fall edge.
ERROR[3]	Ch#x (x=4~7) 3LP Tx data is output during “1” state of DRVSELB or transition period (640 clock cycle) from rise/fall edge. If Error has occurred, Register bit ERROR[3] is set to “1” and “FAULT” pin becomes to “0” until ERROR[3] is cleared. Error[3] is cleared with “EN” fall edge.
ERROR[2]	Ch#x (x=0~3) 3LP Tx data is output during “1” state of DRVSELA or transition period (640 clock cycle) from rise/fall edge. If Error has occurred, Register bit ERROR[2] is set to “1” and “FAULT” pin becomes to “0” until ERROR[2] is cleared. Error[2] is cleared with “EN” fall edge.
ERROR[1]	Ch#x (x=4~7) DAC Tx data is output during “0” state of DRVSELB or transition period (640 clock cycle) from rise/fall edge. If Error has occurred, Register bit ERROR[1] is set to “1” and “FAULT” pin becomes to “0” until ERROR[1] is cleared. Error[1] is cleared with “EN” fall edge.
ERROR[0]	Ch#x (x=0~3) DAC Tx data is output during “0” state of DRVSELA or transition period (640 clock cycle) from rise/fall edge. If Error has occurred, Register bit ERROR[0] is set to “1” and “FAULT” pin becomes to “0” until ERROR[0] is cleared. Error[0] is cleared with “EN” fall edge.

■ CRC & Error Register MAP

Function	REG.#	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Default	W/R
CRC Code	C0	CRC[7:0]								00000000	W/R
	C1	CAL_CRC[7:0]								00000000	R
Error Code	E0	ERROR[47]	ERROR[46]	ERROR[45]	ERROR[44]	ERROR[43]	ERROR[42]	ERROR[41]	ERROR[40]	00000000	R
	E1	ERROR[39]	ERROR[38]	ERROR[37]	ERROR[36]	ERROR[35]	ERROR[34]	ERROR[33]	ERROR[32]	00000000	R
	E2	ERROR[31]	ERROR[30]	ERROR[29]	ERROR[28]	ERROR[27]	ERROR[26]	ERROR[25]	ERROR[24]	00000000	R
	E3	ERROR[23]	ERROR[22]	ERROR[21]	ERROR[20]	ERROR[19]	ERROR[18]	ERROR[17]	ERROR[16]	00000000	R
	E4	ERROR[15]	ERROR[14]	ERROR[13]	ERROR[12]	ERROR[11]	ERROR[10]	ERROR[9]	ERROR[8]	00000000	R

■ Truth Table

IC status	EN	CS			TRIG	Internal Tx-PT(x)	Driver Select	Control Register				Ch(x) DAC MEM. Readout code	Ch(x) TLP MEM. Readout code		Control Register		Ch(x) DAC digital input CHxDAC[11:0]	DAC Ic Bias On/Off	DRVSELy (y=A for ch0~3, y=B for ch4~7), Ch(x) (x=0~7) TLP DATA & DAC current			
mode		to Ch(x) DAC MEM.	to Ch(x) TLP MEM.	to control REG.				DACTX CHx	TLPTX CHx	PWR SAVE	RXCHx	CHxDATA (dec)	CHxCODE[1:0]		INVx	GAINx[5:0]	CHxDAC (*1) (dec)	BIASONx	DRVSELy	PINx	NINx	CHx DAC IOP-ION
Rx	0	0			0	none	*	0	0	0	0	none	none	none	*	*	none	1	0	0	0	0(bias-on)
	0	0			0	none	*	0	0	0	1	none	none	none	*	*	none	1	0	1	1	0(bias-on)
	0	0			0	none	*	0	0	1	0	none	none	none	*	*	none	0	0	0	0	0(bias-off)
	0	0			0	none	*	0	0	1	1	none	none	none	*	*	none	0	0	1	1	0(bias-off)
	0	0			0	none	*	1	*	*	0	none	none	none	*	*	none	1	1	0	0	0(bias-on)
	0	0			0	none	*	1	*	*	1	none	none	none	*	*	none	1	1	1	1	0(bias-on)
TLP Tx	0	0			0	Gen.	0(TLP)	*	1	*	*	none	0	0	*	*	none	1	0	0	0	0(bias-on)
	0	0			0	Gen.	0(TLP)	*	1	*	*	none	0	1	0	*	none	1	0	1	0	0(bias-on)
	0	0			0	Gen.	0(TLP)	*	1	*	*	none	0	1	1	*	none	1	0	0	1	0(bias-on)
	0	0			0	Gen.	0(TLP)	*	1	*	*	none	1	0	0	*	none	1	0	0	1	0(bias-on)
	0	0			0	Gen.	0(TLP)	*	1	*	*	none	1	0	1	*	none	1	0	1	0	0(bias-on)
	0	0			0	Gen.	0(TLP)	*	1	*	*	none	1	1	*	*	none	1	0	0(N/A)	0(N/A)	0(bias-on)
DAC Tx	0	0			0	Gen.	1(DAC)	1	*	*	*	CHxDATA	none	none	0	GAINx	(GAINx+1)/64*CHxDATA	1	1	0	0	2*Ic*CHxDAC
	0	0			0	Gen.	1(DAC)	1	*	*	*	CHxDATA	none	none	1	GAINx	-1*(GAINx+1)/64*CHxDATA	1	1	0	0	2*Ic*CHxDAC
TRIG_ Reset	0	0			1	none	*	0	0	0	0	none	none	none	*	*	none	1	0	0	0	0(bias-on)
	0	0			1	none	*	0	0	0	1	none	none	none	*	*	none	1	0	1	1	0(bias-on)
	0	0			1	none	*	0	0	1	0	none	none	none	*	*	none	0	0	0	0	0(bias-off)
	0	0			1	none	*	0	0	1	1	none	none	none	*	*	none	0	0	1	1	0(bias-off)
	0	0			1	none	*	1	*	*	0	none	none	none	*	*	none	1	1	0	0	0(bias-on)
	0	0			1	none	*	1	*	*	1	none	none	none	*	*	none	1	1	1	1	0(bias-on)
REG Access during Rx	0	-	-	1	0	none	*	0	0	0	0	none	none	none	*	*	none	1	0	0	0	0(bias-on)
	0	-	-	1	0	none	*	0	0	0	1	none	none	none	*	*	none	1	0	1	1	0(bias-on)
	0	-	-	1	0	none	*	0	0	1	0	none	none	none	*	*	none	0	0	0	0	0(bias-off)
	0	-	-	1	0	none	*	0	0	1	1	none	none	none	*	*	none	0	0	1	1	0(bias-off)
	0	-	-	1	0	none	*	1	*	*	0	none	none	none	*	*	none	1	1	0	0	0(bias-on)
	0	-	-	1	0	none	*	1	*	*	1	none	none	none	*	*	none	1	1	1	1	0(bias-on)
REG Access during TLP Tx	0	-	-	1	0	Gen.	0(TLP)	*	1	*	*	none	0	0	*	*	none	1	0	0	0	0(bias-on)
	0	-	-	1	0	Gen.	0(TLP)	*	1	*	*	none	0	1	0	*	none	1	0	1	0	0(bias-on)
	0	-	-	1	0	Gen.	0(TLP)	*	1	*	*	none	0	1	1	*	none	1	0	0	1	0(bias-on)
	0	-	-	1	0	Gen.	0(TLP)	*	1	*	*	none	1	0	0	*	none	1	0	0	1	0(bias-on)
	0	-	-	1	0	Gen.	0(TLP)	*	1	*	*	none	1	0	1	*	none	1	0	1	0	0(bias-on)
	0	-	-	1	0	Gen.	0(TLP)	*	1	*	*	none	1	1	*	*	none	1	0	0(N/A)	0(N/A)	0(bias-on)
REG Access during DAC TX (*2)	0	-	-	1	0	Gen.	1(DAC)	1	*	*	*	CHxDATA	none	none	0	GAINx	(GAINx+1)/64*CHxDATA	1	1	0	0	2*Ic*CHxDAC
	0	-	-	1	0	Gen.	1(DAC)	1	*	*	*	CHxDATA	none	none	1	GAINx	-1*(GAINx+1)/64*CHxDATA	1	1	0	0	2*Ic*CHxDAC

***1: The decimal point is suppressed.**

***2: If ICSELx[2:0] and GAINADJx[7:0] are changed during ch(x) DAC opearting, ch(x) DAC output current will be varied.**

■ Truth Table (continuation)

IC status	EN	CS			TRIG	Internal Tx-PT(x)	Driver Select	Control Register				Ch(x) DAC MEM. Readout code	Ch(x) TLP MEM. Readout code		Control Register		Ch(x) DAC digital input CHxDAC[11:0]	DAC Ic Bias On/Off	DRVSELy (y=A for ch0~3, y=B for ch4~7), Ch(x) (x=0~7) TLP DATA & DAC current			
mode		to Ch(x) DAC MEM.	to Ch(x) TLP MEM.	to control REG.				DACTX CHx	TLPTX CHx	PWR SAVE	RXCHx	CHxDATA (dec)	CHxCODE[1:0]		INVx	GAINx[5:0]	CHxDAC (*1) (dec)	BIASONx	DRVSELy	PINx	NINx	CHx DAC IOP-ION
Ch(x) TLP MEM Access during Rx	0	-	1	-	0	none	*	0	0	0	0	none	none	none	*	*	none	1	0	0	0	0(bias-on)
	0	-	1	-	0	none	*	0	0	0	1	none	none	none	*	*	none	1	0	1	1	0(bias-on)
	0	-	1	-	0	none	*	0	0	1	0	none	none	none	*	*	none	0	0	0	0	0(bias-off)
	0	-	1	-	0	none	*	0	0	1	1	none	none	none	*	*	none	0	0	1	1	0(bias-off)
	0	-	1	-	0	none	*	1	*	*	0	none	none	none	*	*	none	1	1	0	0	0(bias-on)
	0	-	1	-	0	none	*	1	*	*	1	none	none	none	*	*	none	1	1	1	1	0(bias-on)
Ch(x) TLP MEM. Access during TLP Tx	0	-	1	-	0	Gen.	0(TLP)	*	1	*	*	none	*	*	*	*	none	1	Error condition (ERROR[5]=1) N/A			
Ch(x) TLP MEM. Access during DAC Tx	0	-	1	-	0	Gen.	1(DAC)	1	*	*	*	CHxDATA	none	none	0	GAINx	(GAINx+1)/64*CHxDATA	1	1	0	0	2*Ic*CHxDAC
	0	-	1	-	0	Gen.	1(DAC)	1	*	*	*	CHxDATA	none	none	1	GAINx	-1*(GAINx+1)/64*CHxDATA	1	1	0	0	2*Ic*CHxDAC
Ch(x) DAC MEM. Access during Rx	0	1	-	-	0	none	*	0	0	0	0	none	none	none	*	*	none	1	0	0	0	0(bias-on)
	0	1	-	-	0	none	*	0	0	0	1	none	none	none	*	*	none	1	0	1	1	0(bias-on)
	0	1	-	-	0	none	*	0	0	1	0	none	none	none	*	*	none	0	0	0	0	0(bias-off)
	0	1	-	-	0	none	*	0	0	1	1	none	none	none	*	*	none	0	0	1	1	0(bias-off)
	0	1	-	-	0	none	*	1	*	*	0	none	none	none	*	*	none	1	1	0	0	0(bias-on)
	0	1	-	-	0	none	*	1	*	*	1	none	none	none	*	*	none	1	1	1	1	0(bias-on)
Ch(x) DAC MEM. Access during TLP Tx	0	1	-	-	0	Gen.	0(TLP)	*	1	*	*	none	0	0	*	*	none	1	0	0	0	0(bias-on)
	0	1	-	-	0	Gen.	0(TLP)	*	1	*	*	none	0	1	0	*	none	1	0	1	0	0(bias-on)
	0	1	-	-	0	Gen.	0(TLP)	*	1	*	*	none	0	1	1	*	none	1	0	0	1	0(bias-on)
	0	1	-	-	0	Gen.	0(TLP)	*	1	*	*	none	1	0	0	*	none	1	0	0	1	0(bias-on)
	0	1	-	-	0	Gen.	0(TLP)	*	1	*	*	none	1	0	1	*	none	1	0	1	0	0(bias-on)
	0	1	-	-	0	Gen.	0(TLP)	*	1	*	*	none	1	1	*	*	none	1	0	0(N/A)	0(N/A)	0(bias-on)
Ch(x) DAC MEM. Access during DAC Tx	0	1	-	-	0	Gen.	1(DAC)	1	*	*	*	none	*	*	*	*	none	1	Error condition (ERROR[4]=1) N/A			
TRIG rise during CS=Hi	0	1			1	*	*	*	*	*	*	none	*	*	*	*	none	*	Error condition (ERROR[6]=1) N/A			
IC disabled	1	0			*	none	*	*	*	*	*	none	*	*	*	*	none	0	0	0	0	0(bias-off)
SPI access during IC disabled	1	-	-	1	*	none	*	*	*	*	*	none	*	*	*	*	none	0	0	0	0	0(bias-off)
	1	-	1	-	*	none	*	*	*	*	*	none	*	*	*	*	none	0	0	0	0	0(bias-off)
	1	1	-	-	*	none	*	*	*	*	*	none	*	*	*	*	none	0	0	0	0	0(bias-off)

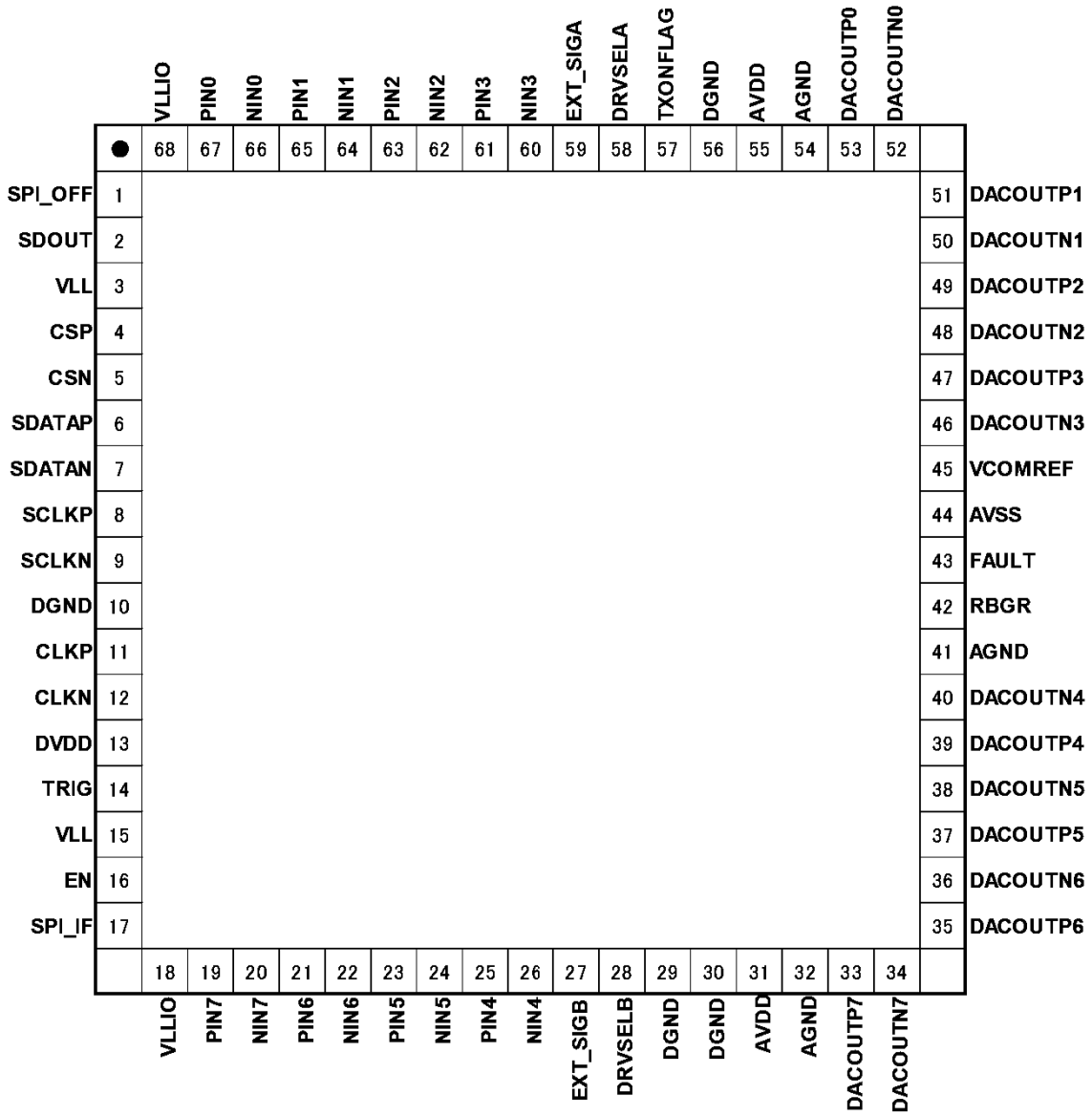
***1: The decimal point is suppressed.**

***2: If ICSELx[2:0] and GAINADJx[7:0] are changed during ch(x) DAC opearting, ch(x) DAC output current will be varied.**

■ PIN Descriptions

Pin#	Pin Name	Function	Pin#	Pin Name	Function
1	SPI_OFF	Control of SPI On/Off (H:Power-off,L:Power-on(50kΩ pull-down))	35	$DAC_{OUTP}6$	CH6 DAC differential outputs
2	SDOUT	SPI serial output data (tri-state output)	36	$DAC_{OUTN}6$	
3	VLL	Positive low voltage power supply for Logic (+1.8V)	37	$DAC_{OUTP}5$	CH5 DAC differential outputs
4	CSP	Positive LVDS chip select (CS) input	38	$DAC_{OUTN}5$	
5	CSN	Negative LVDS chip select (CS) input	39	$DAC_{OUTP}4$	CH4 DAC differential outputs
6	SDATAP	Positive LVDS Serial Data input	40	$DAC_{OUTN}4$	
7	SDATAN	Negative LVDS Serial Data input	41	AGND	Reserved for Testing (Connected to GND)
8	SCLKP	Positive LVDS serial clock input (up to 100MHz)	42	RBGR	Output for Constant Reference Current (Connect 24kΩ to GND)
9	SCLKN	Negative LVDS serial clock input (up to 100MHz)	43	FAULT	Fault output flag, Open N-MOS Drain (H:Normal, L:Fault)
10	DGND	GND for Digital Power Supplies	44	AVSS	Negative Analog Power Supply for DAC (-2~0V)
11	CLKP	Positive LVDS clock input (up to 200MHz)	45	VCOMREF	Output common voltage reference
12	CLKN	Negative LVDS clock Input (up to 200MHz)	46	$DAC_{OUTN}3$	CH3 DAC differential outputs
13	DVDD	Positive Digital Power Supply for LVDS Receiver (+3.3V)	47	$DAC_{OUTP}3$	
14	TRIG	Trigger signal for operation (CMOS)	48	$DAC_{OUTN}2$	CH2 DAC differential outputs
15	VLL	Positive low voltage power supply for Logic (+1.8V)	49	$DAC_{OUTP}2$	
16	EN	IC Disable/Enable control (H: Disable (50kΩ pull-up), L:Enable)	50	$DAC_{OUTN}1$	CH1 DAC differential outputs
17	SPI_IF	I/F selection for SPI (H:Single CMOS, L:LVDS(default))	51	$DAC_{OUTP}1$	
18	VLLIO	Positive low voltage power supply for Logic I/F (+1.8 ~ 3.3V)	52	$DAC_{OUTN}0$	CH0 DAC differential outputs
19	$P_{IN}7$	2bit Tx data for ch7 3LP	53	$DAC_{OUTP}0$	
20	$N_{IN}7$		54	AGND	GND for Analog Power Supplies
21	$P_{IN}6$	2bit Tx data for ch6 3LP	55	AVDD	Positive Analog Power Supply for DAC (+3.3V)
22	$N_{IN}6$		56	DGND	GND for Digital Power Supplies
23	$P_{IN}5$	2bit Tx data for ch5 3LP	57	TXONFLAG	Tx DATA output flag, Open N-MOS Drain (L:Outputting Tx DATA)
24	$N_{IN}5$		58	DRVSELA	Driver select signal for ch0~3
25	$P_{IN}4$	2bit Tx data for ch4 3LP	59	EXT_SIGA	External driver select input for ch0~3
26	$N_{IN}4$		60	$N_{IN}3$	2bit Tx data for ch3 TLP
27	EXT_SIGB	External driver select input for ch4~7	61	$P_{IN}3$	
28	DRVSELB	Driver select signal for ch4~7	62	$N_{IN}2$	2bit Tx data for ch2 TLP
29	DGND	Reserved for Testing (Connected to GND)	63	$P_{IN}2$	
30	DGND	GND for Digital Power Supplies	64	$N_{IN}1$	2bit Tx data for ch1 TLP
31	AVDD	Positive Analog Power Supply for DAC (+3.3V)	65	$P_{IN}1$	
32	AGND	GND for Analog Power Supplies	66	$N_{IN}0$	2bit Tx data for ch0 TLP
33	$DAC_{OUTP}7$	CH7 DAC differential outputs	67	$P_{IN}0$	
34	$DAC_{OUTN}7$		68	VLLIO	Positive low voltage power supply for Logic I/F (+1.8 ~ 3.3V)

■ PIN Configuration



■ Package

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-68(1010)B	QN068-B-P-SD	QN068-B-T-SD	QN068-B-M-SD	QN068-B-L-SD	QN068-B-K-SD

■ Storage, Mounting

1. Storage conditions

1. 1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Figure 1 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

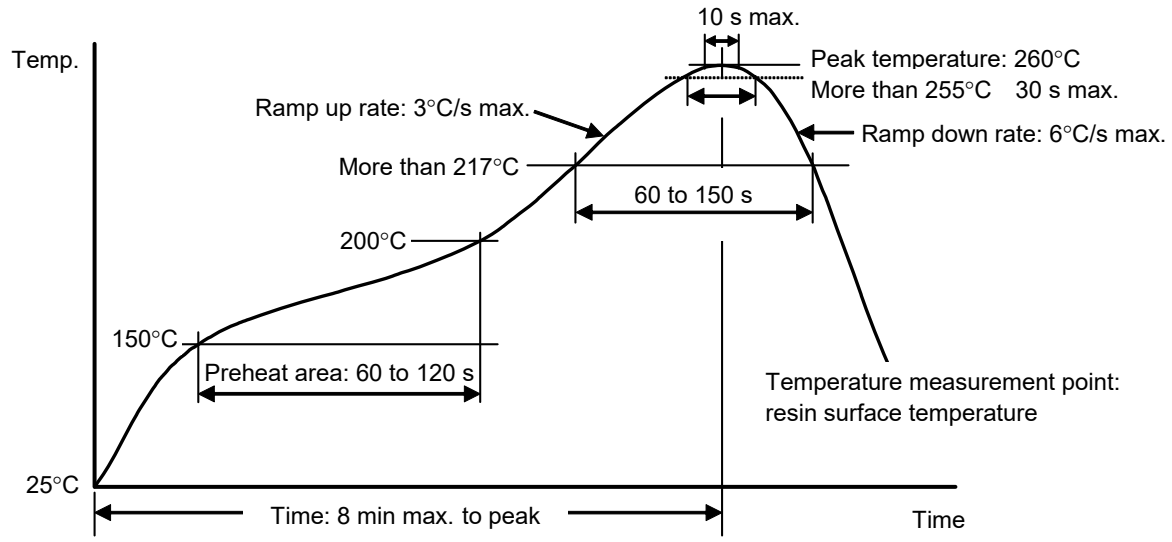


Figure 1 Resistance to Soldering Heat Condition for Package (Reflow Method)

■ Important Notice

1. ABLIC Inc. warrants performance of its hardware products (hereinafter called “products”) to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent ABLIC Inc. needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.

2. Should any claim be made within one month of product delivery about products’ failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before such claim shall not be counted for such response.

3. ABLIC Inc. assumes no obligation or any way of compensation should any fault about customer products and applications using ABLIC Inc. products be found in marketplace. Only in such a case fault of ABLIC Inc. is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.

4. ABLIC Inc. reserves the right to make changes to the Product Specification at any time and to discontinue mass production of the relevant products without notice. Customers are advised before placing orders to confirm that the Product Specification of inquiry is the latest version and that the relevant product is currently on mass production status.

5. In no event shall ABLIC Inc. be liable for any damage that may result from an accident or any other cause during operation of the user’s units according to the Product Specification. ABLIC Inc. assumes no responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in the Product Specification.

6. No license is granted by the Product Specification under any patents or other rights of any third party or ABLIC Inc.

7. The Product Specification may not be reproduced or duplicated, in any form, in whole or in part, without the expressed written permission of ABLIC Inc.

8. Resale of ABLIC Inc. products with statements different from or beyond the parameters described in the Product Specification voids all express and any implied warranties for the products, and is an unfair and deceptive business practice. ABLIC Inc. is not responsible or liable for any such statements.

9. Products (technologies) described in the Product Specification are not to be provided to any party whose purpose in their application will hinder maintenance of international peace and safety nor are they to be applied to that purpose by their direct purchasers or any third party. When exporting those products (technologies), the necessary procedures are to be taken in accordance with related laws and regulations.

■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.

1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1. 4 Prevent friction with other materials made with high polymer.

1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

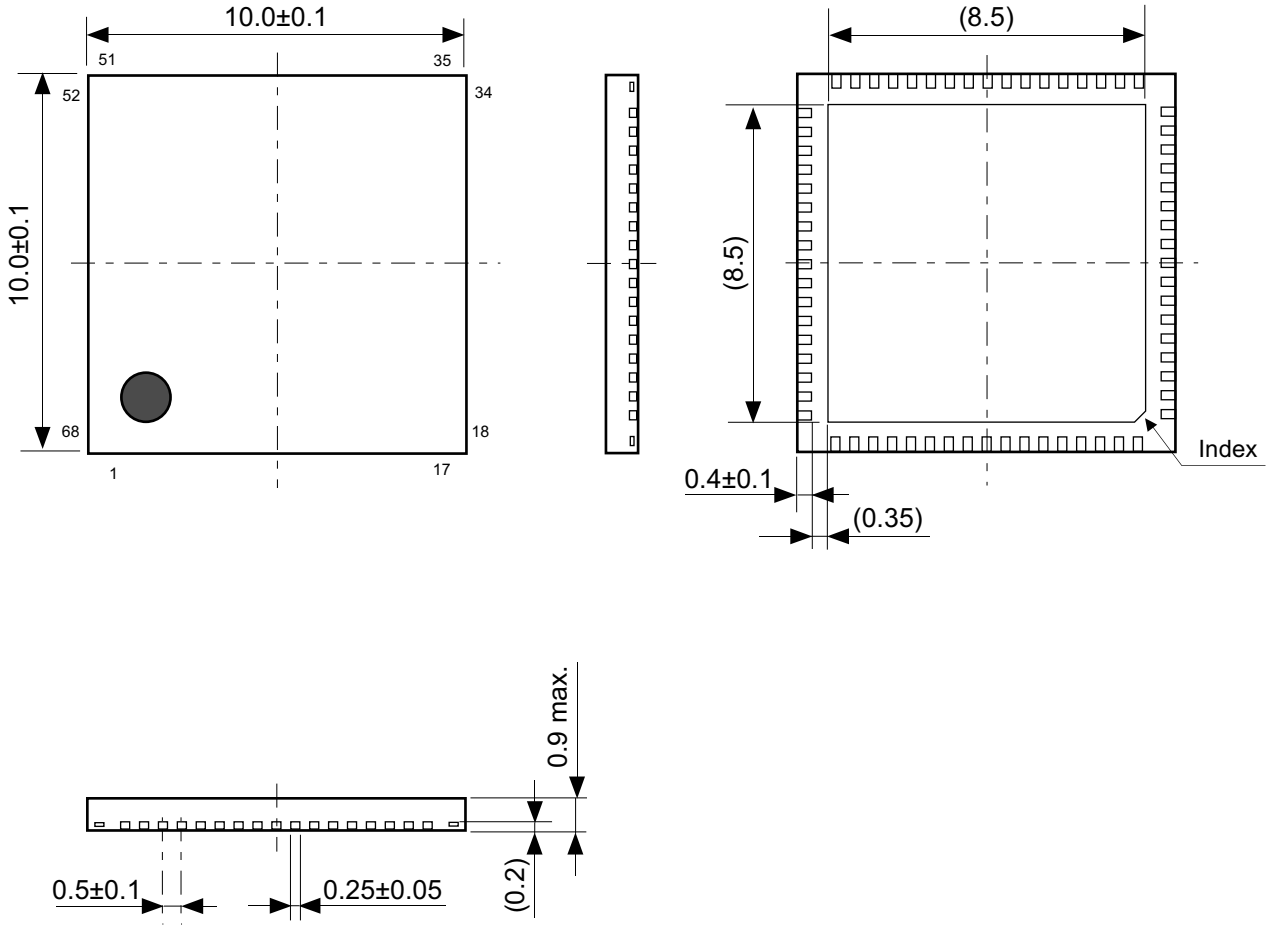
1. 6 Avoid dealing with or storing products in an extremely arid environment.

2. “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

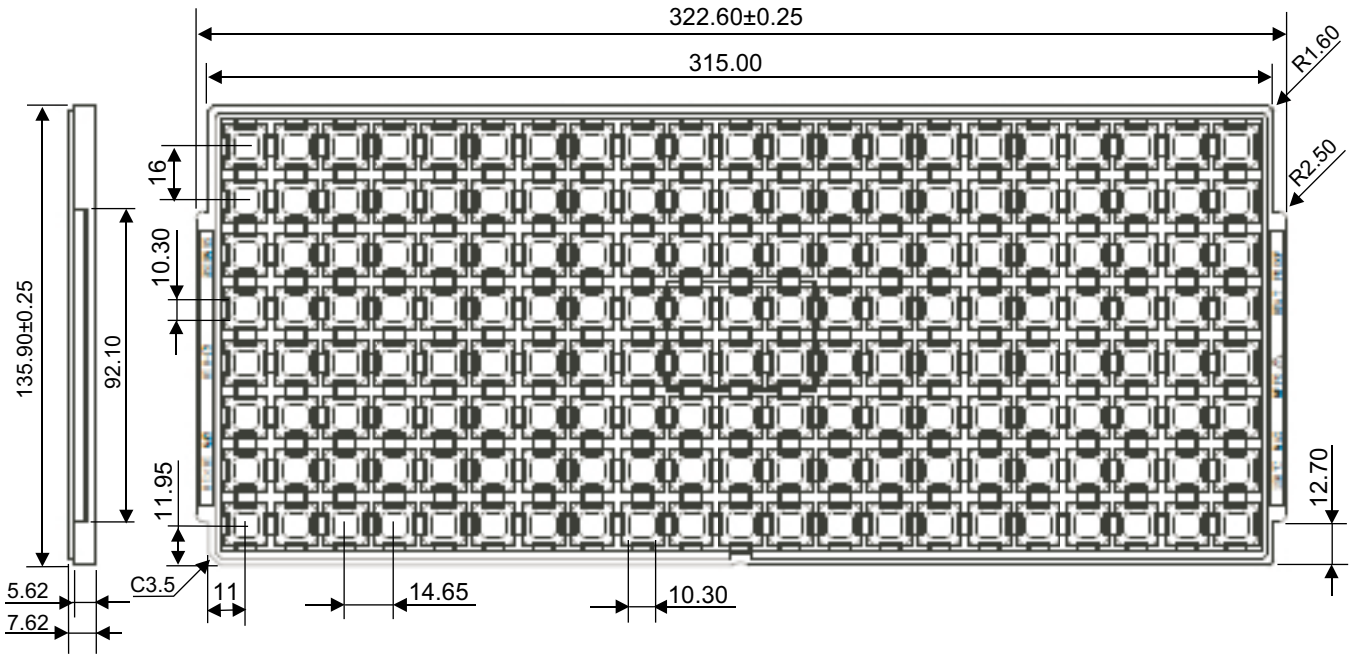
4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

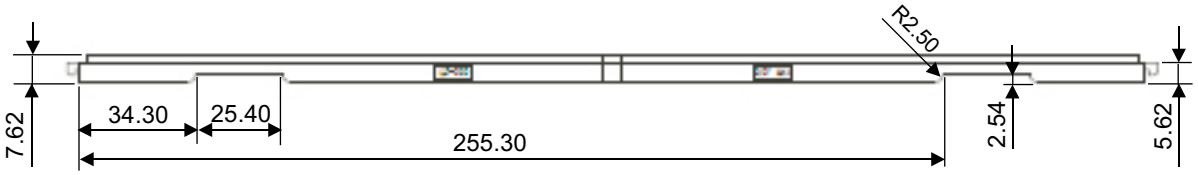
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.



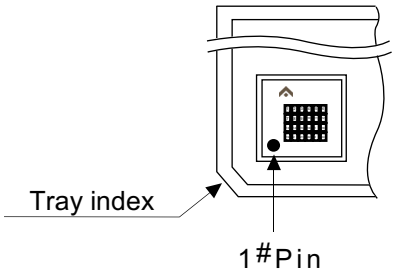
No. QN068-B-P-SD-2.0

TITLE	QFN68-B-PKG Dimensions
No.	QN068-B-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	





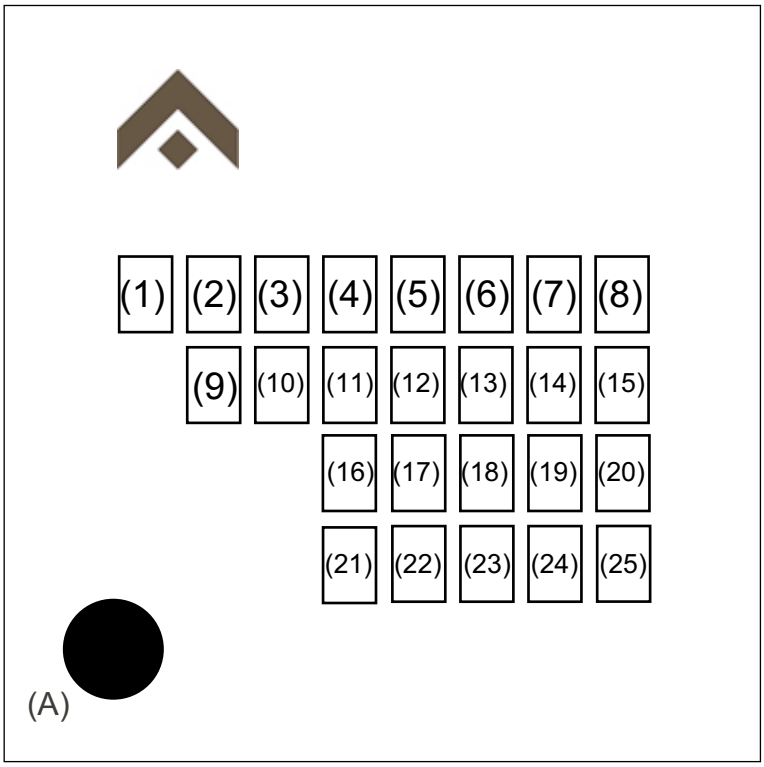
(Direction of IC in tray)



No. QN068-B-T-SD-1.0

TITLE	QFN68-B-Tray		
No.	QN068-B-T-SD-1.0		
ANGLE		QTY.	168
UNIT	mm		

ABLIC Inc.



(1) to (10) : Product code

(11) , (12) : Quality control code

(13) : Year of assembly

(14) : Month of assembly

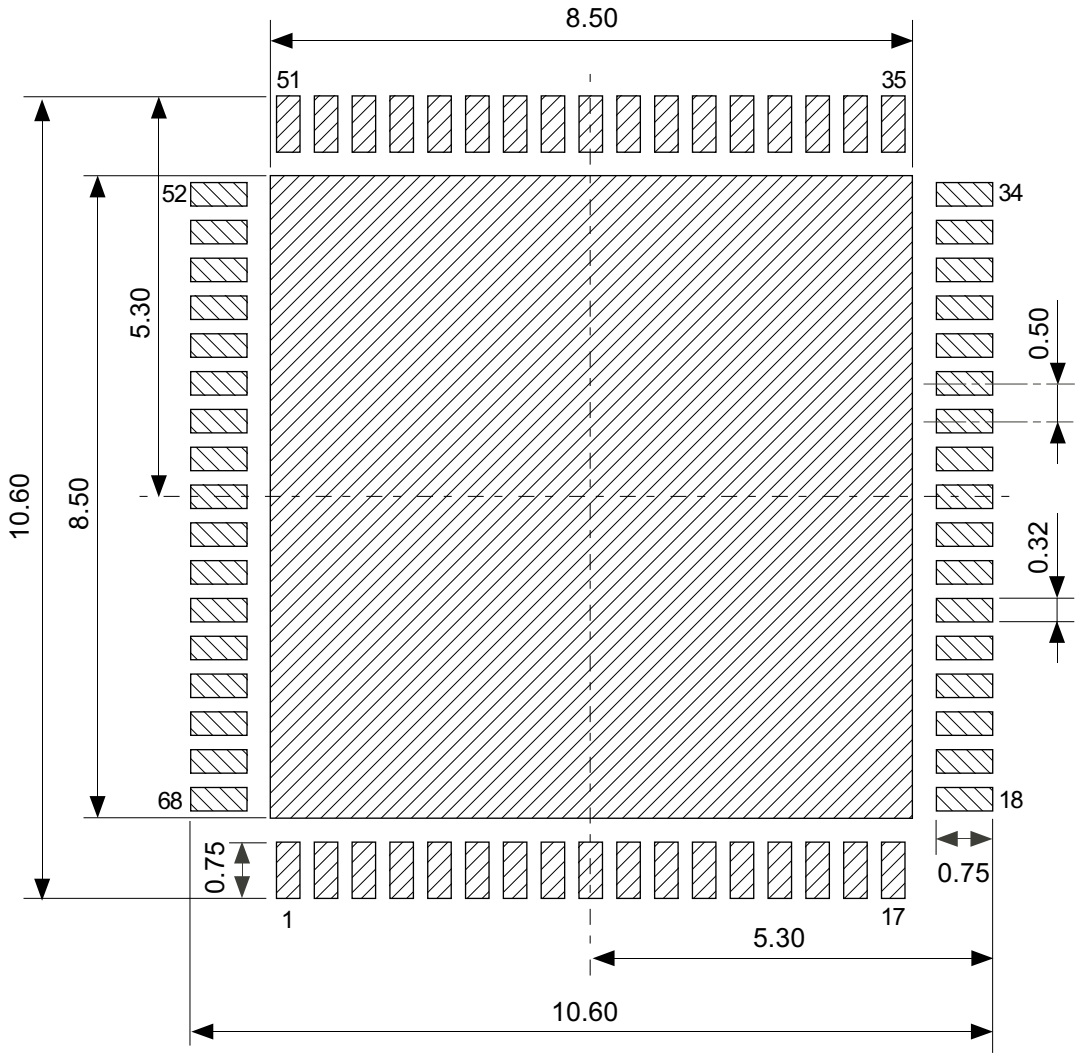
(15) : Week of assembly

(16) to (25) : Quality control code

(A) : 1-pin mark

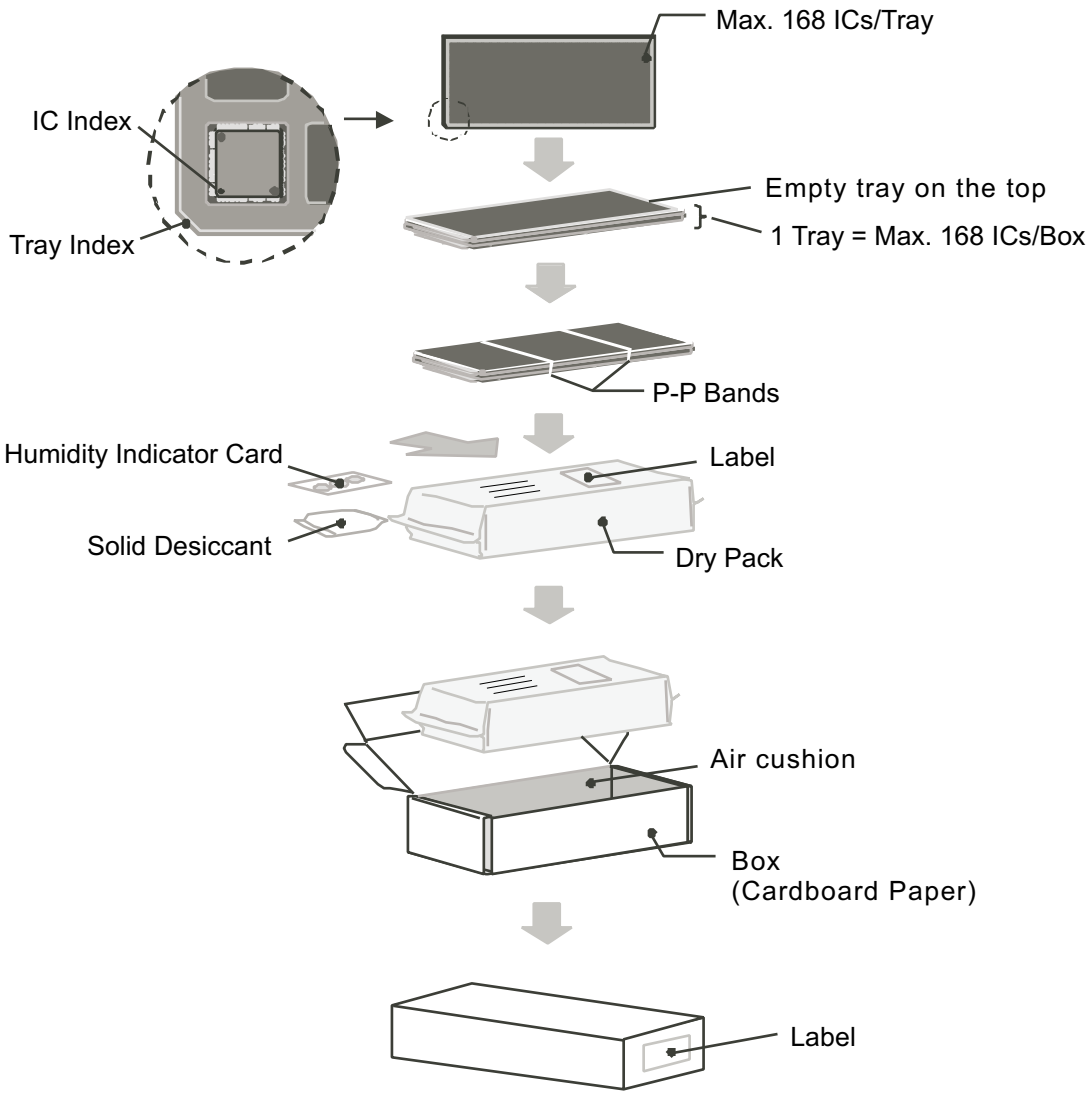
No. QN068-B-M-SD-2.0

TITLE	QFN68-B-Markings		
No.	QN068-B-M-SD-2.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



No. QN068-B-L-SD-2.0

TITLE	QFN68-B -Land Recommendation
No.	QN068-B-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. QN068-B-K-SD-2.0

TITLE	QFN68-B -Packing Procedure
No.	QN068-B-K-SD-2.0
ANGLE	
UNIT	
ABLIC Inc.	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
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14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07