S-82F5B Series

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BATTERY MONITORING IC FOR 3-SERIAL TO 5-SERIAL CELL PACK

This IC includes high-accuracy voltage detection circuits and delay circuits, and can monitor the status of 3-serial to 5-serial cell lithium-ion rechargeable batteries through small 8-pin packages.
Short-circuiting between cells makes it possible for serial connection of 3-cell to 5-cell.

■ Features

- High-accuracy voltage detection circuit for each cell

Overcharge detection voltage n	3.500 V to 4.700 V (5 mV step)	Accuracy ±20 mV (Ta = +25°C)
		Accuracy ±25 mV (Ta = –10°C to +60°C)
Overcharge release voltage n*1	3.100 V to 4.700 V	Accuracy ±50 mV
Overdischarge detection voltage n	1.500 V to 3.200 V (50 mV step)	Accuracy ±80 mV
Overdischarge release voltage n*2	1.500 V to 3.900 V (100 mV step)	Accuracy ±100 mV

- Delay times are generated only by an internal circuit (external capacitors are unnecessary)
  - Overcharge detection delay time: 0.5 s, 1 s, 2 s, 4 s, 6 s, 8 s
  - Overdischarge detection delay time: 128 ms, 256 ms, 0.5 s, 1 s
- CO and DO pin output voltage is limited to 7.5 V max. respectively
- CO pin, DO pin output form: CMOS output, Nch open-drain output
- CO pin, DO pin output logic: Active "H", active "L"
- High-withstand voltage: Absolute maximum rating 28 V
- Wide operation voltage range: 3.6 V to 24 V
- Wide operation temperature range: Ta = –40°C to +85°C
- Low current consumption
  - During operation (3.4 V for each cell): 7.0 µA max.
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected from a range of 0 mV to 400 mV in 50 mV step.)
***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected from a range of 0 mV to 700 mV in 100 mV step.)

Remark n = 1, 2, 3, 4, 5

■ Applications

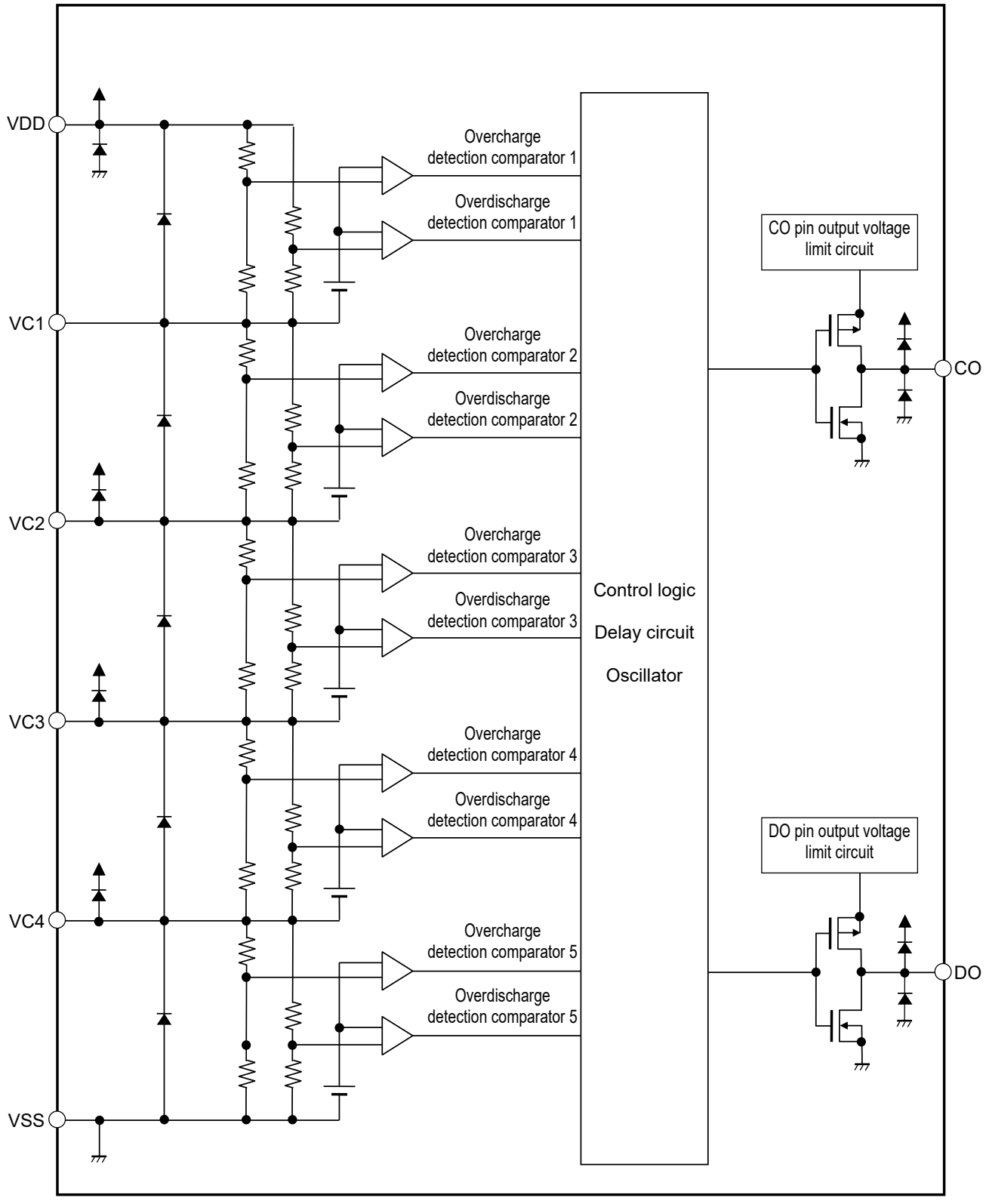
- Lithium-ion rechargeable battery pack

■ Packages

- TMSOP-8
- SNT-8A

■ Block Diagram

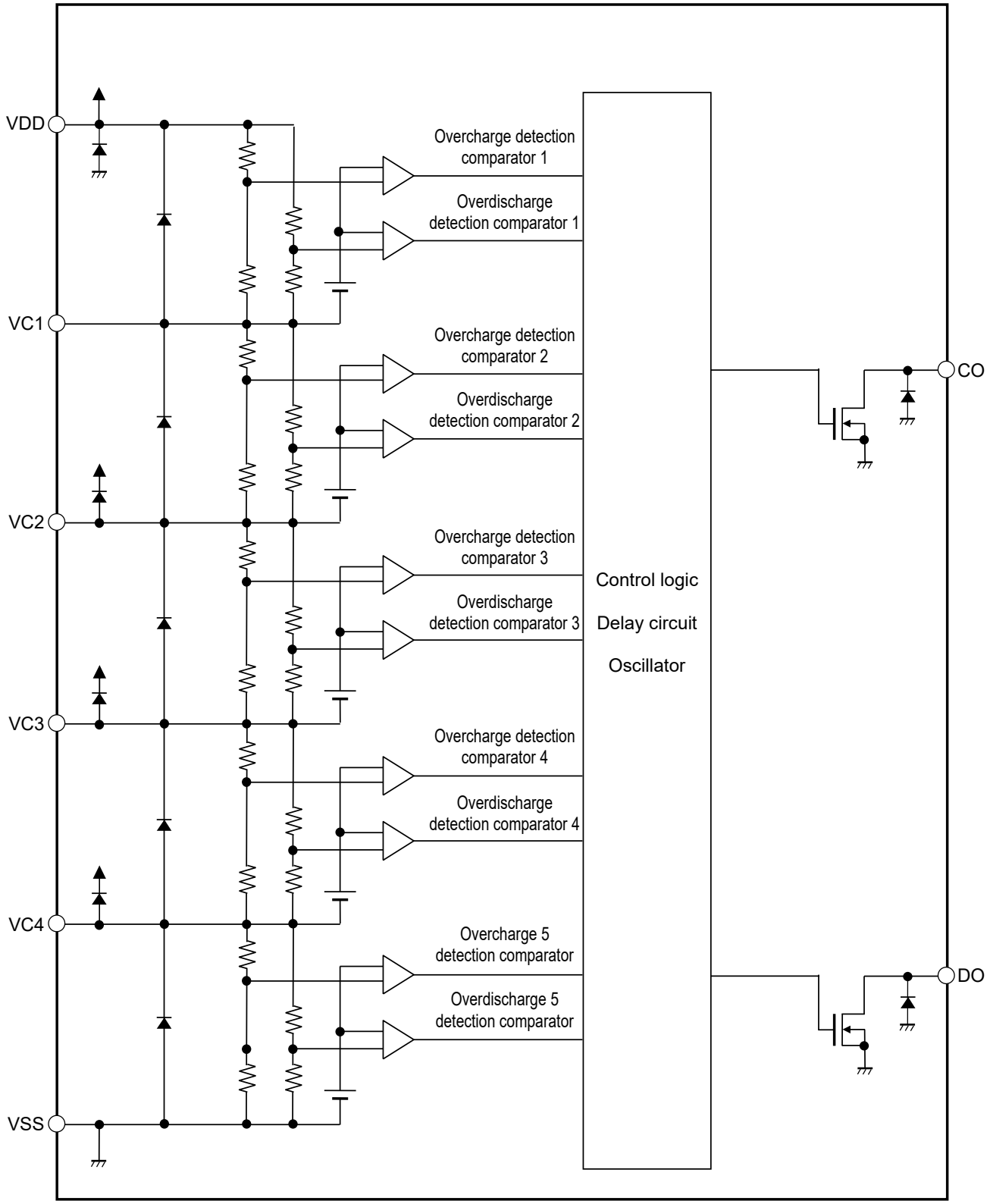
1. CMOS output product



Remark Diodes in the figure are parasitic diodes.

Figure 1

2. Nch open-drain output product



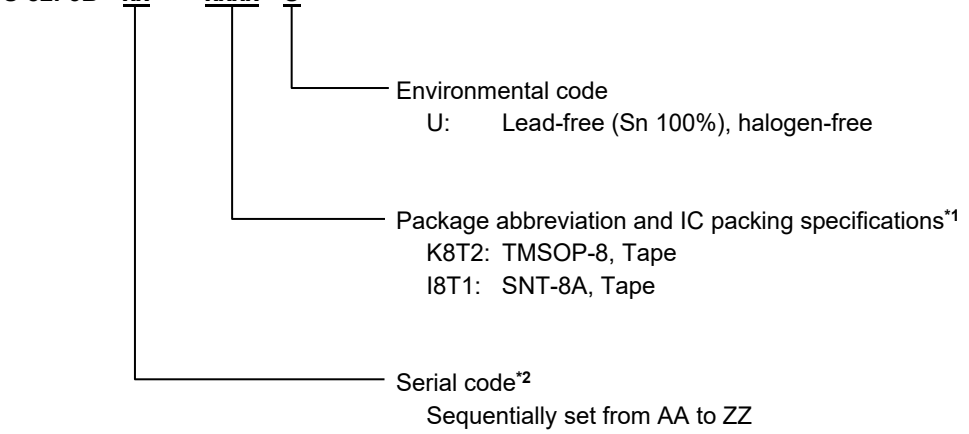
Remark Diodes in the figure are parasitic diodes.

Figure 2

■ Product Name Structure

1. Product name

S-82F5B xx - xxxx U



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	–
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

3. Product name list

3. 1 TMSOP-8

Table 2 (1 / 2)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Overcharge Detection Delay Time*1 [t_{CU}]	Overdischarge Detection Delay Time*2 [t_{DL}]
S-82F5BAA-K8T2U	4.275 V	4.225 V	2.000 V	2.200 V	1.0 s	1.0 s

Table 2 (2 / 2)

Product Name	CO Pin Output Form	CO Pin Output Logic	DO Pin Output Form	DO Pin Output Logic
S-82F5BAA-K8T2U	Nch open-drain output	Active "L"	CMOS output	Active "H"

***1.** Overcharge detection delay time: 0.5 s, 1 s, 2 s, 4 s, 6 s, 8 s
***2.** Overdischarge detection delay time: 128 ms, 256 ms, 0.5 s, 1 s

Remark Please contact our sales representatives for products other than the above.

3. 2 SNT-8A

Table 3 (1 / 2)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Overcharge Detection Delay Time*1 [t_{CU}]	Overdischarge Detection Delay Time*2 [t_{DL}]
S-82F5BAA-I8T1U	4.275 V	4.225 V	2.000 V	2.200 V	1.0 s	1.0 s

Table 3 (2 / 2)

Product Name	CO Pin Output Form	CO Pin Output Logic	DO Pin Output Form	DO Pin Output Logic
S-82F5BAA-I8T1U	Nch open-drain output	Active "L"	CMOS output	Active "H"

***1.** Overcharge detection delay time: 0.5 s, 1 s, 2 s, 4 s, 6 s, 8 s
***2.** Overdischarge detection delay time: 128 ms, 256 ms, 0.5 s, 1 s

Remark Please contact our sales representatives for products other than the above.

■ Pin Configuration

1. TMSOP-8

Top view

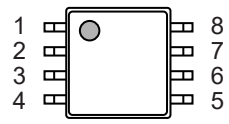


Figure 3

Table 4

Pin No.	Symbol	Description
1	VDD	Positive power supply input pin, Positive voltage connection pin of battery 1
2	VC1	Negative voltage connection pin of battery 1, Positive voltage connection pin of battery 2
3	VC2	Negative voltage connection pin of battery 2, Positive voltage connection pin of battery 3
4	VC3	Negative voltage connection pin of battery 3, Positive voltage connection pin of battery 4
5	VC4	Negative voltage connection pin of battery 4, Positive voltage connection pin of battery 5
6	VSS	Negative power supply input pin, Negative voltage connection pin of battery 5
7	DO	Overdischarge detection output pin
8	CO	Overcharge detection output pin

2. SNT-8A

Top view

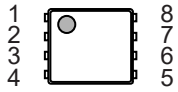


Figure 4

Table 5

Pin No.	Symbol	Description
1	VDD	Positive power supply input pin, Positive voltage connection pin of battery 1
2	VC1	Negative voltage connection pin of battery 1, Positive voltage connection pin of battery 2
3	VC2	Negative voltage connection pin of battery 2, Positive voltage connection pin of battery 3
4	VC3	Negative voltage connection pin of battery 3, Positive voltage connection pin of battery 4
5	VC4	Negative voltage connection pin of battery 4, Positive voltage connection pin of battery 5
6	VSS	Negative power supply input pin, Negative voltage connection pin of battery 5
7	DO	Overdischarge detection output pin
8	CO	Overcharge detection output pin

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item		Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin		V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 28	V
Input pin voltage		V_{IN1}	VC1	V_{DD} – 6.0 to V_{DD} + 0.3, V_{IN2} – 0.3 to V_{IN2} + 6.0	V
		V_{IN2}	VC2	V_{IN3} – 0.3 to V_{IN3} + 6.0, V_{IN3} – 0.3 to V_{DD} + 0.3	V
		V_{IN3}	VC3	V_{IN4} – 0.3 to V_{IN4} + 6.0, V_{IN4} – 0.3 to V_{DD} + 0.3	V
		V_{IN4}	VC4	V_{SS} – 0.3 to V_{SS} + 6.0, V_{SS} – 0.3 to V_{DD} + 0.3	V
Output pin voltage	CMOS output product	V_{OUT}	DO	V_{SS} – 0.3 to V_{DD} + 0.3	V
			CO	V_{SS} – 0.3 to V_{DD} + 0.3	V
	Nch open–drain output product		DO	V_{SS} – 0.3 to V_{SS} + 28	V
			CO	V_{SS} – 0.3 to V_{SS} + 28	V
Operation ambient temperature		T_{opr}	–	–40 to +85	ºC
Storage temperature		T_{stg}	–	–40 to +125	ºC

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Items	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TMSOP-8	Board A	–	160	–	°C/W
			Board B	–	133	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		SNT-8A	Board A	–	211	–	°C/W
			Board B	–	173	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n (n = 1, 2, 3, 4, 5)	V_{CUn}	V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.1 V	V_{CU} – 0.020	V_{CU}	V_{CU} + 0.020	V	1
		Ta = –10°C to +60°C*1, V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.1 V	V_{CU} – 0.025	V_{CU}	V_{CU} + 0.025	V	1
Overcharge release voltage n (n = 1, 2, 3, 4, 5)	V_{CLn}	–	V_{CL} – 0.050	V_{CL}	V_{CL} + 0.050	V	2
Overdischarge detection voltage n (n = 1, 2, 3, 4, 5)	V_{DLn}	–	V_{DL} – 0.08	V_{DL}	V_{DL} + 0.08	V	2
Overdischarge release voltage n (n = 1, 2, 3, 4, 5)	V_{DUn}	–	V_{DU} – 0.10	V_{DU}	V_{DU} + 0.10	V	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	–	3.6	–	24	V	–
Output Voltage							
CO pin voltage "H"	V_{COH}	CMOS output product	5.0	6.0	7.5	V	2
DO pin voltage "H"	V_{DOH}	CMOS output product	5.0	6.0	7.5	V	2
Input Current							
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = V5 = 3.4 V	–	2.5	7.0	µA	2
VCn pin current (n = 1, 2, 3, 4)	I_{VCn}	V1 = V2 = V3 = V4 = V5 = 3.4 V	–1.0	0	1.0	µA	2
Output Current							
DO pin sink current	I_{DOL}	–	20	–	–	µA	2
DO pin source current	I_{DOH}	CMOS output product	–	–	–20	µA	2
DO pin leakage current	I_{DOLL}	Nch open-drain output product	–	–	0.1	µA	2
CO pin sink current	I_{COL}	–	20	–	–	µA	2
CO pin source current	I_{COH}	CMOS output product	–	–	–20	µA	2
CO pin leakage current	I_{COLL}	Nch open-drain output product	–	–	0.1	µA	2
Delay Time							
Overcharge detection delay time	t_{CU}	–	t_{CU} × 0.7	t_{CU}	t_{CU} × 1.3	–	2
Overdischarge detection delay time	t_{DL}	–	t_{DL} × 0.7	tDL	t_{DL} × 1.3	–	2

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Set the initial status of the test circuit as follows.

Table 9

Test Items	CO Pin Output Form	DO Pin Output Form	SW1	SW2	SW3	SW4	SW5	SW6
Current consumption during operation, CO pin sink current, CO pin leakage current, DO pin sink current, DO pin leakage current	–	–	OFF	OFF	OFF	OFF	OFF	OFF
Other than the above	CMOS output	CMOS output	OFF	OFF	OFF	OFF	OFF	OFF
	CMOS output	Nch open-drain output	ON	OFF	OFF	OFF	OFF	OFF
	Nch open-drain output	CMOS output	OFF	ON	OFF	OFF	OFF	OFF
	Nch open-drain output	Nch open-drain output	ON	ON	OFF	OFF	OFF	OFF

1. Overcharge detection voltage n (V_{CUn}) (Test circuit 1)

After setting V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.1 V, V1 is gradually increased. When the CO pin output inverts, the voltage V1 is defined as the overcharge detection voltage 1 (V_{CU1}). Other overcharge detection voltage n (V_{CUn}) can be determined in the same way as when n = 1.

2. Overcharge release voltage n (V_{CLn}) (Test circuit 2)

Set V1 = V_{CU} + 0.1 V, V2 = V3 = V4 = V5 = V_{CL} – 0.1 V and invert the CO pin output. After that, V1 is gradually decreased. When the CO pin output inverts again, the voltage V1 is defined as the overcharge release voltage (V_{CL1}). Other overcharge release voltage n (V_{CLn}) can be determined in the same way as when n = 1.

3. Overdischarge detection voltage n (V_{DLn}), overdischarge release voltage n (V_{DUn}) (Test circuit 2)

After setting V1 = V2 = V3 = V4 = V5 = V_{DL} + 0.1 V, V1 is gradually decreased. When the DO pin output inverts, the voltage V1 is defined as the overdischarge detection voltage 1 (V_{DL1}). After that, set V2 = V3 = V4 = V5 = V_{DU} + 0.15 V. V1 is gradually increased. When the DO pin output inverts again, the voltage V1 is defined as overdischarge release voltage 1 (V_{DU1}). Other overdischarge detection voltage n (V_{DLn}) and overdischarge release voltage n (V_{DUn}) can be determined in the same way as when n = 1.

Remark n = 1, 2, 3, 4, 5

4. CO pin output voltage "H" (V_{COH}), DO pin output voltage "H" (V_{DOH}) (Test circuit 2)

4. 1 CO pin output logic active "H"

The CO pin output voltage "H" (V_{COH}) is the voltage between the CO pin and the VSS pin when setting V1 = 4.8 V, V2 = V3 = V4 = V5 = 3.05 V, I2 = 0.1 μA and SW6 ON.

4. 2 CO pin output logic active "L"

The CO pin output voltage "H" (V_{COH}) is the voltage between the CO pin and the VSS pin when setting V1 = V2 = V3 = V4 = V5 = 3.4 V, I2 = 0.1 μA and SW6 ON.

4. 3 DO pin output logic active "H"

The DO pin output voltage "H" (V_{DOH}) is the voltage between the DO pin and the VSS pin when setting V1 = 1.4 V, V2 = V3 = V4 = V5 = 3.9 V, I1 = 0.1 μA and SW5 ON.

4. 4 DO pin output logic active "L"

The DO pin output voltage "H" (V_{DOH}) is defined as the voltage between the DO pin and the VSS pin when setting V1 = V2 = V3 = V4 = V5 = 3.4 V, I1 = 0.1 μA and SW5 ON.

5. CO pin source current (I_{COH}), CO pin sink current (I_{COL}), CO pin leakage current (I_{COLL}), DO pin source current (I_{DOH}), DO pin sink current (I_{DOL}), DO pin leakage current (I_{DOLL}) (Test circuit 2)

5. 1 CO pin CMOS output product

5. 1. 1 CO pin output logic active "H"

Set SW4 to ON after setting V1 = 4.8 V, V2 = V3 = V4 = V5 = 3.05 V, V7 = V_{COH} – 0.5 V. The CO pin current is the CO pin source current (I_{COH}) at that time.
Set SW4 to ON after setting V1 = V2 = V3 = V4 = V5 = 3.4 V, V7 = 0.5 V. The CO pin current is the CO pin sink current (I_{COL}) at that time.

5. 1. 2 CO pin output logic active "L"

Set SW4 to ON after setting V1 = V2 = V3 = V4 = V5 = 3.4 V, V7 = V_{COH} – 0.5 V. The CO pin current is the CO pin source current (I_{COH}) at that time.
Set SW4 to ON after setting V1 = 4.8 V, V2 = V3 = V4 = V5 = 3.05 V, V7 = 0.5 V. The CO pin current is the CO pin sink current (I_{COL}) at that time.

5. 2 CO pin Nch open-drain output Product

5. 2. 1 CO pin output logic active "H"

Set SW4 to ON after setting V1 = 4.8 V, V2 = V3 = V4 = V5 = 3.05 V, V7 = 17 V. The CO pin current is the CO pin leakage current (I_{COLL}) at this time.
Set SW4 to ON after setting V1 = V2 = V3 = V4 = V5 = 3.4 V, V7 = 0.5 V. The CO pin current is the CO pin sink current (I_{COL}) at that time.

5. 2. 2 CO pin output logic active "L"

Set SW4 to ON after setting V1 = V2 = V3 = V4 = V5 = 3.4 V, V7 = 17 V. The CO pin current is the CO pin leakage current (I_{COLL}) at this time.
Set SW4 to ON after setting V1 = 4.8 V, V2 = V3 = V4 = V5 = 3.05 V, V7 = 0.5 V. The CO pin current is the CO pin sink current (I_{COL}) at that time.

5. 3 DO pin CMOS output product

5. 3. 1 DO pin output logic active "H"

Set SW3 to ON after setting V1 = 1.4 V, V2 = V3 = V4 = V5 = 3.9 V, V6 = V_{DOH} – 0.5 V. The DO pin current is the DO pin source current (I_{DOH}) at this time.
Set SW3 to ON after setting V1 = 4.8 V, V2 = 4.1 V, V3 = 4.1 V, V4 = 4.0 V, V5 = 0 V, V6 = 0.5 V. The DO pin current is the DO pin sink current (I_{DOL}) at this time.

5. 3. 2 DO pin output logic active "L"

Set SW3 to ON after setting V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V_{DOH} – 0.5 V. The DO pin current is the DO pin source current (I_{DOH}) at this time.
Set SW3 to ON after setting V1 = 1.4 V, V2 = V3 = V4 = V5 = 3.9 V, V6 = 0.5 V. The DO pin current is the DO pin sink current (I_{DOL}) at this time.

5. 4 DO pin Nch open-drain output product

5. 4. 1 DO pin output logic active "H"

Set SW3 to ON after setting V1 = 1.4 V, V2 = V3 = V4 = V5 = 3.9 V, V6 = 17 V. The DO pin current is the DO pin leak current (I_{DOLL}) at this time.
Set SW3 to ON after setting V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = 0.5 V. The DO pin current is the DO pin sink current (I_{DOL}) at this time.

5. 4. 2 DO pin output logic active "L"

Set SW3 to ON after setting V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = 17 V. The DO pin current is the DO pin leak current (I_{DOLL}) at this time.
Set SW3 to ON after setting V1 = 1.4 V, V2 = V3 = V4 = V5 = 3.9 V, V6 = 0.5 V. The DO pin current is the DO pin sink current (I_{DOL}) at this time.

6. Overcharge detection delay time (t_{CU}) (Test circuit 2)

After setting V5 = V_{CU} – 0.2 V, V1 = V2 = V3 = V4 = 3.4 V, V5 is increased to V_{CU} + 0.2 V. The overcharge detection delay time (t_{CU}) is the time period until the CO pin output inverts.

7. Overdischarge detection delay time (t_{DL}) (Test circuit 2)

After setting V5 = V_{DL} + 0.2 V, V2 = V3 = V4 = V5 = 3.4 V, V5 is decreased to V_{DL} – 0.2 V. The overdischarge detection delay time (t_{DL}) is the time period until the DO pin output inverts.

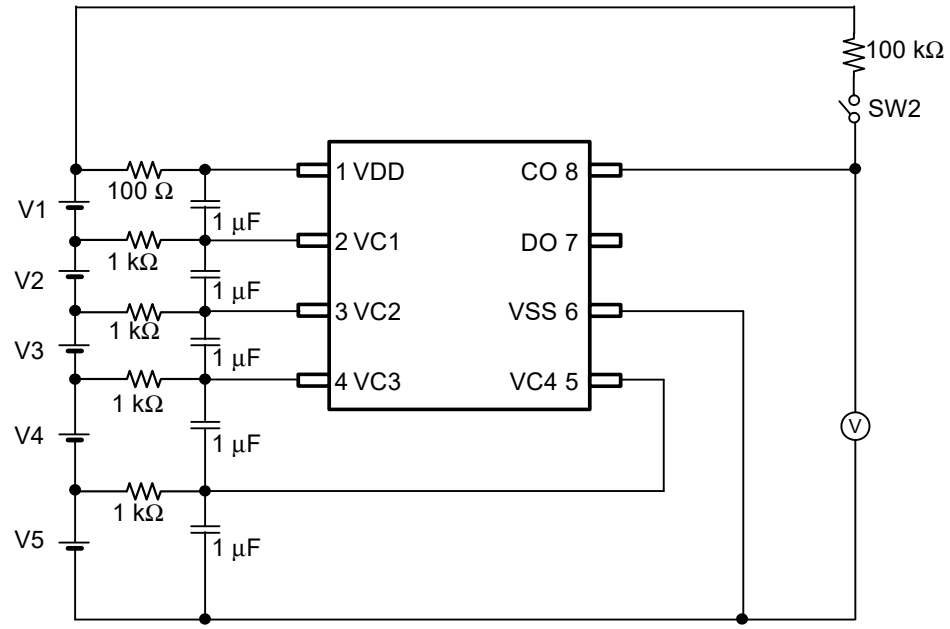


Figure 5 Test Circuit 1

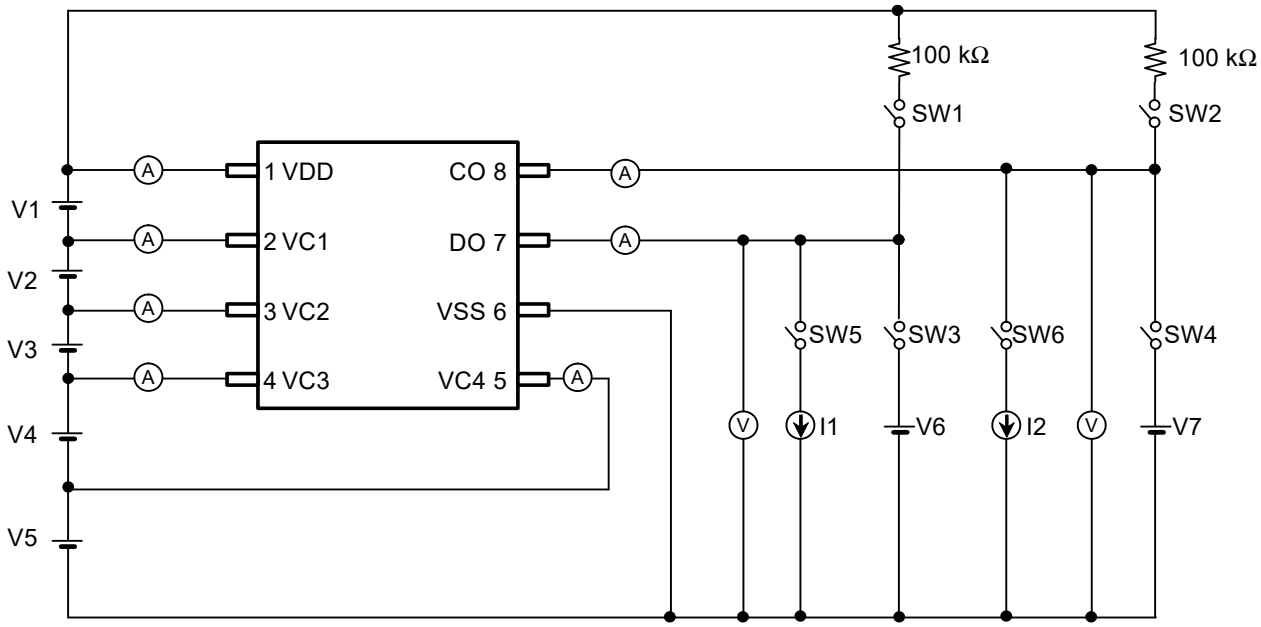


Figure 6 Test Circuit 2

■ Operation

1. Normal status

When the voltage of all batteries is in the range between the overdischarge detection voltage n (V_{DLn}) and the overcharge detection voltage (V_{CUn}), the CO pin output is shown in **Table 10**, and the DO pin output is shown in **Table 11**. This status is called the normal status.

Table 10

CO Pin Output Logic	CO Pin Output
Active "H"	"L"
Active "L"	"H"

Table 11

DO Pin Output Logic	DO Pin Output
Active "H"	"L"
Active "L"	"H"

2. Overcharge status

When the voltage of any of the batteries exceeds the overcharge detection voltage n (V_{CUn}) during charging and this condition continues for the overcharge detection delay time (t_{CU}) or longer, the CO pin output inverts. This status is called the overcharge status.
When the voltage of all batteries falls below the overcharge release voltage n (V_{CLn}), the overcharge status is released, and this IC returns to its normal status.

3. Overdischarge status

When the voltage of any of the batteries falls below the overdischarge detection voltage n (V_{DLn}) during discharging and the status continues for the overdischarge detection delay time (t_{DL}) or longer, the DO pin output inverts. This status is called the overdischarge status.
When the voltage of all batteries becomes overdischarge release voltage n (V_{DUn}) or higher, this IC returns to normal status.

4. Test mode

In this IC, the overcharge detection delay time (t_{CU}) and the overdicharge delay time (t_{DL}) can be shortened by entering the test mode.
This IC transitions to the test mode by setting the DO pin voltage to the following voltage while the IC is in the normal status.

Table 12

DO Pin Output Form	DO Pin Output Logic	DO Pin Voltage
CMOS output	Active "L"	0 V
CMOS output	Active "H"	5 V
Nch open-drain output	–	V_{DD} + 5 V

In the test mode, overdischarge status output is output from the CO pin, not the DO pin.
After transitioning to the test mode, the test mode is retained even if this IC transitions to the overcharge status or the overdischarge status by retaining the DO pin voltage.
The test mode is released when the DO pin voltage input is returned to normal status output.

Caution Set the test mode when all batteries are neither overcharged nor overdischarged.

Remark n = 1, 2, 3, 4, 5

■ Timing Charts

1. Overcharge detection operation

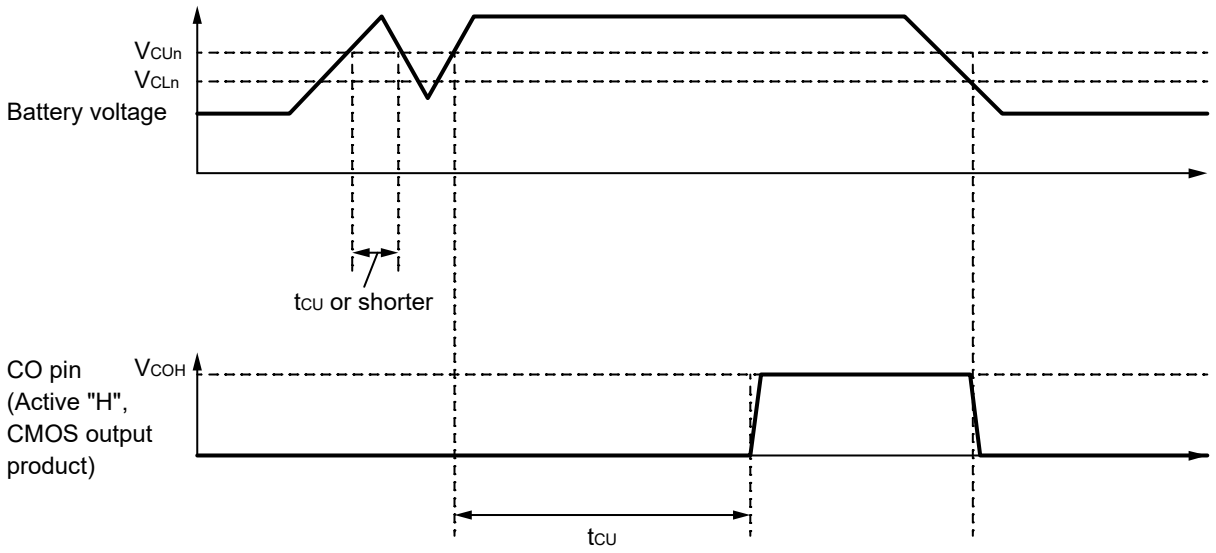


Figure 7

2. Overdischarge detection operation

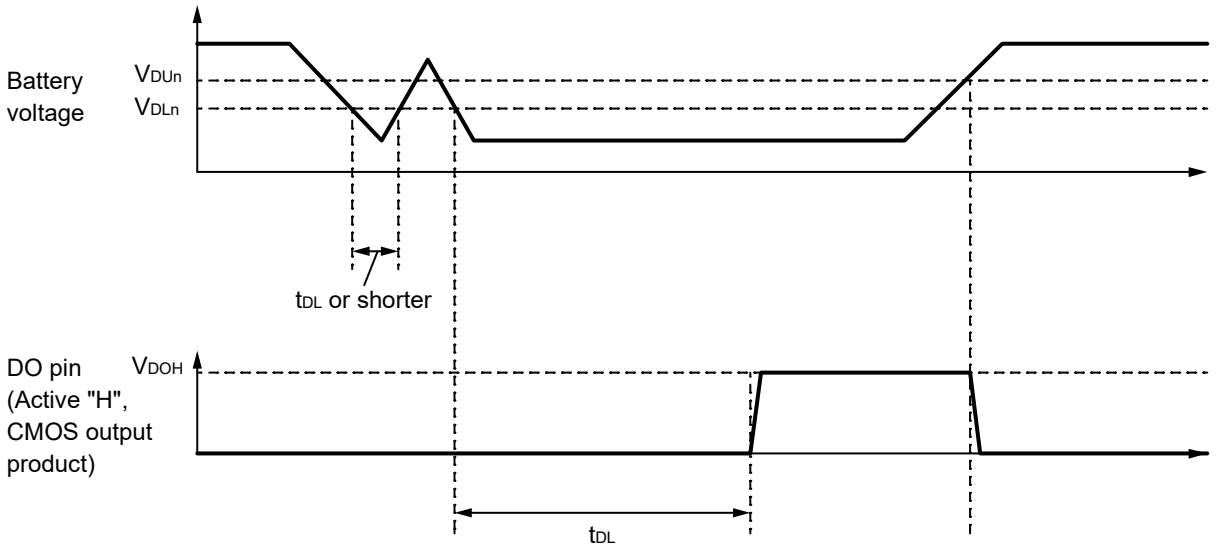


Figure 8

Remark n = 1, 2, 3, 4, 5

■ Battery Protection IC Connection Example

1. 5-serial cell (CO pin output form: CMOS output, DO pin output form: CMOS output)

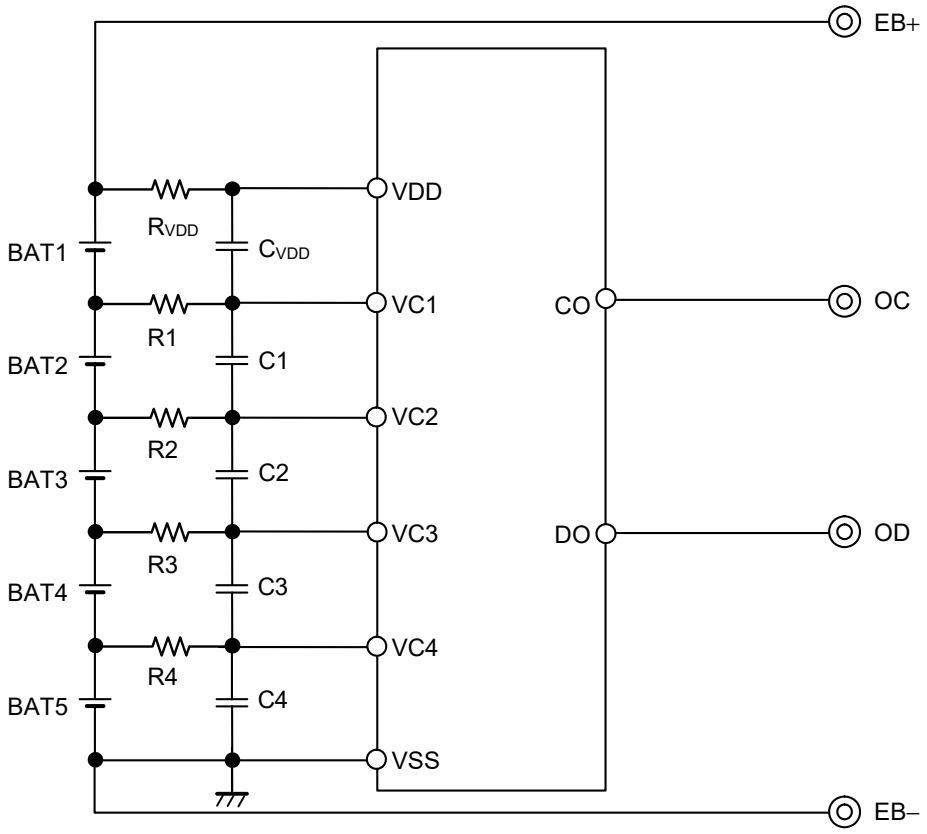


Figure 9

Table 13 Constants for External Components

No.	Part	Typ.	Unit
1	R1 to R4	1	kΩ
2	C1 to C4, C_{VDD}	1	μF
3	R_{VDD}	100	Ω

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

2. 4-serial cell (CO pin output form: CMOS output, DO pin output form: CMOS output)

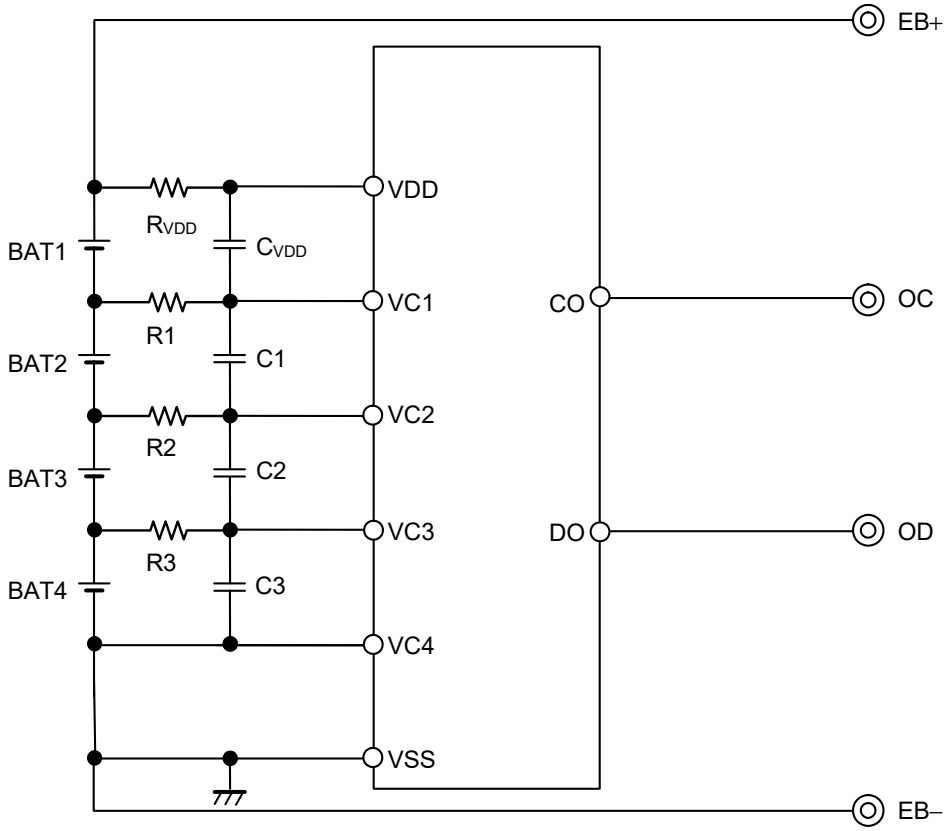


Figure 10

Table 14 Constants for External Components

No.	Part	Typ.	Unit
1	R1 to R3	1	kΩ
2	C1 to C3, C_{VDD}	1	μF
3	R_{VDD}	100	Ω

Caution 1. The constants may be changed without notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

3. 3-serial cell (CO pin output form: CMOS output, DO pin output form: CMOS output)

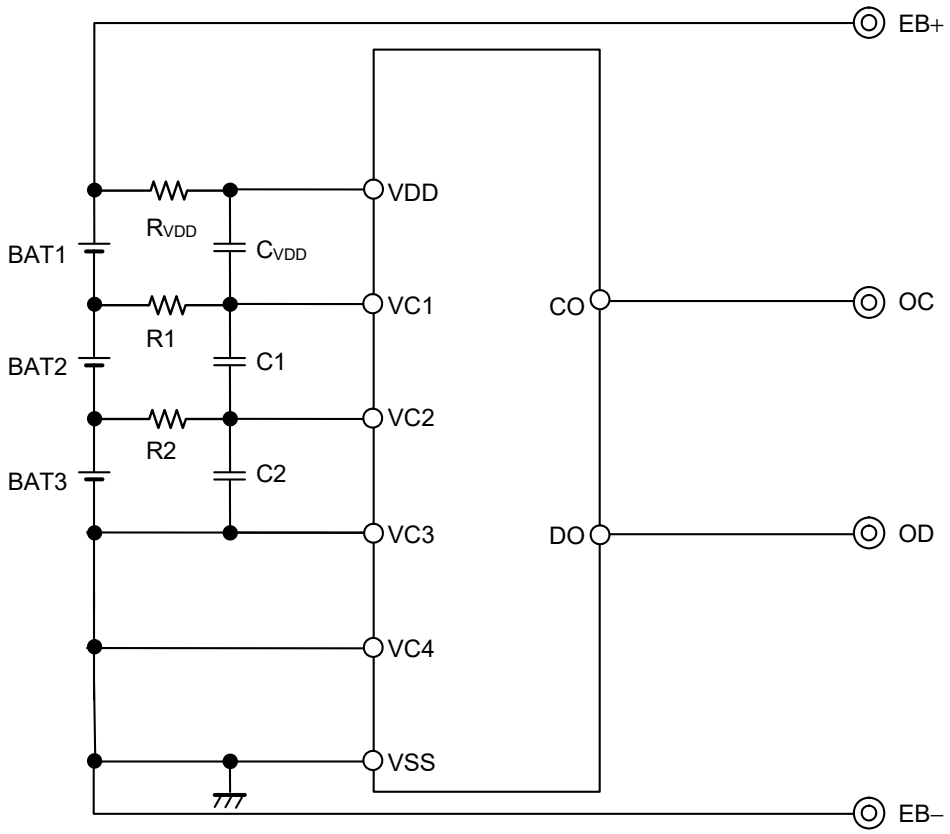


Figure 11

Table 15 Constants for External Components

No.	Part	Typ.	Unit
1	R1, R2	1	kΩ
2	C1, C2, C_{VDD}	1	μF
3	R_{VDD}	100	Ω

Caution 1. The constants may be changed without notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

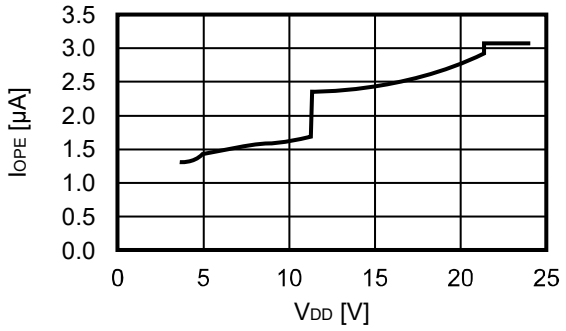
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- If an overcharged battery and an overdischarged battery intermix, this IC will change to the overcharge and overdischarge statuses.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

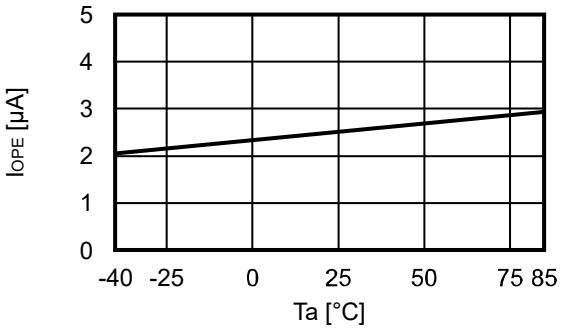
■ Characteristics (Typical Data)

1. Current consumption

1. 1 I_{OPE} vs. V_{DD}

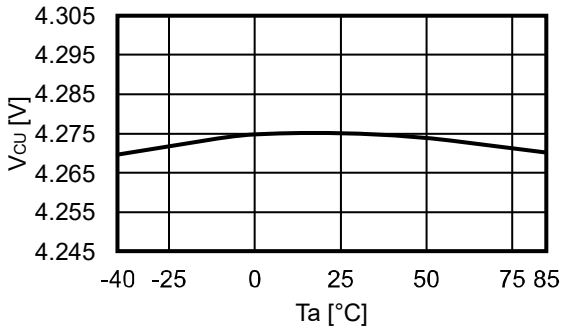


1. 2 I_{OPE} vs. Ta

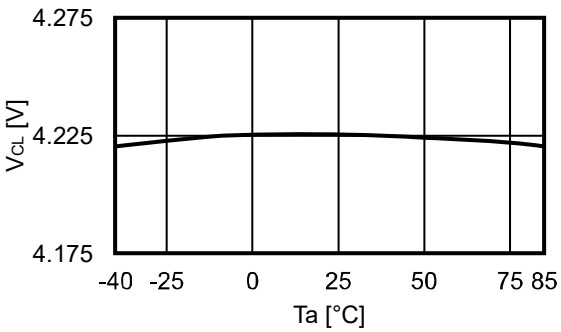


2. Detection voltage, release voltage

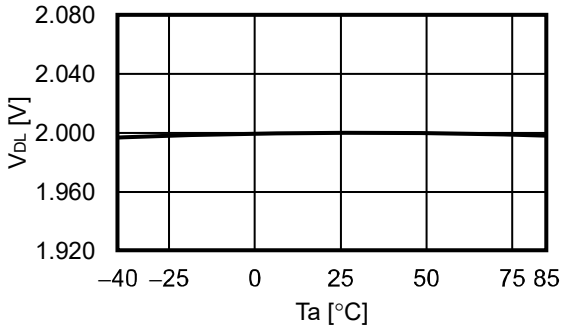
2. 1 V_{CU} vs. Ta



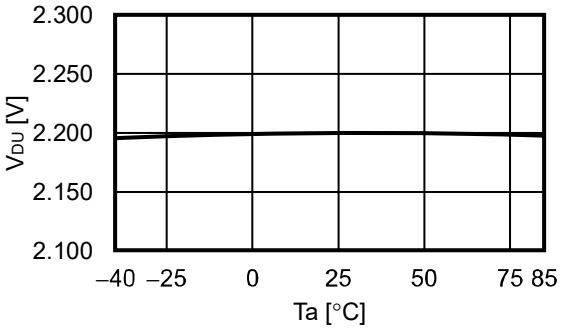
2. 2 V_{CL} vs. Ta



2. 3 V_{DL} vs. Ta

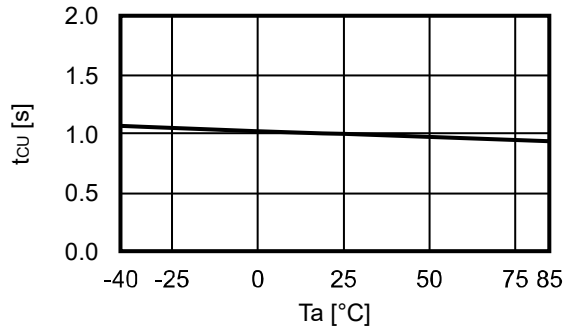


2. 4 V_{DU} vs. Ta

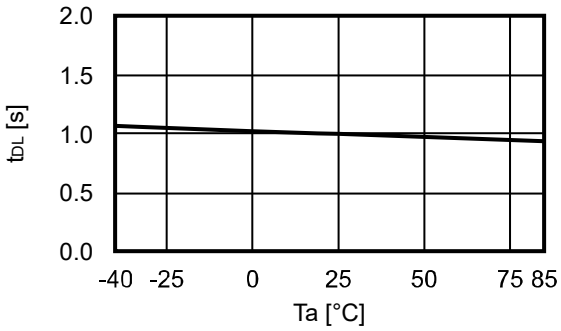


3. Delay time

3. 1 t_{CU} vs. Ta

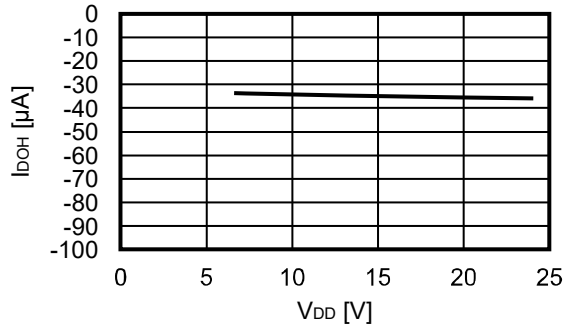


3. 2 t_{DL} vs. Ta

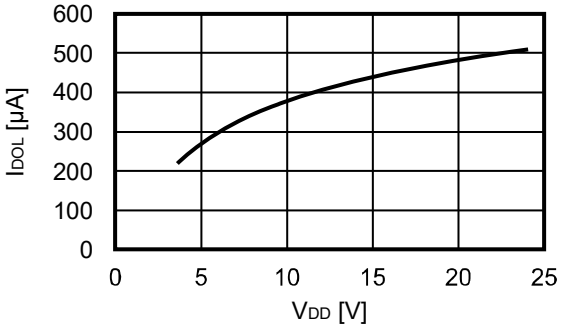


4. Output pin

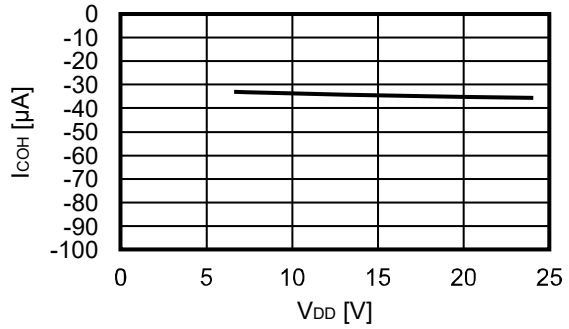
4. 1 I_{DOH} vs. V_{DD}



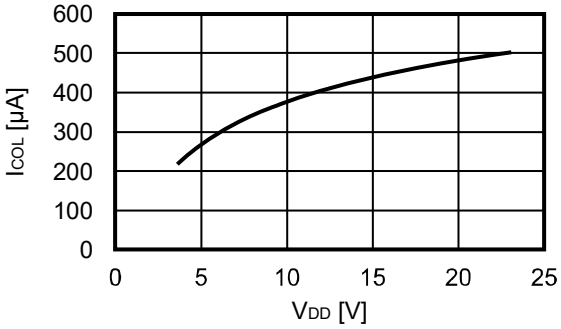
4. 2 I_{DOL} vs. V_{DD}



4. 3 I_{COH} vs. V_{DD}

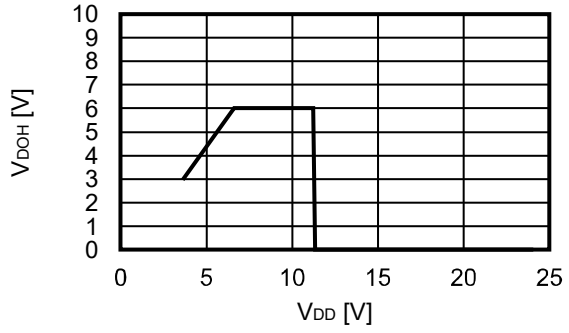


4. 4 I_{COL} vs. V_{DD}



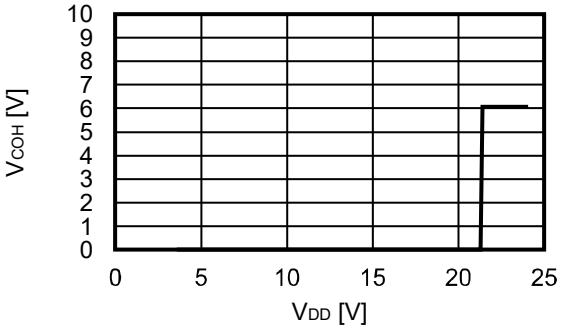
4. 5 V_{DOH} vs. V_{DD}

DO pin output logic active "H"
V_{DU} = 2.200 V



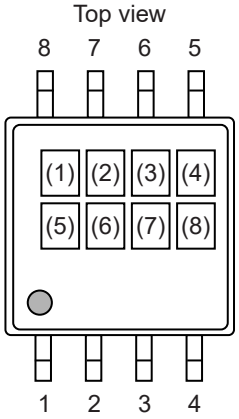
4. 6 V_{COH} vs. V_{DD}

CO pin output logic active "H"
V_{CU} = 4.275 V



■ Marking Specifications

1. TMSOP-8

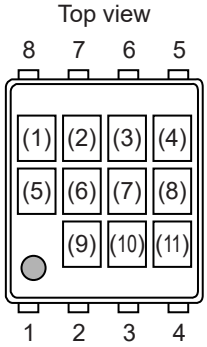


(1): Blank
(2) to (4): Product code (refer to **Product name vs. Product code**)
(5): Blank
(6) to (8): Lot number

Product name vs. Product code

Product Name	Product Code		
	(2)	(3)	(4)
S-82F5BAA-K8T2U	b	E	A

2. SNT-8A



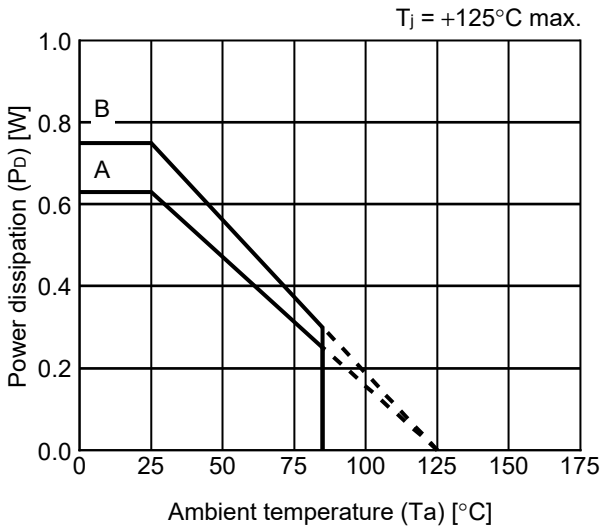
(1): Blank
(2) to (4): Product code (refer to **Product name vs. Product code**)
(5), (6): Blank
(7) to (11): Lot number

Product name vs. Product code

Product Name	Product Code		
	(2)	(3)	(4)
S-82F5BAA-I8T1U	b	E	A

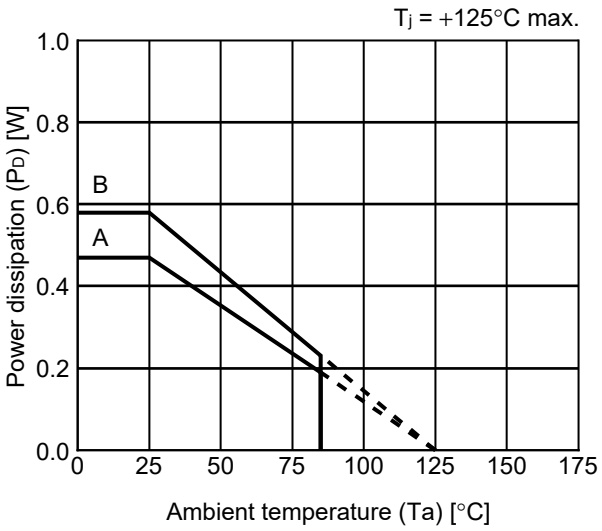
■ Power Dissipation

TMSOP-8



Board	Power Dissipation (P_D)
A	0.63 W
B	0.75 W
C	–
D	–
E	–

SNT-8A

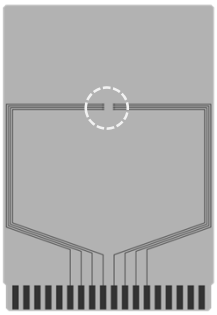


Board	Power Dissipation (P_D)
A	0.47 W
B	0.58 W
C	–
D	–
E	–

TMSOP-8 Test Board

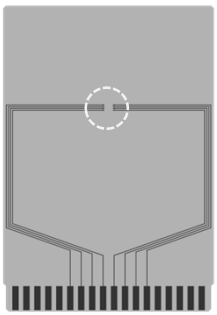
(1) Board A

IC Mount Area



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



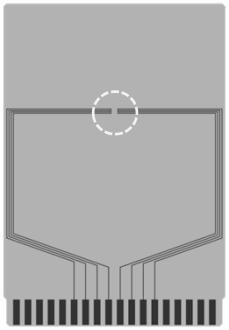
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. TMSOP8-A-Board-SD-1.0

SNT-8A Test Board

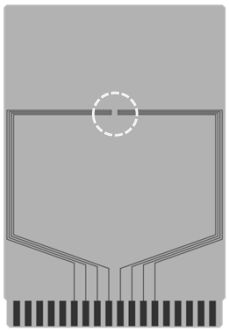
IC Mount Area

(1) Board A



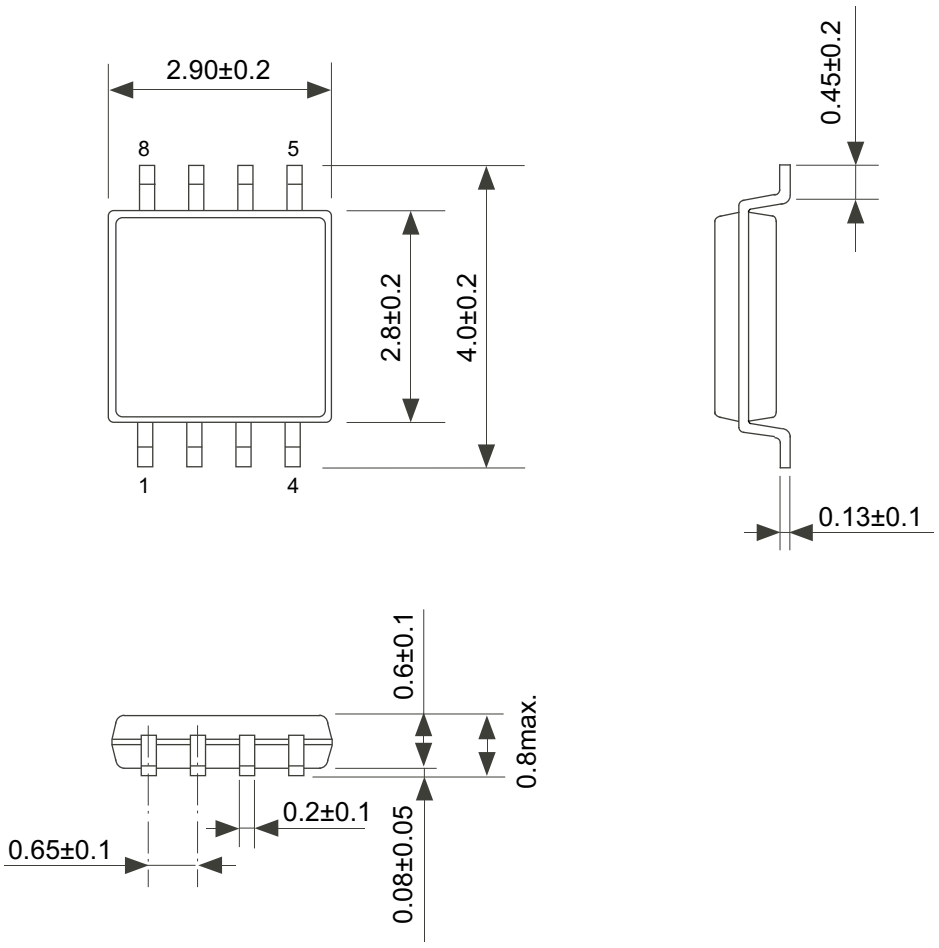
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

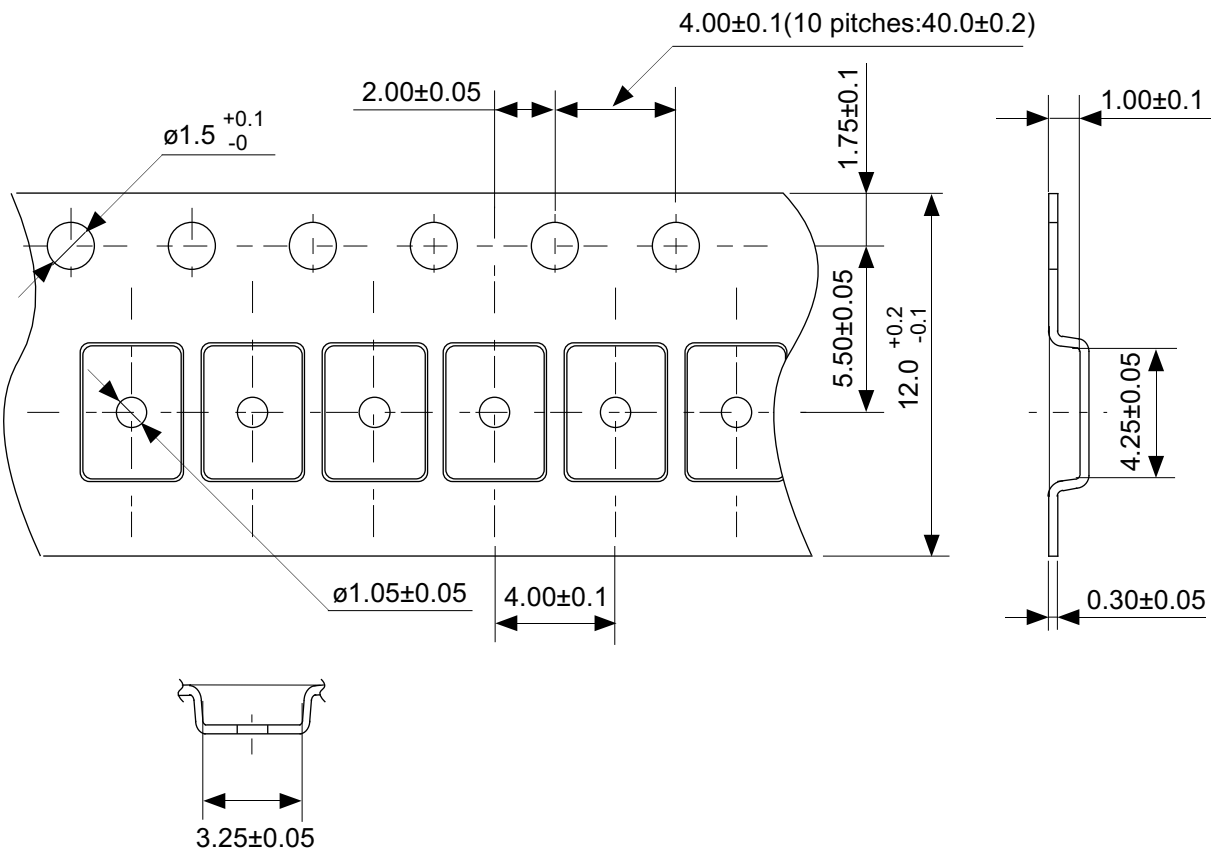
No. SNT8A-A-Board-SD-1.0

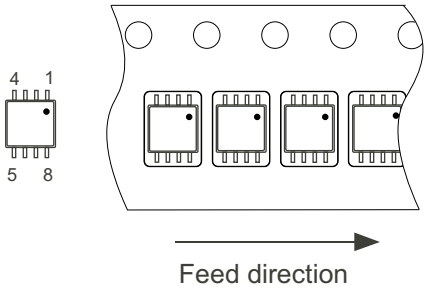


No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm

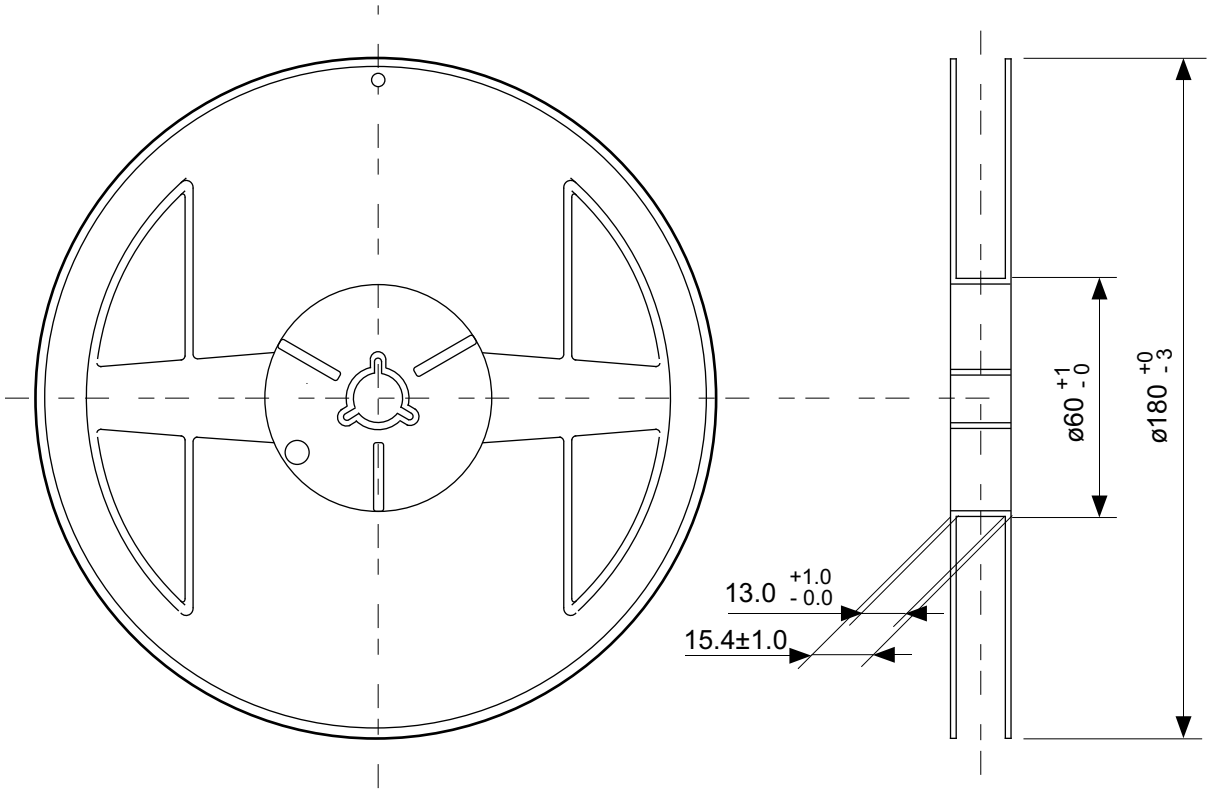
ABLIC Inc.



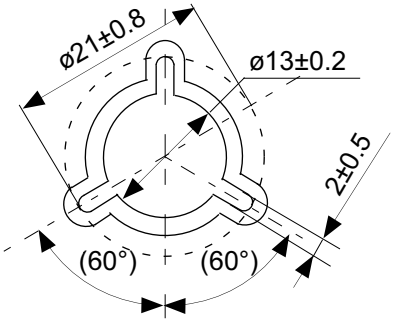


No. FM008-A-C-SD-3.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-3.0
ANGLE	
UNIT	mm
ABLIC Inc.	

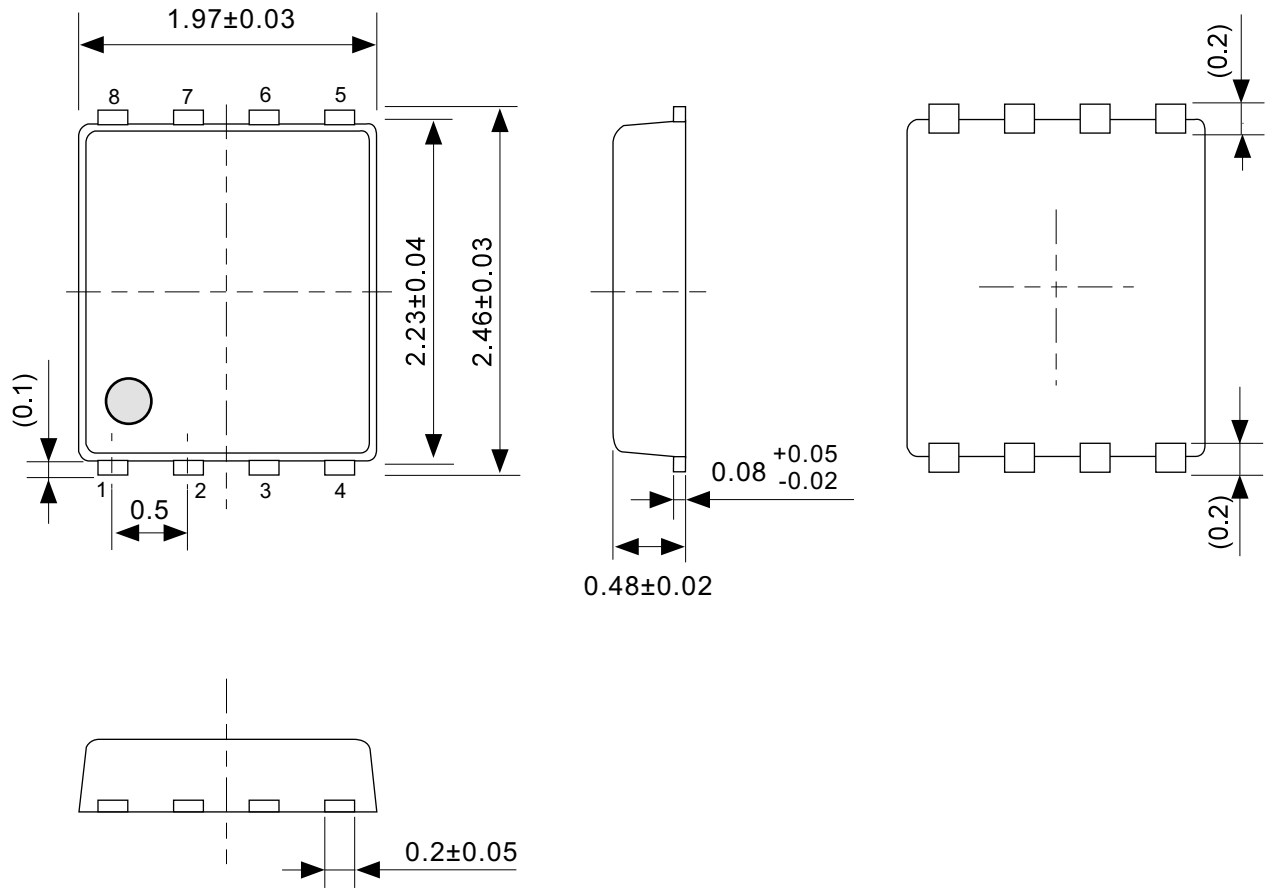


Enlarged drawing in the central part



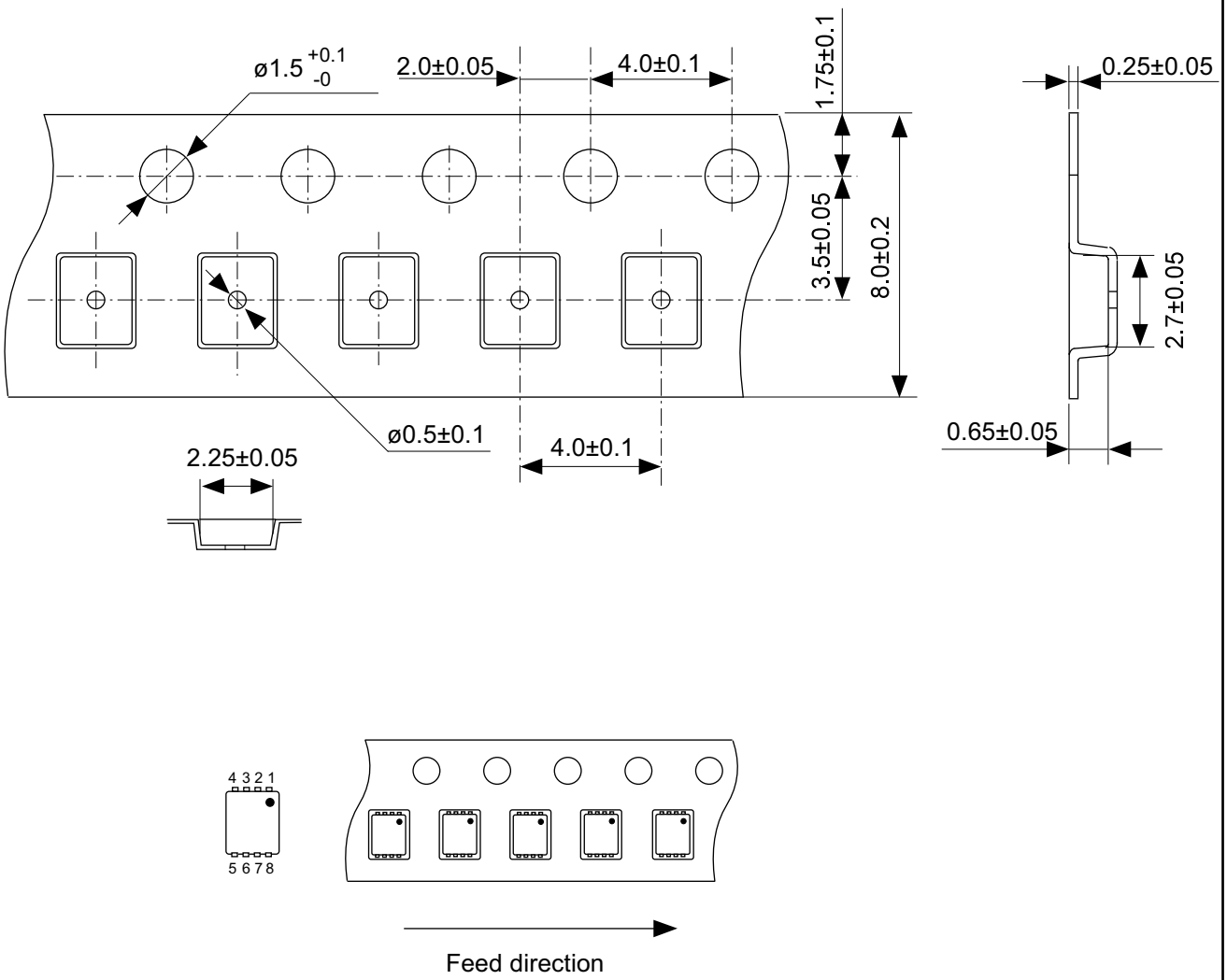
No. FM008-A-R-SD-2.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
	ABLIC Inc.		



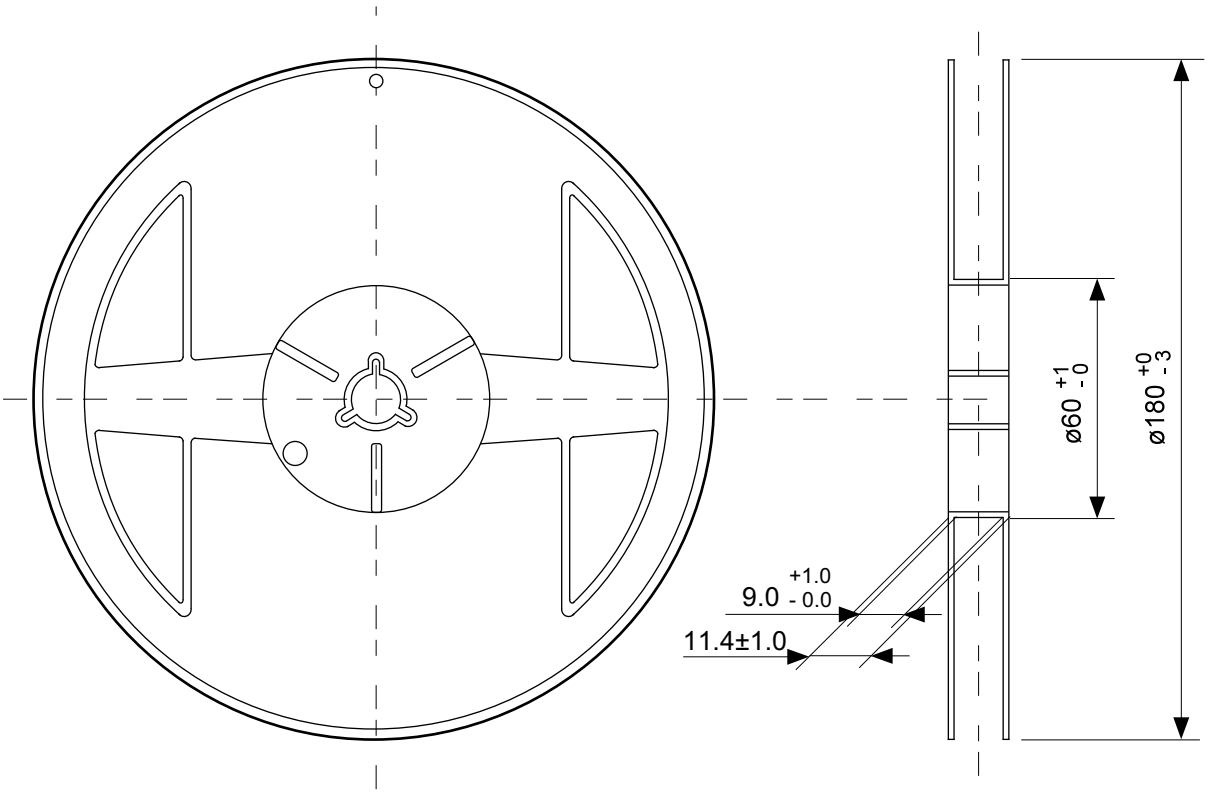
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

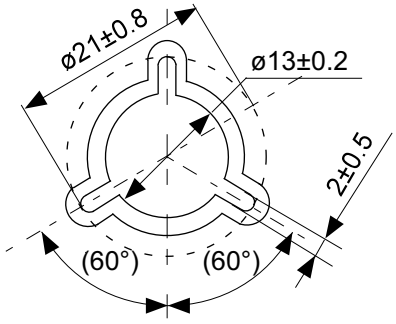


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

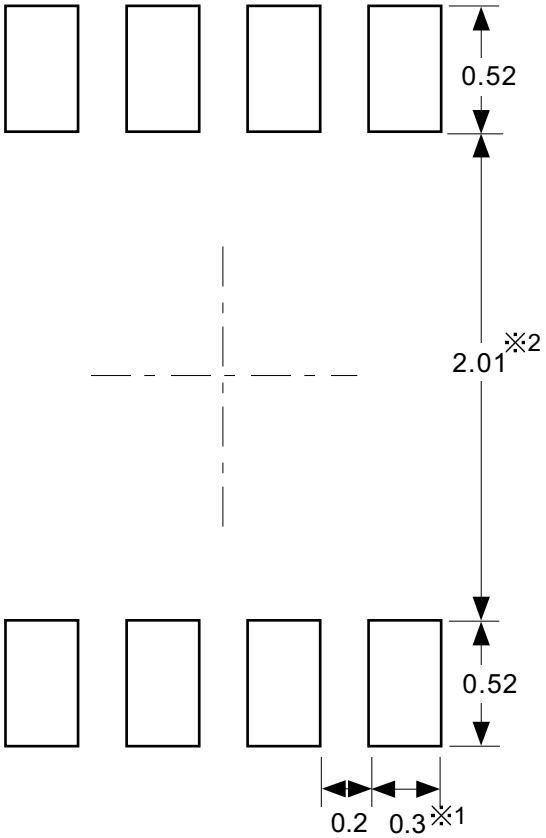


Enlarged drawing in the central part



No. PH008-A-R-SD-2.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
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2.4-2019.07