S-8245A/C Series

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BATTERY PROTECTION IC FOR 3-SERIAL TO 5-SERIAL CELL PACK

Rev.1.4_00

The S-8245A/C Series is a protection IC for 3-serial to 5-serial cell lithium-ion rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. It is suitable for protecting 3-serial to 5-serial cell lithium-ion rechargeable battery packs from overcharge, overdischarge, and overcurrent. Cascade connection using the S-8245A/C Series realizes protecting 6-serial or more cells lithium-ion rechargeable battery packs.
Connecting an NTC, it allows for the temperature detection at four different points: high temperature detection during charging, low temperature detection during charging, high temperature detection during discharging, and low temperature detection during discharging.

■ Features

- High-accuracy voltage detection for each cell
  - Overcharge detection voltage n (n = 1 to 5): 3.550 V to 4.600 V (50 mV step) Accuracy ±20 mV
  - Overcharge release voltage n (n = 1 to 5): 3.150 V to 4.600 V*1 Accuracy ±50 mV
  - Overdischarge detection voltage n (n = 1 to 5): 2.000 V to 3.200 V (100 mV step) Accuracy ±80 mV
  - Overdischarge release voltage n (n = 1 to 5): 2.000 V to 3.400 V*2 Accuracy ±100 mV
- Three-level discharge overcurrent detection:
  - Discharge overcurrent 1 detection voltage: 0.020 V to 0.300 V (10 mV step) Accuracy ±10 mV
  - Discharge overcurrent 2 detection voltage: 0.040 V to 0.500 V (20 mV step) Accuracy ±15 mV
  - Load short-circuiting detection voltage: 0.100 V to 1.000 V (25 mV step) Accuracy ±50 mV
- Charge overcurrent detection:
  - Charge overcurrent detection voltage: −0.300 V to −0.020 V (10 mV step) Accuracy ±10 mV
- Each delay time is settable by an external capacitor
  (Load short-circuiting detection delay time and temperature detection delay time are internally fixed)
- Independent control of charge inhibition, discharge inhibition, and power-saving by each control pin
- 0 V battery charge function is selectable: Available, unavailable
- Power-down function is selectable: Available, unavailable
- CIT pin internal resistance value is selectable: 831 kΩ typ., 8.31 MΩ typ.
- CO and DO pin output voltage is limited to 15 V max. respectively
- Switching control for 3-serial to 5-serial cell is possible by inputting voltage to the SEL1 pin and the SEL2 pin
- Protection of 6-serial or more cells is possible by cascade connection
- Temperature detection is possible at four different points by connecting an NTC
  - High temperature detection ratio during charging / discharging: 0.600 to 0.900 (0.005 step) Accuracy ±0.005
  - Low temperature detection ratio during charging / discharging: 0.030 to 0.400 (0.005 step) Accuracy ±0.005
- High-withstand voltage: Absolute maximum rating 28 V
- Wide operation voltage range: 5 V to 24 V
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  - During operation: 20 μA max. (Ta = +25°C)
  - During power-down: 0.5 μA max. (Ta = +25°C)
  - During power-saving: 0.1 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage n (n = 1 to 5) is selectable in 0 V to 0.4 V in 50 mV step)
***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage n (n = 1 to 5) is selectable in 0 V to 0.7 V in 100 mV step)

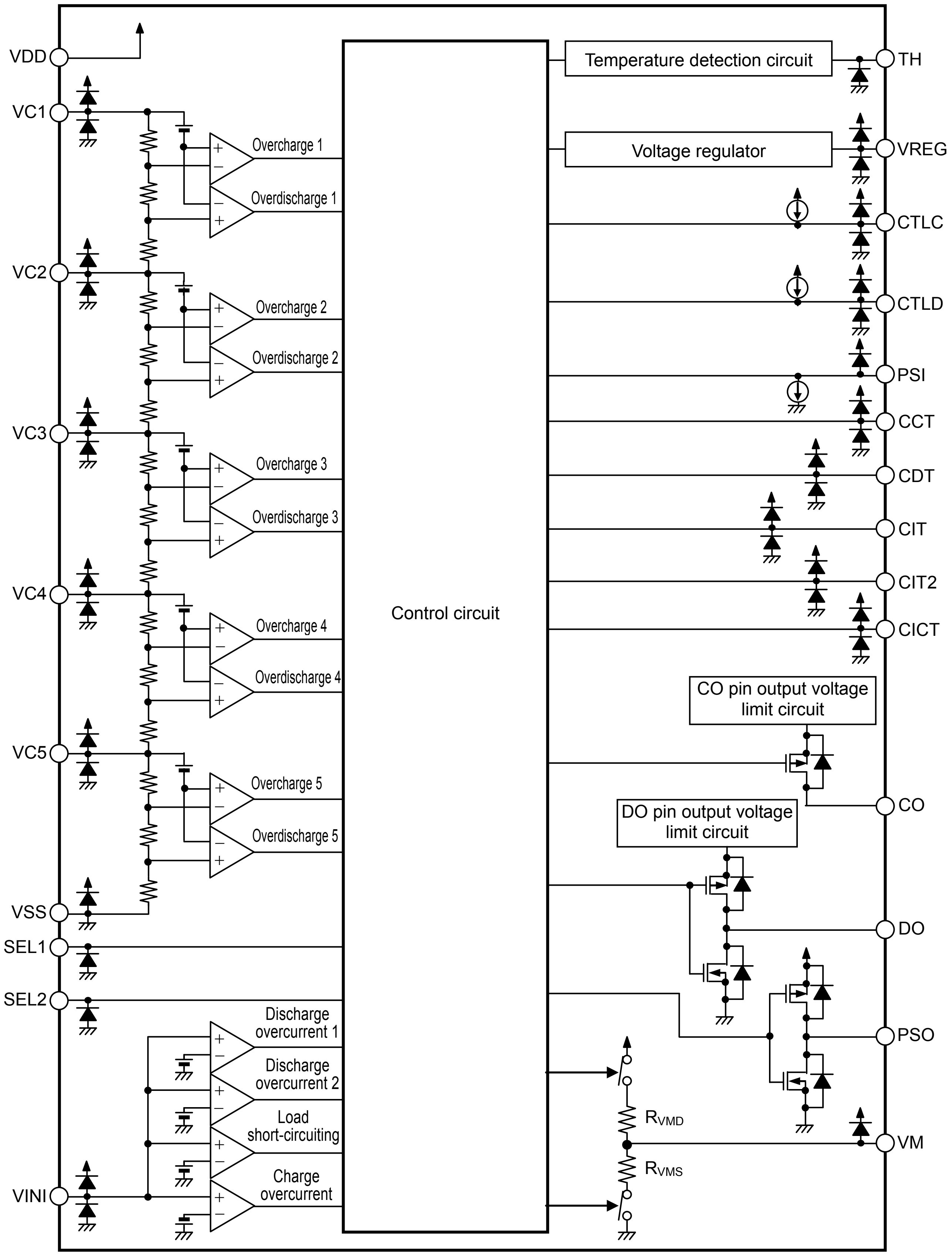
■ Application

- Lithium-ion rechargeable battery pack

■ Package

- 24-Pin SSOP

■ Block Diagram



Remark Diodes in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name

S-8245 x xx - FGT1 U

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications*1
FGT1: 24-Pin SSOP, Tape

Serial code*2
Sequentially set from AA to ZZ

Product type
A: For application circuit with an integrated charge and discharge path
C: For application circuit with separate charge and discharge paths

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Code

Package Name	Dimension	Tape	Reel
24-Pin SSOP	FS024-B-P-SD	FS024-B-C-SD	FS024-B-R-SD

3. Product name list

3. 1 S-8245A Series

Table 2 (1 / 2)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent 1 Detection Voltage [V_{DIOV1}]	Discharge Overcurrent 2 Detection Voltage [V_{DIOV2}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]
S-8245AAA-FGT1U	4.100 V	4.050 V	2.600 V	2.700 V	0.020 V	0.040 V	0.100 V	−0.020 V
S-8245AAB-FGT1U	4.350 V	4.150 V	2.400 V	2.700 V	0.150 V	0.300 V	0.500 V	−0.150 V
S-8245AAC-FGT1U	4.250 V	4.150 V	2.500 V	3.000 V	0.100 V	0.200 V	0.500 V	−0.100 V

Table 2 (2 / 2)

Product Name	0 V Battery Charge Function*1	Power-down Function*2	CIT Pin Internal Resistance Value*3 [R_{CIT}]	High Temperature Detection Ratio during Charging [r_{THCH}]	Low Temperature Detection Ratio during Charging [r_{THCL}]	High Temperature Detection Ratio during Discharging [r_{THDH}]	Low Temperature Detection Ratio during Discharging [r_{THDL}]
S-8245AAA-FGT1U	Available	Available	831 kΩ	0.670	0.270	0.795	0.190
S-8245AAB-FGT1U	Unavailable	Available	831 kΩ	0.850	0.150	0.900	0.100
S-8245AAC-FGT1U	Unavailable	Available	831 kΩ	0.670	0.270	0.795	0.190

***1.** 0 V battery charge function "available" / "unavailable" is selectable.
***2.** Power-down function "available" / "unavailable" is selectable.
***3.** CIT pin internal resistance value 831 kΩ typ. / 8.31 MΩ typ. is selectable.

Remark Please contact our sales office for products other than those specified above.

3. 2 S-8245C Series

Table 3 (1 / 2)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent 1 Detection Voltage [V_{DIOV1}]	Discharge Overcurrent 2 Detection Voltage [V_{DIOV2}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]
S-8245CAA-FGT1U	4.100 V	4.050 V	2.600 V	2.700 V	0.020 V	0.040 V	0.100 V	−0.020 V
S-8245CAB-FGT1U	4.250 V	4.150 V	2.500 V	3.000 V	0.100 V	0.200 V	0.500 V	−0.100 V

Table 3 (2 / 2)

Product Name	0 V Battery Charge Function*1	Power-down Function*2	CIT Pin Internal Resistance Value*3 [R_{CIT}]	High Temperature Detection Ratio during Charging [r_{THCH}]	Low Temperature Detection Ratio during Charging [r_{THCL}]	High Temperature Detection Ratio during Discharging [r_{THDH}]	Low Temperature Detection Ratio during Discharging [r_{THDL}]
S-8245CAA-FGT1U	Unavailable	Available	831 kΩ	0.670	0.270	0.795	0.190
S-8245CAB-FGT1U	Unavailable	Available	831 kΩ	0.670	0.270	0.795	0.190

***1.** 0 V battery charge function "available" / "unavailable" is selectable.
***2.** Power-down function "available" / "unavailable" is selectable.
***3.** CIT pin internal resistance value 831 kΩ typ. / 8.31 MΩ typ. is selectable.

Remark Please contact our sales office for products other than those specified above.

■ Pin Configuration

1. 24-Pin SSOP

Top view

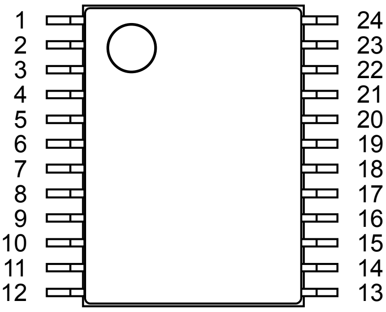


Figure 2

Table 4

Pin No.	Symbol	Description
1	TH	Input pin for temperature detection
2	VDD	Input pin for positive power supply, connection pin for positive voltage of battery 1
3	VC1	Connection pin for positive voltage of battery 1
4	VC2	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
5	VC3	Connection pin for negative voltage of battery 2, connection pin for positive voltage of battery 3
6	VC4	Connection pin for negative voltage of battery 3, connection pin for positive voltage of battery 4
7	VC5	Connection pin for negative voltage of battery 4, connection pin for positive voltage of battery 5
8	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 5
9	VINI	Voltage detection pin between VSS pin and VINI pin
10	SEL1	Switching pins for number of cells in series [SEL1, SEL2] = ["L", "L"] : 5-serial cell [SEL1, SEL2] = ["L", "H"] : 4-serial cell [SEL1, SEL2] = ["H", "L"] : 3-serial cell [SEL1, SEL2] = ["H", "H"] : Setting inhibited
11	SEL2	
12	CICT	Capacitor connection pin for delay for charge overcurrent detection
13	CCT	Capacitor connection pin for delay for overcharge detection voltage
14	CDT	Capacitor connection pin for delay for overdischarge detection voltage
15	CIT	Capacitor connection pin for delay for discharge overcurrent 1 detection
16	CIT2	Capacitor connection pin for delay for discharge overcurrent 2 detection
17	PSO	Output pin for power-saving signal (CMOS output)
18	DO	Connection pin of discharge control FET gate (CMOS output)
19	CO	Connection pin of charge control FET gate (Pch open-drain output)
20	VM	Voltage detection pin between VSS pin and VM pin
21	CTLC	Control pin for CO pin output
22	CTLD	Control pin for DO pin output
23	PSI	Control pin for Power-saving
24	VREG	Voltage output pin for temperature detection

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 28	V
Input pin voltage 1	V_{IN1}	VC1, VC2, VC3, VC4, VC5, CCT, CDT, CIT, CIT2, CICT, SEL1, SEL2, TH	V_{SS} − 0.3 to V_{DD} + 0.3	V
Input pin voltage 2	V_{IN2}	VM, VINI, PSI	V_{DD} − 28 to V_{DD} + 0.3	V
Input pin voltage 3	V_{IN3}	CTLC, CTLD	V_{SS} − 0.3 to V_{SS} + 28	V
Output pin voltage 1	V_{OUT1}	DO, PSO, VREG	V_{SS} − 0.3 to V_{DD} + 0.3	V
Output pin voltage 2	V_{OUT2}	CO	V_{DD} − 28 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	−	−40 to +85	°C
Storage temperature	T_{stg}	−	−40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	24-Pin SSOP	Board A	−	70	−	°C/W
			Board B	−	60	−	°C/W
			Board C	−	−	−	°C/W
			Board D	−	−	−	°C/W
			Board E	−	−	−	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 7 (1 / 3)

(V1 = V2 = V3 = V4 = V5 = 3.5 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n (n = 1 to 5)	V_{CUn}	V1 = V2 = V3 = V4 = V5 = V_{CUn} − 0.050 V	V_{CUn} − 0.020	V_{CUn}	V_{CUn} + 0.020	V	1
Overcharge release voltage n (n = 1 to 5)	V_{CLn}	−	V_{CLn} − 0.050	V_{CLn}	V_{CLn} + 0.050	V	1
Overdischarge detection voltage n (n = 1 to 5)	V_{DLn}	−	V_{DLn} − 0.080	V_{DLn}	V_{DLn} + 0.080	V	1
Overdischarge release voltage n (n = 1 to 5)	V_{DUn}	−	V_{DUn} − 0.100	V_{DUn}	V_{DUn} + 0.100	V	1
Discharge overcurrent 1 detection voltage	V_{DIOV1}	−	V_{DIOV1} − 0.010	V_{DIOV1}	V_{DIOV1} + 0.010	V	1
Discharge overcurrent 2 detection voltage	V_{DIOV2}	−	V_{DIOV2} − 0.015	V_{DIOV2}	V_{DIOV2} + 0.015	V	1
Load short-circuiting detection voltage	V_{SHORT}	−	V_{SHORT} − 0.050	V_{SHORT}	V_{SHORT} + 0.050	V	1
Charge overcurrent detection voltage	V_{CIOV}	−	V_{CIOV} − 0.010	V_{CIOV}	V_{CIOV} + 0.010	V	1
Delay Time Function[*1]							
CCT pin internal resistance	R_{CCT}	V1 = V_{CU} + 0.025	6.15	8.31	10.20	MΩ	1
CDT pin internal resistance	R_{CDT}	V1 = V_{DL} − 0.085	615	831	1020	kΩ	1
CIT pin internal resistance	R_{CIT}	R_{CIT} = 831 kΩ	615	831	1020	kΩ	1
		R_{CIT} = 8.31 MΩ	6.15	8.31	10.20	MΩ	1
CIT2 pin internal resistance	R_{CIT2}	−	123	166	204	kΩ	1
CICT pin internal resistance	R_{CICT}	−	123	166	204	kΩ	1
CCT pin detection voltage	V_{CCT}	V1 = V_{CU} + 0.025	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	1
CDT pin detection voltage	V_{CDT}	V1 = V_{DL} − 0.085	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	1
CIT pin detection voltage	V_{CIT}	−	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	1
CIT2 pin detection voltage	V_{CIT2}	−	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	1
CICT pin detection voltage	V_{CICT}	−	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	1
Load short-circuiting detection delay time	t_{SHORT}	Internally fixed delay time	100	300	600	μs	1
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	Fixed output voltage of DO pin and CO pin	5	−	24	V	−

***1.** Refer to "**6. Delay time setting**" in "**■ Operation**" for details of the delay time function.

Table 7 (2 / 3)

(V1 = V2 = V3 = V4 = V5 = 3.5 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Input Current							
Current consumption during operation	I_{OPE}	–	–	10	20	μA	1
Current consumption during power-down	I_{PDN}	V1 = V2 = V3 = V4 = V5 = 1.5 V	–	–	0.5	μA	1
Current consumption during power-saving	I_{PSV}	–	–	–	0.1	μA	1
VC1 pin current	I_{VC1}	–	–	0.25	0.50	μA	1
VC2 pin current	I_{VC2}	–	−0.8	0.0	0.8	μA	1
VC3 pin current	I_{VC3}	–	−0.8	0.0	0.8	μA	1
VC4 pin current	I_{VC4}	–	−0.8	0.0	0.8	μA	1
VC5 pin current	I_{VC5}	–	−0.8	0.0	0.8	μA	1
Internal Resistance							
Resistance between VM pin and VDD pin	R_{VMD}	V1 = V2 = V3 = V4 = V5 = 1.5 V	1.35	2.70	5.40	MΩ	1
Resistance between VM pin and VSS pin	R_{VMS}	–	7.5	15.0	30.0	kΩ	1
Output Pin							
CO pin voltage "H"*1	V_{COH}	$V_{COH} < V_{DS}$	11.0	13.0	15.0	V	1
DO pin voltage "H"*2	V_{DOH}	$V_{DOH} < V_{DS}$	11.0	13.0	15.0	V	1
CO pin source current	I_{COH}	–	10	–	–	μA	1
CO pin leakage current	I_{COL}	V1 = V2 = V3 = V4 = V5 = 5.6 V	–	–	0.1	μA	1
DO pin source current	I_{DOH}	–	10	–	–	μA	1
DO pin sink current	I_{DOL}	–	10	–	–	μA	1
PSO pin source current	I_{PSOH}	–	10	–	–	μA	1
PSO pin sink current	I_{PSOL}	V1 = V2 = V3 = V4 = V5 = 1.9 V	10	–	–	μA	1
0 V Battery Charge Function							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge function "available", V1 = V2 = V3 = V4 = V5 = 0 V	–	0.8	1.5	V	1
0 V battery charge inhibition battery voltage n (n = 1 to 5)	V_{0INHn}	0 V battery charge function "unavailable"	1.0	1.3	1.5	V	1

***1.** When $V_{COH} \geq V_{DS}$, $V_{COH} = V_{DD}$
***2.** When $V_{DOH} \geq V_{DS}$, $V_{DOH} = V_{DD}$

Remark V_{DS}: Input voltage between the VDD pin and VSS pin (V1 + V2 + V3 + V4 + V5)

Table 7 (3 / 3)

(V1 = V2 = V3 = V4 = V5 = 3.5 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Control Pin							
SEL1 pin voltage "H"	V_{SEL1H}	–	V_{DS} × 0.95	–	–	V	–
SEL2 pin voltage "H"	V_{SEL2H}	–	V_{DS} × 0.95	–	–	V	–
SEL1 pin voltage "L"	V_{SEL1L}	–	–	–	V_{DS} × 0.05	V	–
SEL2 pin voltage "L"	V_{SEL2L}	–	–	–	V_{DS} × 0.05	V	–
CTLC pin reverse voltage	V_{CTLC}	–	0.1	0.7	2.0	V	1
CTLD pin reverse voltage	V_{CTLD}	–	0.1	0.7	2.0	V	1
PSI pin reverse voltage	V_{PSI}	–	0.1	4.0	8.0	V	1
CTLC pin response delay time	t_{CTLC}	–	0.275	0.500	0.725	ms	1
CTLD pin response delay time	t_{CTLD}	–	0.275	0.500	0.725	ms	1
PSI pin response delay time	t_{PSI}	–	0.3	0.9	3.0	ms	1
CTLC pin curent "H"	I_{CTLCH}	–	−0.1	0.0	0.1	μA	1
CTLC pin curent "L"	I_{CTLCL}	–	−0.45	−0.20	−0.05	μA	1
CTLD pin curent "H"	I_{CTLDH}	–	−0.1	0.0	0.1	μA	1
CTLD pin curent "L"	I_{CTLDL}	–	−0.45	−0.20	−0.05	μA	1
PSI pin curent "H"	I_{PSIH}	–	0.0	0.2	0.4	μA	1
PSI pin curent "L"	I_{PSIL}	–	−0.1	0.0	0.1	μA	1
CTLC pin reverse voltage during communication	V_{CTLC_C}	5.1 MΩ resistance connected to the CTLC pin	V_{DS} + 0.2	V_{DS} + 0.7	V_{DS} + 1.3	V	3
CTLD pin reverse voltage during communication	V_{CTLD_C}	5.1 MΩ resistance connected to the CTLD pin	V_{DS} + 0.2	V_{DS} + 0.7	V_{DS} + 1.3	V	3
PSI pin reverse voltage during communication	V_{PSI_C}	5.1 MΩ resistance connected to the PSI pin	V_{SS} − 1.9	V_{SS} − 1.0	V_{SS} − 0.3	V	3
Temperature Detection Function							
Output voltage for temperature detection	V_{REG}	Voltage between VDD pin and VREG pin	4.0	5.0	6.0	V	2
High temperature detection ratio during charging	r_{THCH}	$r_{THCH} = (V_{REG} - V_{TH}) / V_{REG}$	r_{THCH} − 0.005	r_{THCH}	r_{THCH} + 0.005	–	2
Low temperature detection ratio during charging	r_{THCL}	$r_{THCL} = (V_{REG} - V_{TH}) / V_{REG}$	r_{THCL} − 0.005	r_{THCL}	r_{THCL} + 0.005	–	2
High temperature detection ratio during discharging	r_{THDH}	$r_{THDH} = (V_{REG} - V_{TH}) / V_{REG}$	r_{THDH} − 0.005	r_{THDH}	r_{THDH} + 0.005	–	2
Low temperature detection ratio during discharging	r_{THDL}	$r_{THDL} = (V_{REG} - V_{TH}) / V_{REG}$	r_{THDL} − 0.005	r_{THDL}	r_{THDL} + 0.005	–	2
Charge-discharge discriminating voltage	V_{CHG}	–	−0.03	−0.02	−0.01	V	2
Temperature detection delay time	t_{TH}	–	1.0	2.0	3.0	s	2

■ Test Circuits

Unless otherwise specified, for the CO pin output voltage (V_{CO}), DO pin output voltage (V_{DO}), and PSO pin output voltage (V_{PSO}), "L" or "H" is judged as follows.

L : $[V_{CO}, V_{DO}, V_{PSO}] \leq V_{DS} \times 0.1$ V
H : $[V_{CO}, V_{DO}, V_{PSO}] > V_{DS} \times 0.1$ V

Remark V_{DS}: Input voltage between the VDD pin and VSS pin (V1 + V2 + V3 + V4 + V5)

1. Test circuit 1

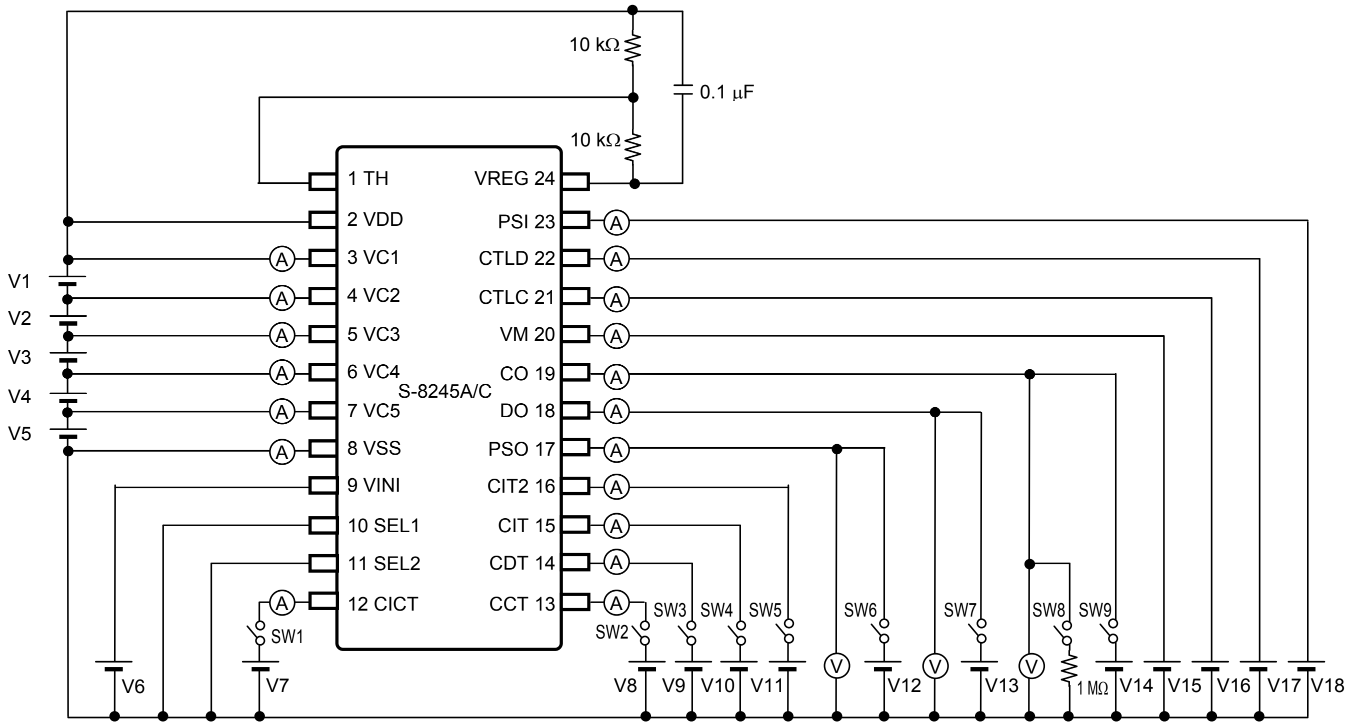


Figure 3 Test Circuit 1

This section provides explanations of Test items using Test circuit 1.
Perform each test after setting as shown in **Table 8**.

Table 8 Initial Setting of Test Circuit 1 (1 / 2)

V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14
3.5 V	3.5 V	3.5 V	3.5 V	3.5 V	0 V	–	–	–	–	–	–	–	–

Table 8 Initial Setting of Test Circuit 1 (2 / 2)

V15	V16	V17	V18	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9
0 V	0 V	0 V	V_{DS}	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF

1. 1 Overcharge detection voltage n (V_{CUn}), overcharge release voltage n (V_{CLn})

When the voltage V1 is gradually increased after setting V1 = V2 = V3 = V4 = V5 = $V_{CUn} - 0.05$ V and V_{CO} changes from "H" to "L", V1 is defined as the overcharge detection voltage 1 (V_{CU1}). When the voltage V1 is then gradually decreased after setting V2 = V3 = V4 = V5 = 3.5 V and V15 = −5 mV and V_{CO} changes from "L" to "H", V1 is defined as the overcharge release voltage 1 (V_{CL1}).
Overcharge detection voltage n (V_{CUn}) and overcharge release voltage n (V_{CLn}) (n = 2 to 5) can be determined in the same way as when n = 1.

1. 2 Overdischarge detection voltage n (V_{DLn}), overdischarge release voltage n (V_{DUn})

When the voltage V1 is gradually decreased and V_{DO} changes from "H" to "L", V1 is defined as the overdischarge detection voltage 1 (V_{DL1}). When the voltage V1 is then gradually increased after setting V15 = 0.1 V and V_{DO} changes from "L" to "H", V1 is defined as the overdischarge release voltage 1 (V_{DU1}).
Overdischarge detection voltage n (V_{DLn}) and overdischarge release voltage n (V_{DUn}) (n = 2 to 5) can be determined in the same way as when n = 1.

1. 3 Discharge overcurrent 1 detection voltage (V_{DIOV1})

When the voltage V6 is gradually increased and V_{DO} changes from "H" to "L", V6 is defined as the discharge overcurrent 1 detection voltage (V_{DIOV1}).

1. 4 Discharge overcurrent 2 detection voltage (V_{DIOV2})

When the voltage V6 is gradually increased after setting V10 = 0 V and SW4 to ON and V_{DO} changes from "H" to "L", V6 is defined as the discharge overcurrent 2 detection voltage (V_{DIOV2}).

1. 5 Load short-circuiting detection voltage (V_{SHORT})

When the voltage V6 is gradually increased after setting V10 = V11 = 0 V and SW4 and SW5 to ON and V_{DO} changes from "H" to "L", V6 is defined as the load short-circuiting detection voltage (V_{SHORT}).

1. 6 Charge overcurrent detection voltage (V_{CIOV})

When the voltage V6 is gradually decreased and V_{CO} changes from "H" to "L", V6 is defined as the charge overcurrent detection voltage (V_{CIOV}).

1. 7 CCT pin internal resistance (R_{CCT}), CCT pin detection voltage (V_{CCT})

The CCT pin internal resistance (R_{CCT}) is defined by $R_{CCT} = V_{DS} / I_{CCT}$ under the set conditions of V1 = $V_{CU1} + 0.025$ V after setting V8 = 0 V and setting SW2 to ON. When the voltage V8 is then gradually increased and V_{CO} changes from "H" to "L", V8 is defined as the CCT pin detection voltage (V_{CCT}).

1. 8 CDT pin internal resistance (R_{CDT}), CDT pin detection voltage (V_{CDT})

The CDT pin internal resistance (R_{CDT}) is defined by $R_{CDT} = V_{DS} / I_{CDT}$ under the set conditions of V1 = $V_{DL1} - 0.085$ V after setting V9 = 0 V and setting SW3 to ON. When the voltage V9 is then gradually increased and V_{DO} changes from "H" to "L", V9 is defined as the CDT pin detection voltage (V_{CDT}).

1. 9 CIT pin internal resistance (R_{CIT}), CIT pin detection voltage (V_{CIT})

The CIT pin internal resistance (R_{CIT}) is defined by $R_{CIT} = V_{DS} / I_{CIT}$ under the set conditions of V6 = $V_{DIOV1} + 0.015$ V after setting V10 = 0 V and setting SW4 to ON. When the voltage V10 is then gradually increased and V_{DO} changes from "H" to "L", V10 is defined as the CIT pin detection voltage (V_{CIT}).

1. 10 CIT2 pin internal resistance (R_{CIT2}), CIT2 pin detection voltage (V_{CIT2})

The CIT2 pin internal resistance (R_{CIT2}) is defined by $R_{CIT2} = V_{DS} / I_{CIT2}$ under the set conditions of V6 = $V_{DIOV2} + 0.020$ V after setting V10 = V11 = 0 V and setting SW4 and SW5 to ON. When the voltage V11 is then gradually increased and V_{DO} changes from "H" to "L", V11 is defined as the CIT2 pin detection voltage (V_{CIT2}).

1. 11 CICT pin internal resistance (R_{CICT}), CICT pin detection voltage (V_{CICT})

The CICT pin internal resistance (R_{CICT}) is defined by $R_{CICT} = V_{DS} / I_{CICT}$ under the set conditions of V6 = $V_{CIOV} - 0.015$ V after setting V7 = 0 V and setting SW1 to ON. When the voltage V7 is then gradually increased and V_{CO} changes from "H" to "L", V7 is defined as the CICT pin detection voltage (V_{CICT}).

1. 12 Load short-circuiting detection delay time (t_{SHORT})

The load short-circuiting detection delay time (t_{SHORT}) is the time period from when the voltage V6 changes to V6 = $V_{SHORT} + 0.055$ V until when V_{DO} changes from "H" to "L" after setting V10 = V11 = 0 V and setting SW4 and SW5 to ON.

1. 13 Current consumption during operation (I_{OPE})

The current consumption during operation (I_{OPE}) is I_{VSS} when SW8 is OFF.

1. 14 Current consumption during power-down (I_{PDN})

The current consumption during power-down (I_{PDN}) is I_{VSS} when V1 = V2 = V3 = V4 = V5 = 1.5 V, V15 = V_{DS} and SW8 is OFF.

1. 15 Current consumption during power-saving (I_{PSV})

The current consumption during power-saving (I_{PSV}) is I_{VSS} when V18 = 0 V and SW8 is OFF.

1. 16 Resistance between VM pin and VDD pin (R_{VMD})

The resistance between VM pin and VDD pin (R_{VMD}) is defined by $R_{VMD} = V_{DS} / I_{VM}$ when setting V1 = V2 = V3 = V4 = V5 = 1.5 V.

1. 17 Resistance between VM pin and VSS pin (R_{VMS})

The resistance between VM pin and VSS pin (R_{VMS}) is defined by R_{VMS} = V15 / I_{VM} when setting V6 = $V_{DIOV1} + 0.015$ V and V15 = 2.0 V.

1. 18 CO pin source current (I_{COH})

The CO pin source current (I_{COH}) is I_{CO} when V14 = $V_{COH} - 0.5$ V, SW8 is OFF, and SW9 is ON.

1. 19 CO pin leakage current (I_{COL})

The CO pin leakage current (I_{COL}) is I_{CO} when V1 = V2 = V3 = V4 = V5 = 5.6 V, V14 = 0 V, SW8 is OFF, and SW9 is ON.

1. 20 DO pin source current (I_{DOH})

The DO pin source current (I_{DOH}) is I_{DO} when V13 = $V_{DOH} - 0.5$ V and SW7 is ON.

1. 21 DO pin sink current (I_{DOL})

The DO pin sink current (I_{DOL}) is I_{DO} when V1 = V2 = V3 = V4 = V5 = 1.9 V, V13 = 0.5 V, and SW7 is ON.

1. 22 PSO pin source current (I_{PSOH})

The PSO pin source current (I_{PSOH}) is I_{PSO} when V18 = 0 V, V12 = $V_{DS} - 0.5$ V, and SW6 is ON.

1. 23 PSO pin sink current (I_{PSOL})

The PSO pin sink current (I_{PSOL}) is I_{PSO} when V12 = 0.5 V and SW6 is ON.

1. 24 0 V battery charge starting charger voltage (V_{0CHA}) (0 V battery charge function "available")

When the voltage V15 is gradually decreased after setting V1 = V2 = V3 = V4 = V5 = 0 V and V_{CO} is "H", the absolute value of V15 is defined as the 0 V battery charge starting charger voltage (V_{0CHA}).

1. 25 0 V battery charge inhibition battery voltage n (V_{0INHn}) (0 V battery charge function "unavailable")

When the voltage V1 is gradually decreased and V_{CO} changes from "H" to "L", V1 is defined as the 0 V battery charge inhibition battery voltage 1 (V_{0INH1}).
0 V battery charge inhibition battery voltage n (V_{0INHn}) (n = 2 to 5) can be determined in the same way as when n = 1.

1. 26 CTLC pin reverse voltage (V_{CTLC})

When the voltage V16 is gradually increased and V_{CO} changes from "H" to "L", V16 is defined as the CTLC pin reverse voltage (V_{CTLC}).

1. 27 CTLD pin reverse voltage (V_{CTLD})

When the voltage V17 is gradually increased and V_{DO} changes from "H" to "L", V17 is defined as the CTLD pin reverse voltage (V_{CTLD}).

1. 28 PSI pin reverse voltage (V_{PSI})

When the voltage V18 is gradually decreased and V_{PSO} changes from "L" to "H", V18 is defined as the PSI pin reverse voltage (V_{PSI}).

1. 29 CTLC pin response delay time (t_{CTLC})

The CTLC pin response delay time (t_{CTLC}) is the time period from when the voltage V16 changes to V16 = V_{DS} until when V_{CO} changes from "H" to "L".

1. 30 CTLD pin response delay time (t_{CTLD})

The CTLD pin response delay time (t_{CTLD}) is the time period from when the voltage V17 changes to V17 = V_{DS} until when V_{DO} changes from "H" to "L".

1. 31 PSI pin response delay time (t_{PSI})

The PSI pin response delay time (t_{PSI}) is the time period from when the voltage V18 changes to V18 = 0 V until when V_{PSO} changes from "L" to "H".

1. 32 CTLC pin current "H" (I_{CTLCH}), CTLC pin current "L" (I_{CTLCL})

The CTLC pin current "H" (I_{CTLCH}) is I_{CTLC} when V16 = V_{DS}.
The CTLC pin current "L" (I_{CTLCL}) is I_{CTLC} when V16 = 0 V.

1. 33 CTLD pin current "H" (I_{CTLDH}), CTLD pin current "L" (I_{CTLDL})

The CTLD pin current "H" (I_{CTLDH}) is I_{CTLD} when V17 = V_{DS}.
The CTLD pin current "L" (I_{CTLDL}) is I_{CTLD} when V17 = 0 V.

1. 34 PSI pin current "H" (I_{PSIH}), PSI pin current "L" (I_{PSIL})

The PSI pin current "H" (I_{PSIH}) is I_{PSI} when V18 = V_{DS}.
The PSI pin current "L" (I_{PSIL}) is I_{PSI} when V18 = 0 V.

2. Test circuit 2

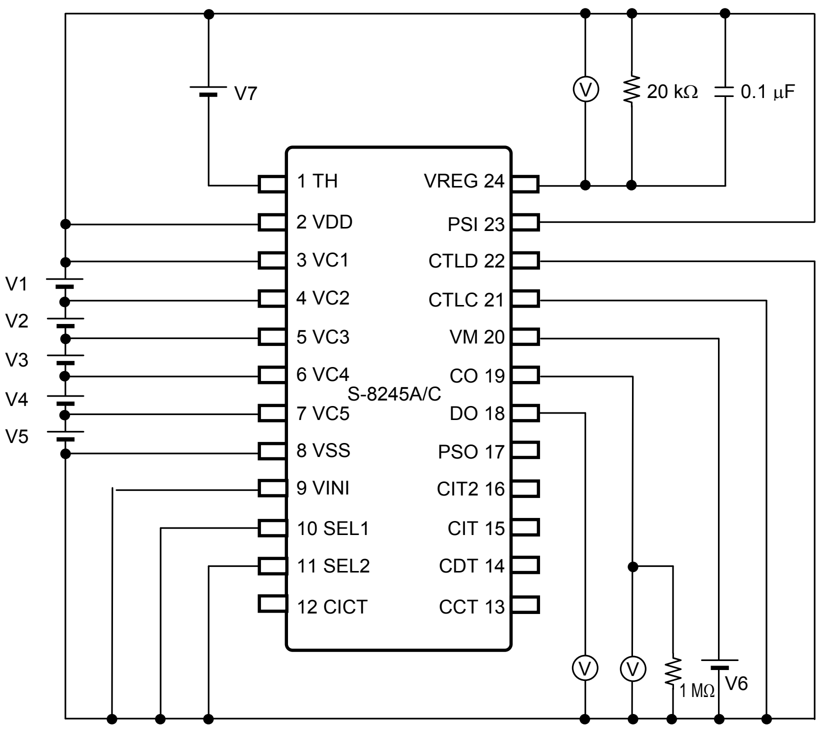


Figure 4 Test Circuit 2

This section provides explanations of Test items using Test circuit 2.
Perform each test after setting as shown in **Table 9**.

Table 9 Initial Setting of Test Circuit 2

V1	V2	V3	V4	V5	V6	V7*1
3.5 V	3.5 V	3.5 V	3.5 V	3.5 V	0 V	2.5 V

***1.** V7 is an absolute value.

2. 1 Output voltage for temperature detection (V_{REG})

The maximum voltage between the VDD pin and VREG pin is defined as the output voltage for temperature detection (V_{REG}).

2. 2 High temperature detection ratio during charging (r_{THCH})

When the voltage V7 is gradually decreased after setting V6 = −0.03 V and V_{CO} changes from "H" to "L" and V_{DO} changes from "H" to "L", the high temperature detection ratio during charging (r_{THCH}) is defined by (V_{REG} − V7) / V_{REG}.

2. 3 Low temperature detection ratio during charging (r_{THCL})

When the voltage V7 is gradually increased after setting V6 = −0.03 V and V_{CO} changes from "H" to "L" and V_{DO} changes from "H" to "L", the low temperature detection ratio during charging (r_{THCL}) is defined by (V_{REG} − V7) / V_{REG}.

2. 4 High temperature detection ratio during discharging (r_{THDH})

When the voltage V7 is gradually decreased and V_{CO} changes from "H" to "L" and V_{DO} changes from "H" to "L", the high temperature detection ratio during discharging (r_{THDH}) is defined by (V_{REG} − V7) / V_{REG}.

2. 5 Low temperature detection ratio during discharging (r_{THDL})

When the voltage V7 is gradually increased and V_{CO} changes from "H" to "L" and V_{DO} changes from "H" to "L", the low temperature detection ratio during discharging (r_{THDL}) is defined by (V_{REG} − V7) / V_{REG}.

2. 6 Charge-discharge discriminating voltage (V_{CHG})

When the voltage V6 is gradually decreased after setting $(1 - r_{THDH}) \times V_{REG} < V7 < (1 - r_{THCH}) \times V_{REG}$ and V_{CO} changes from "H" to "L" and V_{DO} changes from "H" to "L", V6 is defined as the charge-discharge discriminating voltage (V_{CHG}).

2. 7 Temperature detection delay time (t_{TH})

The temperature detection delay time (t_{TH}) is the time period from when the voltage V7 changes to 0 V until when V_{CO} changes from "H" to "L" and V_{DO} changes from "H" to "L".

3. Test circuit 3

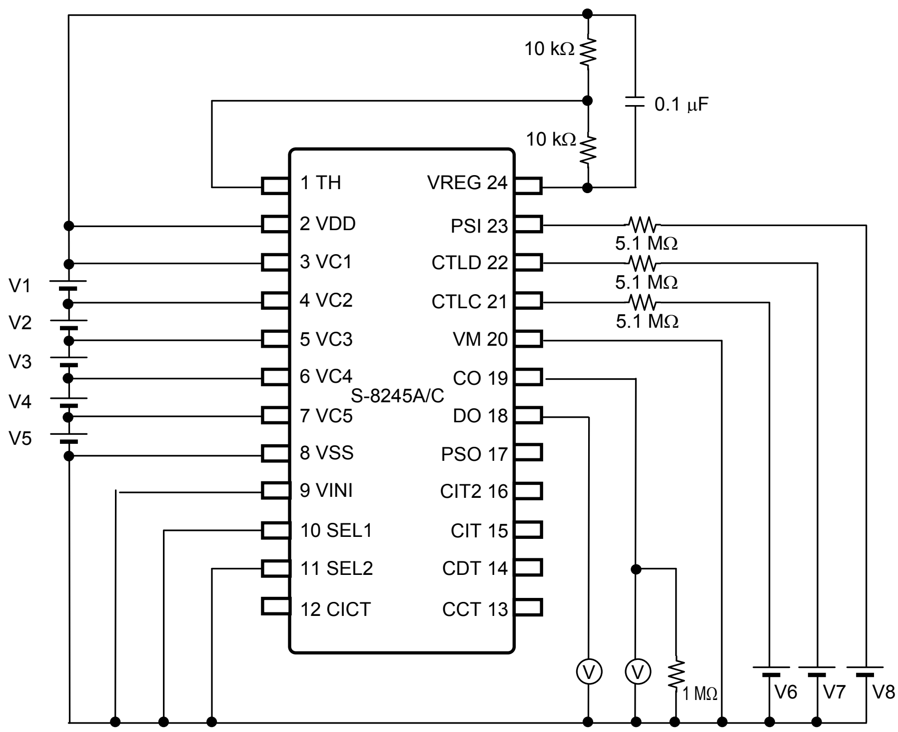


Figure 5 Test Circuit 3

This section provides explanations of Test items using Test circuit 3.
Perform each test after setting as shown in **Table 10**.

Table 10 Initial Setting of Test Circuit 3

V1	V2	V3	V4	V5	V6	V7	V8
3.5 V	3.5 V	3.5 V	3.5 V	3.5 V	V_{DS} + 2.0 V	V_{DS} + 2.0 V	−2.0 V

3. 1 CTLC pin reverse voltage during communication (V_{CTLC_C})

When the voltage V6 is gradually decreased and V_{CO} changes from "H" to "L", V6 is defined as the CTLC pin reverse voltage during communication (V_{CTLC_C}).

3. 2 CTLD pin reverse voltage during communication (V_{CTLD_C})

When the voltage V7 is gradually decreased and V_{DO} changes from "H" to "L", V7 is defined as the CTLD pin reverse voltage during communication (V_{CTLD_C}).

3. 3 PSI pin reverse voltage during communication (V_{PSI_C})

When the voltage V8 is gradually increased and V_{PSO} changes from "L" to "H", V8 is defined as the PSI pin reverse voltage during communication (V_{PSI_C}).

■ Operation

Remark Refer to "**■ Connection Examples of Battery Protection IC**".

1. Normal status

The status when the CO pin output voltage (V_{CO}) = "H", DO pin output voltage (V_{DO}) = "H", and PSO pin output voltage (V_{PSO}) = "L" is the normal status.
All the conditions mentioned below should be satisfied for returning to the normal status.

- The voltage of each of the batteries is in the range from the overcharge detection voltage n (V_{CUn}) to overdischarge detection voltage n (V_{DLn}).
- The VINI pin voltage is in the range of the charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent 1 detection voltage (V_{DIOV1}).
- The CTLC pin voltage and CTLD pin voltage are lower than the CTLC pin reverse voltage (V_{CTLC}) and CTLD pin reverse voltage (V_{CTLD}), respectively, and the PSI pin voltage is higher than the PSI pin reverse voltage (V_{PSI}).
- Either (1) or (2) below is satisfied for the TH pin voltage (V_{TH}).

(1) When $V_{VM} \leq V_{CHG}$: $(1 - r_{THCH}) \times V_{REG} < V_{TH} < (1 - r_{THCL}) \times V_{REG}$
(2) When $V_{VM} > V_{CHG}$: $(1 - r_{THDH}) \times V_{REG} < V_{TH} < (1 - r_{THDL}) \times V_{REG}$

Caution After a battery is connected, there may be cases when discharging cannot be performed. In this case, the S-8245A/C Series returns to the normal status when any of the following conditions is satisfied.

(1) Connecting a charger
(2) Shorting between the VM pin and the VSS pin
(3) Changing the PSI pin voltage to be $V_{DS} \rightarrow 0$ V $\rightarrow V_{DS}$

Remark V_{VM}: VM pin voltage
V_{CHG}: Charge-discharge discriminating voltage
r_{THCH}: High temperature detection ratio during charging
r_{THCL}: Low temperature detection ratio during charging
r_{THDH}: High temperature detection ratio during discharging
r_{THDL}: Low temperature detection ratio during discharging
V_{REG}: Output voltage for temperature detection
V_{DS}: Input voltage between the VDD pin and VSS pin (V1 + V2 + V3 + V4 + V5)

2. Overcharge status

When the voltage of any of the batteries exceeds the overcharge detection voltage n (V_{CUn}) and the status continues for the overcharge detection delay time (t_{CU})*1 or longer, the CO pin changes to high impedance. This is the overcharge status. The CO pin is pulled down to EB− by an external resistor so that the charge control FET is turned off to stop charging.

The overcharge status is released if either condition mentioned below is satisfied.

(1) $V_{VM} < V_{DS}$ / 100, and voltage of battery $\leq V_{CLn}$
(2) $V_{VM} \geq V_{DS}$ / 100, and voltage of all batteries $\leq V_{CUn}$

***1.** Refer to "**6. Delay time setting**" for details.

Remark V_{VM}: VM pin voltage
V_{DS}: Input voltage between the VDD pin and VSS pin (V1 + V2 + V3 + V4 + V5)
V_{CUn}: Overcharge detection voltage n (n = 1 to 5)
V_{CLn}: Overcharge release voltage n (n = 1 to 5)

3. Overdischarge status

When the voltage of any of the batteries falls below the overdischarge detection voltage n (V_{DLn}) and the status continues for the overdischarge detection delay time (t_{DL})*1 or longer, the DO pin changes to the V_{SS} level. This is the overdischarge status. The discharge control FET is turned off to stop discharging.

The overdischarge status is released if either condition mentioned below is satisfied.

(1) $V_{VM} \leq V_{CHG}$, and voltage of all batteries $\geq V_{DLn}$
(2) $V_{VM} > V_{CHG}$, and voltage of battery $\geq V_{DUn}$

***1.** Refer to "**6. Delay time setting**" for details.

Remark V_{VM}: VM pin voltage
V_{CHG}: Charge-discharge discriminating voltage
V_{DLn}: Overdischarge detection voltage n (n = 1 to 5)
V_{DUn}: Overdischarge release voltage n (n = 1 to 5)

3. 1 With power-down function

When S-8245A/C Series reaches the overdischarge status, the VM pin is pulled up to the V_{DD} level by a resistance between VM pin and VDD pin (R_{VMD}). If the voltage difference between the VDD pin and the VM pin decreases to 1.0 V typ. or lower, the power-down function starts to operate and most operations in the S-8245A/C Series halt. In this case, the CO pin changes to high impedance, and the PSO pin changes to the V_{DD} level.
The power-down function is released when the VM pin voltage changes to 0.7 V typ. or lower.

4. Discharge overcurrent status

When the discharge current increases to a certain value or more, the VINI pin voltage increases to the level of discharge overcurrent 1 detection voltage (V_{DIOV1}) or higher. If the status continues for the discharge overcurrent 1 detection delay time (t_{DIOV1})*1 or longer, the DO pin changes to the V_{SS} level. This is the discharge overcurrent status. The discharge control FET is turned off to stop discharging. The VM pin is pulled down to the V_{SS} level by resistance between VM pin and VSS pin (R_{VMS}).
Discharge overcurrent is detected at the following three levels: V_{DIOV1}, V_{DIOV2}, and V_{SHORT}. When discharge overcurrent 2 detection voltage (V_{DIOV2}) and load short-circuiting detection voltage (V_{SHORT}) are detected, the same operations as V_{DIOV1} detection are performed.

The discharge overcurrent status is released if the following conditions are satisfied.

- S-8245A Series: $V_{VM} \leq V_{DS}$ / 4 typ.
- S-8245C Series: $V_{VM} \leq V_{DS}$ / 5 typ.

***1.** Refer to "**6. Delay time setting**" for details.

Remark V_{VM}: VM pin voltage
V_{DS}: Input voltage between the VDD pin and VSS pin (V1 + V2 + V3 + V4 + V5)

5. Charge overcurrent status

When the charge current increases to a certain value or more, the VINI pin voltage decreases to the level of charge overcurrent detection voltage (V_{CIOV}) or lower. If the status continues for the charge overcurrent detection delay time (t_{CIOV})*1 or longer, the CO pin changes to high impedance. This is the charge overcurrent status. The charge control FET is turned off to stop charging.

The charge overcurrent status is released if $V_{VM} \geq V_{DS}$ / 100 typ.

***1.** Refer to "**6. Delay time setting**" for details.

Remark V_{VM}: VM pin voltage
V_{DS}: Input voltage between the VDD pin and VSS pin (V1 + V2 + V3 + V4 + V5)

6. Delay time setting

Users are able to set delay time for the period from when the S-8245A/C Series detects change in the voltage of any of the batteries or the VINI pin until when it outputs to the CO pin or DO pin. Each delay time is determined by a resistor in the S-8245A/C Series and an external capacitor.
In the overchage detection, when the voltage of any of the batteries exceeds overcharge detection voltage n (V_{CUn}), the S-8245A/C Series starts charging to the CCT pin's capacitor (C_{CCT}) via the CCT pin internal resistance (R_{CCT}). After a certain period, the CO pin changes to high impedance when the CCT pin reaches the CCT pin detection voltage (V_{CCT}). This period is overcharge detection delay time (t_{CU}).

t_{CU} is calculated using the following equation.

$$t_{CU}\ [s] = -\ln(1 - V_{CCT} / V_{DS}) \times C_{CCT}\ [\mu F] \times R_{CCT}\ [M\Omega]$$
$$= -\ln(1 - 0.7\ \text{typ.}) \times C_{CCT}\ [\mu F] \times 8.31\ [M\Omega]\ \text{typ.}$$
$$= 10.0\ [M\Omega]\ \text{typ.} \times C_{CCT}\ [\mu F]$$

Overdischarge detection delay time (t_{DL}), discharge overcurrent 1 detection delay time (t_{DIOV1}), discharge overcurrent 2 detection delay time (t_{DIOV2}) and charge overcurrent detection delay time (t_{CIOV}) are calculated using the following equations as well.

$$t_{DL}\ [ms] = -\ln(1 - V_{CDT} / V_{DS}) \times C_{CDT}\ [\mu F] \times R_{CDT}\ [k\Omega]$$
$$t_{DIOV1}\ [ms] = -\ln(1 - V_{CIT} / V_{DS}) \times C_{CIT}\ [\mu F] \times R_{CIT}\ [k\Omega]$$
$$t_{DIOV2}\ [ms] = -\ln(1 - V_{CIT2} / V_{DS}) \times C_{CIT2}\ [\mu F] \times R_{CIT2}\ [k\Omega]$$
$$t_{CIOV}\ [ms] = -\ln(1 - V_{CICT} / V_{DS}) \times C_{CICT}\ [\mu F] \times R_{CICT}\ [k\Omega]$$

When $C_{CCT} = C_{CDT} = C_{CIT} = C_{CIT2} = C_{CICT} = 0.1\ [\mu F]$, each delay time is calculated as follows.

t_{CU} [s] = 10.0 [MΩ] typ. × 0.1 [μF] = 1.0 [s] typ.
t_{DL} [ms] = 1000 [kΩ] typ. × 0.1 [μF] = 100 [ms] typ.
t_{DIOV1} [ms] = 1000 [kΩ] typ. × 0.1 [μF] = 100 [ms] typ. (when R_{CIT} = 831 kΩ typ.)
t_{DIOV1} [ms] = 10.0 [MΩ] typ. × 0.1 [μF] = 1.0 [s] typ. (when R_{CIT} = 8.31 MΩ typ.)
t_{DIOV2} [ms] = 200 [kΩ] typ. × 0.1 [μF] = 20 [ms] typ.
t_{CIOV} [ms] = 200 [kΩ] typ. × 0.1 [μF] = 20 [ms] typ.

Load short-circuiting detection delay time (t_{SHORT}) is fixed internally.

Remark V_{DS}: Input voltage between the VDD pin and VSS pin (V1 + V2 + V3 + V4 + V5)

7. 0 V Battery charge function

Regarding how to charge a self-discharged battery (0 V battery), users are able to select either function mentioned below.

(1) 0 V battery charge function "available"
A 0 V battery is charged when charger voltage is higher than V_{0CHA}.
(2) 0 V battery charge function "unavailable"
A 0 V battery is not charged when the voltage of any of the batteries is V_{0INHn} or lower.

Caution When the VDD pin voltage is lower than the minimum value of operation voltage between the VDD pin and VSS pin (V_{DSOP}), the S-8245A/C Series' operation is not assured.

Remark V_{0CHA}: 0 V battery charge starting charger voltage
V_{0INHn}: 0 V battery charge inhibition battery voltage n (n = 1 to 5)

8. SEL1 pin and SEL2 pin

Switching control for 3-serial to 5-serial cell is possible by inputting voltage to the SEL1 pin and the SEL2 pin.
Be sure to use the SEL1 pin and the SEL2 pin at the "H" or "L" level.

Table 11 Settings of SEL1 Pin and SEL2 Pin

SEL1 Pin	SEL2 Pin	Setting
"L"	"L"	5-serial cell
"L"	"H"	4-serial cell
"H"	"L"	3-serial cell
"H"	"H"	Setting inhibited

Remark "H" is the status when $V_{SEL1} \geq V_{SEL1H}$, $V_{SEL2} \geq V_{SEL2H}$, and "L" is the status when $V_{SEL1} \leq V_{SEL1L}$, $V_{SEL2} \leq V_{SEL2L}$.

V_{SEL1H}: SEL1 pin voltage "H"
V_{SEL2H}: SEL2 pin voltage "H"
V_{SEL1L}: SEL1 pin voltage "L"
V_{SEL2L}: SEL2 pin voltage "L"

9. CTLC pin and CTLD pin

The CTLC pin controls the CO pin, and the CTLD pin controls the DO pin. Thus it is possible for users to control the CO pin and the DO pin respectively. These controls precede the battery protection circuit.

Table 12 Status Set by CTLC Pin

CTLC Pin	CO Pin
V_{SS} level $\leq$ CTLC pin voltage $<$ V_{CTLC}	"H"
V_{CTLC} $\leq$ CTLC pin voltage $\leq$ V_{DD} level	High impedance
V_{DD} level $<$ CTLC pin voltage $\leq$ V_{CTLC_C}	High impedance
V_{CTLC_C} $<$ CTLC pin voltage	"H"

Remark The CTLC pin is at the V_{DD} level or higher in cascade connection.
Connect a resistor of 5.1 MΩ to the CTLC pin in this case.

V_{CTLC}: CTLC pin reverse voltage
V_{CTLC_C}: CTLC pin reverse voltage during communication

Table 13 Status Set by CTLD Pin

CTLD Pin	DO Pin
V_{SS} level $\leq$ CTLD pin voltage $<$ V_{CTLD}	"H"
V_{CTLD} $\leq$ CTLD pin voltage $\leq$ V_{DD} level	V_{SS} level
V_{DD} level $<$ CTLD pin voltage $\leq$ V_{CTLD_C}	V_{SS} level
V_{CTLD_C} $<$ CTLD pin voltage	"H"

Remark The CTLD pin is at the V_{DD} level or higher in cascade connection.
Connect a resistor of 5.1 MΩ to the CTLD pin in this case.

V_{CTLD}: CTLD pin reverse voltage
V_{CTLD_C}: CTLD pin reverse voltage during communication

After the DO pin reaches the V_{SS} level due to CTLD pin control, if the voltage difference between the VDD pin and the VM pin decreases to 1.0 V typ. or lower, the power-down function starts to operate.
The power-down function is released if either condition mentioned below is satisfied.

(1) $V_{VM} \leq 0.7$ V typ. (Refer to "**3. 1 With power-down function**")
(2) Changing the PSI pin voltage to be $V_{DS} \rightarrow 0\text{ V} \rightarrow V_{DS}$ (Refer to "**10. PSI pin**")

Remark V_{VM}: VM pin voltage
V_{DS}: Input voltage between the VDD pin and VSS pin (V1 + V2 + V3 + V4 + V5)

10. PSI pin

When the PSI pin is activated, the power-saving function starts to operate, and most operations halt. In this case, the CO pin changes to high impedance, DO pin changes to the V_{SS} level, and the PSO pin changes to the V_{DD} level.

Table 14 Status Set by PSI Pin

PSI Pin	CO Pin	DO Pin	PSO Pin
V_{PSI} < PSI pin voltage ≤ V_{DD} level	"H"	"H"	V_{SS} level
V_{SS} level ≤ PSI pin voltage ≤ V_{PSI}	High impedance	V_{SS} level	V_{DD} level
V_{PSI_C} < PSI pin voltage < V_{SS} level	High impedance	V_{SS} level	V_{DD} level
PSI pin voltage < V_{PSI_C}	"H"	"H"	V_{SS} level

Remark The PSI pin is at the V_{SS} level or lower in cascade connection.
Connect a resistor of 5.1 MΩ to the PSI pin in this case.

V_{PSI}: PSI pin reverse voltage
V_{PSI_C}: PSI pin reverse voltage during communication

The S-8245A/C Series is initialized and the power-saving function is released by deactivating the PSI pin. As a result, each detection operation is carried out after returning to the normal status.

11. Temperature detection

Serially connect an NTC and a low temperature-dependent resistor (R_{TH}) between the VDD pin and the VREG pin, and then connect their middle point to the TH pin. It allows for temperature detection at four different points: high temperature detection during charging, low temperature detection during charging, high temperature detection during discharging, low temperature detection during discharging.

When the temperature rises, according to the NTC temperature characteristics, the resistance (R_{NTC}) decreases, and the ratio between R_{NTC} and R_{TH} changes, and then the TH pin voltage (V_{TH}) increases.
When the temperature falls, according to the NTC temperature characteristics, the resistance (R_{NTC}) increases, and the ratio between R_{NTC} and R_{TH} changes, and then the TH pin voltage (V_{TH}) decreases.
The temperature detection during charging and temperature detection during discharging switch by comparing the VM pin voltage (V_{VM}) and charge-discharge discriminating voltage (V_{CHG}).
If the relation between R_{NTC}, R_{TH}, and V_{VM} satisfies the itemized condition in **Table 15** in each temperature detection, and each status continues for the temperature detection delay time (t_{TH}) or longer, the CO pin changes to high impedance, and the DO pin changes to the V_{SS} level. This is the temperature protection status.
If the itemized condition in **Table 15** is not satisfied in each temperature detection, and each status continues for t_{TH} or longer, the temperature protection status is released.

Table 15 Conditions for Each Temperature Detection

Item	TH Pin	VM Pin	CO Pin	DO Pin
High temperature detection during charging	$r_{THCH} \leq R_{TH} / (R_{NTC} + R_{TH})$	$V_{VM} \leq V_{CHG}$	High impedance	V_{SS} level
Low temperature detection during charging	$r_{THCL} \geq R_{TH} / (R_{NTC} + R_{TH})$	$V_{VM} \leq V_{CHG}$		
High temperature detection during discharging	$r_{THDH} \leq R_{TH} / (R_{NTC} + R_{TH})$	$V_{VM} > V_{CHG}$		
Low temperature detection during discharging	$r_{THDL} \geq R_{TH} / (R_{NTC} + R_{TH})$	$V_{VM} > V_{CHG}$		

Remark r_{THCH}: High temperature detection ratio during charging
r_{THCL}: Low temperature detection ratio during charging
r_{THDH}: High temperature detection ratio during discharging
r_{THDL}: Low temperature detection ratio during discharging

The detection temperature can be set according to the NTC and R_{TH} characteristics.
For example, if R_{NTC}[*1] and R_{TH} (10 kΩ) are connected to the S-8245AAA, each detection temperature is as follows.

Table 16

Item	Temperature Detection Ratio	R_{NTC}	Detection Temperature
Temperature for high temperature detection during charging	r_{THCH} = 0.670	4.9 kΩ	45°C
Temperature for low temperature detection during charging	r_{THCL} = 0.270	27.0 kΩ	0°C
Temperature for high temperature detection during discharging	r_{THDH} = 0.795	2.6 kΩ	65°C
Temperature for low temperature detection during discharging	r_{THDL} = 0.190	42.6 kΩ	−10°C

***1.** The calculation method for R_{NTC} is as follows.

$$
\begin{aligned}
r_{THCL} &= R_{TH} / (R_{NTC} + R_{TH}) \\
R_{NTC} &= R_{TH} / r_{THCL} - R_{TH} \\
&= 10\ \text{k}\Omega / 0.270 - 10\ \text{k}\Omega \\
&= 27.0\ \text{k}\Omega
\end{aligned}
$$

When low temperature during charging is detected, R_{NTC} = 27.0 kΩ, so detection temperature = 0°C according to the R_{NTC} characteristics shown in **Figure 6**.

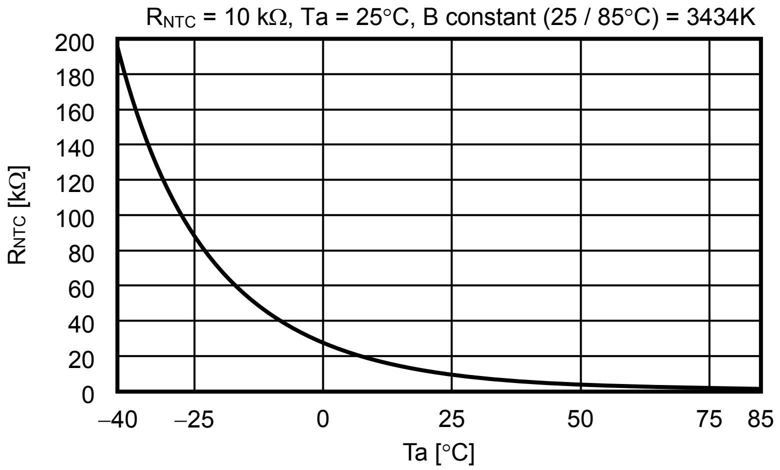
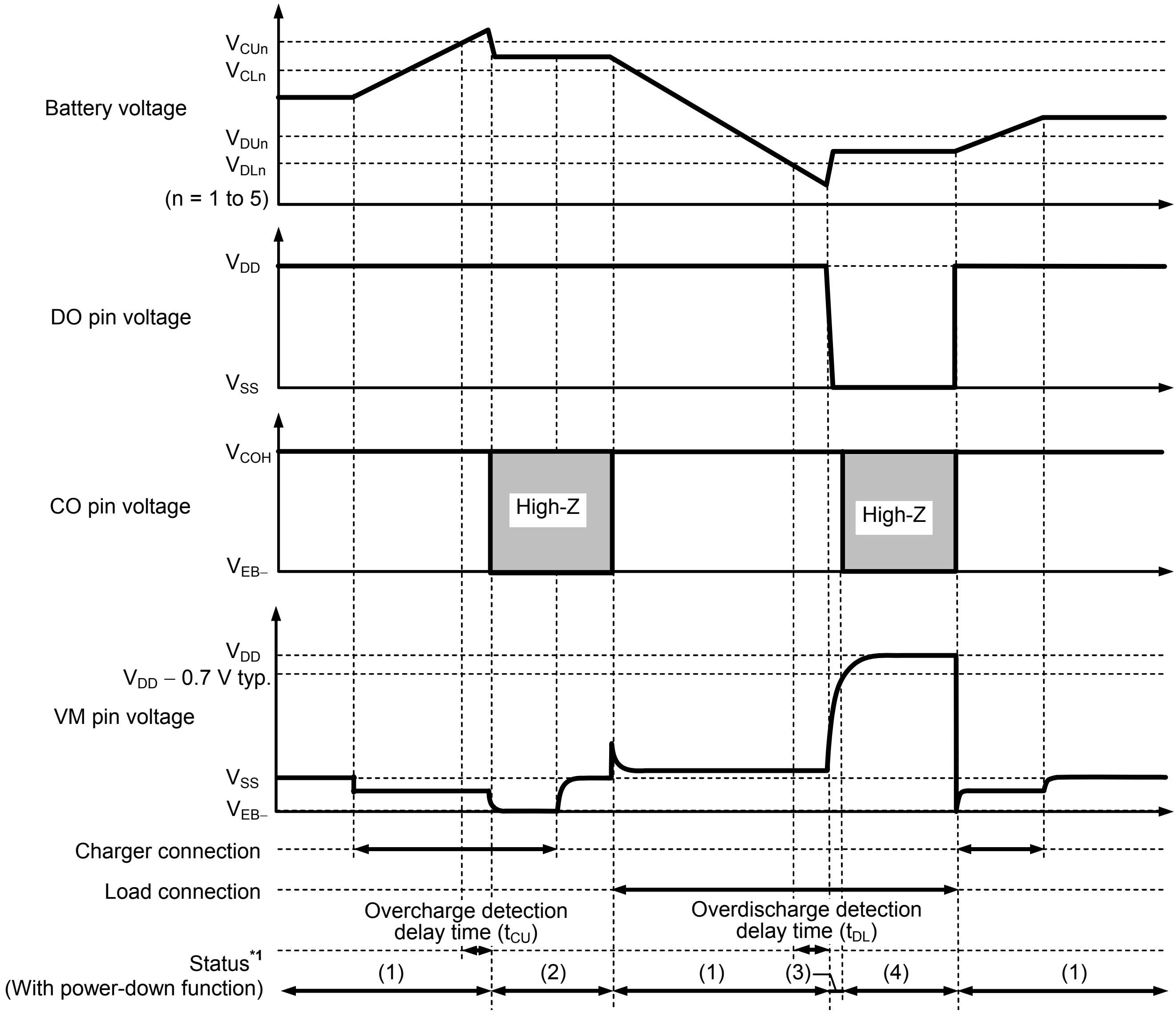


Figure 6 Example of R_{NTC} Characteristics

Remark Temperature detection is carried out intermittently for 512 ms typ. per cycle, of which 1 ms typ. is the detection operation period.
The VREG pin voltage is output only during detection operation. During other periods, the VREG pin is at the V_{DD} level.
Regarding details of intermittent operation, refer to "**4. Temperature detection (High temperature detection during charging)**" in "**■ Timing Charts**".

■ Timing Charts

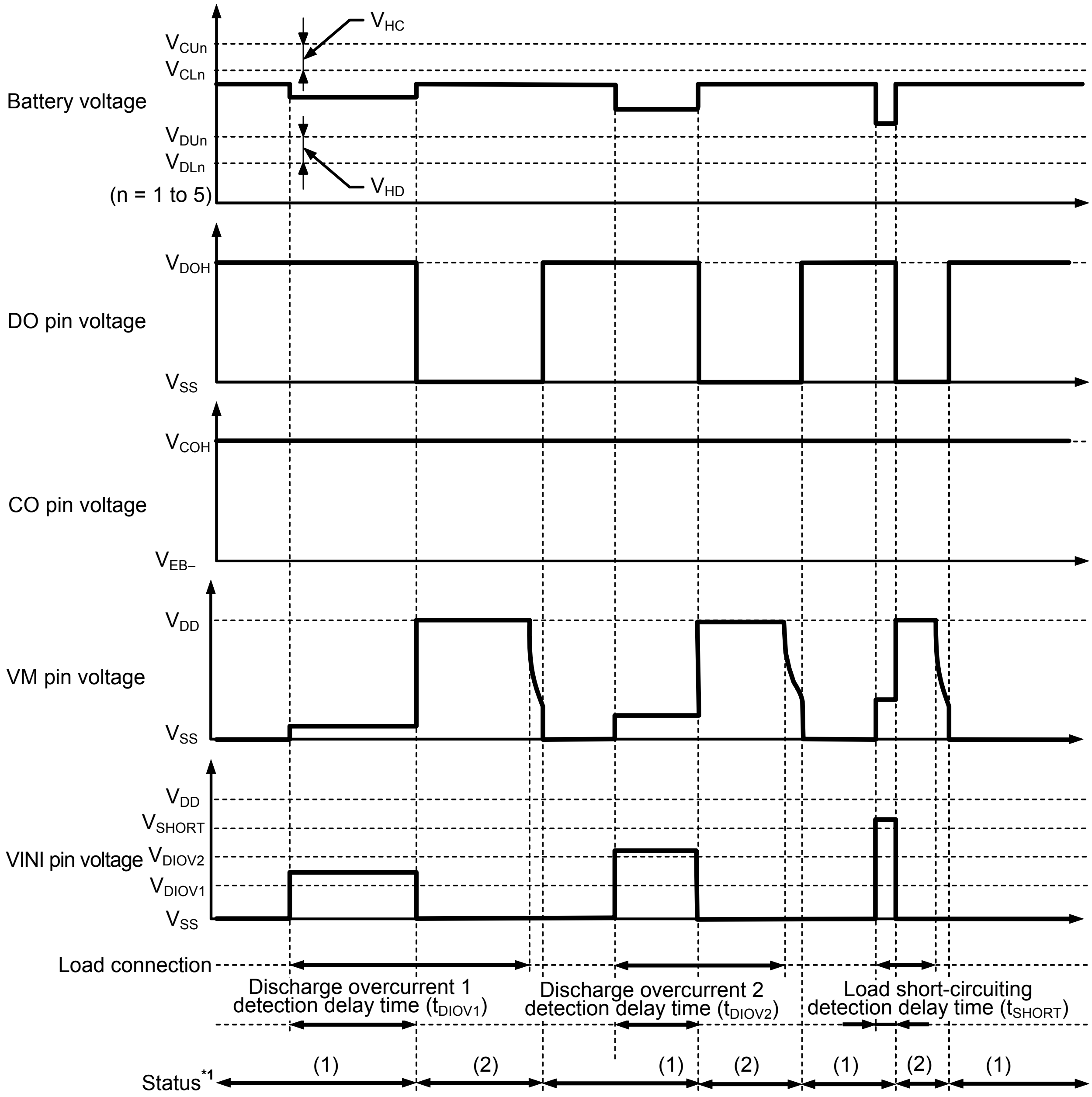
1. Overcharge detection, overdischarge detection



***1.** (1) : Normal status
(2) : Overcharge status
(3) : Overdischarge status
(4) : Power-down status

Figure 7

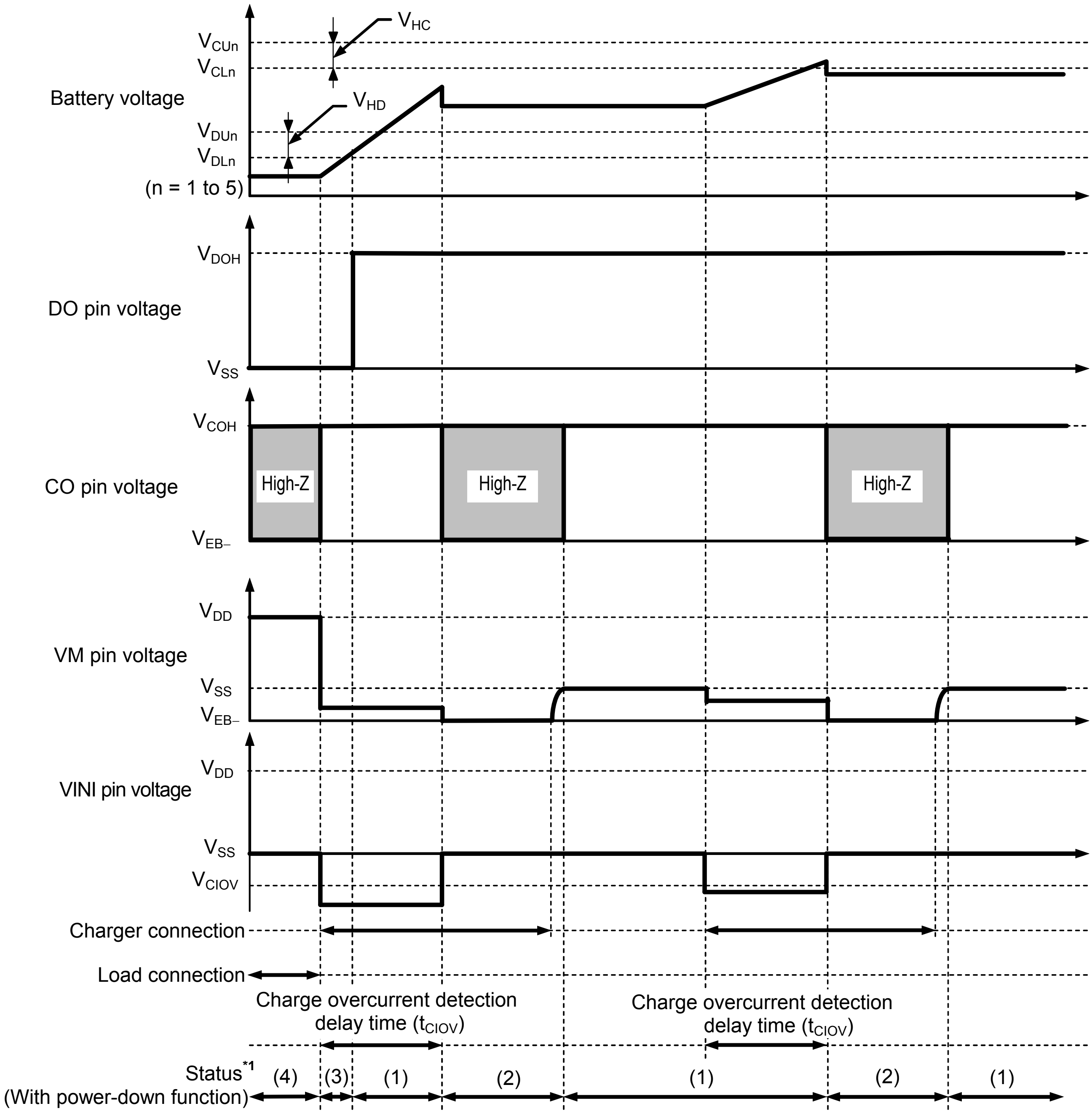
2. Discharge overcurrent detection



***1.** (1) : Normal status
(2) : Discharge overcurrent status

Figure 8

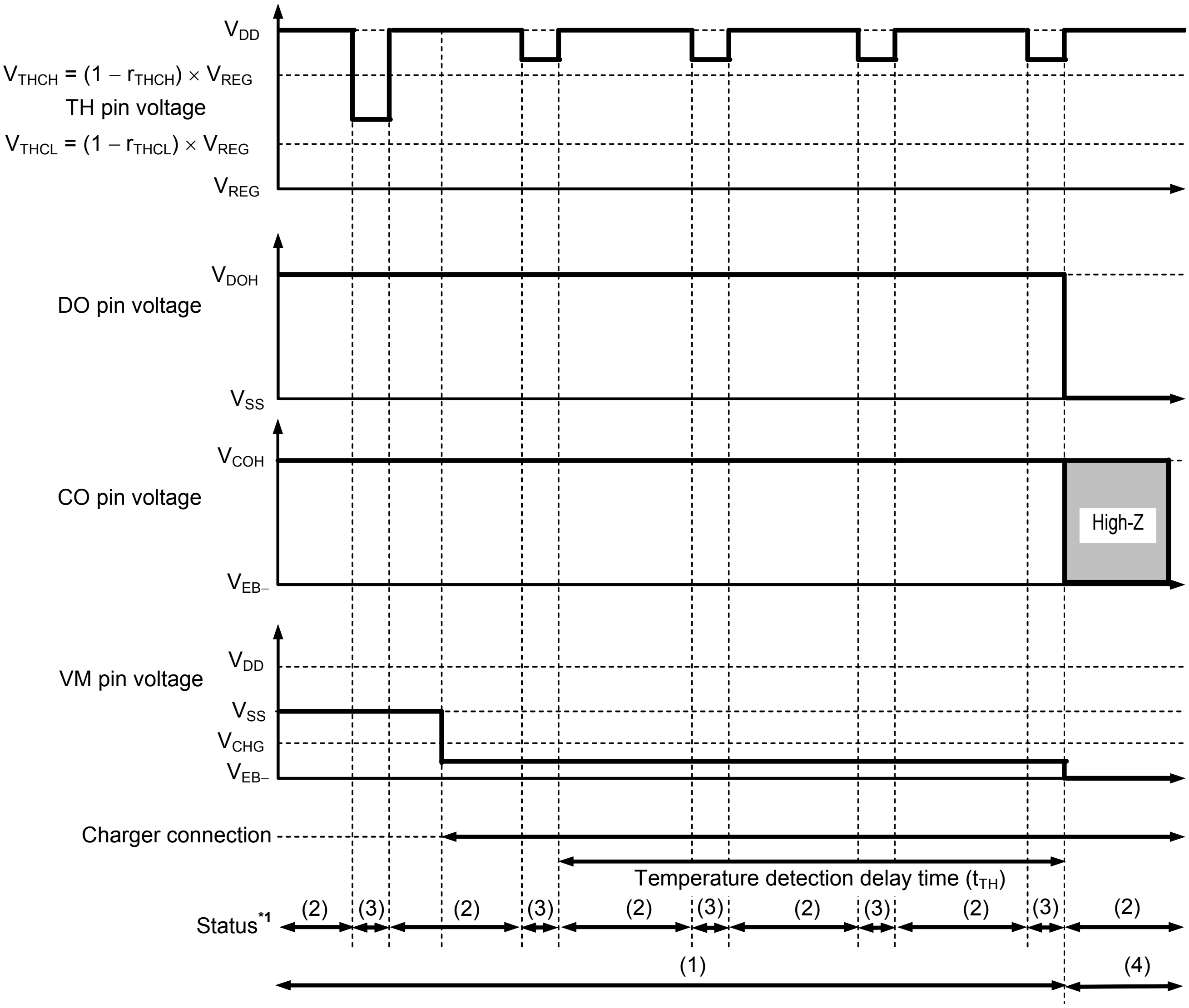
3. Charge overcurrent detection



***1.** (1) : Normal status
(2) : Charge overcurrent status
(3) : Overdischarge status
(4) : Power-down status

Figure 9

4. Temperature detection (High temperature detection during charging)

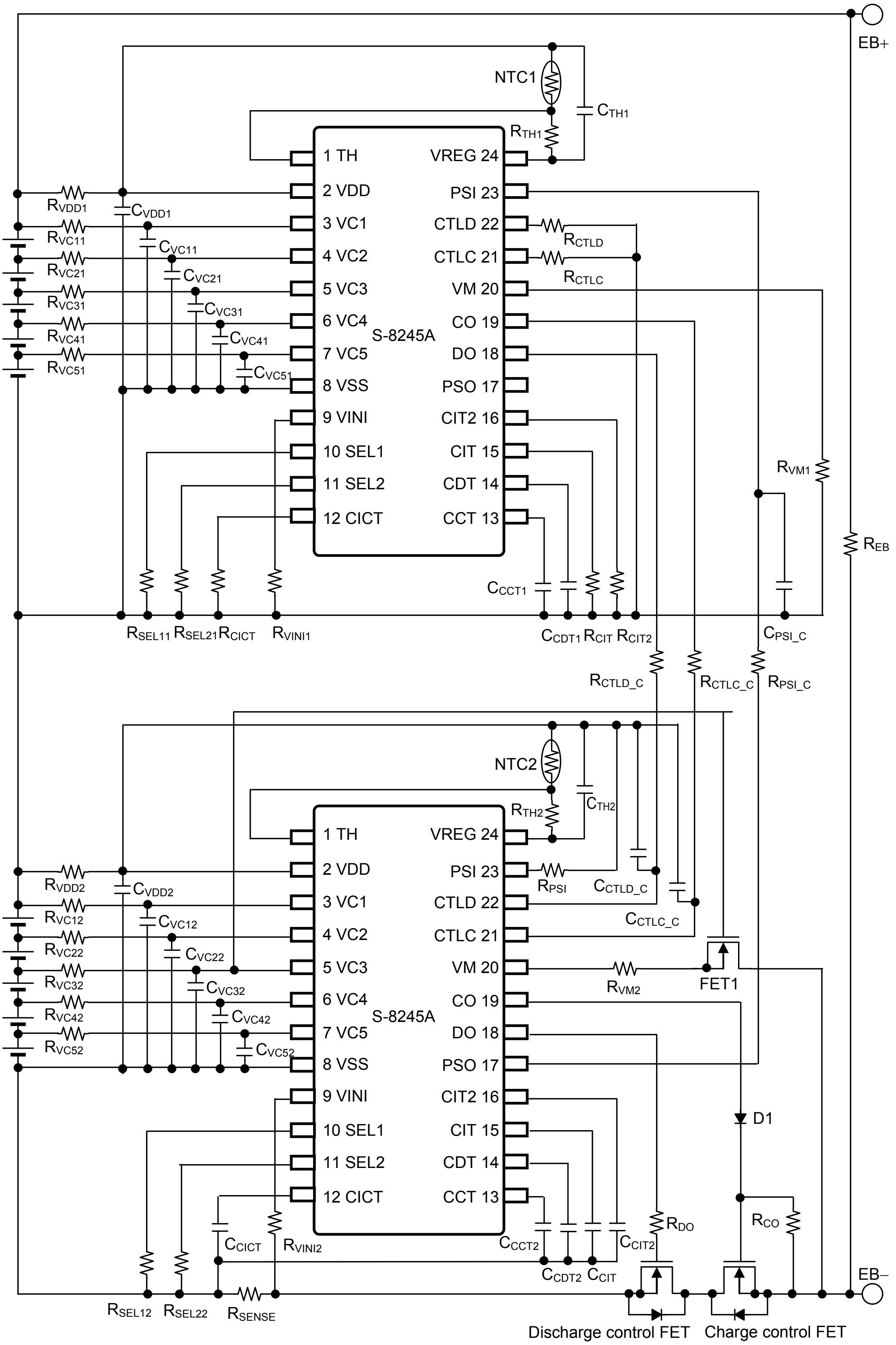


***1.** (1) : Normal status
(2) : Temperature detection sleep time
(3) : Temperature detection awake time
(4) : Temperature protection status

Figure 10

■ Connection Examples of Battery Protection IC

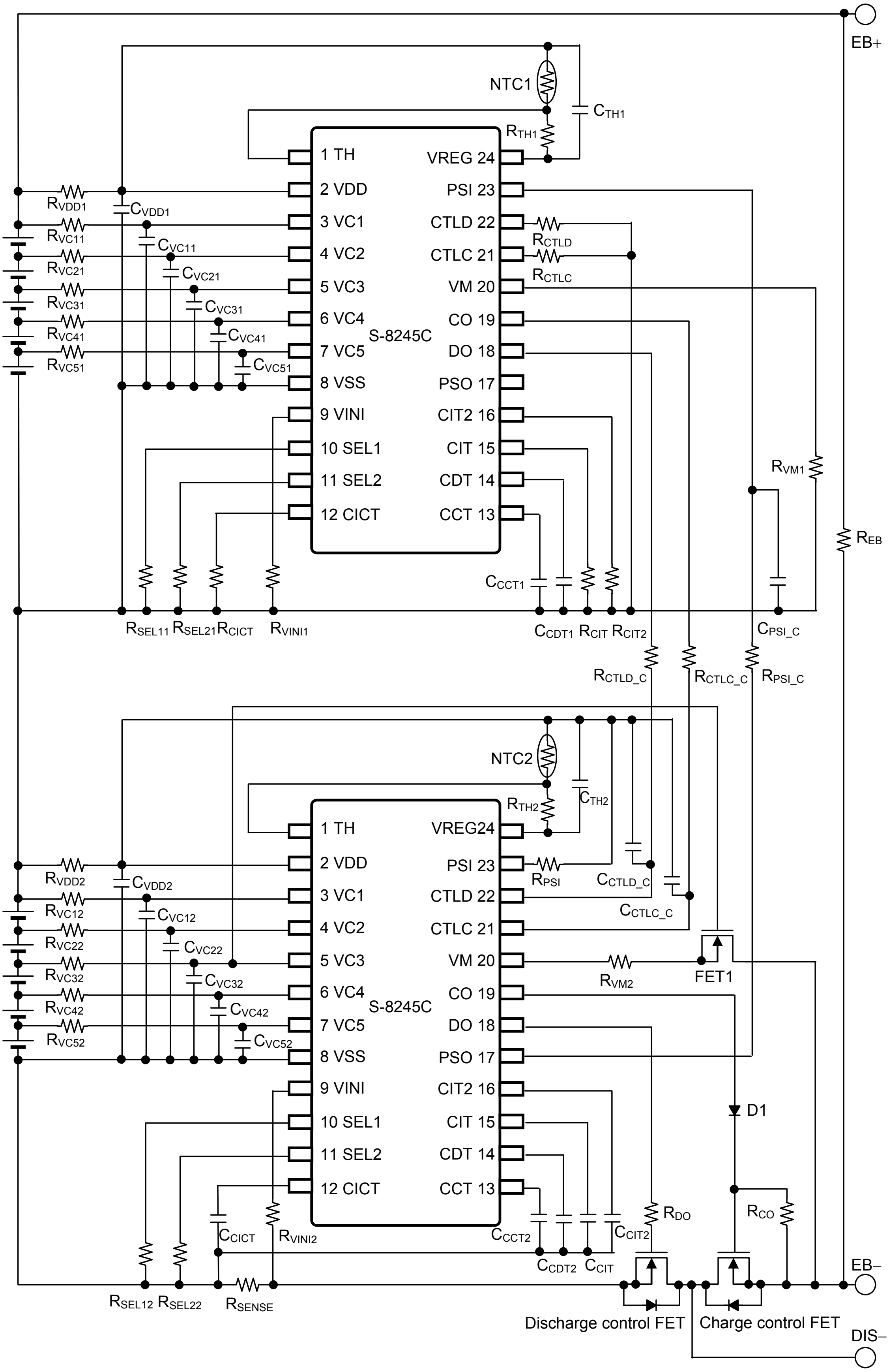
1. S-8245A Series (10-serial cell with an integrated charge and discharge path)



Remark Regarding the recommended values for external components, refer to "**Table 17 Constants for External Components**".

Figure 11

2. S-8245C Series (10-serial cell with separate charge and discharge paths)



Remark Regarding the recommended values for external components, refer to "**Table 17 Constants for External Components**".

Figure 12

Table 17 Constants for External Components

Symbol	Min.	Typ.	Max.	Unit
R_{VDD1}*1, R_{VDD2}*1	68	100	100	Ω
R_{VCn1}, R_{VCn2} (n = 1 to 5)*1	0.68	1.00	1.00	kΩ
R_{SEL11}, R_{SEL12}, R_{SEL21}, R_{SEL22}	1	1	–	kΩ
R_{VINI1}, R_{VINI2}	1.0	1.0	5.1	kΩ
R_{CTLC}, R_{CTLD}, R_{PSI}	1.0	2.0	5.1	kΩ
R_{VM1}, R_{VM2}	1.0	5.1	5.1	kΩ
R_{CTLC_C}, R_{CTLD_C}, R_{PSI_C}	4.0	5.1	6.0	MΩ
R_{CIT}, R_{CIT2}, R_{CICT}	1	1	–	kΩ
R_{CO}	1.0	5.1	–	MΩ
R_{DO}	1.0	5.1	20.0	kΩ
R_{EB}	–	10	10	MΩ
NTC1, NTC2	–	10	–	kΩ
R_{TH1}, R_{TH2}	–	10	–	kΩ
R_{SENSE}	–	–	–	mΩ
C_{VDD1}, C_{VDD2}*1	0.68	1.00	10.00	μF
C_{VCn1}, C_{VCn2} (n = 1 to 5)*1	0.068	0.100	1.000	μF
C_{CTLC_C}, C_{CTLD_C}, C_{PSI_C}	470	470	–	pF
C_{CCT1}, C_{CCT2}	0.01	0.10	–	μF
C_{CDT1}, C_{CDT2}	0.01	0.10	–	μF
C_{CIT}	0.01	0.10	–	μF
C_{CIT2}	0.01	0.10	–	μF
C_{CICT}	0.01	0.10	–	μF
C_{TH1}, C_{TH2}	0.1	0.1	0.1	μF
D1	–	–	–	–

***1.** $R_{VDD1} \times C_{VDD1} = R_{VDD2} \times C_{VDD2}$ = 100 μF • Ω is recommended.
Set filter constants to satisfy $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VC3} \times C_{VC3} = R_{VC4} \times C_{VC4} = R_{VC5} \times C_{VC5} = R_{VDD1} \times C_{VDD1}$.

Caution 1. The above constants may be changed without notice.
2. Sufficient evaluation of transient power supply fluctuation and overcurrent protection function with the actual application is needed to determine the proper constants when setting the filter constants between the VDD pin and VSS pin. Contact our sales office if setting the constants between the VDD pin and VSS pin to anything other than the recommended values.
3. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.

- Batteries can be connected in any order; however, there may be cases when discharging cannot be performed after a battery is connected. In this case, the S-8245A/C Series returns to the normal status when any of the following conditions is satisfied.

  (1) Connecting a charger
  (2) Shorting between the VM pin and the VSS pin
  (3) Changing the PSI pin voltage to be $V_{DS} \rightarrow 0$ V $\rightarrow V_{DS}$

  Remark V_{DS}: Input voltage between the VDD pin and the VSS pin (V1 + V2 + V3 + V4 + V5)

- If an overcharged battery and an overdischarged battery intermix, the S-8245A/C Series will change to the overcharge and overdischarge statuses. Therefore, in this case, both charging and discharging are impossible.

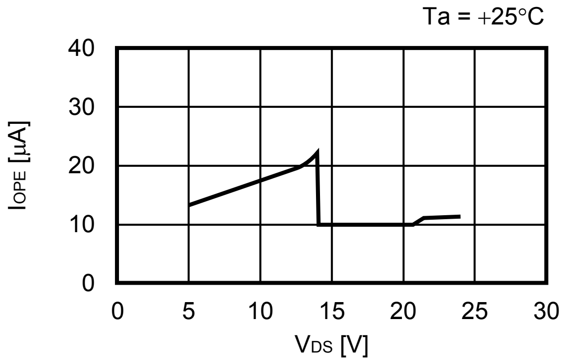
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

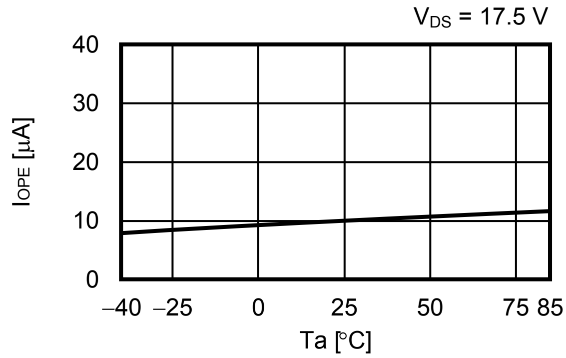
■ Characteristics (Typical Data)

1. Current consumption

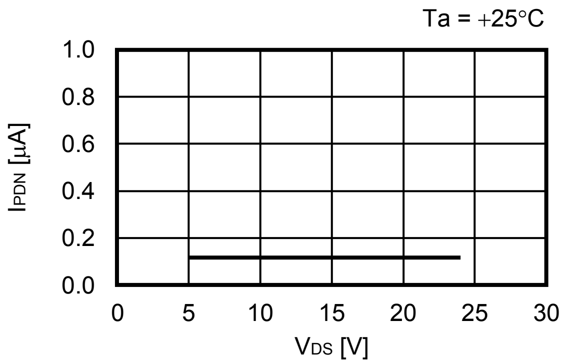
1. 1 I_{OPE} vs. V_{DS}



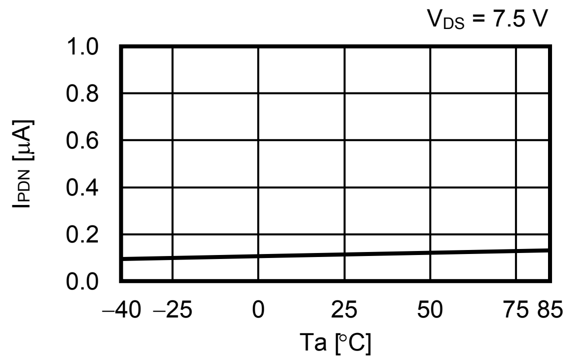
1. 2 I_{OPE} vs. Ta



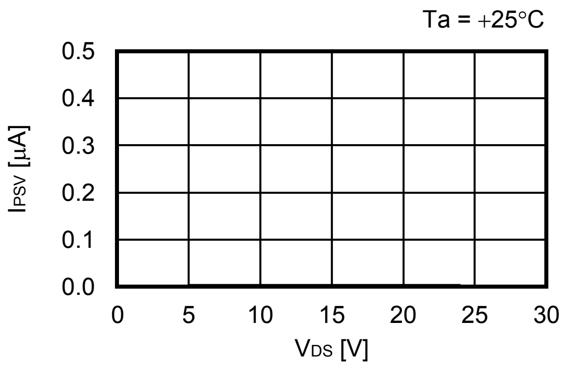
1. 3 I_{PDN} vs. V_{DS}



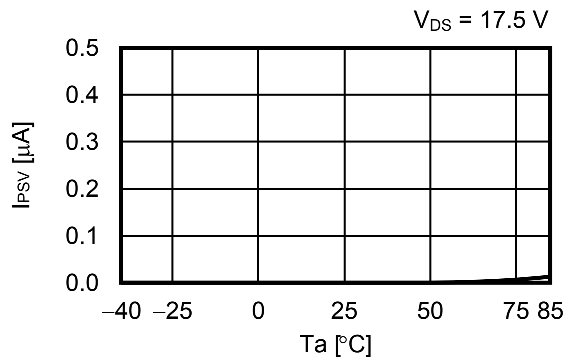
1. 4 I_{PDN} vs. Ta



1. 5 I_{PSV} vs. V_{DS}

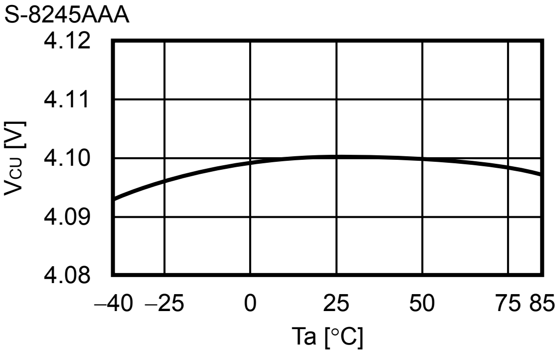


1. 6 I_{PSV} vs. Ta

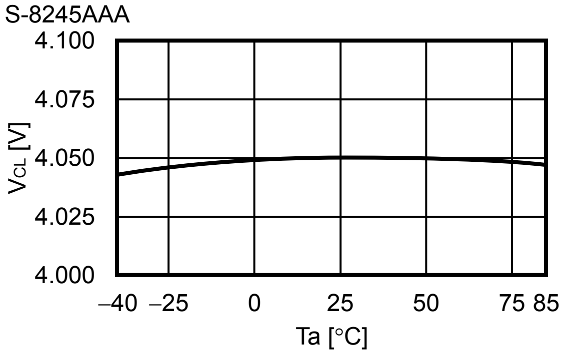


2. Detection voltage, release voltage

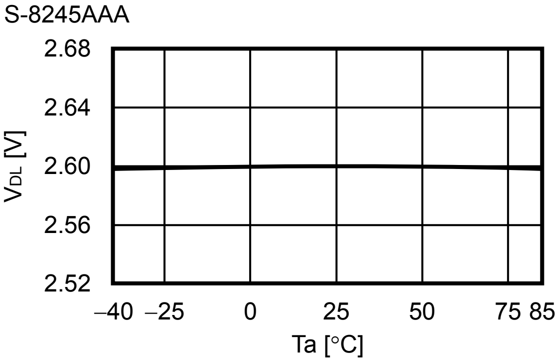
2. 1 V_{CU} vs. Ta



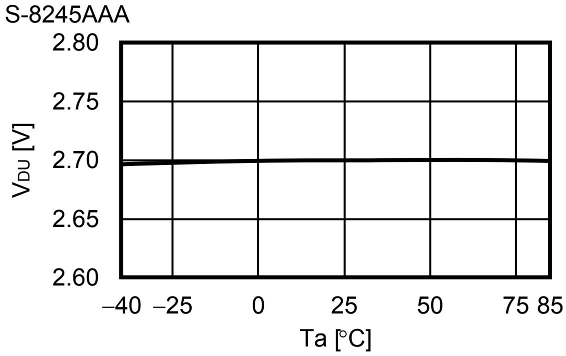
2. 2 V_{CL} vs. Ta



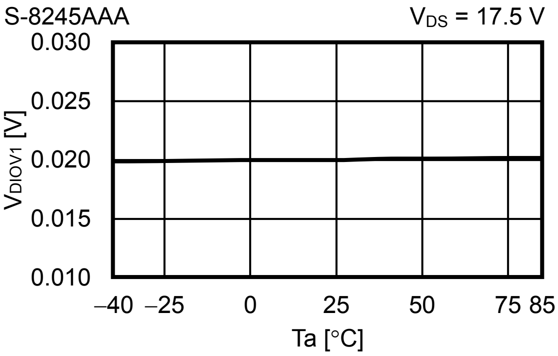
2. 3 V_{DL} vs. Ta



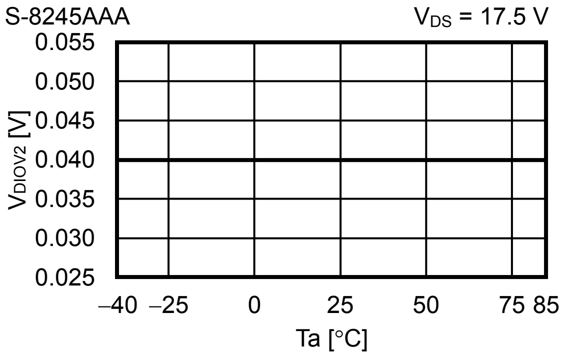
2. 4 V_{DU} vs. Ta



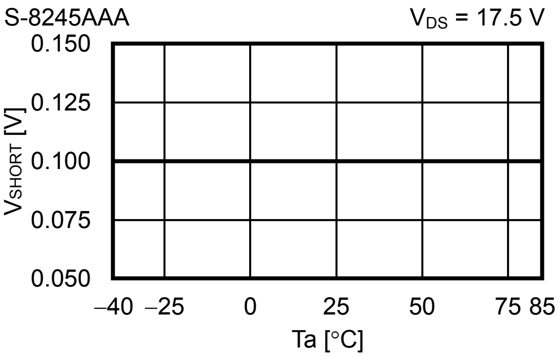
2. 5 V_{DIOV1} vs. Ta



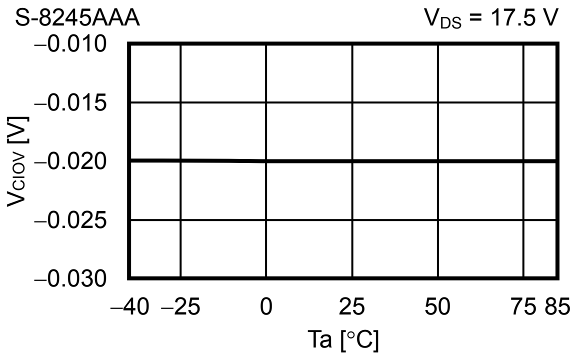
2. 6 V_{DIOV2} vs. Ta



2. 7 V_{SHORT} vs. Ta

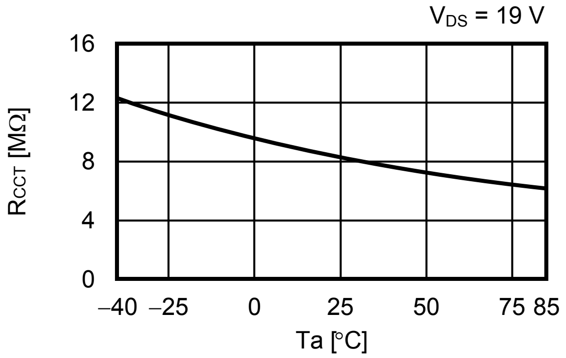


2. 8 V_{CIOV} vs. Ta

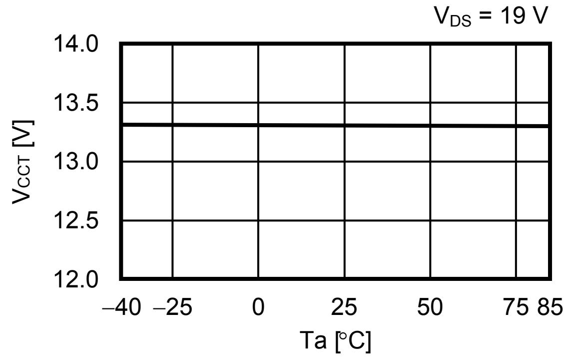


3. Delay time function

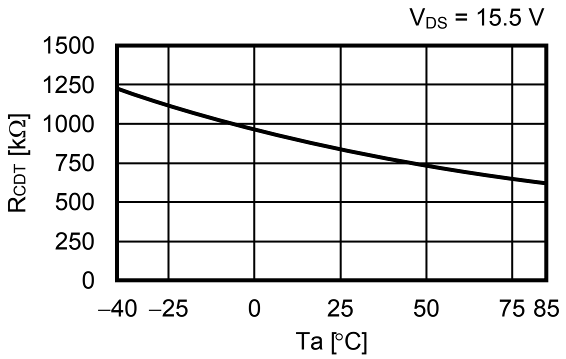
3. 1 R_{CCT} vs. Ta



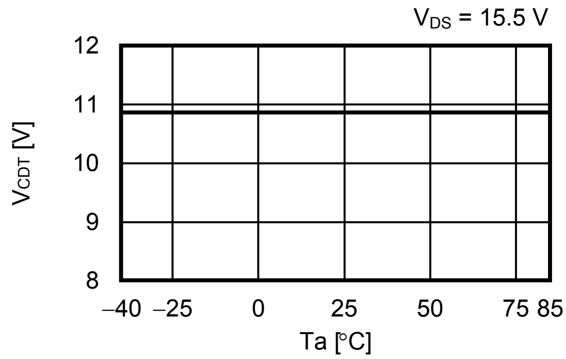
3. 2 V_{CCT} vs. Ta



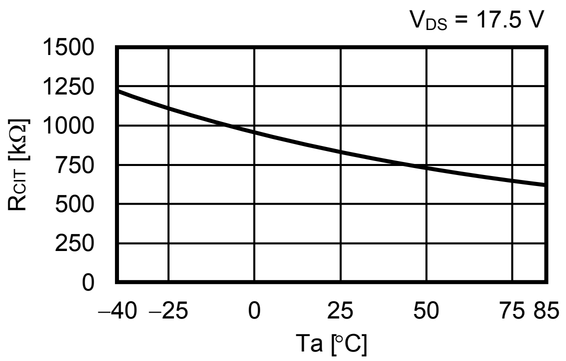
3. 3 R_{CDT} vs. Ta



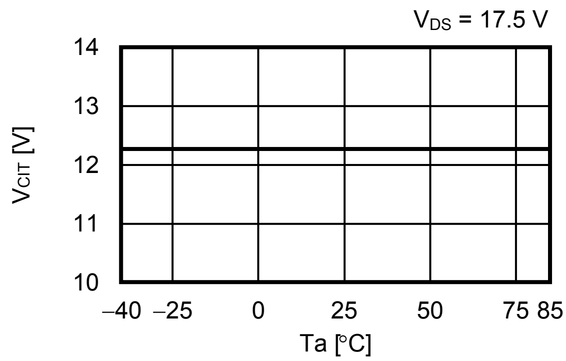
3. 4 V_{CDT} vs. Ta



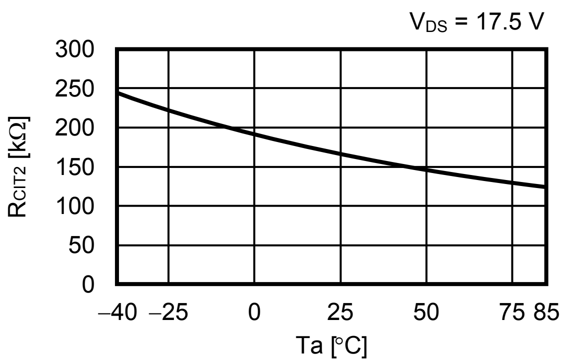
3. 5 R_{CIT} vs. Ta



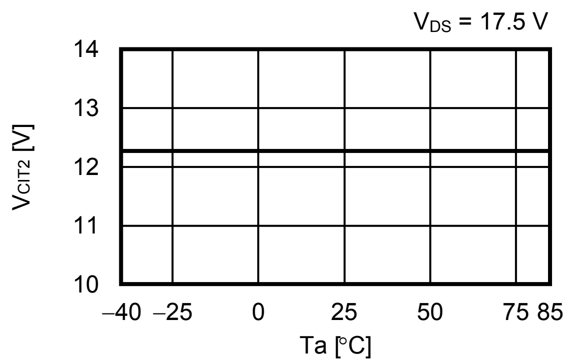
3. 6 V_{CIT} vs. Ta



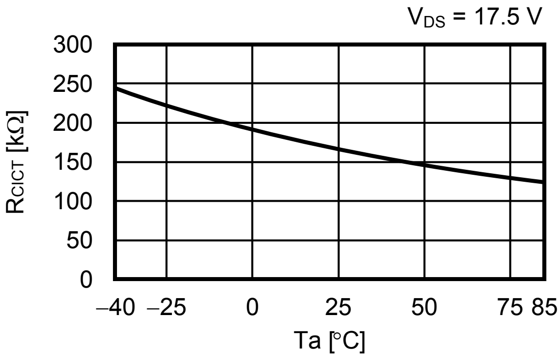
3. 7 R_{CIT2} vs. Ta



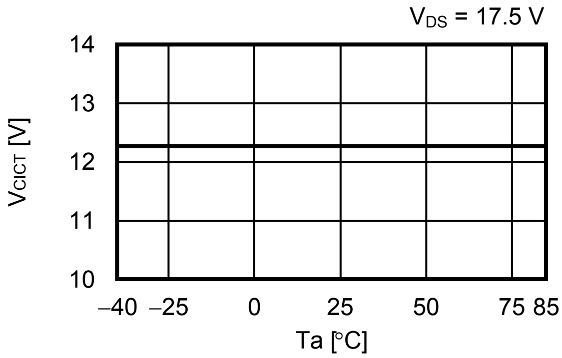
3. 8 V_{CIT2} vs. Ta



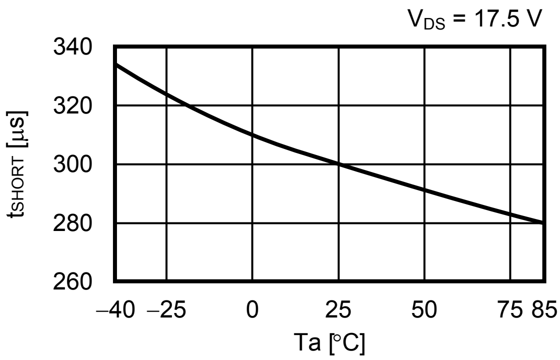
3. 9 R_{CICT} vs. Ta



3. 10 V_{CICT} vs. Ta

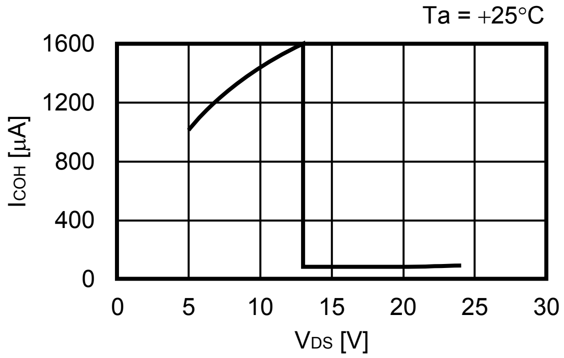


3. 11 t_{SHORT} vs. Ta

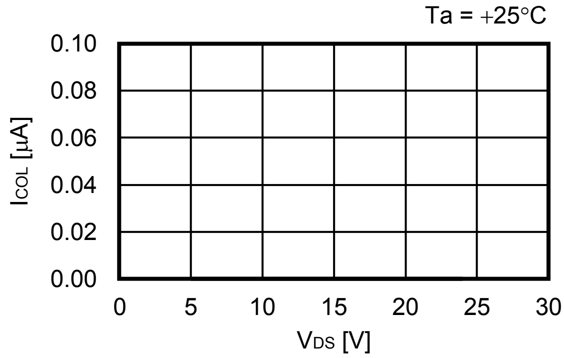


4. Output pin

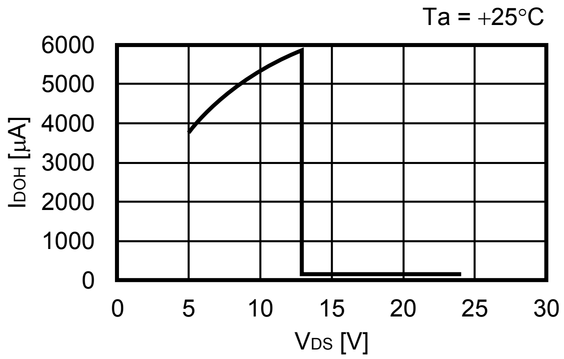
4. 1 I_{COH} vs. V_{DS}



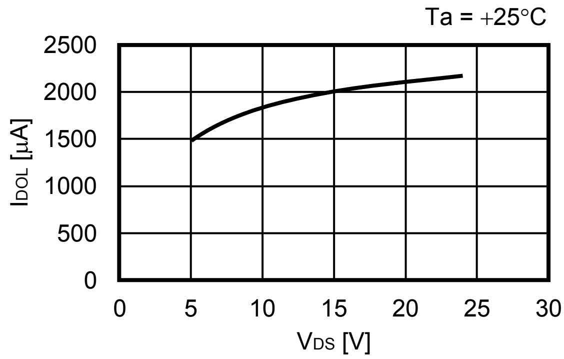
4. 2 I_{COL} vs. V_{DS}



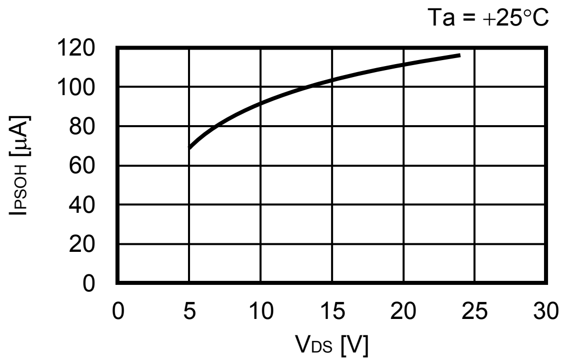
4. 3 I_{DOH} vs. V_{DS}



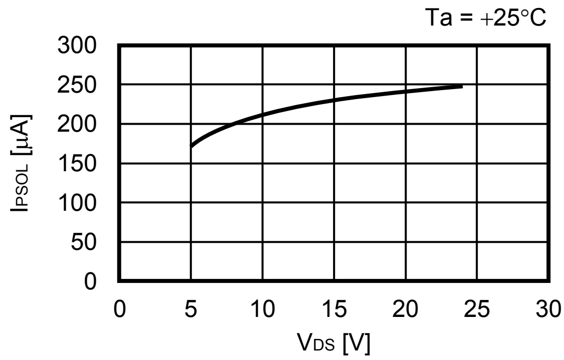
4. 4 I_{DOL} vs. V_{DS}



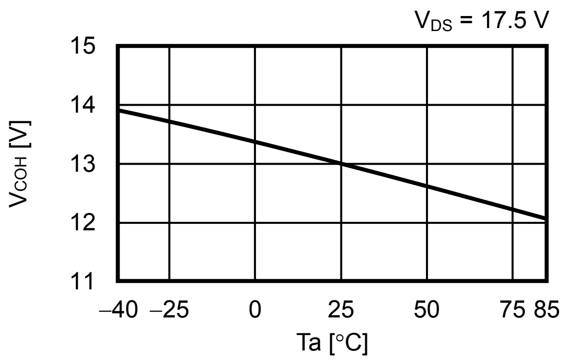
4. 5 I_{PSOH} vs. V_{DS}



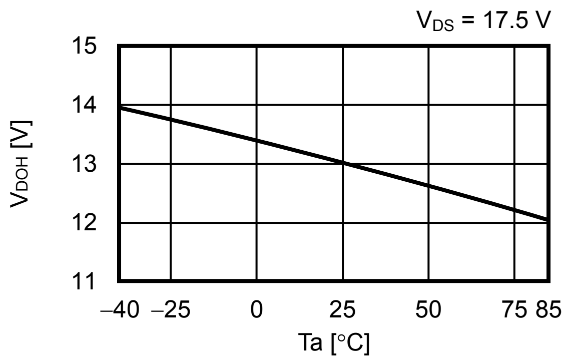
4. 6 I_{PSOL} vs. V_{DS}



4. 7 V_{COH} vs. Ta

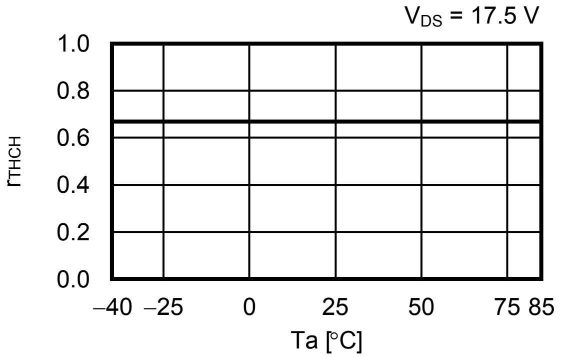


4. 8 V_{DOH} vs. Ta

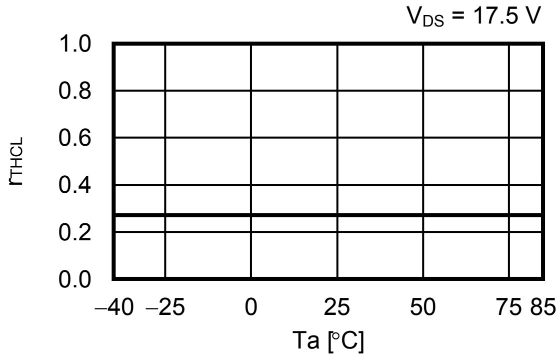


5. Temperature detection function

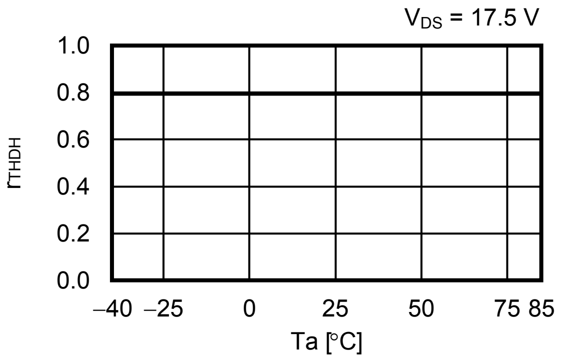
5. 1 r_{THCH} vs. Ta



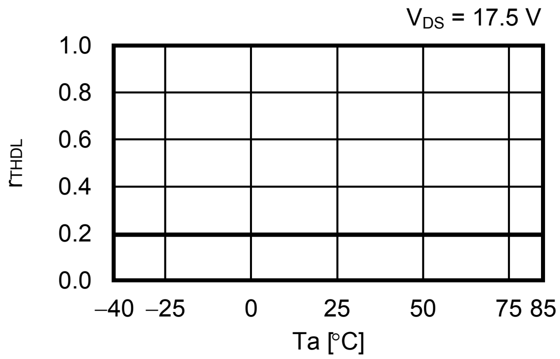
5. 2 r_{THCL} vs. Ta



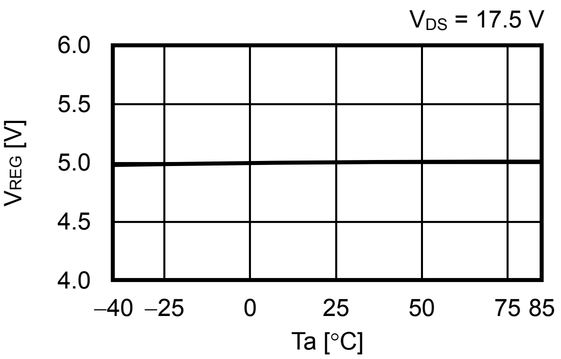
5. 3 r_{THDH} vs. Ta



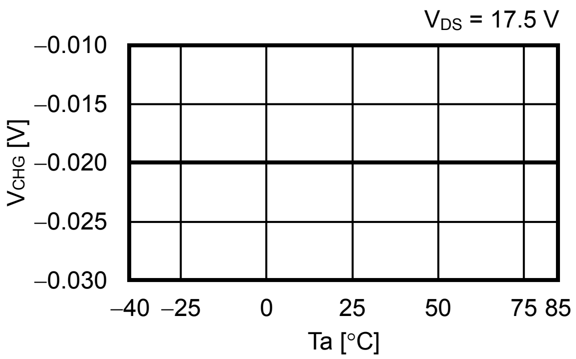
5. 4 r_{THDL} vs. Ta



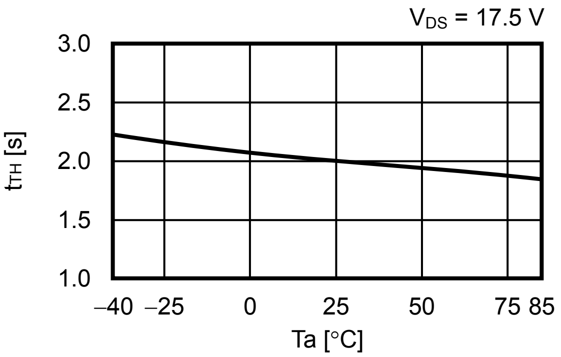
5. 5 V_{REG} vs. Ta



5. 6 V_{CHG} vs. Ta

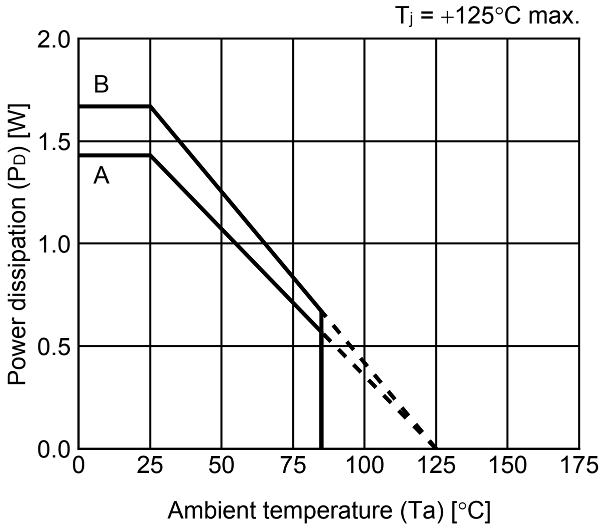


5. 7 t_{TH} vs. Ta



■ Power Dissipation

24-Pin SSOP

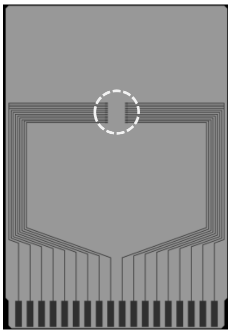


Board	Power Dissipation (P_D)
A	1.43 W
B	1.67 W
C	−
D	−
E	−

24-Pin SSOP Test Board

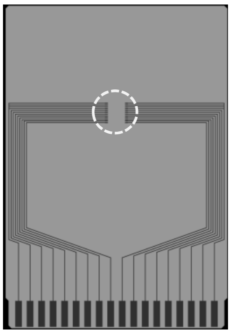
IC Mount Area

(1) Board A



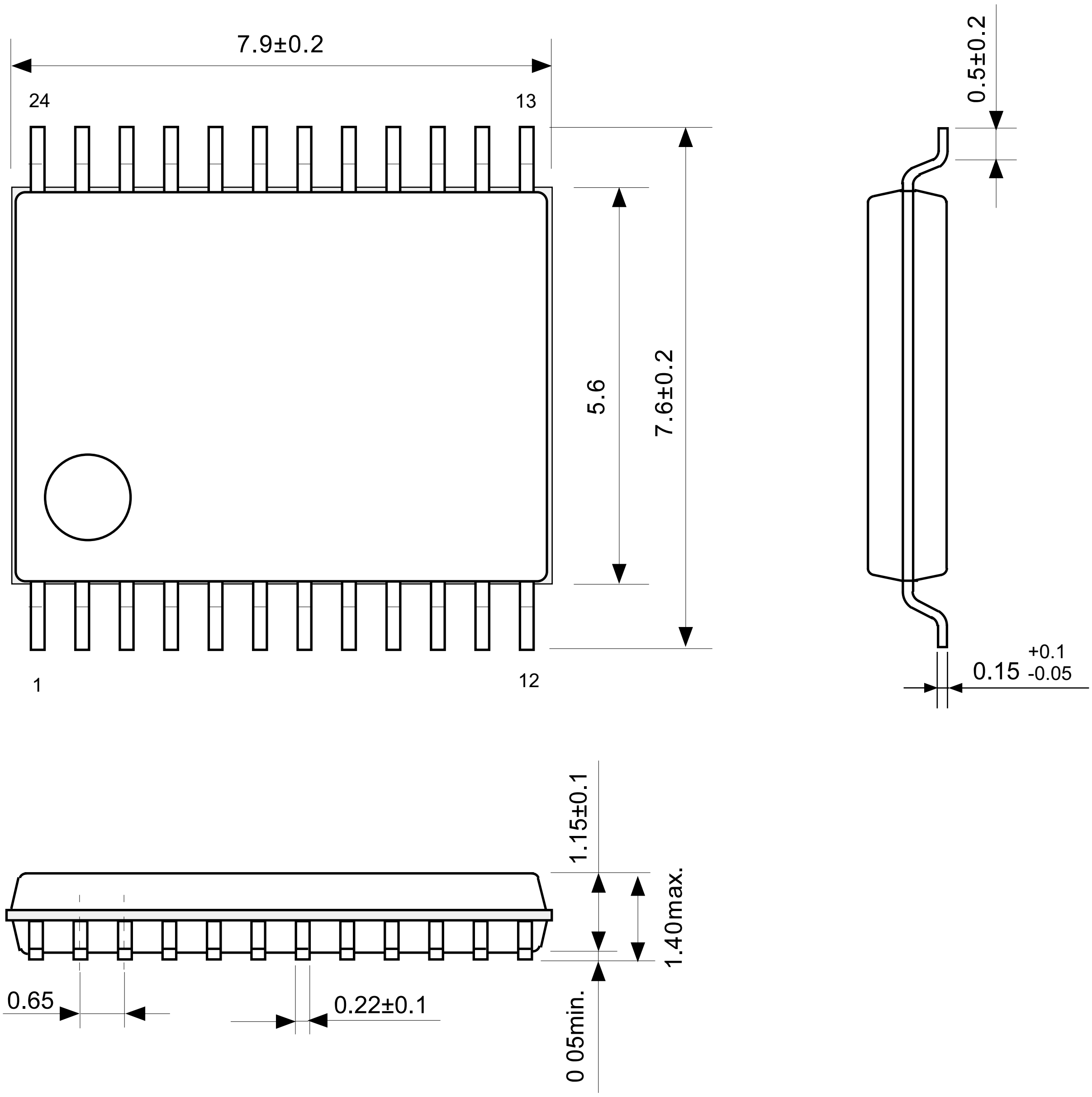
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SSOP24-A-Board-SD-1.0



No. FS024-B-P-SD-1.0

TITLE	SSOP24-B-PKG Dimensions
No.	FS024-B-P-SD-1.0
ANGLE	
UNIT	mm

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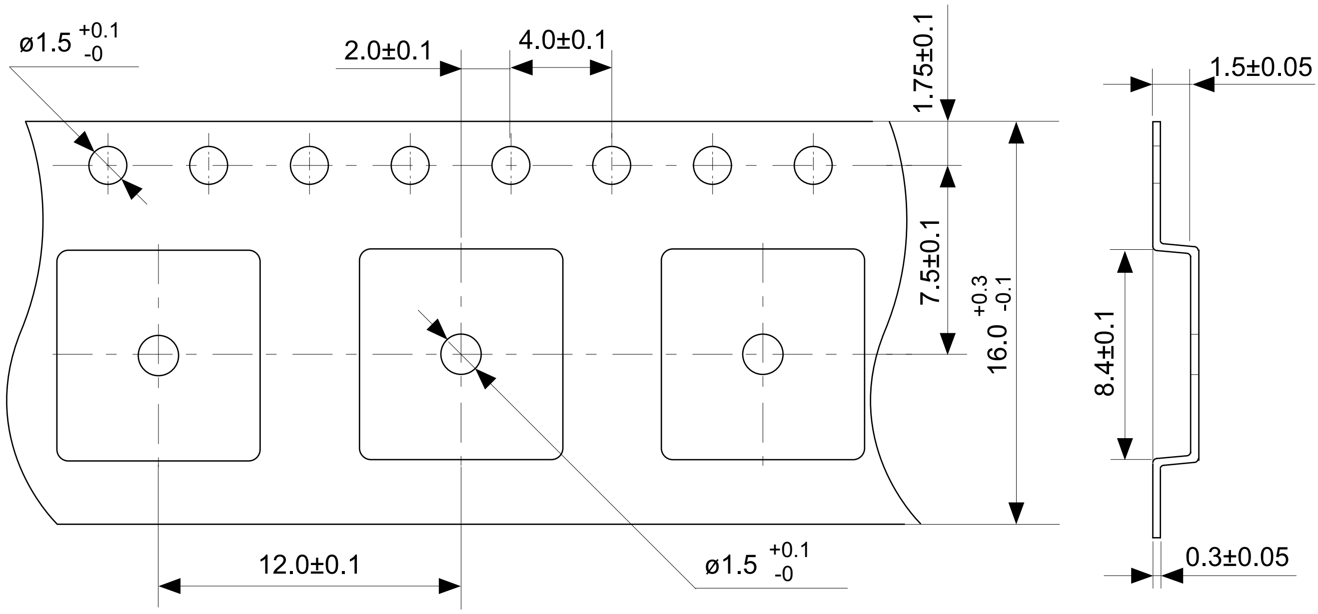

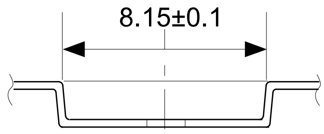

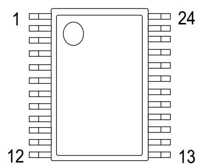

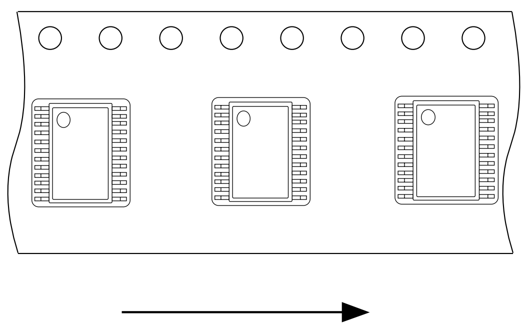

No. FS024-B-C-SD-1.0

TITLE	SSOP24-B-Carrier Tape
No.	FS024-B-C-SD-1.0
ANGLE	
UNIT	mm

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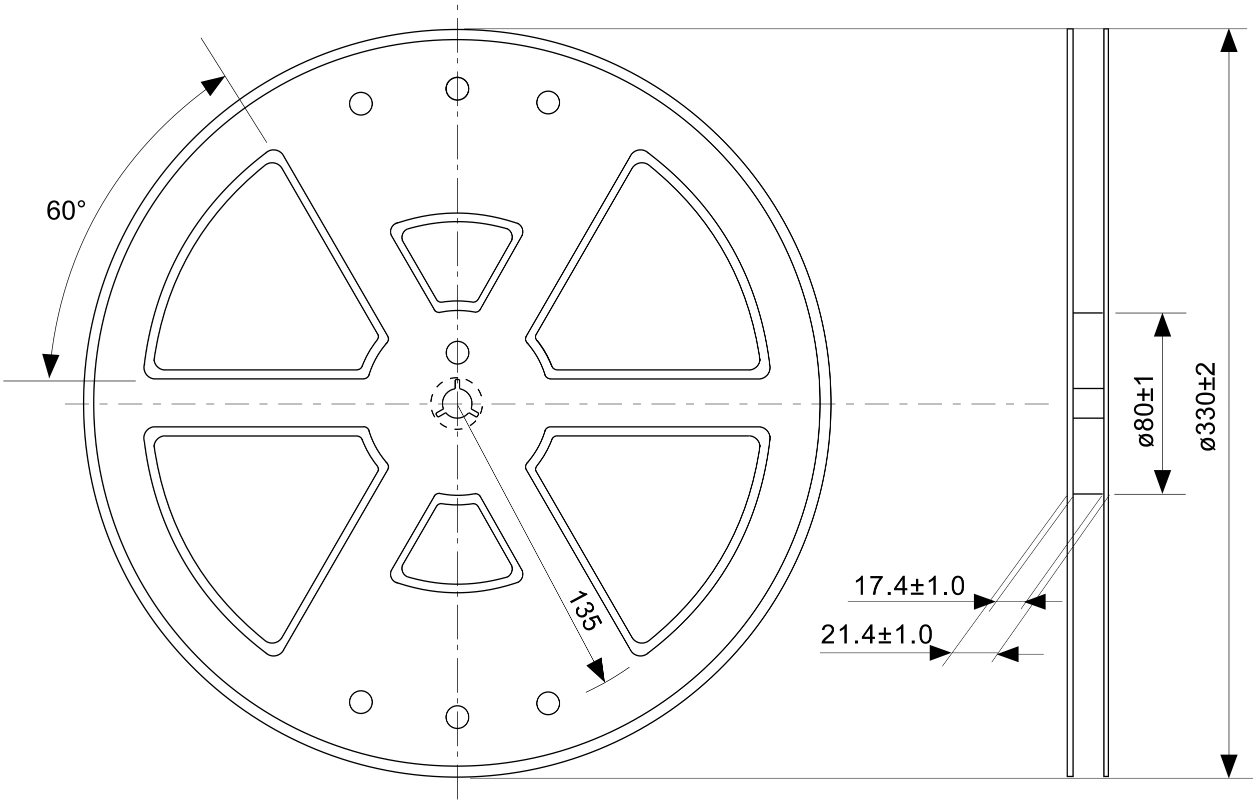
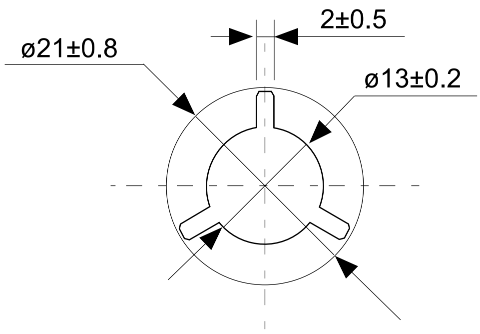


Enlarged drawing in the central part



No. FS024-B-R-SD-1.0

TITLE	SSOP24-B-Reel		
No.	FS024-B-R-SD-1.0		
ANGLE		QTY.	3000
UNIT	mm		

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2.4-2019.07