S-19115xxxH Series

AUTOMOTIVE, 105°C OPERATION, 36 V, VOLTAGE DETECTOR FOR OVERVOLTAGE DETECTION WITH DELAY FUNCTION (EXTERNAL DELAY TIME SETTING)

This IC, developed using CMOS technology, is a high-accuracy voltage detector. The detection voltage and release voltage are fixed internally with an accuracy of ±1.5%.
Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared, so the output is stable even if the SENSE pin voltage (V_{SENSE}) falls to 0 V. The SENSE pin also has a built-in reverse connection protection circuit that reduces current in the SENSE pin during a reverse connection.
The release signal can be delayed by setting a capacitor externally, and the release delay time accuracy is ±15% (C_D = 3.3 nF). The output form is Nch open-drain output.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

■ Features

- Detection voltage: 16.0 V to 18.0 V (0.1 V step)
- Detection voltage accuracy: ±1.5%
- Hysteresis width selectable from "Available" / "Unavailable": "Available": 5.0%, 10.0%
"Unavailable": 0%
- Release delay time accuracy: ±15% (C_D = 3.3 nF)
- Current consumption: 0.6 µA typ.
- Output form: Nch open-drain output
- Built-in reverse connection protection circuit: Reduces current in the SENSE pin during a reverse connection.
- Operation voltage range: 3.0 V to 36.0 V
- Operation temperature range: Ta = –40°C to +105°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified*1

***1.** Contact our sales representatives for details.

■ Applications

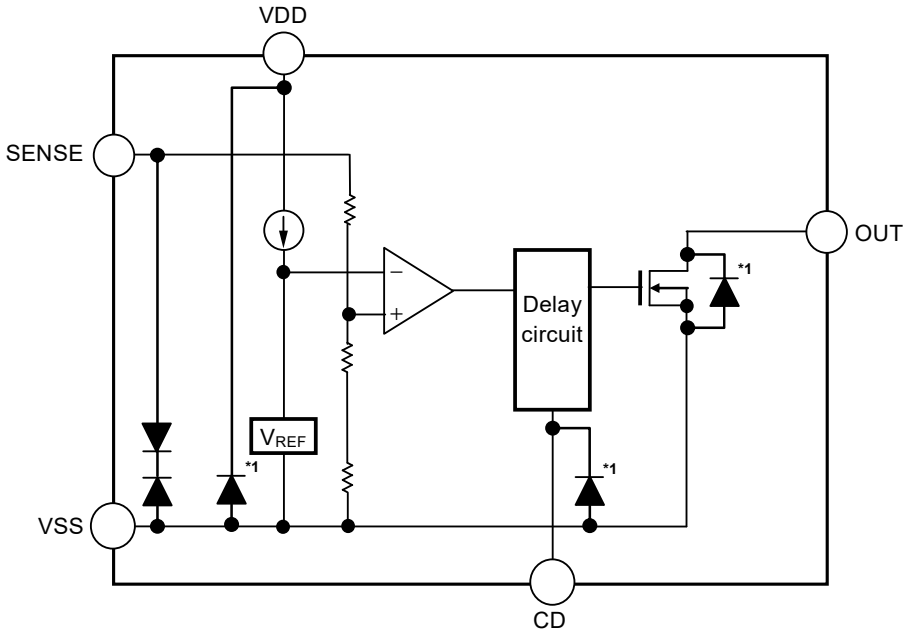
- Automotive battery voltage detection
- For automotive use (car body, headlight, ITS, accessory, car navigation system, car audio system, etc.)

■ Packages

- HTMSOP-8
- HSNT-8(2030)
- SOT-23-5

■ Block Diagrams

1. S-19115 Series L type

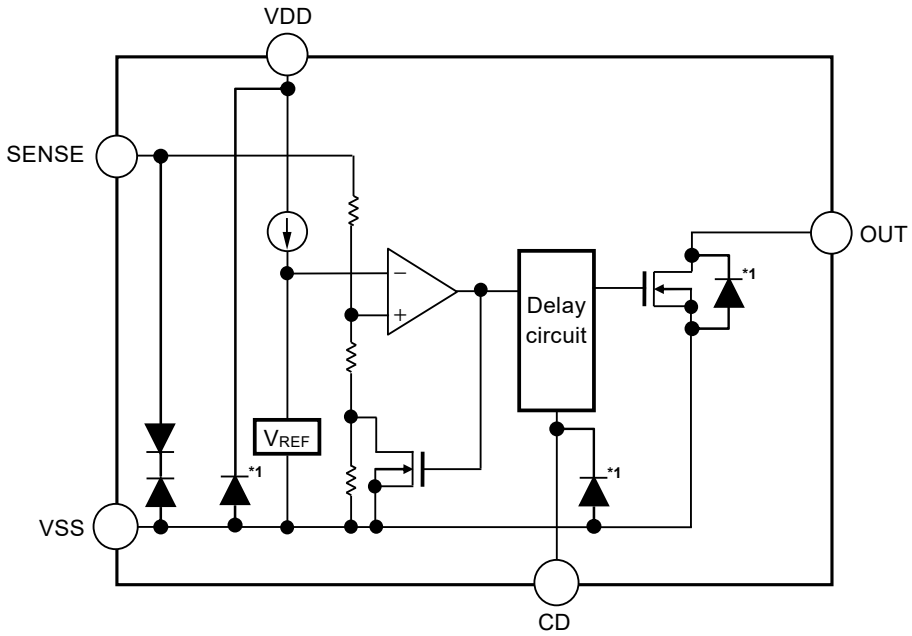


***1.** Parasitic diode

Figure 1

Product Type	Hysteresis Width	Output Form	Output Logic
L type	0%	Nch open-drain output	Active "L"

2. S-19115 Series M / N type



1. Parasitic diode

Figure 2

Product Type	Hysteresis Width	Output Form	Output Logic
M type	5.0%	Nch open-drain output	Active "L"
N type	10.0%	Nch open-drain output	Active "L"

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 2.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name

S-19115 x xx H - xxxx U 7

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - S8T1: HTMSOP-8, Tape
  - A8T1: HSNT-8(2030), Tape
  - M5T1: SOT-23-5, Tape
- Operation temperature
  - H: Ta = –40°C to +105°C
- Overvoltage detection voltage*2
  - G0 to J0
- Product type*3

***1.** Refer to the tape drawing.
***2.** Refer to **Table 1** for the overvoltage detection voltage.
***3.** Refer to "**2. Function list of product types**".

Table 1

Overvoltage Detection Voltage	Symbol	Overvoltage Detection Voltage	Symbol	Overvoltage Detection Voltage	Symbol
16.0 V	G0	16.7 V	G7	17.4 V	H4
16.1 V	G1	16.8 V	G8	17.5 V	H5
16.2 V	G2	16.9 V	G9	17.6 V	H6
16.3 V	G3	17.0 V	H0	17.7 V	H7
16.4 V	G4	17.1 V	H1	17.8 V	H8
16.5 V	G5	17.2 V	H2	17.9 V	H9
16.6 V	G6	17.3 V	H3	18.0 V	J0

2. Function list of product types

Table 2

Product Type	Hysteresis Width	Output Form	Output Logic
L type	0%	Nch open-drain output	Active "L"
M type	5.0%	Nch open-drain output	Active "L"
N type	10.0%	Nch open-drain output	Active "L"

3. Packages

Table 3 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
HTMSOP-8	FP008-A-P-SD	FP008-A-C-SD	FP008-A-R-SD	FP008-A-L-SD
HSNT-8(2030)	PP008-A-P-SD	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–

■ Pin Configurations

1. HTMSOP-8

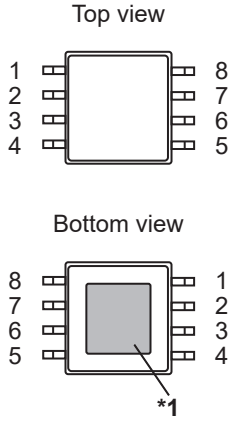


Figure 3

Table 4

Pin No.	Symbol	Description
1	NC*2	No connection
2	VDD	Voltage input pin
3	NC*2	No connection
4	SENSE	Detection voltage input pin
5	CD*3	Connection pin for release delay time adjustment capacitor
6	VSS	GND pin
7	OUT	Voltage detection output pin
8	NC*2	No connection

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.
***2.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.
***3.** Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance.

2. HSNT-8(2030)

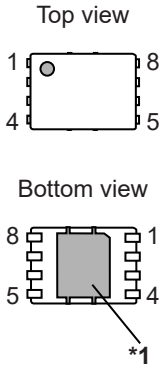


Figure 4

Table 5

Pin No.	Symbol	Description
1	NC*2	No connection
2	VDD	Voltage input pin
3	NC*2	No connection
4	SENSE	Detection voltage input pin
5	CD*3	Connection pin for release delay time adjustment capacitor
6	VSS	GND pin
7	OUT	Voltage detection output pin
8	NC*2	No connection

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.
***2.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.
***3.** Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance.

3. SOT-23-5

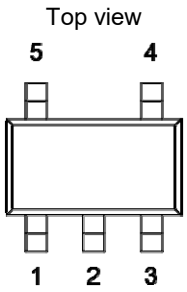


Figure 5

Table 6

Pin No.	Symbol	Description
1	OUT	Overvoltage detection output pin
2	VSS	GND pin
3	CD*1	Connection pin for release delay capacitor
4	SENSE	Detection voltage input pin
5	VDD	Voltage input pin

***1.** Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance.

■ Absolute Maximum Ratings

Table 7

(Ta = –40°C to +105°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	V_{SS} – 0.3 to V_{SS} + 45.0	V
SENSE pin voltage	V_{SENSE}	V_{SS} – 30.0 to V_{SS} + 45.0	V
CD pin input voltage	V_{CD}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
Output voltage	V_{OUT}	V_{SS} – 0.3 to V_{SS} + 45.0	V
Output current	I_{OUT}	25	mA
Junction temperature	T_j	–40 to +150	°C
Operation ambient temperature	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 8

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	HTMSOP-8	Board A	–	159	–	°C/W
			Board B	–	113	–	°C/W
			Board C	–	39	–	°C/W
			Board D	–	40	–	°C/W
			Board E	–	30	–	°C/W
		HSNT-8(2030)	Board A	–	181	–	°C/W
			Board B	–	135	–	°C/W
			Board C	–	40	–	°C/W
			Board D	–	42	–	°C/W
			Board E	–	32	–	°C/W
		SOT-23-5	Board A	–	192	–	°C/W
			Board B	–	160	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 9

(Ta = –40°C to +105°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	V_{DET}	V_{DD} = 13.5 V, 16.0 V ≤ $V_{DET(S)}$ ≤ 18.0 V	$V_{DET(S)}$ × 0.985	$V_{DET(S)}$	$V_{DET(S)}$ × 1.015	V	1
Hysteresis width*2	V_{HYS}	L type (V_{HYS} = 0%)	–	V_{DET} × 0.00	–	V	1
		M type (V_{HYS} = 5.0%)	V_{DET} × 0.04	V_{DET} × 0.05	V_{DET} × 0.06	V	1
		N type (V_{HYS} = 10.0%)	V_{DET} × 0.09	V_{DET} × 0.10	V_{DET} × 0.11	V	1
Current consumption	I_{SS1}	V_{DD} = 13.5 V, V_{SENSE} = 13.5 V	–	0.6	2.4	μA	4
Operation voltage	V_{DD}	–	3.0	–	36.0	V	1
Output current	I_{OUT}	OUT pin Nch driver, V_{DD} = 3.0 V, V_{DS}*3 = 0.1 V, V_{SENSE} = $V_{DET(S)}$ + 1 V	0.60	–	–	mA	2
Leakage current	I_{LEAK}	OUT pin Nch driver, V_{DD} = 36 V, V_{OUT} = 36 V, V_{SENSE} = 13.5 V	–	–	2.0	μA	2
Detection response time*4	t_{RESET}	–	–	80	200	μs	3
Release delay time*5	t_{DELAY}	C_D = 3.3 nF	8.5	10.0	11.5	ms	3
SENSE pin resistance	R_{SENSE}	–	6.8	–	200	MΩ	4
CD pin discharge ON resistance	R_{CDD}	V_{DD} = 3.0 V, V_{CD} = 0.7 V	0.15	–	0.90	kΩ	–

***1.** V_{DET}: Actual detection voltage value, $V_{DET(S)}$: Set detection voltage value

***2.** The release voltage (V_{REL}) are as follows.
L type (hysteresis width "Unavailable"): V_{REL} = V_{DET}
M / N type (hysteresis width "Available"): V_{REL} = V_{DET} – V_{HYS}

***3.** V_{DS}: Drain-to-source voltage of the output transistor

***4.** The time period from when the pulse voltage of $V_{DET(S)}$ – 1.0 V → $V_{DET(S)}$ + 1.0 V is applied to the SENSE pin after V_{SENSE} reaches the release voltage once, until V_{OUT} reaches 50% of V_{DD}.

***5.** $V_{REL(S)}$: Set release voltage value
The time period from when the pulse voltage of $V_{REL(S)}$ + 1.0 V → $V_{REL(S)}$ – 1.0 V is applied to the SENSE pin to when V_{OUT} reaches 50% of V_{DD}.

■ Test Circuits

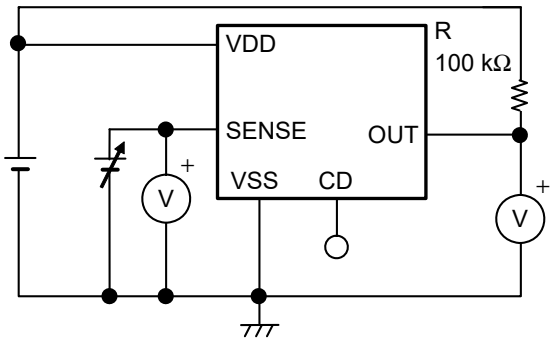


Figure 6 Test Circuit 1

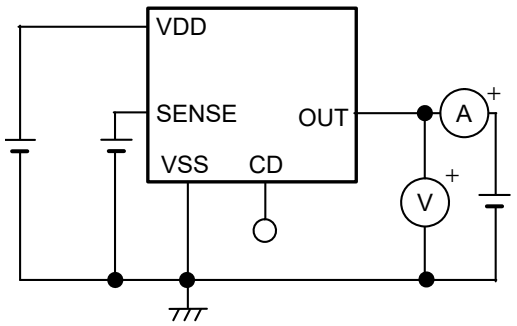


Figure 7 Test Circuit 2

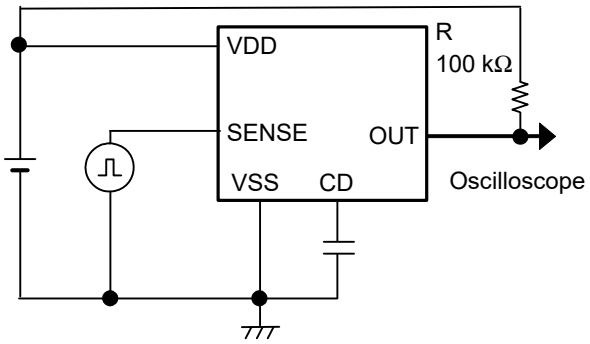


Figure 8 Test Circuit 3

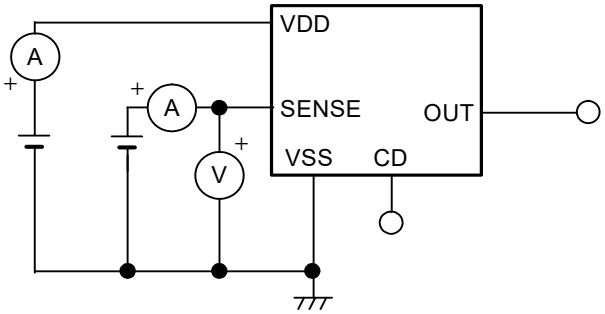
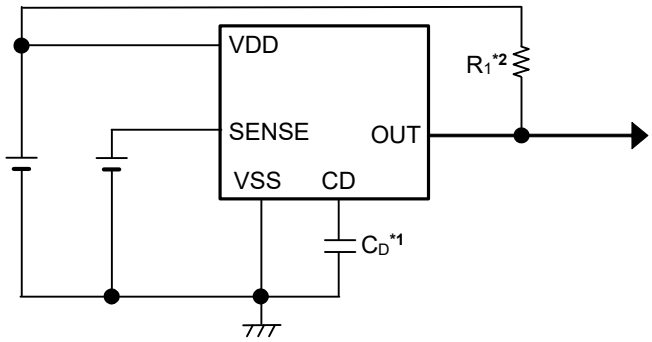


Figure 9 Test Circuit 4

■ Standard Circuit



***1.** C_D is a release delay time adjustment capacitor. The C_D should be connected directly to the CD pin and the VSS pin.

***2.** R_1 are the external pull-up resistors for the reset output pin.

Figure 10

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

■ Condition of Application

Release delay time adjustment capacitor (C_D): A ceramic capacitor with capacitance of 1.0 nF or more is recommended.

■ Selection of Release Delay Time Adjustment Capacitor (C_D)

In this IC, the release delay time adjustment capacitor (C_D) is necessary between the CD pin and the VSS pin to adjust the release delay time (t_{DELAY}) of the detector. Refer to "**1. 4 Delay circuit**" in "**■ Operation**" for details.

Caution Perform thorough evaluation including the temperature characteristics with an actual application to select C_D.

■ Explanation of Terms

1. Detection voltage (V_{DET})

The detection voltage is a SENSE pin voltage at which the output voltage in **Figure 13** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum and the maximum is called the detection voltage range (Refer to "**Figure 11 Detection Voltage**").

Example: In V_{DET} = 16.0 V product, the detection voltage is at any point in the range of 15.760 V ≤ V_{DET} ≤ 16.240 V.
This means that some V_{DET} = 16.0 V product has V_{DET} = 15.760 V and some has V_{DET} = 16.240 V.

2. Release voltage (V_{REL})

The release voltage is a SENSE pin voltage at which the output voltage in **Figure 13** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum and the maximum is called the release voltage range (Refer to "**Figure 12 Release Voltage**").
The release voltage becomes the value differs from the detection voltage within the range shown below.

- M type: 4% to 6% (5% typ.)
- N type: 9% to 11% (10% typ.)

Example: For N type, V_{DET} = 16.0 V product, the release voltage is at any point in the range of 14.026 V ≤ V_{REL} ≤ 14.779 V despite V_{REL} = 14.400 V typ.
This means that some N type, V_{DET} = 16.0 V product has V_{REL} = 14.026 V and some has V_{REL} = 14.779 V.

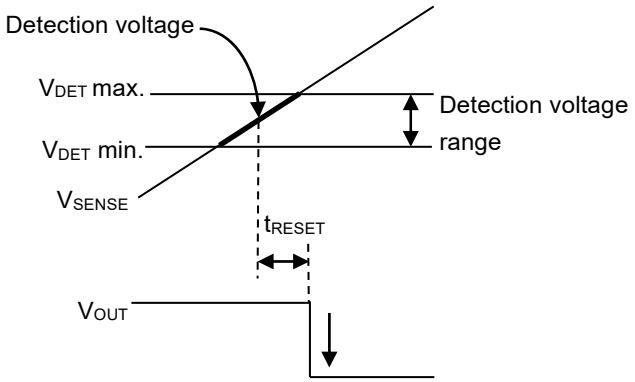


Figure 11 Detection Voltage

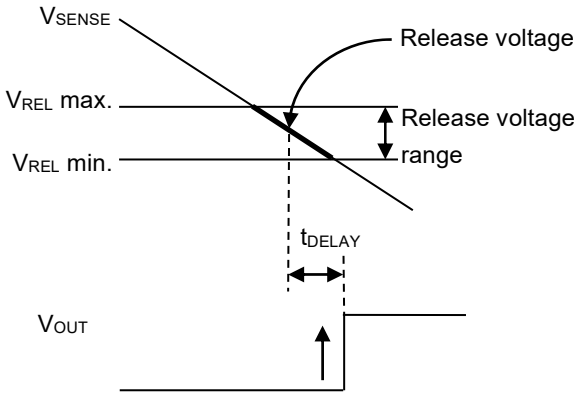


Figure 12 Release Voltage

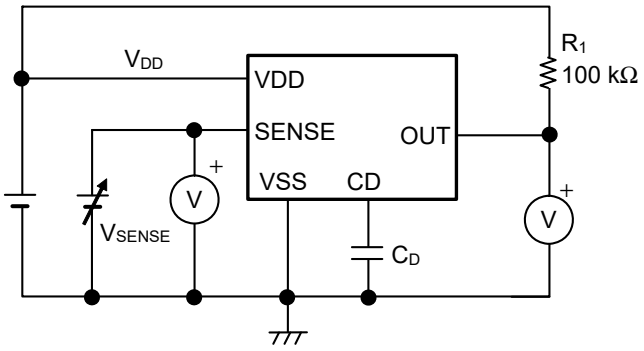


Figure 13 Test Circuit of Detection Voltage and Release Voltage

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage (V_{DET}) and the release voltage (V_{REL}). Voltage difference between V_{REL} and V_{DET} is the hysteresis width (V_{HYS}*1) of the OUT pin. Setting the hysteresis width between V_{DET} and V_{REL}, prevents malfunction caused by noise on the input voltage.

***1.** Refer to "**1. 2 S-19115 Series M / N type**" in "**■ Operation**" for details.

4. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector.

■ Operation

1. Basic operation

Figure 14 and **Figure 16** show that the OUT pin being pulled up by resistors (R_1) is an example of basic detector block operation.

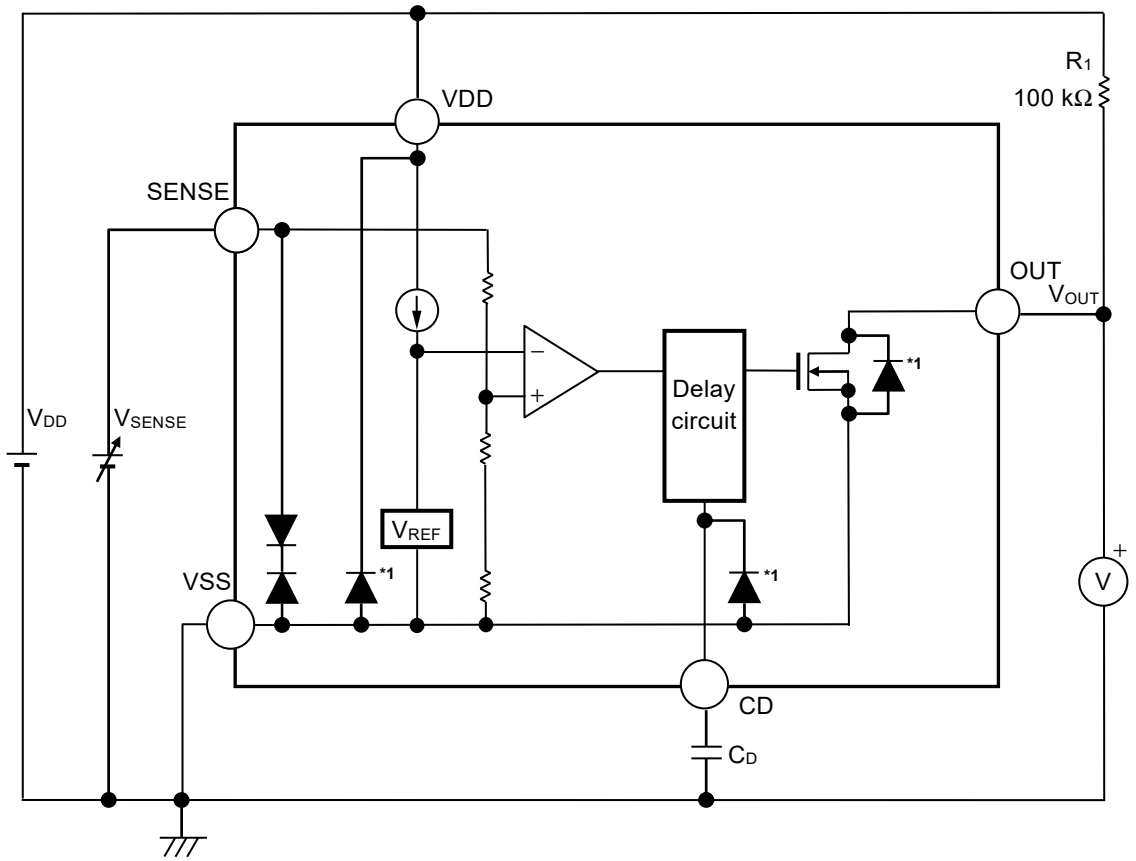
1. 1 S-19115 Series L type

(1) Release status to detection status

The SENSE pin voltage (V_{SENSE}) rises, and when it exceeds the detection voltage (V_{DET}), the OUT pin output becomes "L" after detection response time (t_{RESET}).

(2) Detection status to release status

V_{SENSE} drops, and when it goes below the release voltage (V_{REL} = V_{DET}), the OUT pin output changes to "H" after release delay time (t_{DELAY}).



1. Parasitic diode

Figure 14 Operation of S-19115 Series L type

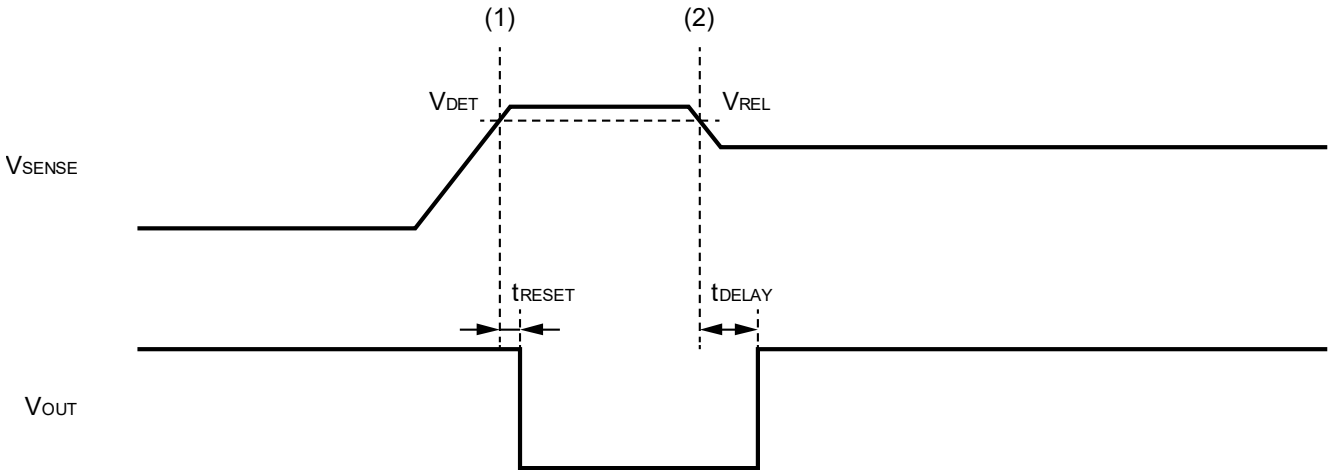


Figure 15 Timing Chart of S-19115 Series L Type

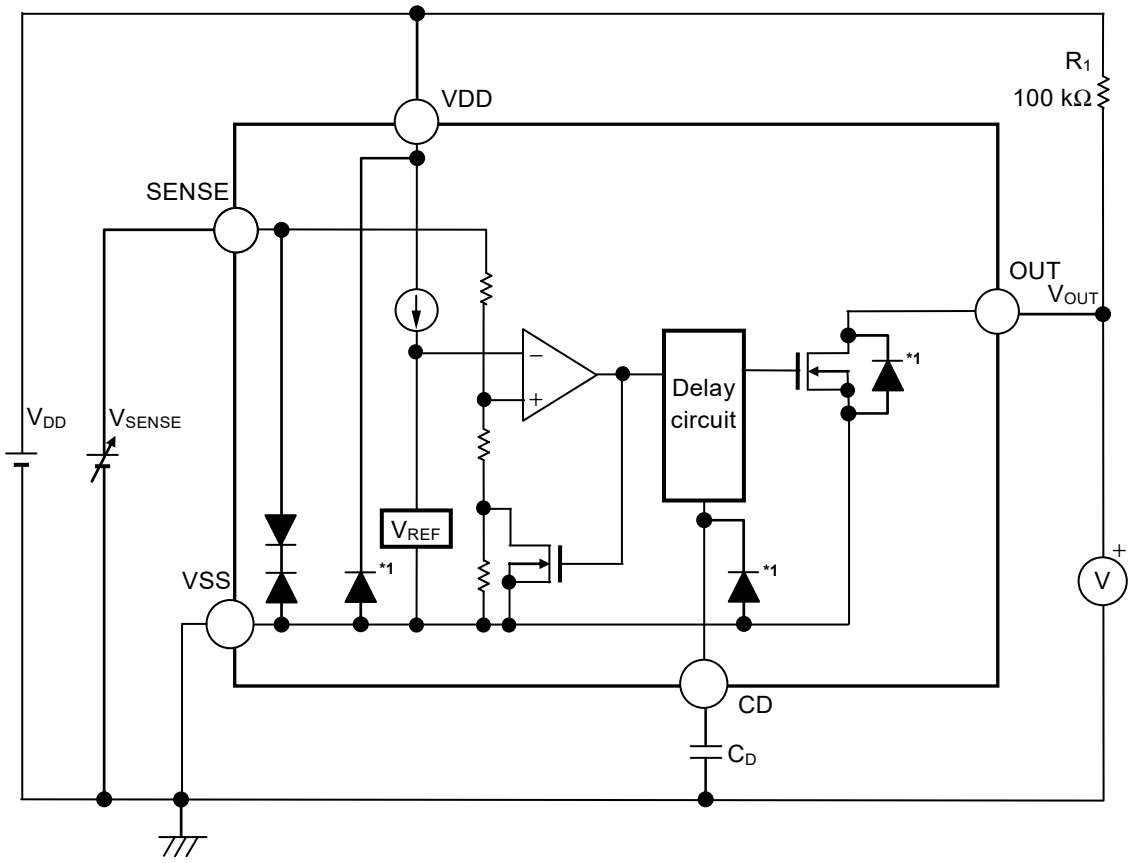
1. 2 S-19115 Series M / N type

(1) Release status to detection status

The SENSE pin voltage (V_{SENSE}) rises, and when it exceeds the detection voltage (V_{DET}), the OUT pin output becomes "L" after detection response time (t_{RESET}).

(2) Detection status to release status

V_{SENSE} drops, and when it goes below the release voltage ($V_{REL} = V_{DET} - V_{HYS}$), the OUT pin output changes to "H" after release delay time (t_{DELAY}).



***1.** Parasitic diode

Figure 16 Operation of S-19115 Series M / N type

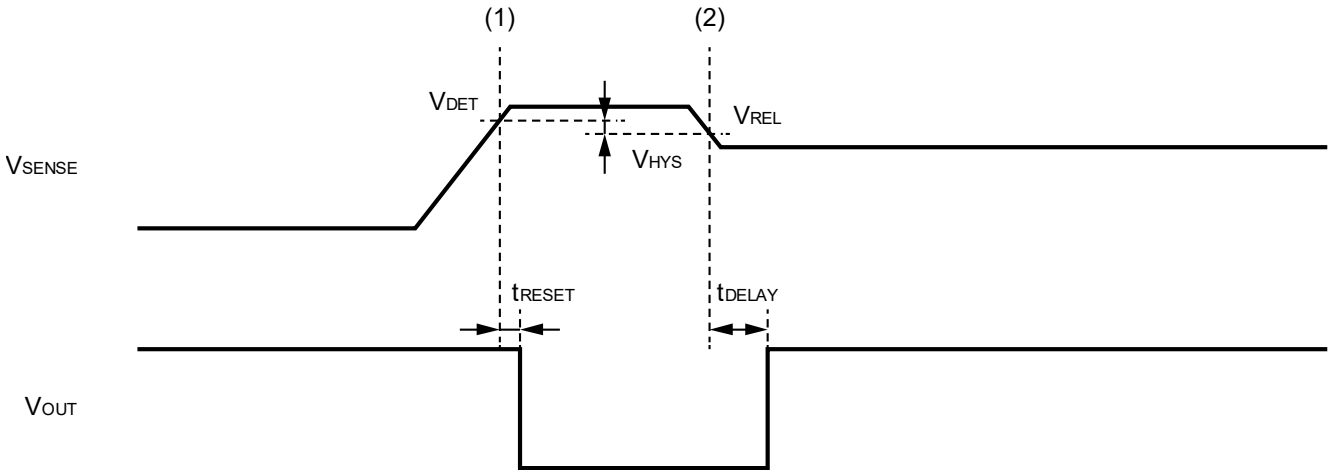


Figure 17 Timing Chart of S-19115 Series M / N Type

1. 3 SENSE pin

The SENSE pin is the input pin for the detection voltage. The power supply VDD pin and SENSE pin, for voltage detection, are divided. Therefore, as long as a voltage is supplied to the VDD pin, the release signal will be held even if the input voltage to the SENSE pin drops below the minimum operation voltage. Also, the SENSE pin of this IC has a built-in reverse connection protection circuit. Even when the SENSE pin voltage is less than the VSS pin voltage, the voltage flowing from the VSS pin to the SENSE pin is reduced to 0.05 mA typ.

1. 3. 1 Error when detection voltage is set externally

The detection voltage can be set externally by connecting a node that was resistance-divided by the resistor (R_A) and the resistor (R_B) to the SENSE pin as shown in **Figure 18**.
For conventional products without the SENSE pin, external resistor cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if external resistor is large, problems such as oscillation or larger error in the hysteresis width may occur.
In this IC, R_A and R_B in **Figure 18** are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance (R_{SENSE}) that will occur.
Although R_{SENSE}*1 in this IC is large to make the error small, R_A and R_B should be selected such that the error is within the allowable limits.

***1.** 6.8 MΩ min.

1. 3. 2 Selection of R_A and R_B

In **Figure 18**, the relation between the external setting detection voltage (V_{DX}) and the actual detection voltage (V_{DET}) is ideally calculated by the equation below.

$$V_{DX} = V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) \cdots\cdots(1)$$

However, in reality there is an error in the current flowing through R_{SENSE}.
When considering this error, the relation between V_{DX} and V_{DET} is calculated as follows.

$$\begin{aligned} V_{DX} &= V_{DET} \times \left(1 + \frac{R_A}{R_B \,||\, R_{SENSE}}\right) \\ &= V_{DET} \times \left(1 + \frac{R_A}{\dfrac{R_B \times R_{SENSE}}{R_B + R_{SENSE}}}\right) \\ &= V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times V_{DET} \cdots\cdots(2) \end{aligned}$$

By using equations (1) and (2), the error is calculated as $V_{DET} \times \dfrac{R_A}{R_{SENSE}}$.
The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100\ [\%] = \frac{R_A \,||\, R_B}{R_{SENSE}} \times 100\ [\%] \cdots(3)$$

As seen in equation (3), the smaller the resistance values of R_A and R_B compared to R_{SENSE}, the smaller the error rate becomes.

Also, the relation between the external setting hysteresis width (V_{HX}) and the hysteresis width (V_{HYS}) is calculated by equation below. Error due to R_{SENSE} also occurs to the relation in a similar way to the detection voltage.

$$V_{HX} = V_{HYS} \times \left(1 + \frac{R_A}{R_B}\right) \cdots\cdots(4)$$

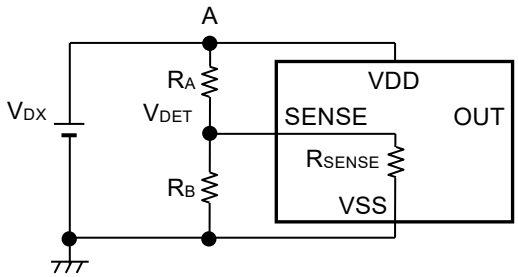


Figure 18 Detection Voltage External Setting Circuit

Caution If R_A and R_B are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.

1. 4 Delay circuit

The delay circuit comes with a function for adjusting the release delay time (t_{DELAY}) from when the SENSE pin voltage (V_{SENSE}) reaches the detection voltage ($V_{REL} = V_{DET} - V_{HYS}$) or lower to when the output from OUT pin inverts.
t_{DELAY} is determined by the delay coefficient, the release delay time adjustment capacitor (C_D) and the release delay time when the CD pin is open (t_{DELAY0}). They are calculated by the equations below.

t_{DELAY} [ms] = Delay coefficient × C_D [nF] + t_{DELAY0} [ms]

Table 10

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +105°C	2.71	3.05	3.35
Ta = +25°C	2.92	3.06	3.14
Ta = –40°C	2.65	3.09	3.41

Table 11

Operation Temperature	Release Delay Time when CD Pin is Open (t_{DELAY0})		
	Min.	Typ.	Max.
Ta = +105°C	0.05	0.10	0.17
Ta = +25°C	0.06	0.11	0.19
Ta = –40°C	0.06	0.13	0.25

Caution 1. Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.
2. There is no limit for the capacitance of C_D as long as the leakage current of the capacitor can be ignored against the built-in constant current value (approximately 160 nA). The leakage current may cause error in delay time. When the leakage current is larger than the built-in constant current, no detect or release takes place.
3. The above equations will not guarantee successful operation. Determine the capacitance of C_D through thorough evaluation including temperature characteristics in the actual usage conditions.

■ Usage Precautions

1. Power on sequence

Turn on the power in one of the following two procedures.

(1) Order of VDD pin and SENSE pin (Refer to **Figure 19**)
(2) VDD pin and SENSE pin at the same time

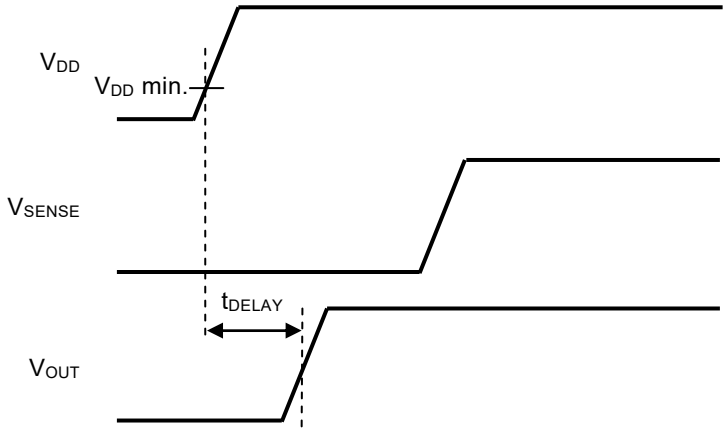


Figure 19

Caution When the SENSE pin is turned on before the VDD pin, a detection may mistakenly occur even if V_{SENSE} is less than V_{DET}.

2. SENSE pin voltage glitch (Typical data)

2. 1 Detection operation

Figure 20 shows the relation between pulse width and pulse voltage difference (V_{OD}) where the release status can be maintained when a pulse equal to or higher than the detection voltage (V_{DET}) is input to the SENSE pin during release status.

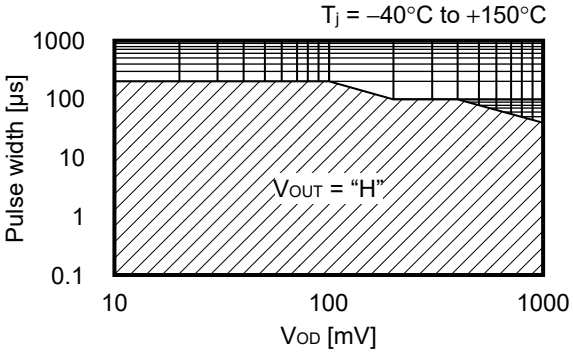
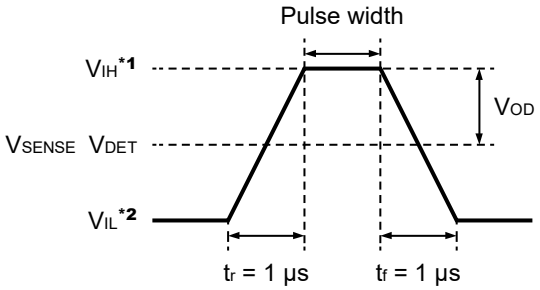


Figure 20



***1.** $V_{IH} = V_{DET} + V_{OD}$
***2.** V_{IL} = 13.5 V

Figure 21 SENSE Pin Input Voltage Waveform

Caution Figure 20 shows the pulse condition which can maintain the release status. If the pulse whose pulse width and V_{OD} are larger than this condition is input to the SENSE pin, the OUT pin may change to a detection status.

2. 2 Release operation

Figure 22 shows the relation between pulse width and pulse voltage difference (V_{OD}) where the detection status can be maintained when a pulse equal to or lower than the release voltage (V_{REL}) is input to the SENSE pin during detection status.

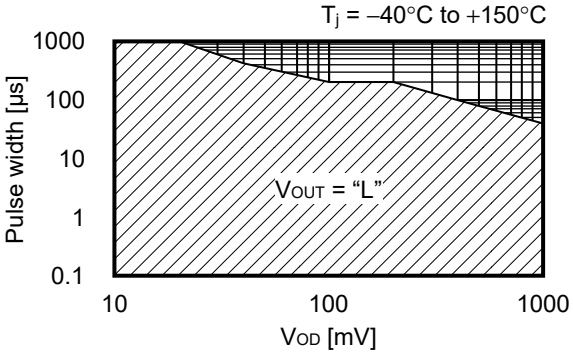
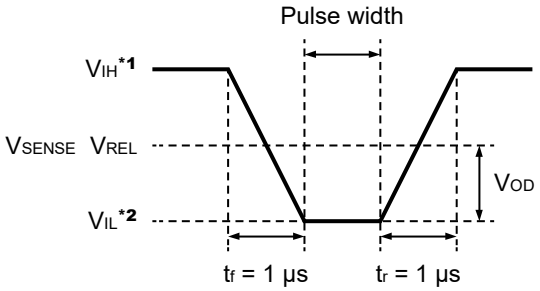


Figure 22



***1.** $V_{IH} = V_{DET} + 1.0$ V
***2.** $V_{IL} = V_{REL} – V_{OD}$

Figure 23 SENSE Pin Input Voltage Waveform

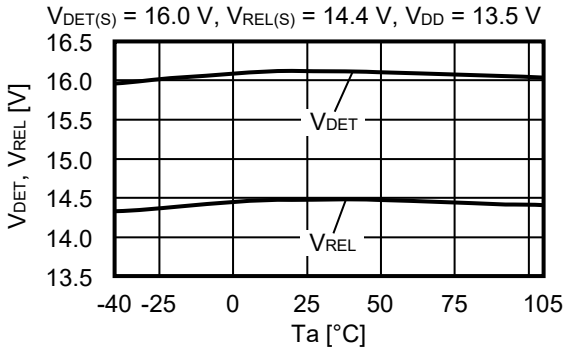
Caution Figure 22 shows the pulse condition which can maintain the detection status. If the pulse whose pulse width and V_{OD} are larger than this condition is input to the SENSE pin, the OUT pin may change to a release status.

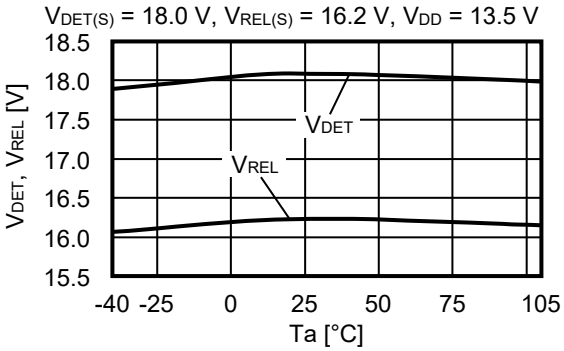
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Because the SENSE pin has a high impedance, malfunctions may occur due to noise.
  Be careful of wiring adjoining SENSE pin wiring in actual applications.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

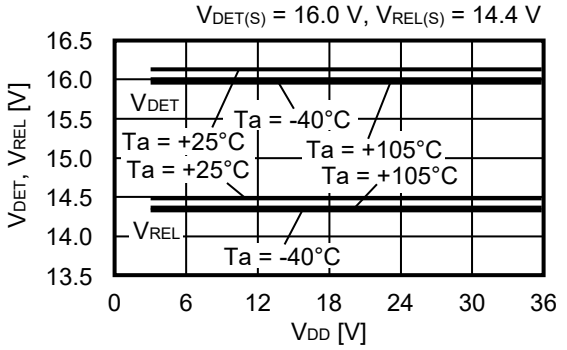
■ Characteristics (Typical Data)

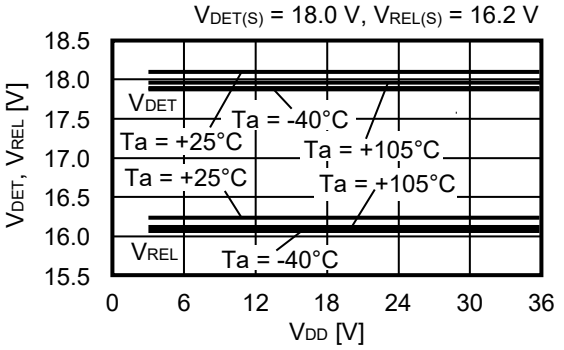
1. Detection voltage (V_{DET}), Release voltage (V_{REL}) vs. Temperature (Ta)



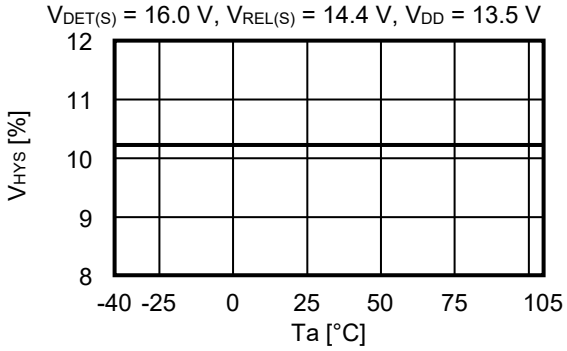


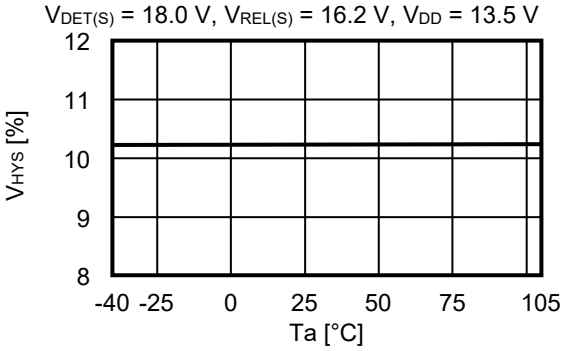
2. Detection voltage (V_{DET}), Release voltage (V_{REL}) vs. Power supply voltage (V_{DD})



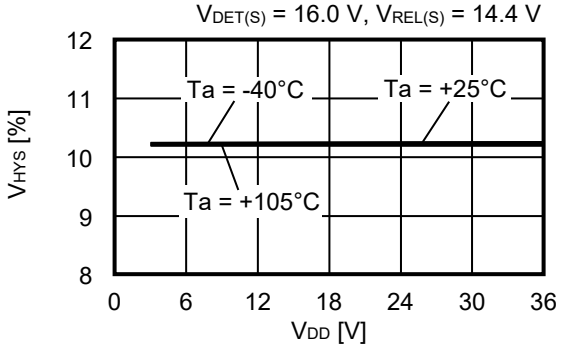


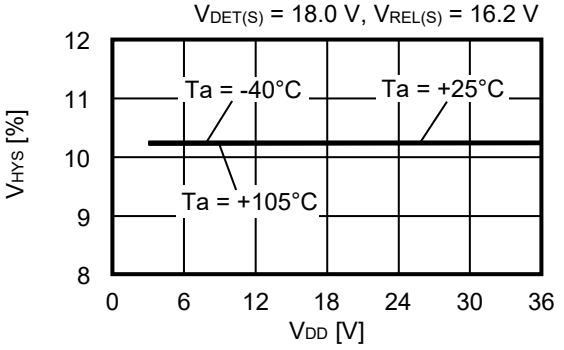
3. Hysteresis width (V_{HYS}) vs. Temperature (Ta)





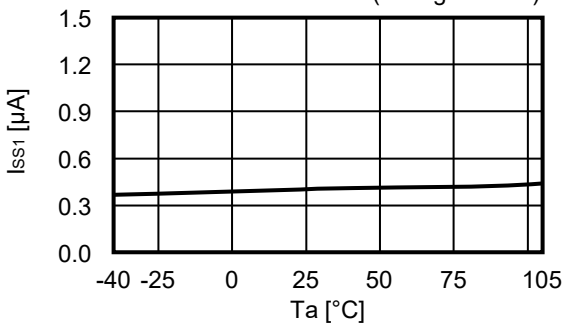
4. Hysteresis width (V_{HYS}) vs. Power supply voltage (V_{DD})



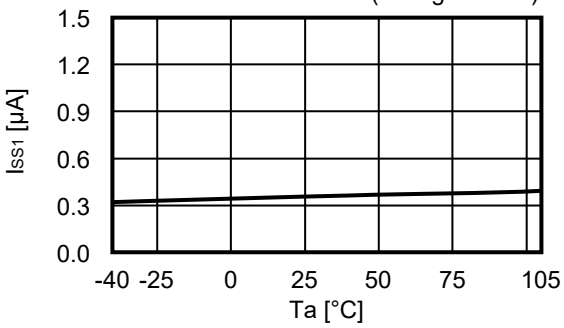


5. Current consumption (I_{SS1}) vs. Temperature (Ta)

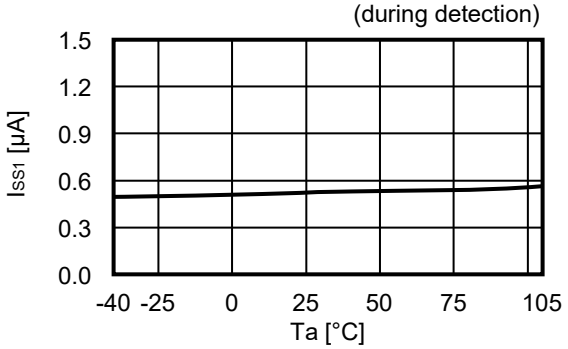
$V_{DET(S)}$ = 16.0 V, V_{DD} = 13.5 V, V_{SENSE} = 13.5 V
(during release)



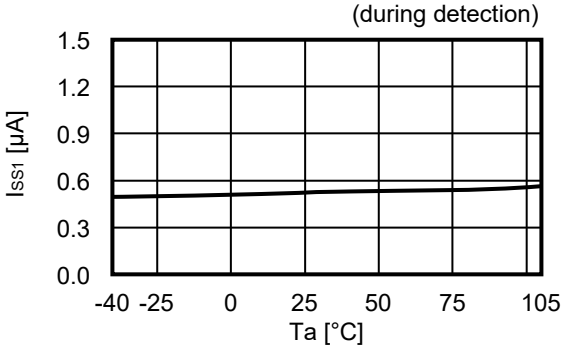
$V_{DET(S)}$ = 18.0 V, V_{DD} = 13.5 V, V_{SENSE} = 13.5 V
(during release)



$V_{DET(S)}$ = 16.0 V, V_{DD} = 13.5 V, V_{SENSE} = 17.0 V
(during detection)

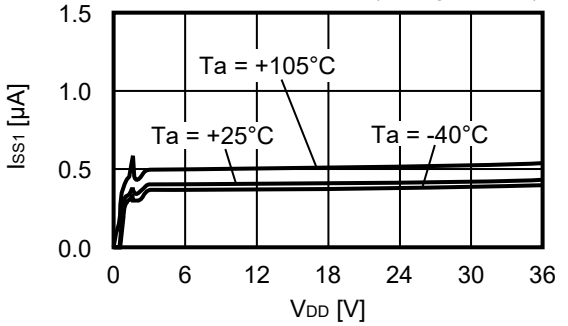


$V_{DET(S)}$ = 18.0 V, V_{DD} = 13.5 V, V_{SENSE} = 19.0 V
(during detection)

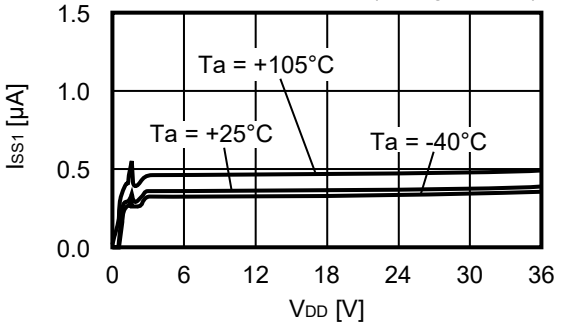


6. Current consumption (I_{SS1}) vs. Power supply voltage (V_{DD}) (No load)

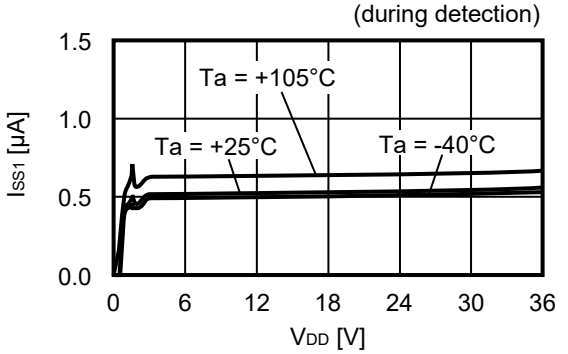
$V_{DET(S)}$ = 16.0 V,
V_{DD} = 0 V → 36.0 V, V_{SENSE} = 13.5 V
(during release)



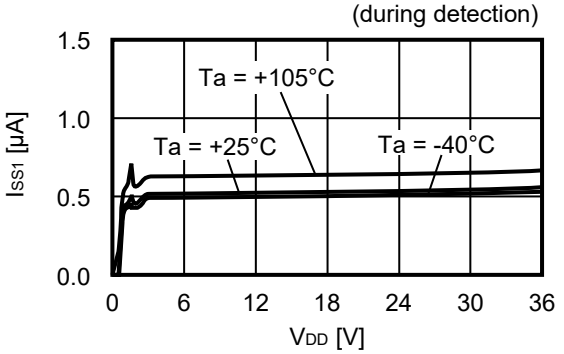
$V_{DET(S)}$ = 18.0 V,
V_{DD} = 0 V → 36.0 V, V_{SENSE} = 13.5 V
(during release)



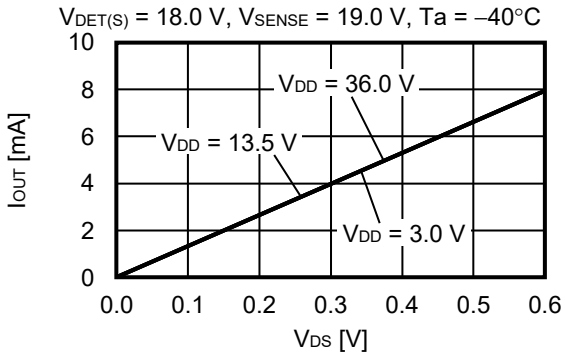
$V_{DET(S)}$ = 16.0 V,
V_{DD} = 0 V → 36.0 V, V_{SENSE} = 17.0 V
(during detection)

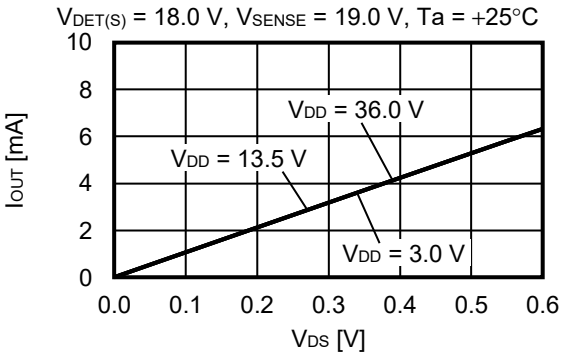


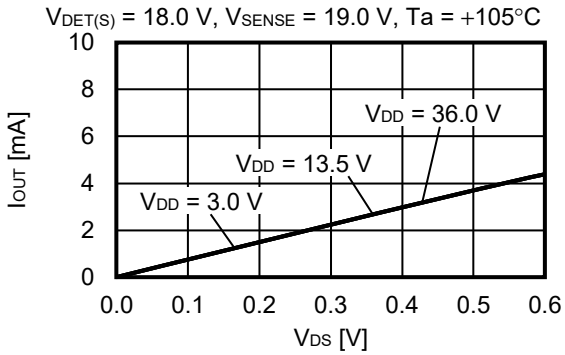
$V_{DET(S)}$ = 18.0 V,
V_{DD} = 0 V → 36.0 V, V_{SENSE} = 19.0 V
(during detection)



7. Nch transistor output current (I_{OUT}) vs. V_{DS}

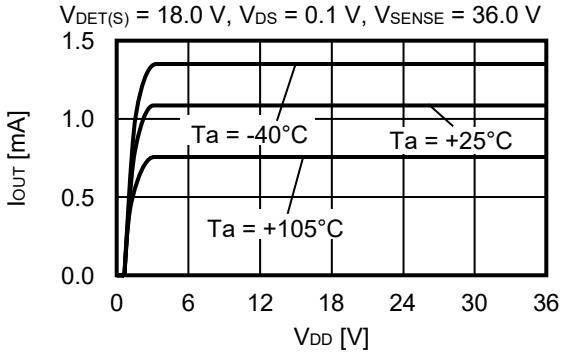






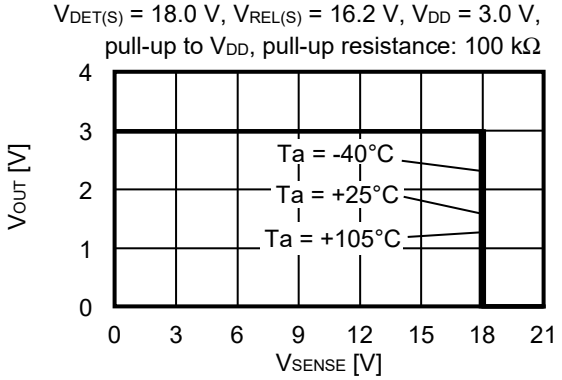
Remark V_{DS}: Drain-to-source voltage of the output transistor

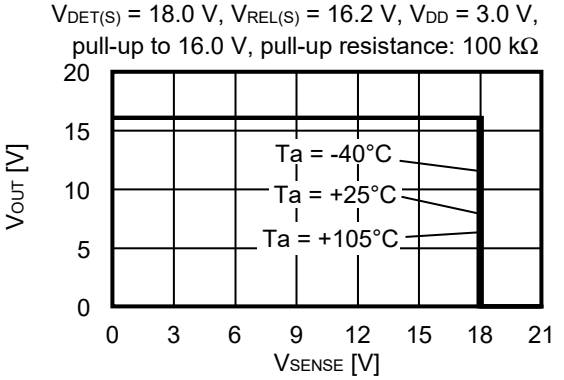
8. Nch transistor output current (I_{OUT}) vs. Power supply voltage (V_{DD})



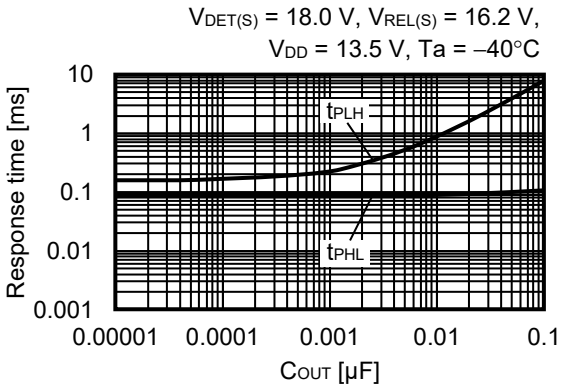
Remark V_{DS}: Drain-to-source voltage of the output transistor

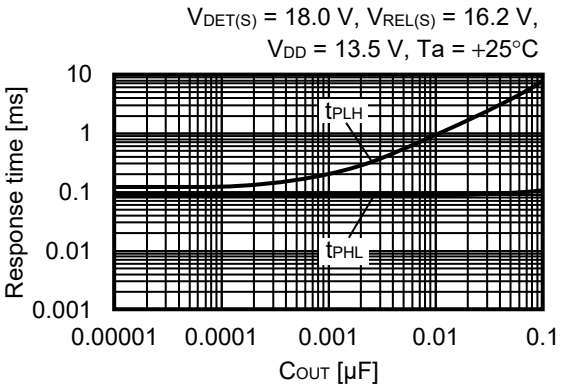
9. Output voltage (V_{OUT}) vs. SENSE pin voltage (V_{SENSE})

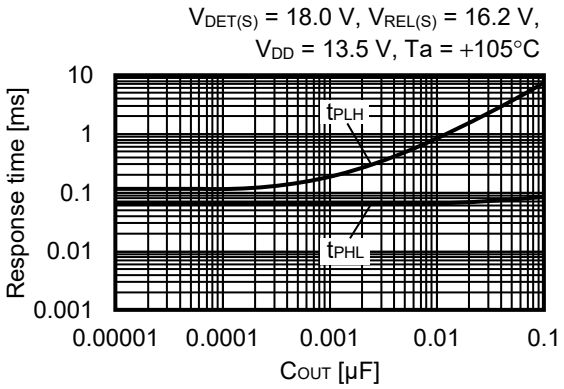


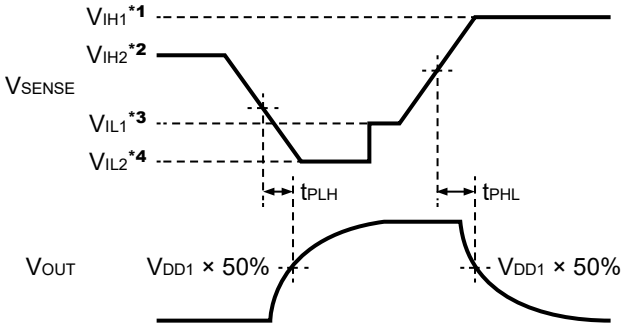


10. Dynamic response vs. Output pin capacitance (C_{OUT}) (CD pin; open)









***1.** $V_{IH1} = V_{DET(S)} + 1.0$ V
***2.** $V_{IH2} = V_{REL(S)} + 1.0$ V
***3.** $V_{IL1} = V_{DET(S)} - 1.0$ V
***4.** $V_{IL2} = V_{REL(S)} - 1.0$ V

Figure 24 Test Condition of Response Time

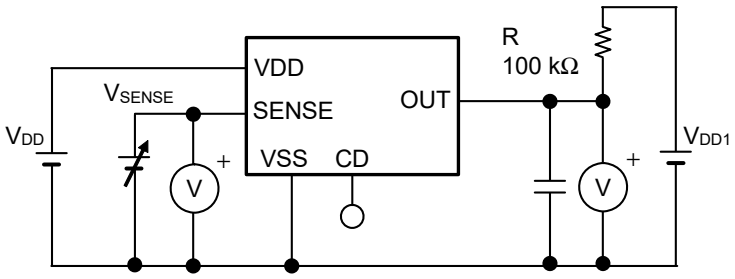
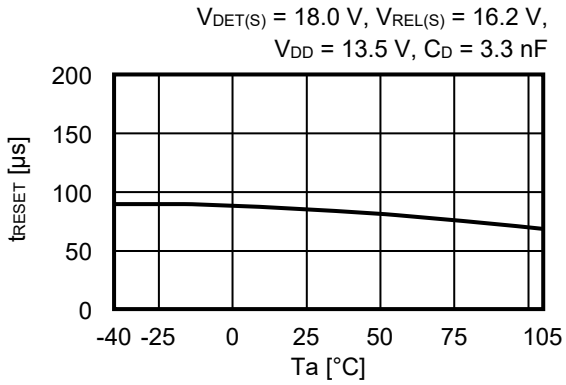


Figure 25 Test Circuit of Response Time

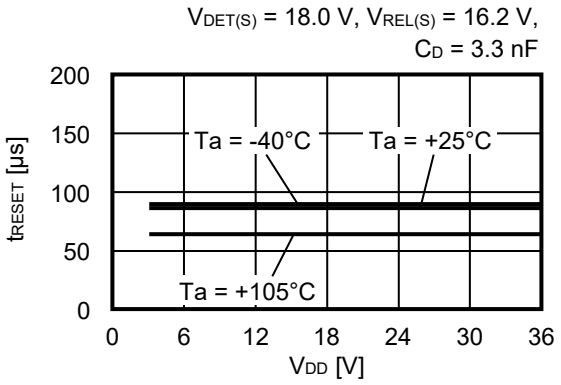
Caution 1. The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.
2. When the CD pin is open, a double pulse may appear at release.
To avoid the double pulse, attach 1 nF or more capacitor to the CD pin.

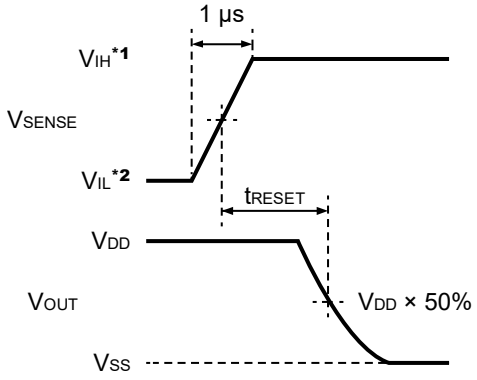
■ Reference Data

1. Detection response time (t_{RESET}) vs. Temperature (Ta)



2. Detection response time (t_{RESET}) vs. Power supply voltage (V_{DD})





***1.** $V_{IH} = V_{DET(S)} + 1.0$ V
***2.** $V_{IL} = V_{DET(S)} - 1.0$ V

Figure26 Test Condition of Detection Response Time

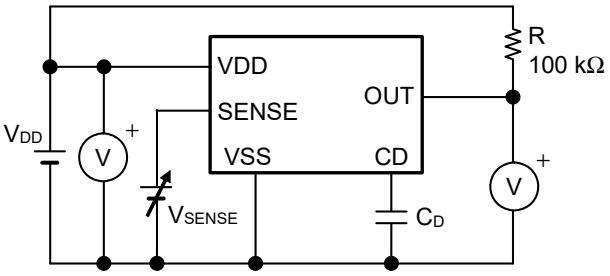
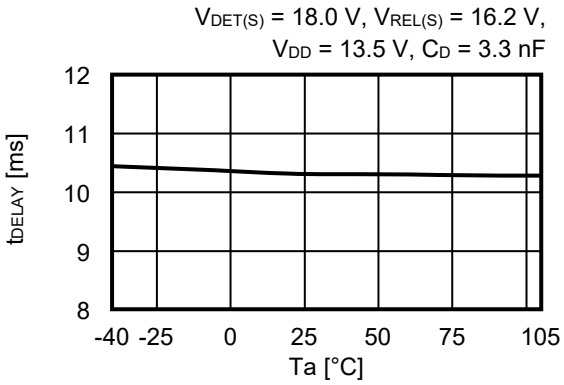


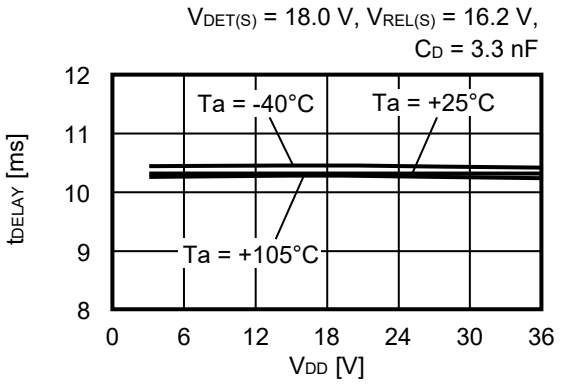
Figure 27 Test Circuit of Detection Response Time

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

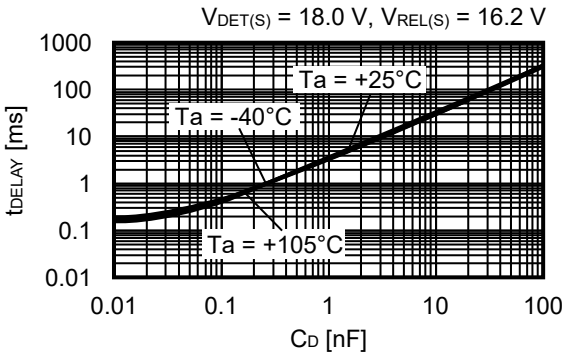
3. Release delay time (t_{DELAY}) vs. Temperature (Ta)

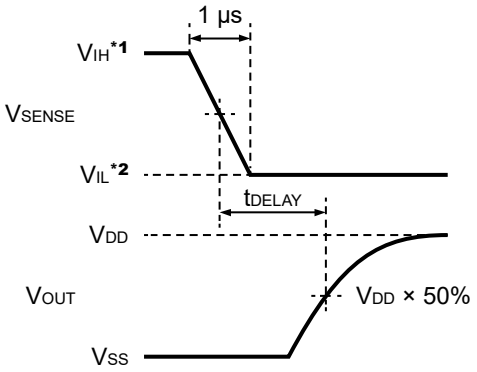


4. Release delay time (t_{DELAY}) vs. Power supply voltage (V_{DD})



5. Release delay time (t_{DELAY}) vs. CD pin capacitance (C_D) (Without output pin capacitance)





***1.** $V_{IH} = V_{REL(S)} + 1.0$ V

***2.** $V_{IL} = V_{REL(S)} - 1.0$ V

Figure 28 Test Condition of Release Delay Time

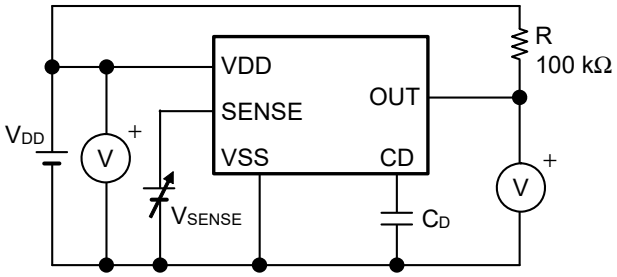
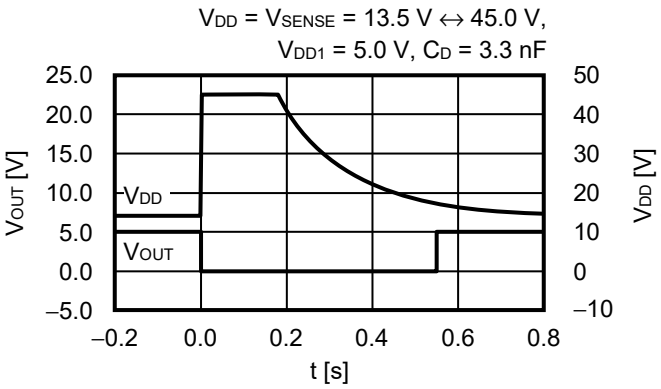


Figure 29 Test Circuit of Release Delay Time

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

6. Load dump characteristics (Ta = +25°C)

6. 1 $V_{DET(S)}$ = 18.0 V



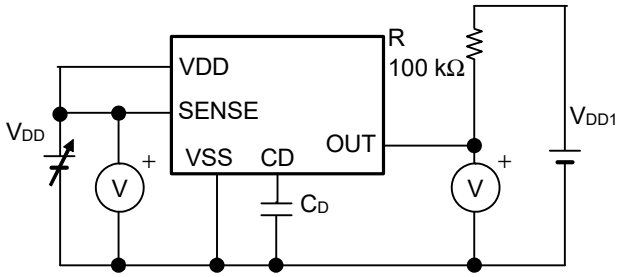
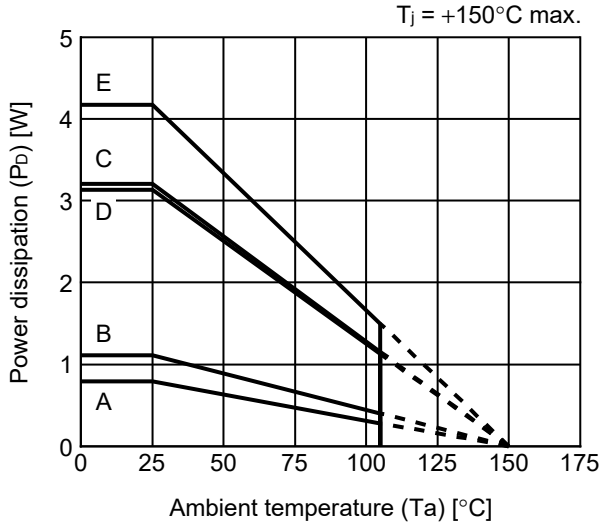


Figure 30

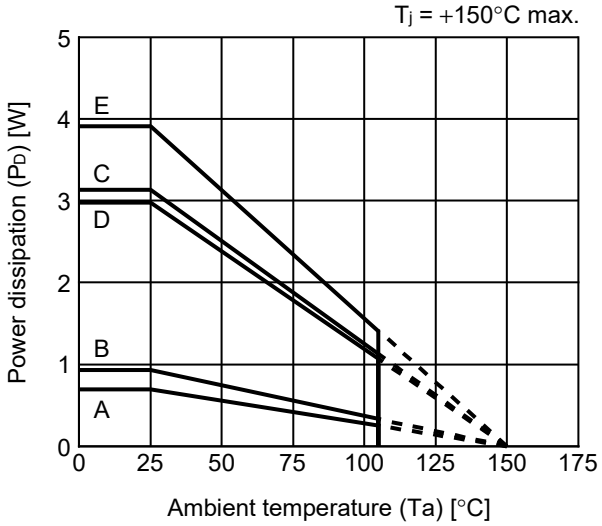
■ Power Dissipation

HTMSOP-8



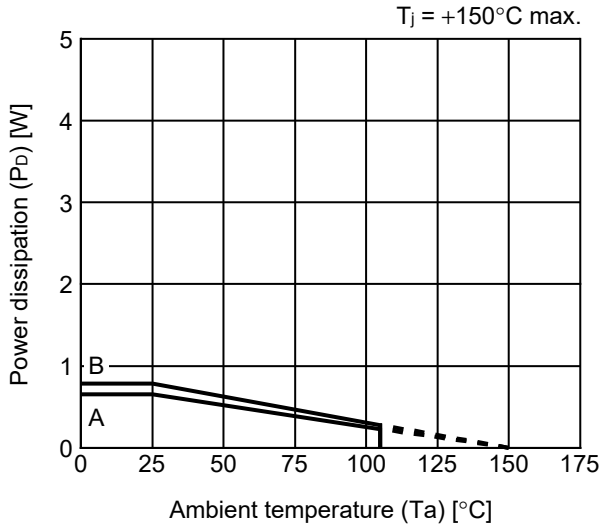
Board	Power Dissipation (P_D)
A	0.79 W
B	1.11 W
C	3.21 W
D	3.13 W
E	4.17 W

HSNT-8(2030)



Board	Power Dissipation (P_D)
A	0.69 W
B	0.93 W
C	3.13 W
D	2.98 W
E	3.91 W

SOT-23-5

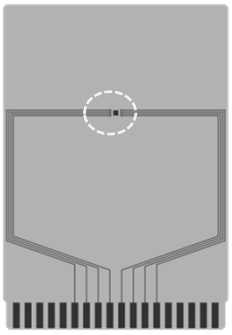


Board	Power Dissipation (P_D)
A	0.65 W
B	0.78 W
C	–
D	–
E	–

HTMSOP-8 Test Board

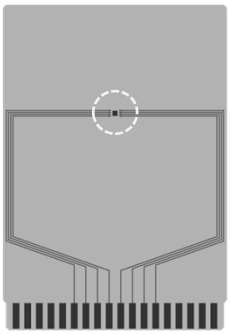
IC Mount Area

(1) Board A



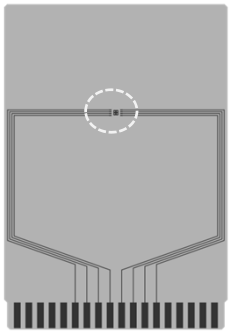
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

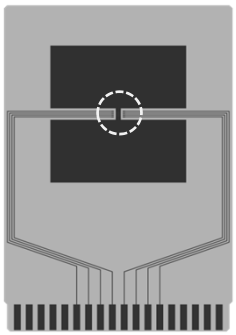
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HTMSOP8-A-Board-SD-1.0

HTMSOP-8 Test Board

IC Mount Area

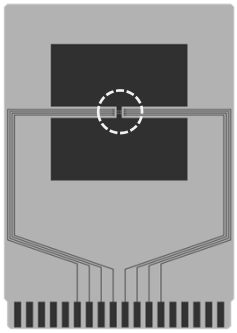
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



enlarged view

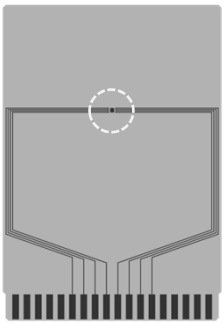
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HTMSOP8-A-Board-SD-1.0

HSNT-8(2030) Test Board

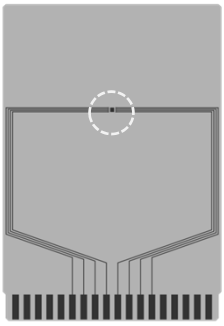
IC Mount Area

(1) Board A



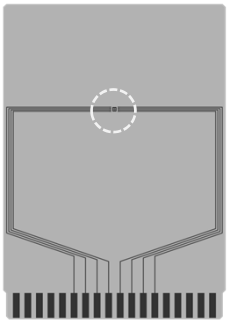
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

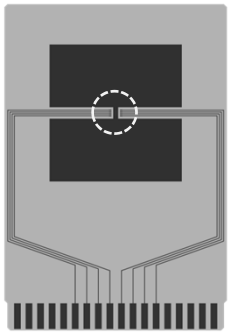
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-A-Board-SD-2.0

HSNT-8(2030) Test Board

IC Mount Area

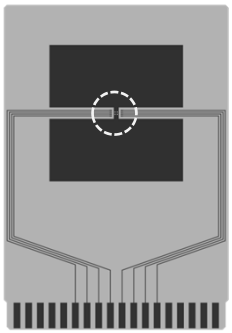
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



enlarged view

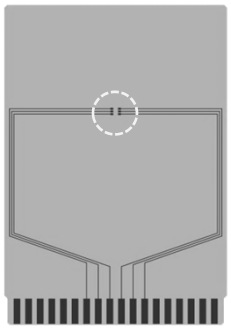
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-A-Board-SD-2.0

SOT-23-3/3S/5/6 Test Board

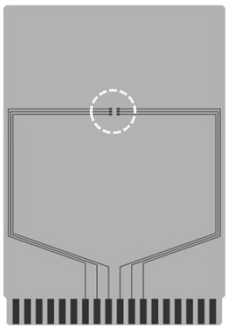
IC Mount Area

(1) Board A



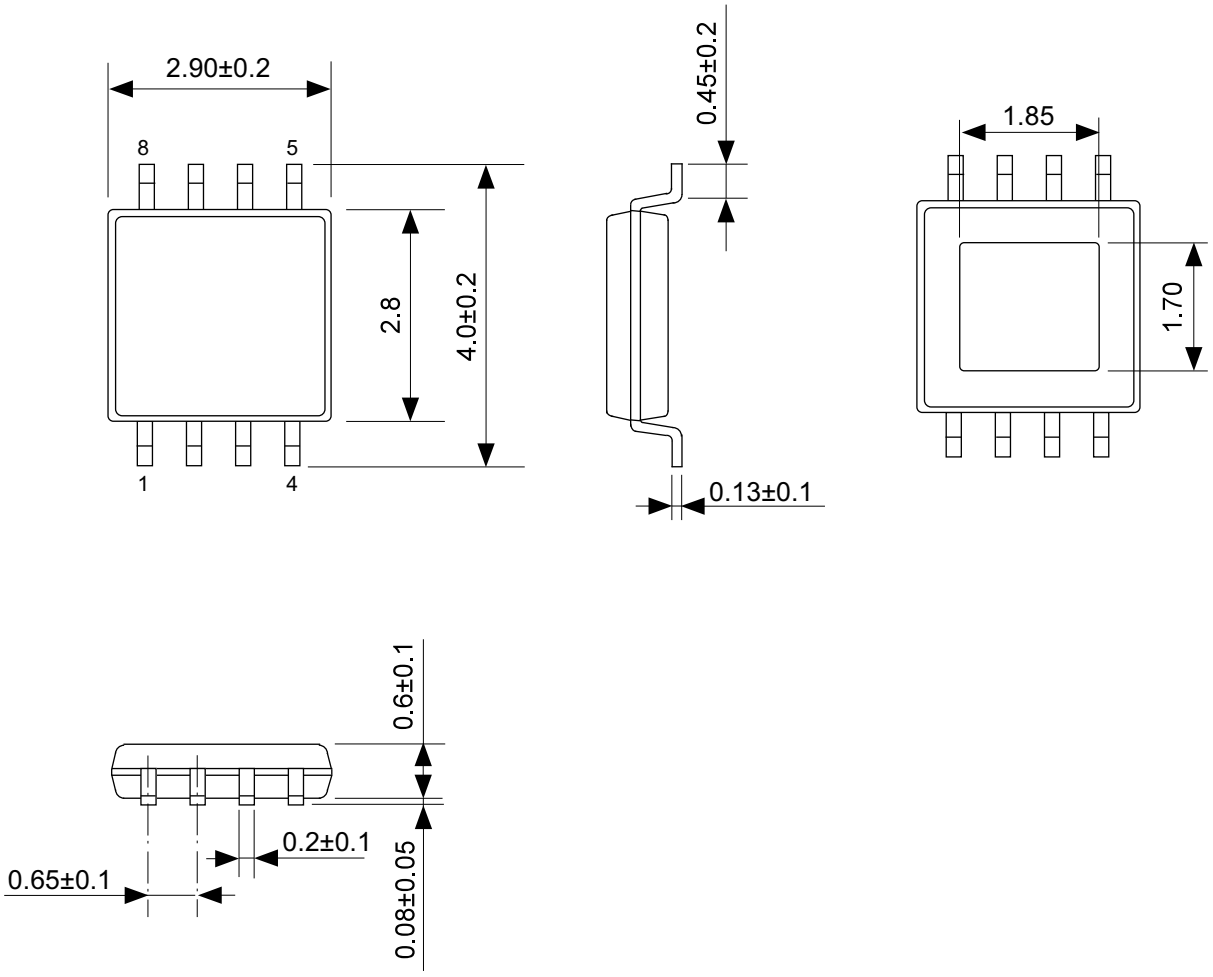
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



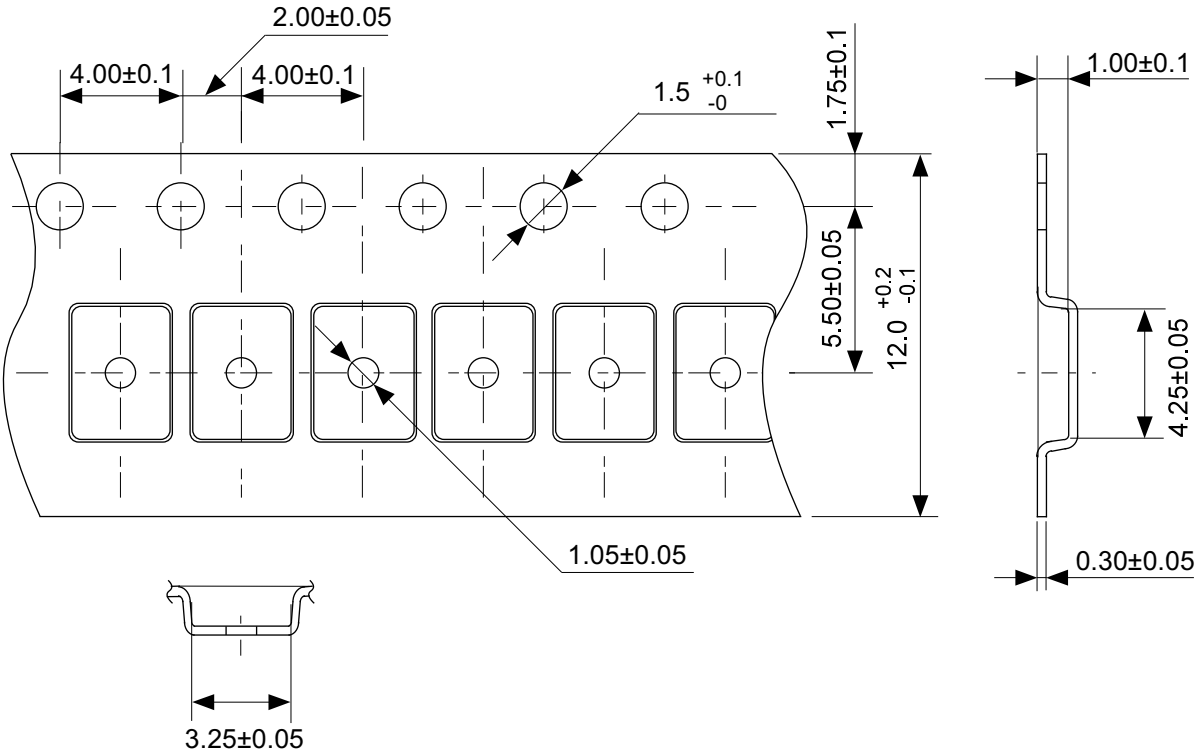
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

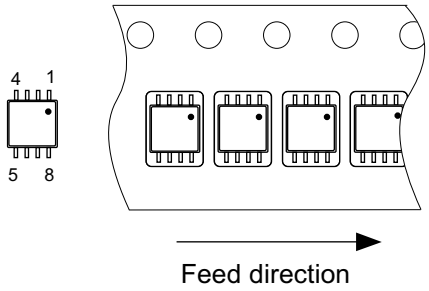
No. SOT23x-A-Board-SD-2.0



No. FP008-A-P-SD-2.0

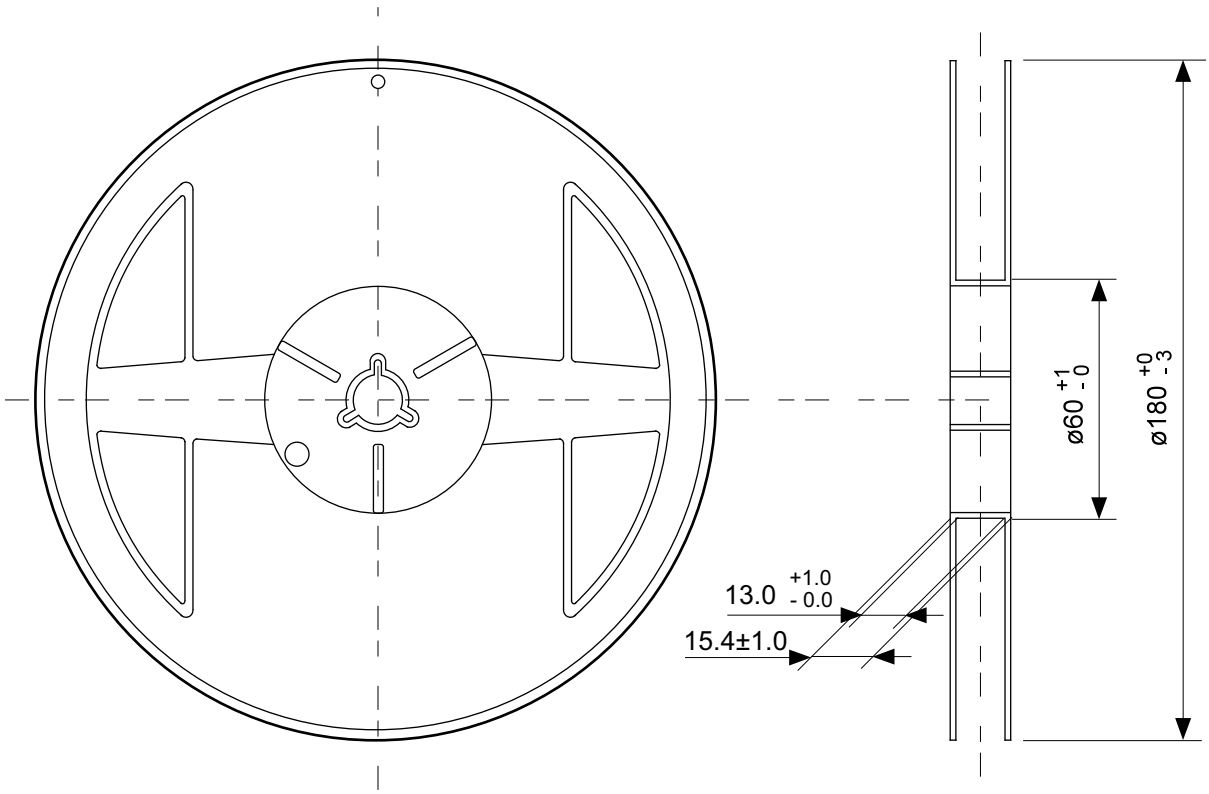
TITLE	HTMSOP8-A-PKG Dimensions
No.	FP008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



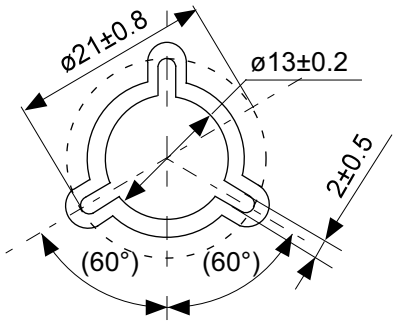


No. FP008-A-C-SD-1.0

TITLE	HTMSOP8-A-Carrier Tape
No.	FP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

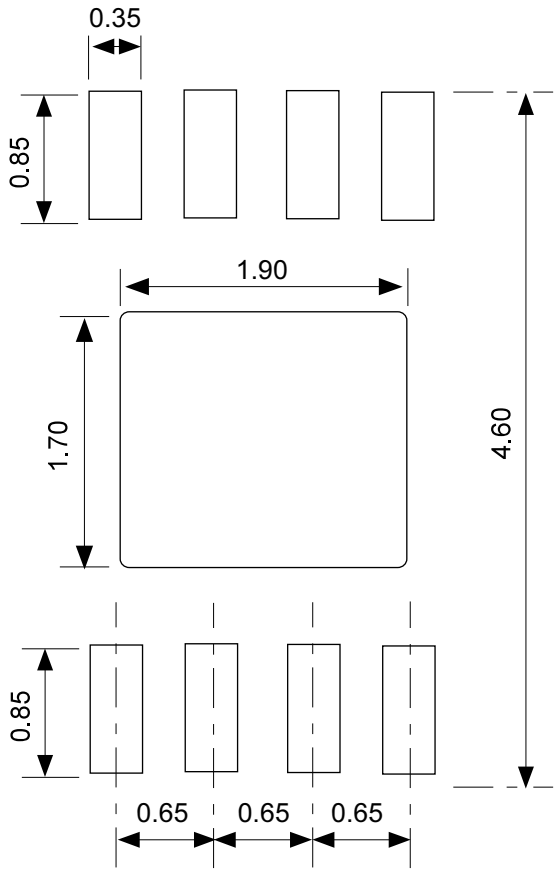


Enlarged drawing in the central part



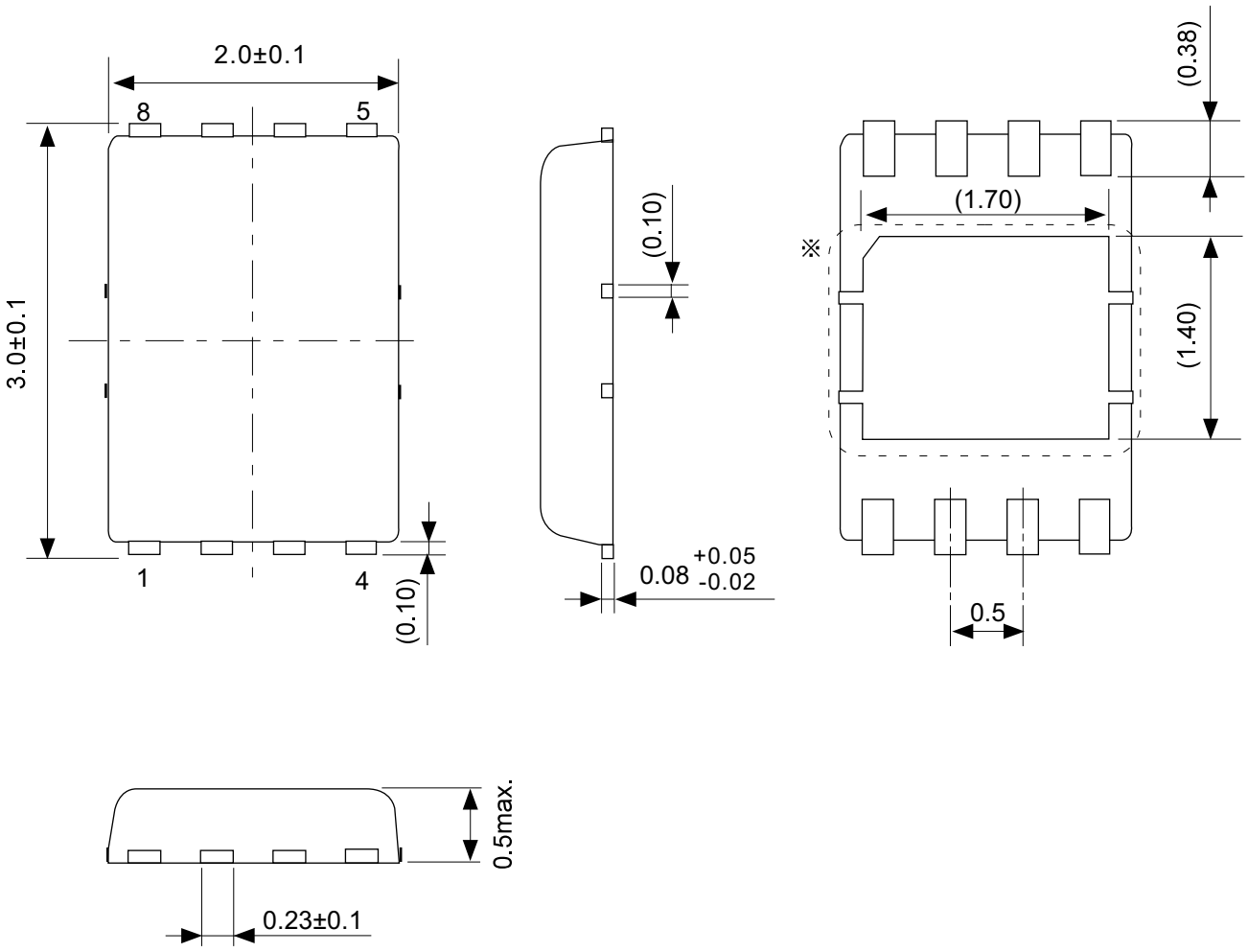
No. FP008-A-R-SD-2.0

TITLE	HTMSOP8-A-Reel		
No.	FP008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



No. FP008-A-L-SD-2.0

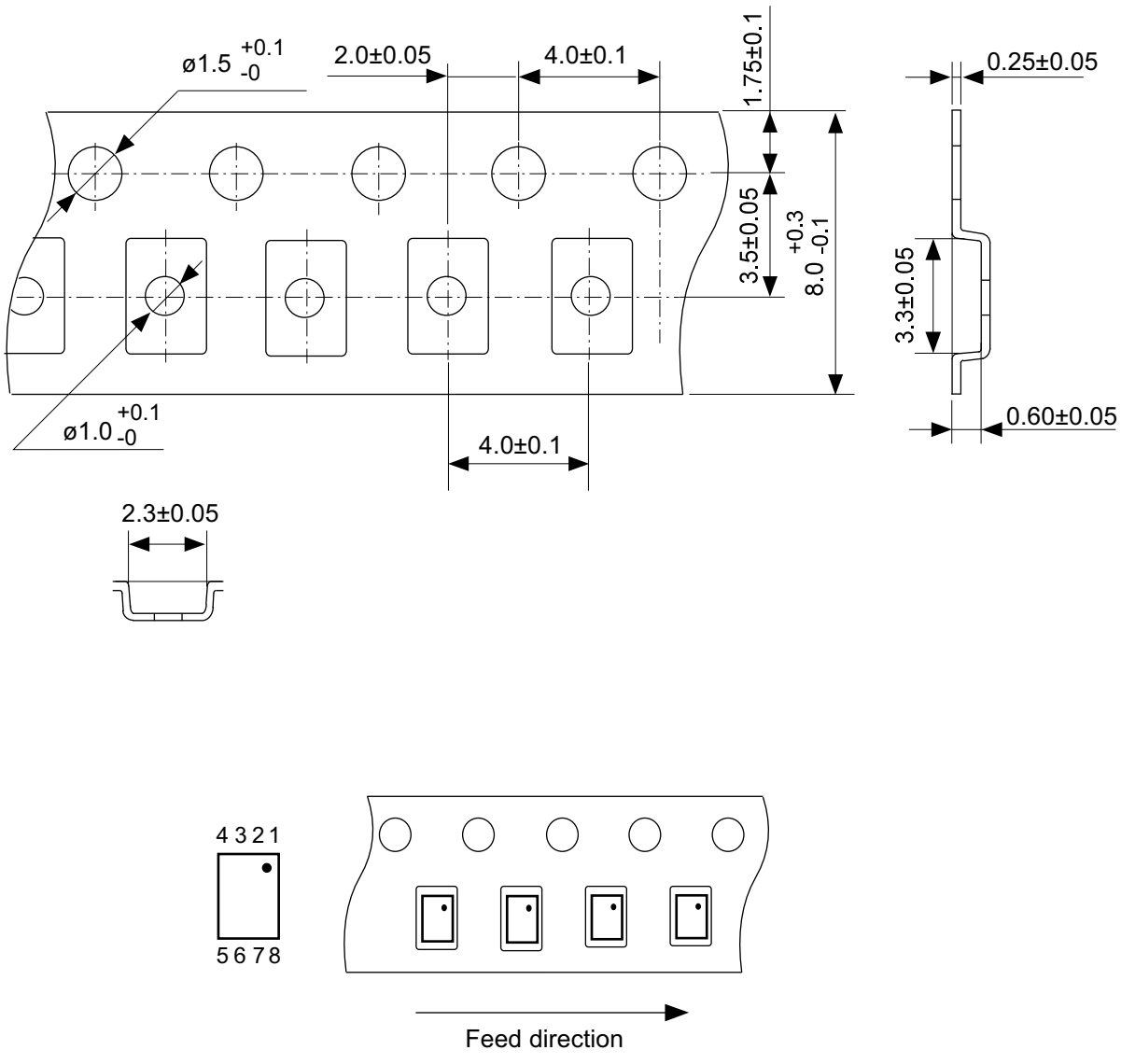
TITLE	HTMSOP8-A -Land Recommendation
No.	FP008-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

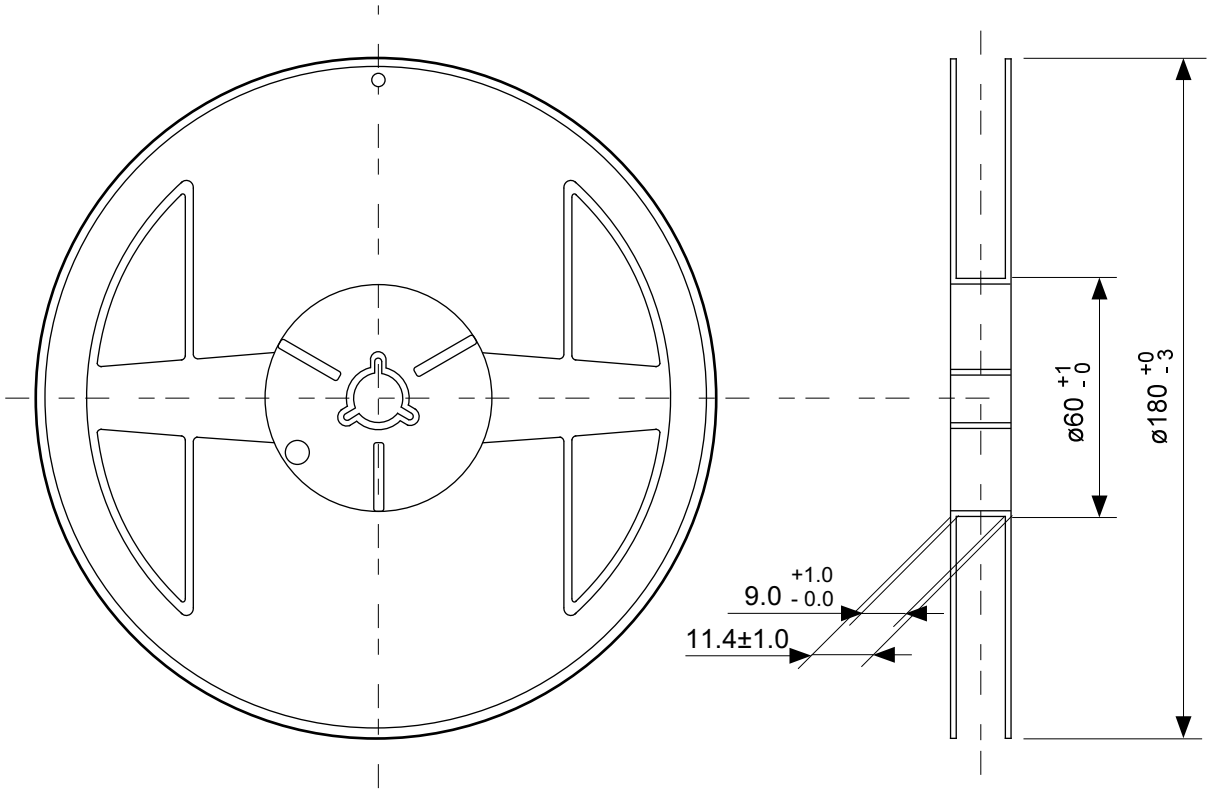
No. PP008-A-P-SD-2.0

TITLE	HSNT-8-A-PKG Dimensions
No.	PP008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

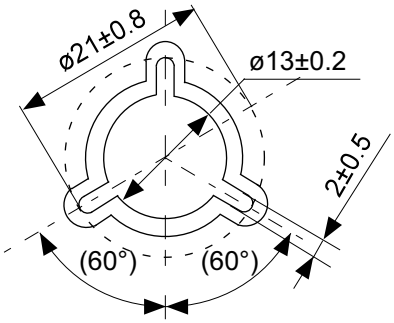


No. PP008-A-C-SD-1.0

TITLE	HSNT-8-A-Carrier Tape
No.	PP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

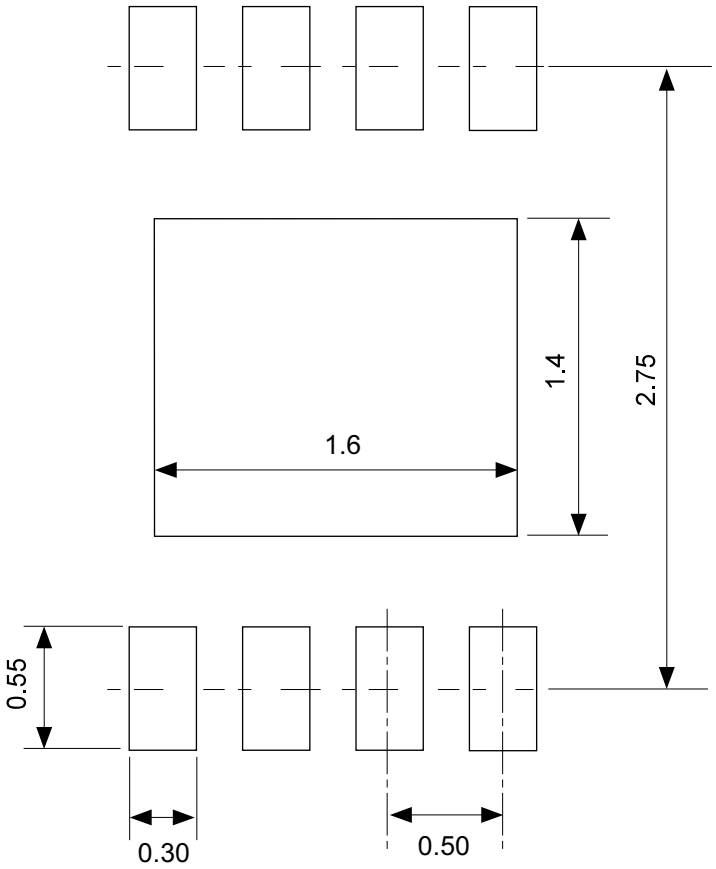


Enlarged drawing in the central part



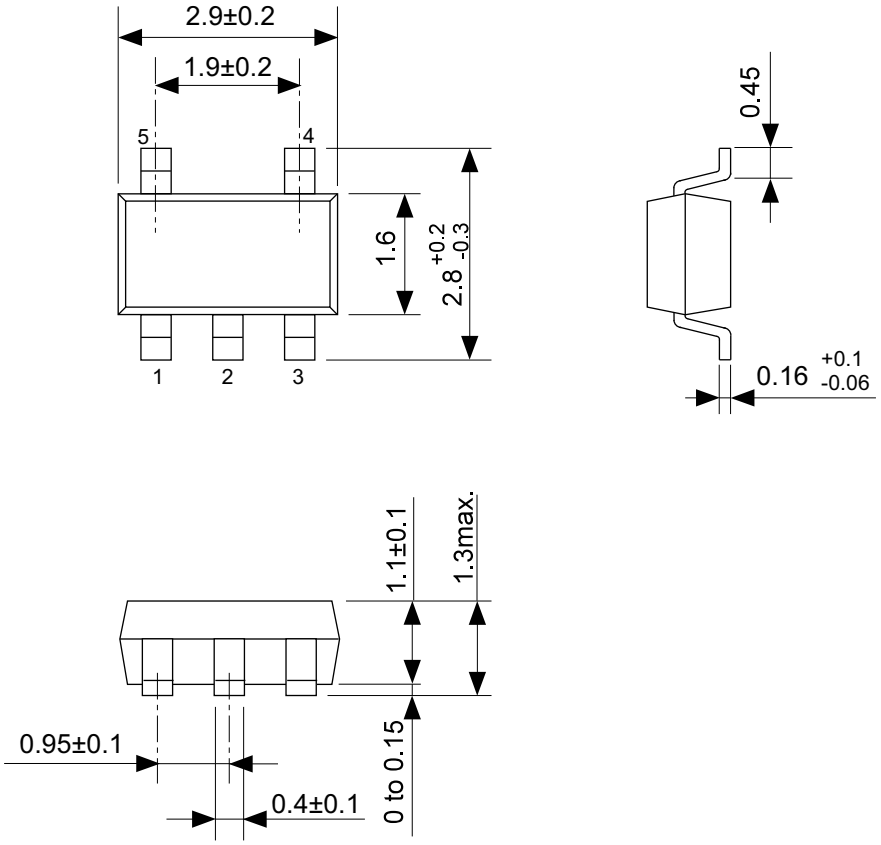
No. PP008-A-R-SD-2.0

TITLE	HSNT-8-A-Reel		
No.	PP008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



No. PP008-A-L-SD-1.0

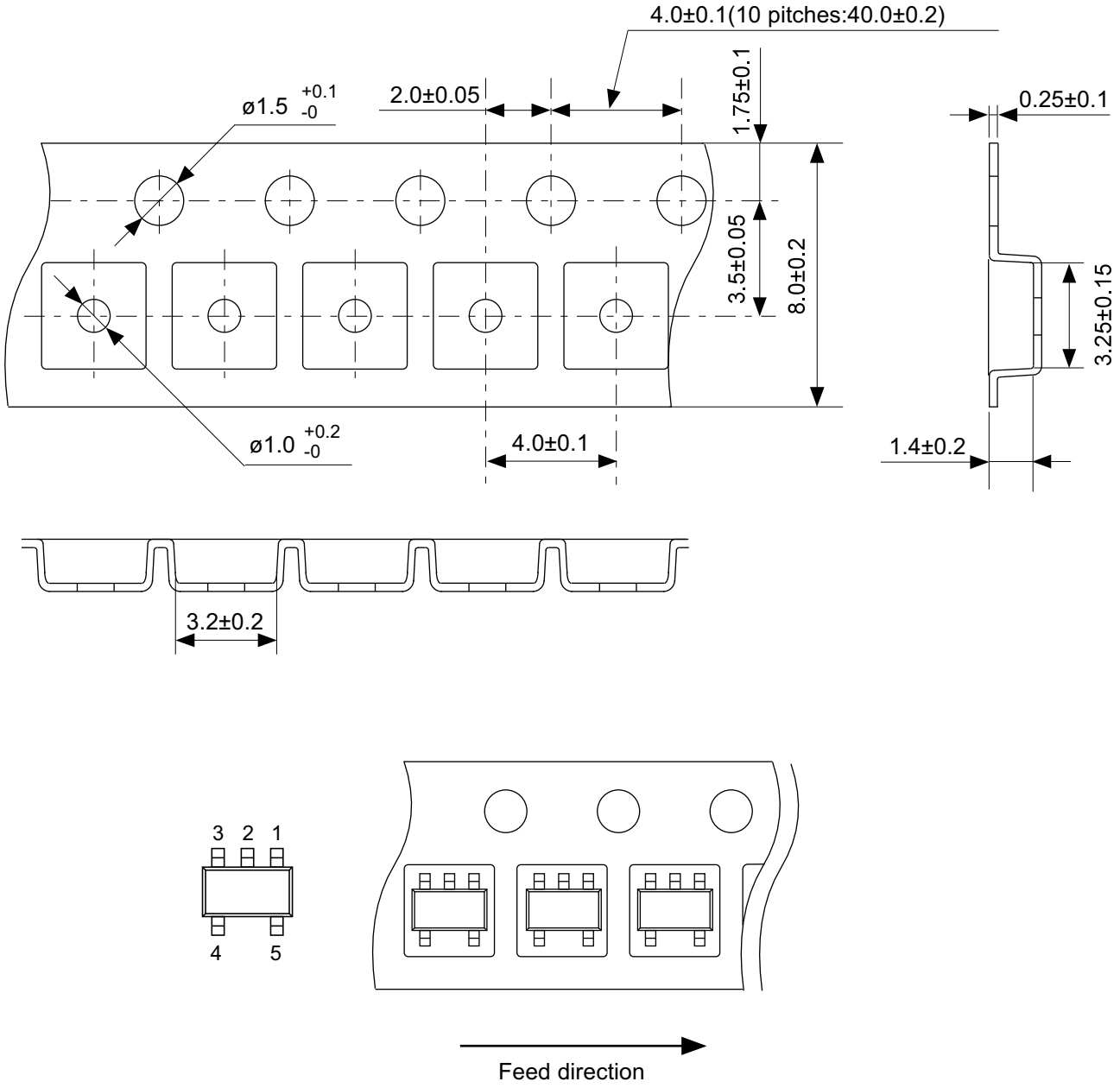
TITLE	HSNT-8-A -Land Recommendation
No.	PP008-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. MP005-A-P-SD-1.3

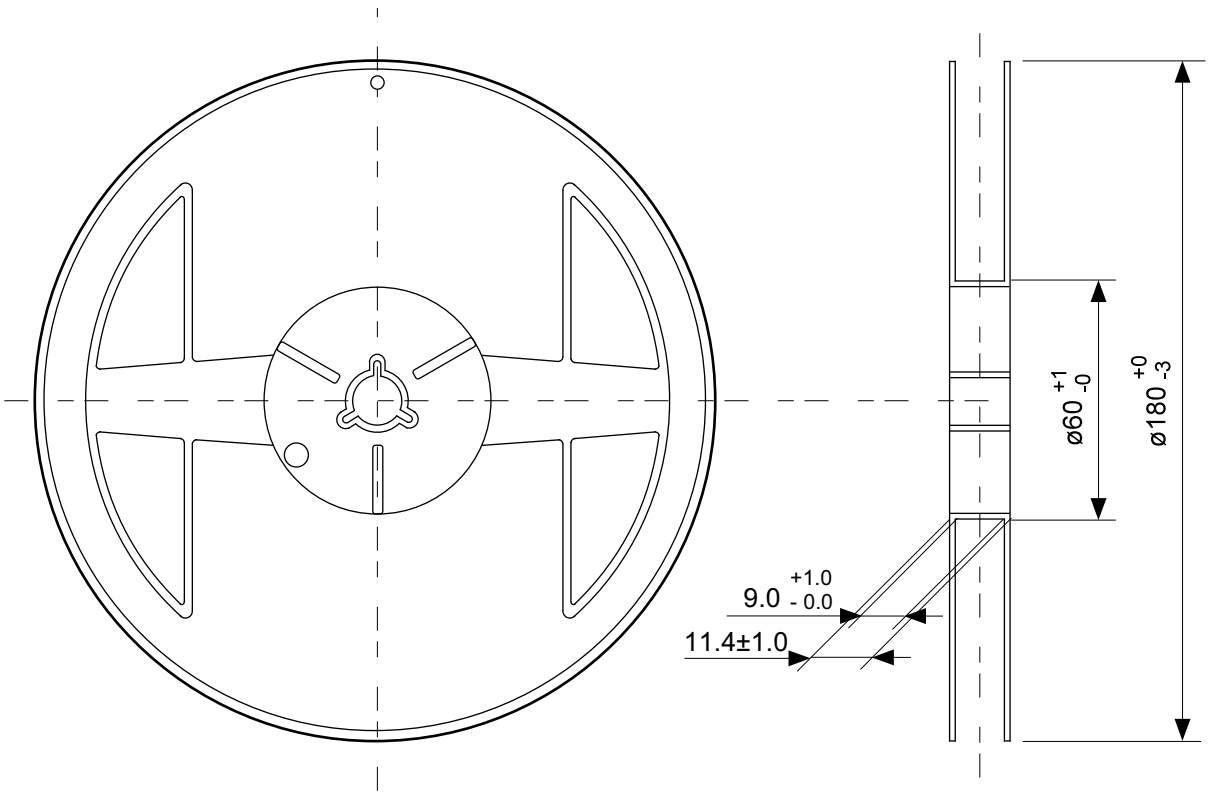
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

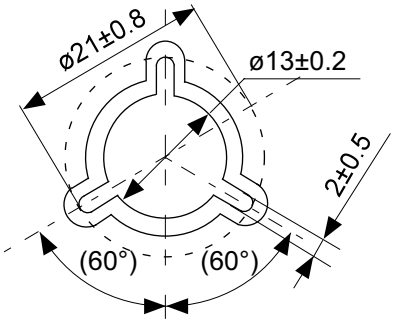


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. MP005-A-R-SD-2.0

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-2.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

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2.4-2019.07