S-35770 A Series

CONVENIENCE TIMER

AUTOMOTIVE, 125°C OPERATION, 2-WIRE COUNTER

www.ablic.com

Rev.2.0_00

The convenience timer is a CMOS timer IC which operates with low current consumption, and is suitable for the time management of the relative time.
The S-35770 Series counts the number of clocks input from an external device.
The counter of the S-35770 Series is a 24-bit binary-up counter.
The counter data can be read via a 2-wire serial interface.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.**

■ Features

- External clock signal count function: Countable from 0 to 16,777,215, with output pin for counter loop flag
- Low current consumption: 0.01 μA typ. (V_{DD} = 3.0 V, Ta = +25°C, out of communication (CLKIN pin = 0 V))
- Wide range of operation voltage: 1.5 V to 5.5 V
- 2-wire (I^2C-bus) CPU interface
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*1

***1.** Contact our sales office for details.

■ Application

- Various pulse counters

■ Package

- TMSOP-8

■ Block Diagram

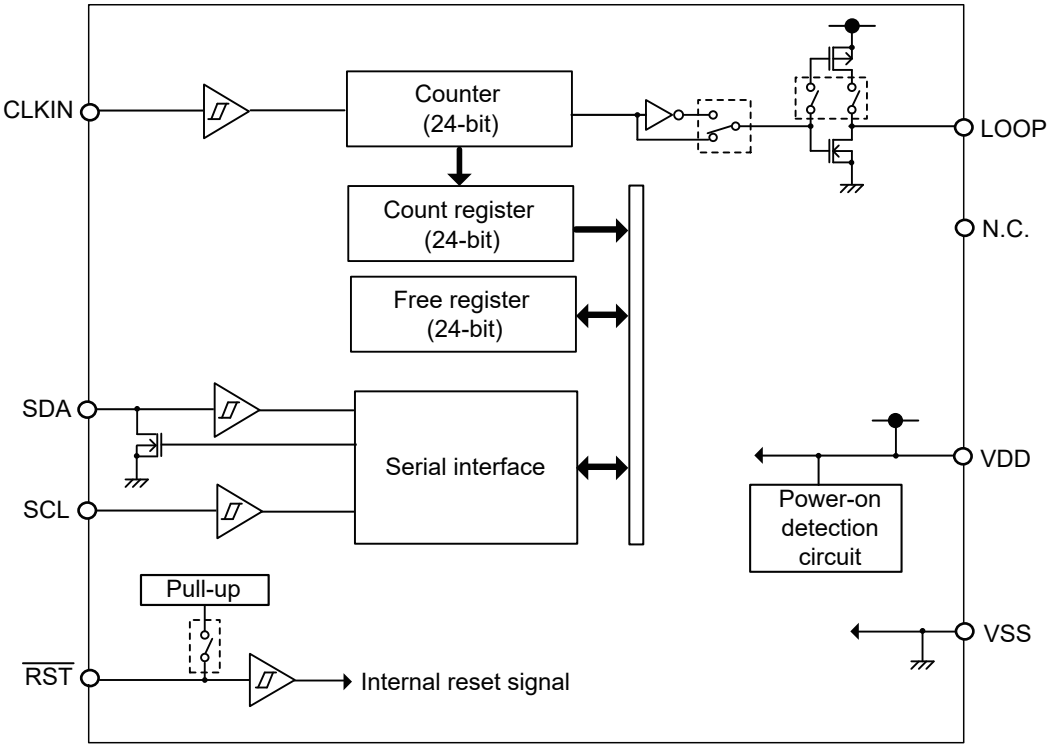


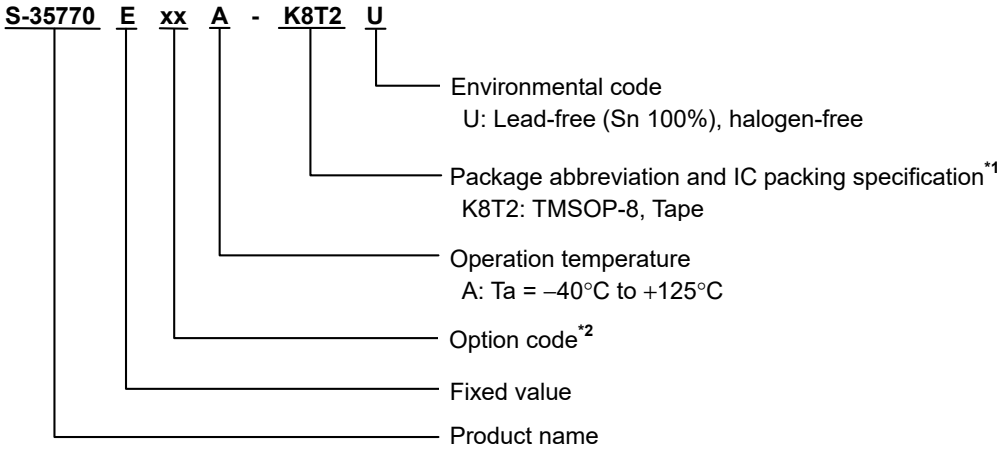
Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** A sequence number added by the optional function that is user-selected.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	$\overline{RST}$ Pin*1	LOOP Pin Output Form*2	LOOP Pin Output*3
S-35770E01A-K8T2U	Without pull-up resistor	CMOS output	"L"

***1.** The pin with / without pull-up resistor is selectable. Refer to "■ **Pin Functions**".
***2.** The pin of Nch open-drain output / CMOS output is selectable. Refer to "■ **Pin Functions**".
***3.** The output status at power-on.

Remark Please contact our sales office for products with specifications other than the above.

■ Pin Configuration

1. TMSOP-8

Top view

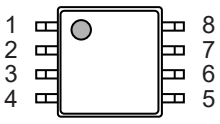


Figure 2

Table 3 List of Pins

Pin No.	Symbol	Description	I/O	Configuration
1	$\overline{\text{RST}}$	Input pin for reset signal	Input	CMOS input (With / without pull-up resistor is selectable)
2	NC*1	No connection	–	–
3	CLKIN	Input pin for external clock	Input	CMOS input
4	VSS	GND pin	–	–
5	LOOP	Output pin for counter loop flag	Output	Nch open-drain output / CMOS output is selectable
6	SDA	I/O pin for serial data	Bi-directional	Nch open-drain output, CMOS input
7	SCL	Input pin for serial clock	Input	CMOS input
8	VDD	Pin for positive power supply	–	–

***1.** The NC pin is electrically open.
Therefore, leave it open or connect it to VDD pin or VSS pin.

■ Pin Functions

1. SDA (I/O for serial data) pin

This is a data input / output pin for I^2C-bus interface. The SDA pin inputs / outputs data by synchronizing with a clock pulse from the SCL pin. This pin has CMOS input and Nch open-drain output. Generally in use, the SDA pin is pulled up to V_{DD} potential via a resistor, and is used with wired-OR connection of other device of Nch open-drain output or open collector output.

2. SCL (Input for serial clock) pin

This is a clock input pin for I^2C-bus interface. The SDA pin inputs / outputs data by synchronizing with this clock

3. $\overline{\text{RST}}$ (Input for reset signal) pin

This pin inputs the reset signal. The counter is reset when inputting "L" to the $\overline{\text{RST}}$ pin. When inputting "H" to the $\overline{\text{RST}}$ pin, the count-up action of the counter is started.
Also, the $\overline{\text{RST}}$ pin with / without a pull-up resistor can be selected.

4. CLKIN (Input for external clock) pin

This pin inputs an external clock. The counter is incremented by 1 when the CLKIN pin input changes from "L" to "H".

5. LOOP (Output for counter loop flag) pin

Each time the counter loops back to 0 after reaching 16,777,215, the LOOP pin performs a toggle operation.
Regarding the operation of the LOOP pin, refer to "■ **LOOP Pin**".
The LOOP pin output form of Nch open-drain output / CMOS output can be selected.

6. VDD (Positive power supply) pin

Connect this pin with a positive power supply. Regarding the values of voltage to be applied, refer to "■ **Recommended Operation Condition**".

7. VSS pin

Connect this pin to GND.

■ Equivalent Circuits of Pins

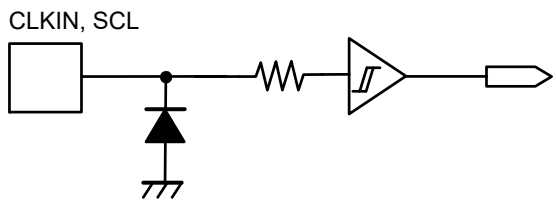


Figure 3 CLKIN Pin and SCL Pin

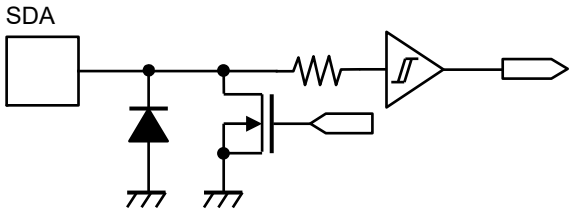


Figure 4 SDA Pin

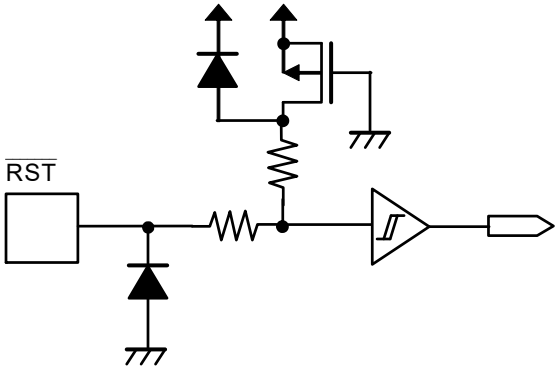


Figure 5 $\overline{\text{RST}}$ Pin (With Pull-up Resistor)

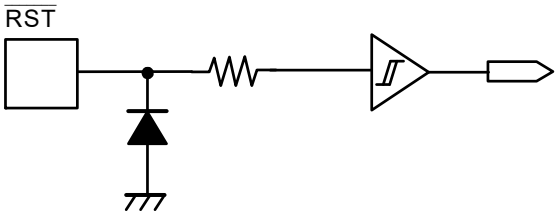


Figure 6 $\overline{\text{RST}}$ Pin (Without Pull-up Resistor)

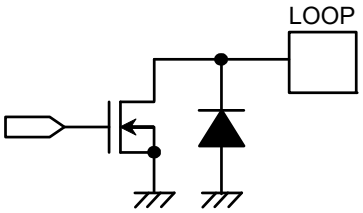


Figure 7 LOOP Pin (Nch Open-drain Output)

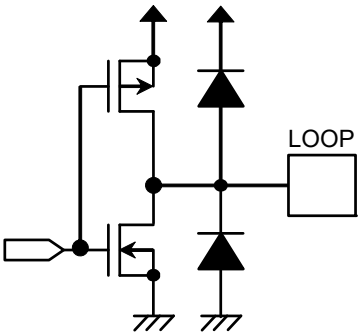


Figure 8 LOOP Pin (CMOS Output)

■ Absolute Maximum Ratings

Table 4

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	–	V_{SS} – 0.3 to V_{SS} + 6.5	V
Input voltage	V_{IN}	CLKIN, SDA, SCL, $\overline{RST}$ *1	V_{SS} – 0.3 to V_{SS} + 6.5	V
		$\overline{RST}$ *2	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 6.5	V
Output voltage	V_{OUT}	SDA, LOOP*3	V_{SS} – 0.3 to V_{SS} + 6.5	V
		LOOP*4	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 6.5	V
Operation ambient temperature*5	T_{opr}	–	–40 to +125	°C
Storage temperature	T_{stg}	–	–55 to +150	°C

***1.** When a product without a pull-up resistor is selected.
***2.** When a product with a pull-up resistor is selected.
***3.** When an Nch open-drain output product is selected.
***4.** When a CMOS output product is selected.
***5.** Conditions with no condensation or frost. Condensation or frost causes short-circuiting between pins, resulting in a malfunction.

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operation Condition

Table 5

(V_{SS} = 0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operation power supply voltage	V_{DD}	Ta = –40°C to +125°C	1.5	–	5.5	V

■ DC Electrical Characteristics

Table 6

($Ta = -40°C$ to $+125°C$, $V_{SS} = 0$ V)

Item	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	–	V_{DD} = 3.0 V, Ta = −40°C to +85°C, Out of communication (CLKIN pin = 0 V), LOOP pin = no load	–	0.01	0.1	µA
			V_{DD} = 3.0 V, Ta = +125°C, Out of communication (CLKIN pin = 0 V), LOOP pin = no load	–	0.7	0.95	µA
Current consumption 2	I_{DD2}	–	V_{DD} = 3.0 V, f_{SCL} = 1 MHz, During communication, LOOP pin = no load	–	170	300	µA
High level input leakage current	I_{IZH}	CLKIN, SDA, SCL, $\overline{RST}$	$V_{IN} = V_{DD}$	−0.5	–	0.5	µA
Low level input leakage current	I_{IZL}	CLKIN, SDA, SCL, $\overline{RST}$ *1	$V_{IN} = V_{SS}$	−0.5	–	0.5	µA
High level output leakage current	I_{OZH}	SDA	$V_{OUT} = V_{DD}$	−0.5	–	0.5	µA
Low level output leakage current	I_{OZL}	SDA	$V_{OUT} = V_{SS}$	−0.5	–	0.5	µA
High level input voltage	V_{IH}	CLKIN, SDA, SCL, $\overline{RST}$ *1	–	$0.7 \times V_{DD}$	–	$V_{SS} + 5.5$	V
		$\overline{RST}$ *2	–	$0.7 \times V_{DD}$	–	$V_{DD} + 0.3$	V
Low level input voltage	V_{IL}	CLKIN, SDA, SCL, $\overline{RST}$	–	$V_{SS} - 0.3$	–	$0.3 \times V_{DD}$	V
Low level output voltage	V_{OL}	SDA	I_{OL} = 2.0 mA	–	–	0.4	V
Low level input current*2	I_{IL}	$\overline{RST}$	V_{DD} = 3.0 V, $V_{IN} = V_{SS}$	−100	−30	−5	µA

***1.** When a product without a pull-up resistor is selected.

***2.** When a product with a pull-up resistor is selected.

■ AC Electrical Characteristics

Table 7 Measurement Conditions

Input pulse voltage	$V_{IH} = 0.8 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$
Input pulse rise / fall time	20 ns
Output reference voltage	$V_{OH} = 0.7 \times V_{DD}$, $V_{OL} = 0.3 \times V_{DD}$
Output load	100 pF

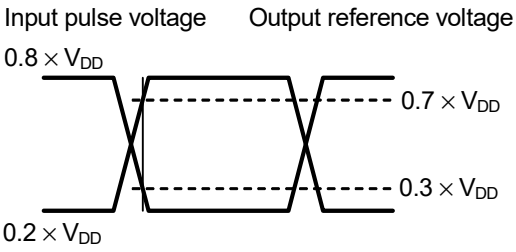


Figure 9 Input / Output Waveform during AC Measurement

Table 8 AC Electrical Characteristics

(Ta = −40°C to +125°C)

Item	Symbol	V_{DD} = 1.5 V to 2.5 V		V_{DD} = 2.5 V to 5.5 V		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	400	0	1000	kHz
SCL clock "L" time	t_{LOW}	1.3	–	0.4	–	µs
SCL clock "H" time	t_{HIGH}	0.6	–	0.3	–	µs
SDA output delay time*1	t_{AA}	–	0.9	–	0.5	µs
Start condition set-up time	$t_{SU.STA}$	0.6	–	0.25	–	µs
Start condition hold time	$t_{HD.STA}$	0.6	–	0.25	–	µs
Data input set-up time	$t_{SU.DAT}$	100	–	80	–	ns
Data input hold time	$t_{HD.DAT}$	0	–	0	–	ns
Stop condition set-up time	$t_{SU.STO}$	0.6	–	0.25	–	µs
SCL, SDA rise time	t_R	–	0.3	–	0.3	µs
SCL, SDA fall time	t_F	–	0.3	–	0.3	µs
Bus release time	t_{BUF}	1.3	–	0.5	–	µs
Noise suppression time	t_I	–	50	–	50	ns
CLKIN clock frequency	f_{CLKIN}	0	400	0	1000	kHz
CLKIN clock "L" time	t_{CLKIN_L}	1.3	–	0.4	–	µs
CLKIN clock "H" time	t_{CLKIN_H}	0.6	–	0.3	–	µs
CLKIN rise time	t_{CLKIN_R}	–	0.3	–	0.3	µs
CLKIN fall time	t_{CLKIN_F}	–	0.3	–	0.3	µs

*1. Since the output form of the SDA pin is Nch open-drain output, the SDA output delay time is determined by the values of the load resistance and load capacitance outside the IC. **Figure 11** shows the relationship between the output load values.

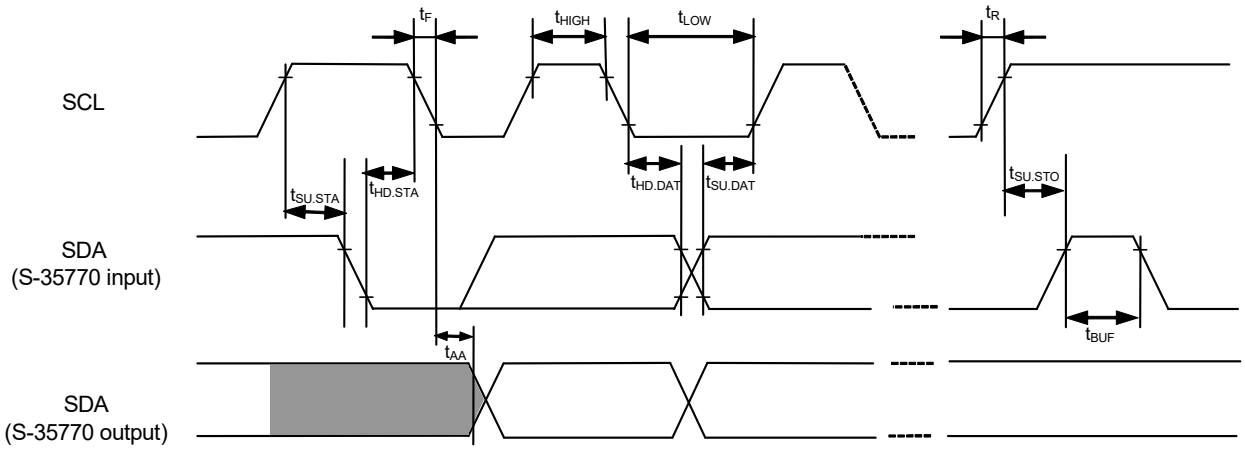


Figure 10 Bus Timing

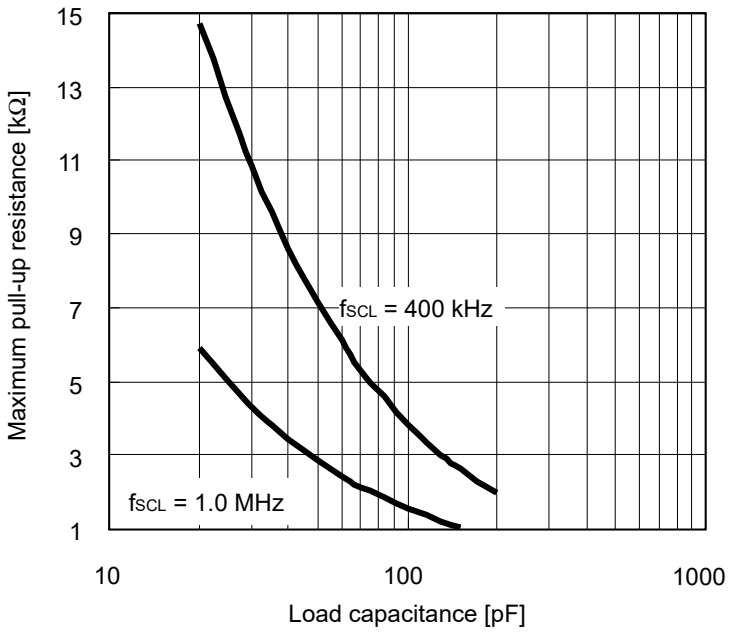


Figure 11 Output Load

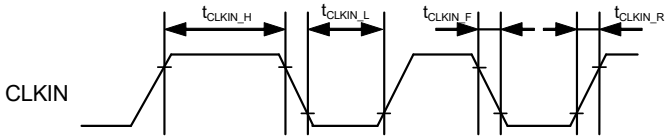


Figure 12 CLKIN Pin Clock Timing

■ External Clock Signal Count Function

The S-35770 Series detects the change of the CLKIN pin from "L" to "H", and then starts the count-up action of the counter. The counter is a 24-bit binary counter which can count from 0 to 16,777,215 (FFFFFF h). After reaching 16,777,215, the S-35770 Series detects the change of the CLKIN pin from "L" to "H", the counter loops back to 0.
The counter value can be confirmed by reading the count register. To initialize the counter, input "L" to the $\overline{RST}$ pin or input the reset command to the free register. Regarding the count register and the reset command, refer to "**■ Configuration of registers**".

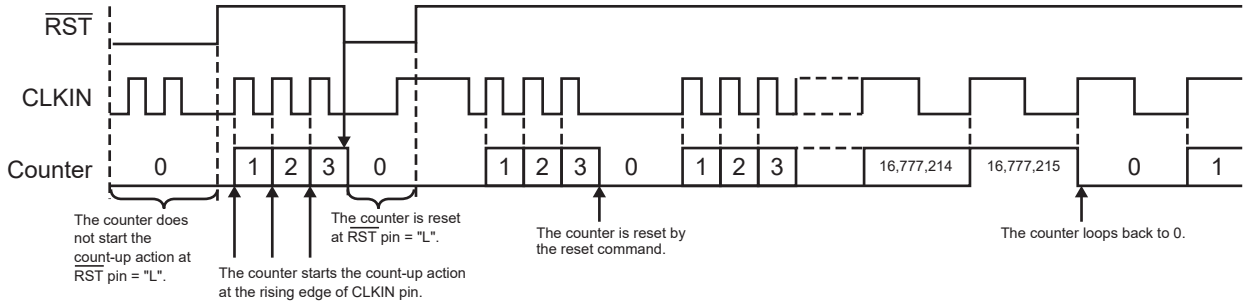


Figure 13 Counter Operation

During communication, the S-35770 Series does not detect the change of the CLKIN pin from "L" to "H" and maintains the counter data. The duration of the communication is defined as the time period from the start condition to the stop condition. The count-up action of the counter is executed 1 time if the CLKIN pin is "L" when the start condition is recognized and if the CLKIN pin is "H" when the stop condition is recognized.

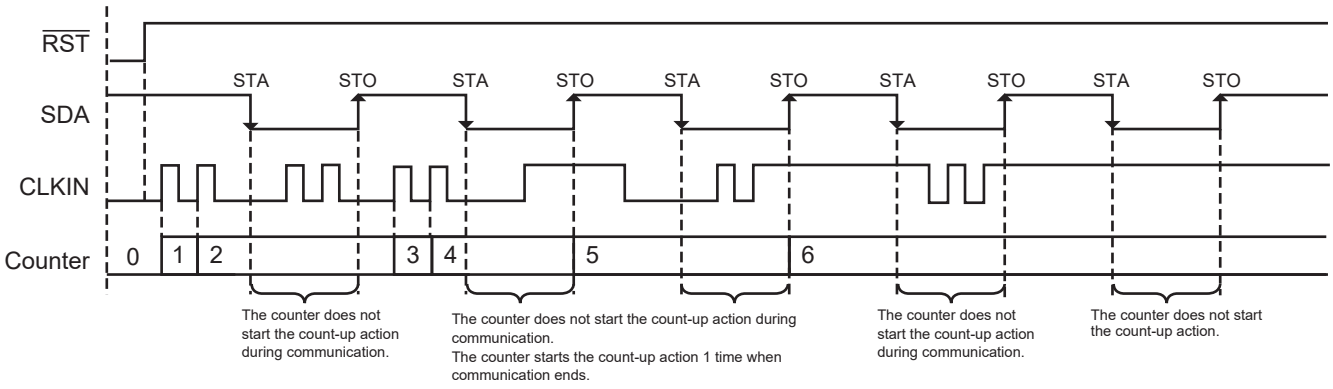


Figure 14 Counter Operation during Communication

■ LOOP Pin

The S-35770 Series detects the change of the CLKIN pin from "L" to "H", and then starts the count-up action of the counter. The counter loops back to 0 after reaching 16,777,215. At this time, the LOOP pin changes from "H" to "L". To change the LOOP pin to "H", input "L" to the $\overline{\text{RST}}$ pin or input the reset command to the free register.
Furthermore, if the counter loops back to 0 again after reaching 16,777,215 under the condition the LOOP pin maintains "L", the LOOP pin changes from "L" to "H". In other word, each time the counter loops back to 0 after reaching 16,777,215, the LOOP pin performs a toggle operation.

Remark The above description is the example of Nch open-drain output product.
In CMOS output product, the LOOP pin output is the inverse logic of Nch open-drain output product.

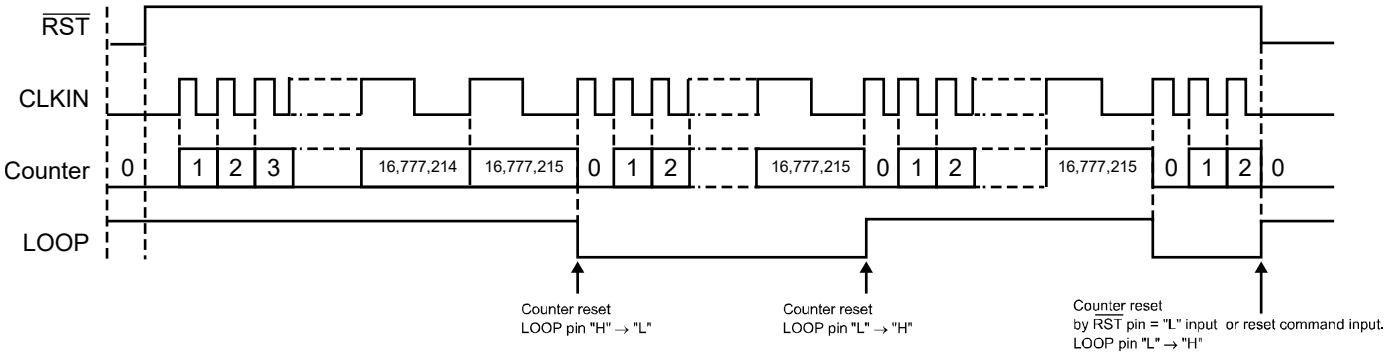


Figure 15 LOOP Pin Operation (Nch Open-drain Output)

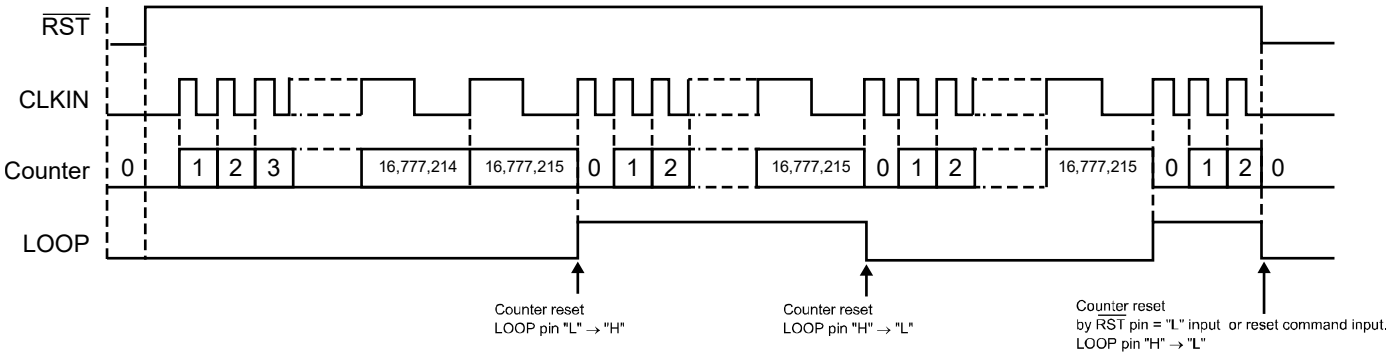


Figure 16 LOOP Pin Operation (CMOS Output)

■ Configuration of Registers

1. Count register

The count register is a 3-byte register that stores the counter value as binary code.
The count register is read-only.
Perform the read operation of the count register in 3-byte unit from CNT23 to CNT0.

Example:	3	(0000_0000_0000_0000_0000_0011)
	45	(0000_0000_0000_1010_1000_1100)
	19,800	(0000_0000_0100_1101_0101_1000)

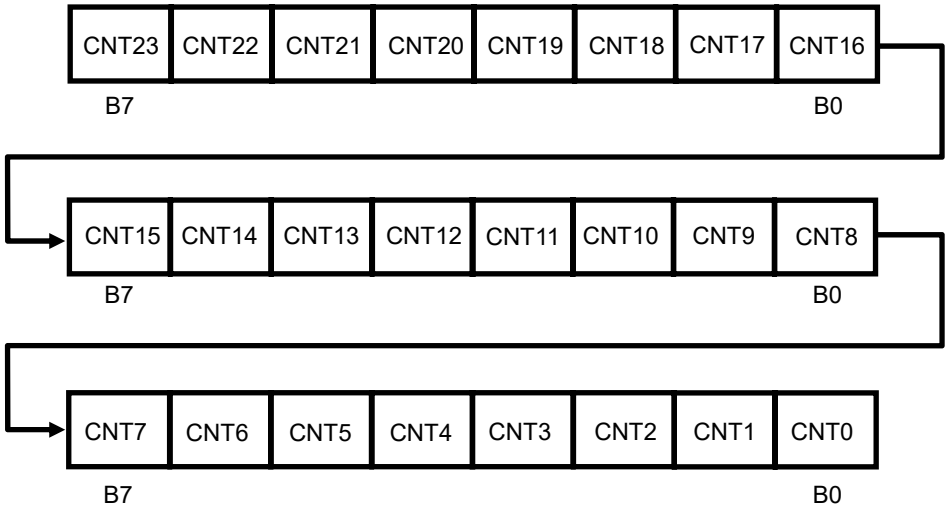


Figure 17

2. Free register

The free register is a 3-byte register that can be freely read and written by the user. The lower 3 bits, RST2 to RST0 are used as a register to input the counter reset command. The counter is reset by writing RST2 = "0", RST1 = "1", and RST0 = "0". The data of F20 to F0 are not reset when inputting the reset command; however, the data when the reset command is input are set.
When only the data of F20 to F0 are rewritten without resetting the counter, write the data except for the above mentioned ones, such as RST2 = "1", RST1 = "1" and RST0 = "1" to the free register.
Perform the write and read operation of the free register in 3-byte unit.

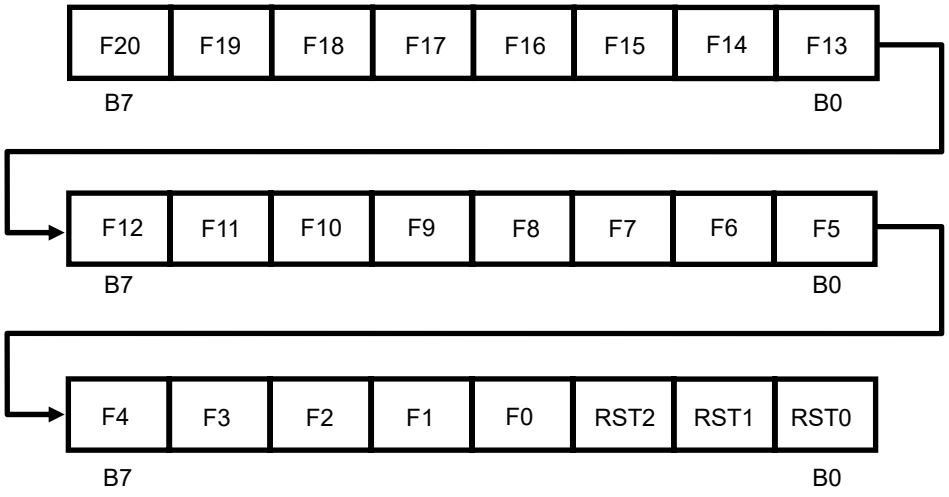


Figure 18

■ Serial Interface

The S-35770 Series transmits and receives various commands via I²C-bus serial interface to read / write data.

1. Start condition

When SDA changes from "H" to "L" with SCL at "H", the S-35770 Series recognizes start condition and the access operation is started.

2. Stop condition

When SDA changes from "L" to "H" with SCL at "H", the S-35770 Series recognizes stop condition and the access operation is completed. The S-35770 Series enters standby mode, consequently.

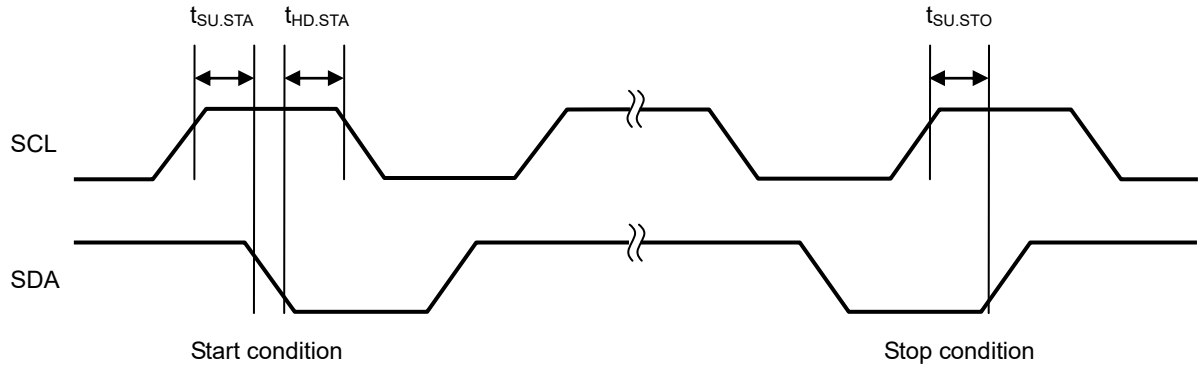


Figure 19 Start / Stop Condition

3. Data transmission and acknowledge

The data transmission is performed at every one byte after the start condition detection. Pay attention to the specification of $t_{SU.DAT}$ and $t_{HD.DAT}$ when changing SDA, and perform the operation when SCL is "L". If SDA changes when SCL is "H", the start / stop condition is recognized even during the data transmission, and the access operation will be interrupted.

Whenever a one-byte data is received during data transimmion, the receiving device returns an acknowledge. For example, as shown in **Figure 20**, assume that the S-35770 Series is a receiving device, and the master device is a transmitting device. If the clock pulse at the 8th bit falls, the master device releases SDA. Consequently, the S-35770 Series, as an acknowledge, sets SDA to "L" during the 9th bit pulse. The access operation is not performed properly when the S-35770 Series does not output an acknowledge.

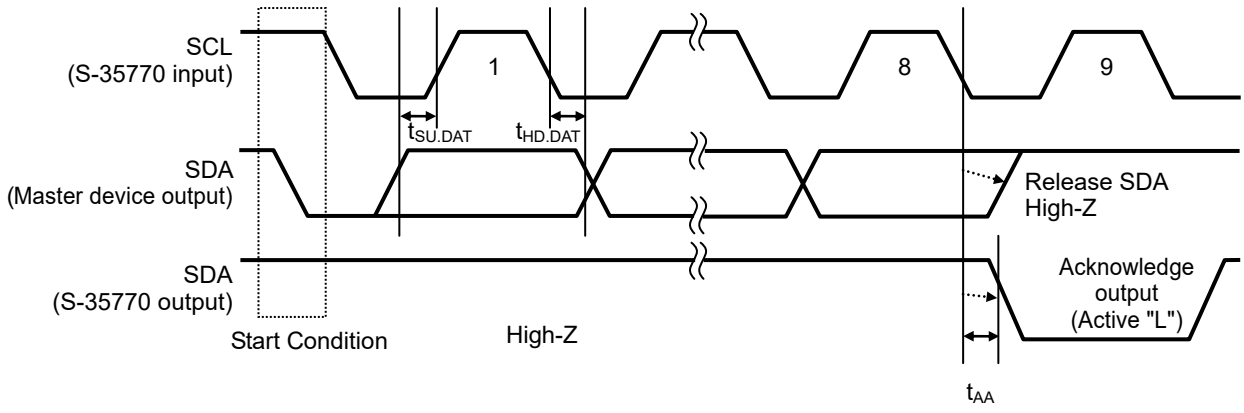


Figure 20 Acknowledge Output Timing

4. Data transmission format

After the start condition transmission, the 1st byte is a slave address and a command (read / write bit) that shows the transmission direction at the 2nd byte or subsequent bytes.

The slave address of the S-35770 Series is specified to "0110010". The data can be written to the free register when read / write bit is "0", and the data of count register or the free regiister can be read when read / write bit is "1".

When the data can be written to the free register, input the data from the master device in order of B7 to B0. The acknowledge ("L") is output from the S-35770 Series whenever a one-byte data is input.

When the data of the count register or the free register can be read, the data from the S-35770 Series is output in order of B7 to B0 in byte unit. Input the acknowledge ("L") from the master device whenever a one-byte data is input. However, do not input the acknowledge for the last byte (NO_ACK). By this, the end of the data read is informed.

After the master device receives / transmits the acknowledge for the last byte data, input the stop condition to the S-35770 Series to finish the access operation.

When the master device inputs start condition instead of stop condition, the S-35770 Series becomes restart condition, and can transmit / receive the data if the master device inputs the slave address continuously.

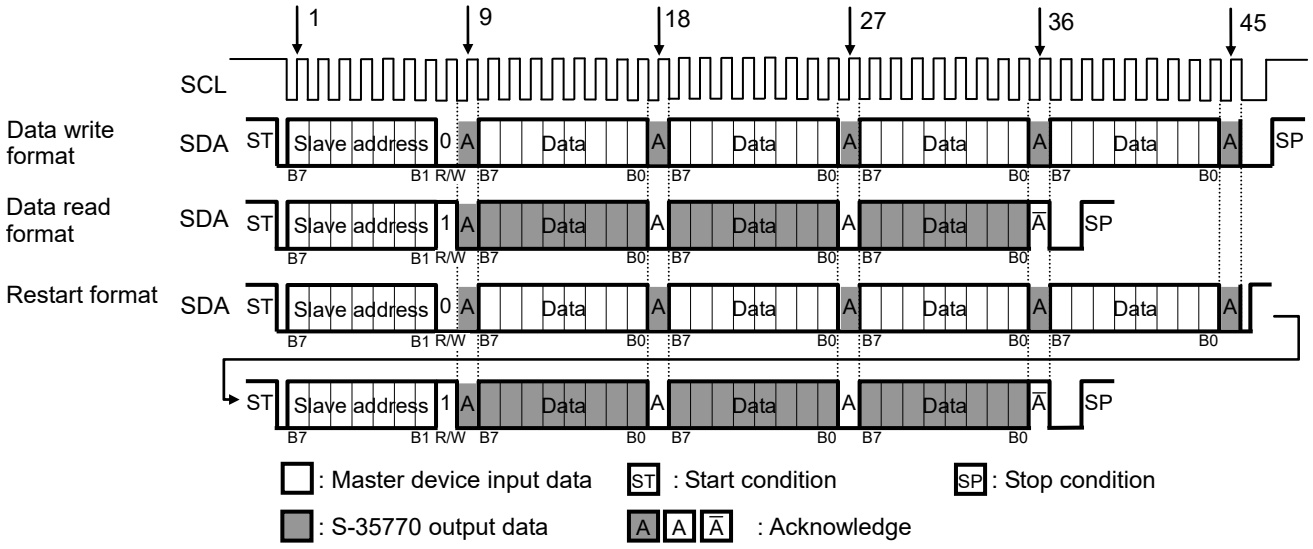


Figure 21 Data Transmission Format of Serial Interface

In the time period from the start condition to the stop condition, the S-35770 Series does not detect the change of the CLKIN pin from "L" to "H" and maintains the counter data. Therefore, the output data of the count register does not change even if an external clock is input during a read operation of the count register.

Regarding the counter operation during communication, refer to "■ **External Clock Signal Count Function**".

5. Read operation of count register

Transmit the start condition and slave address from the master device. The slave address of the S-35770 Series is specified to "0110010". The data of the count register can be read when the read / write bit is "1".
The 2nd byte to the 4th byte are used as the count register. Each byte from B7 is transmitted.
When the read operation of the count register is finished, transmit "1" (NO_ACK) to the acknowledge after B0 is output from the master device, and then transmit the stop condition.
The count register is a 3-byte register. "1" is read if the read operation is performed continuously after reading 3 bytes of the count register. Regarding the count register, refer to "■ **Configuration of Registers**".

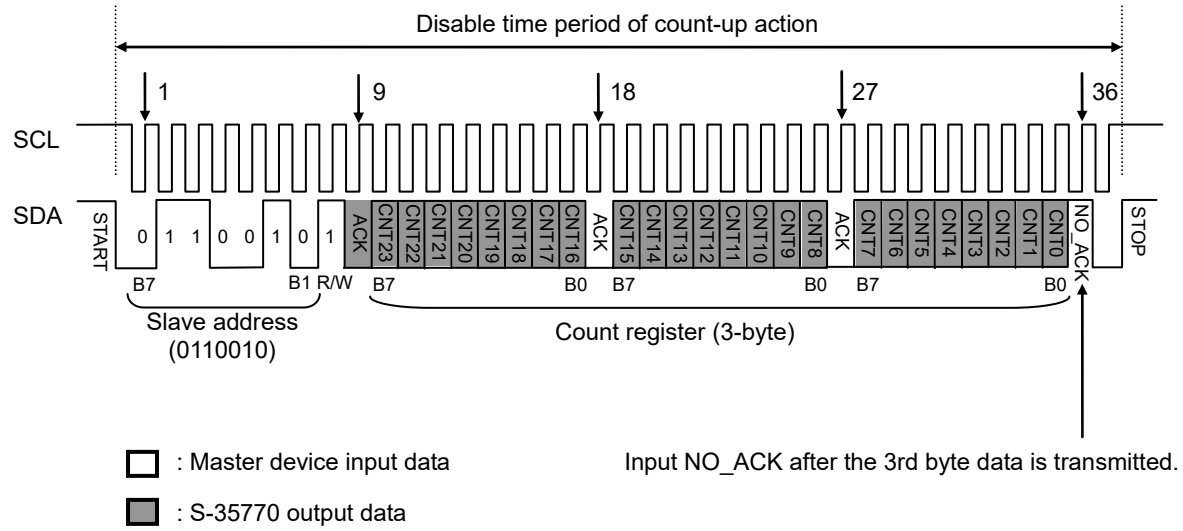


Figure 22 Read Timing of Count Register

6. Write operation of free register

Transmit the start condition and slave address from the master device. The slave address of the S-35770 Series is specified to "0110010". Next, transmit "0" to the read / write bit.

Transmit the 2nd byte data. Set B7 to "1" since it is an address pointer. Set B6 to B1 to "0" or "1" since they are dummy data. Be sure to set B0 to "1" since it is a test bit.

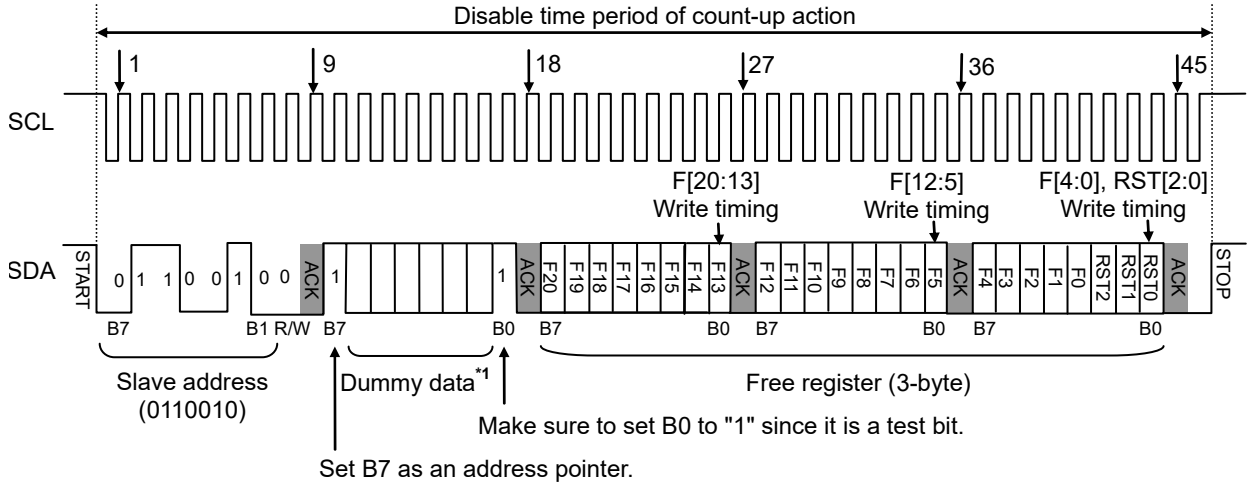
B7 in the 3rd byte to B3 in the 5th byte are used as the free register.

B2 to B0 (RST2 to RST0) in the 5th byte are used as a register to input the counter reset command. The counter is reset when transmitting RST2 = "0", RST1 = "1" and RST0 = "0". When not resetting the counter, transmit the data except for the above mentioned ones, such as RST2 = "1", RST1 = "1" and RST0 = "1".

Transmit the stop condition from the master device to finish the access operation.

Regarding the free register, refer to "■ **Configuration of Registers**".

Write operation of the free register is performed each byte, so transmit the data in 3-byte unit. Note that the S-35770 Series may not operate as desired if the data is not transmitted in 3-byte unit.



: Master device input data
: S-35770 output data

***1.** Set B6 to B1 to "0" or "1" since they are dummy data.

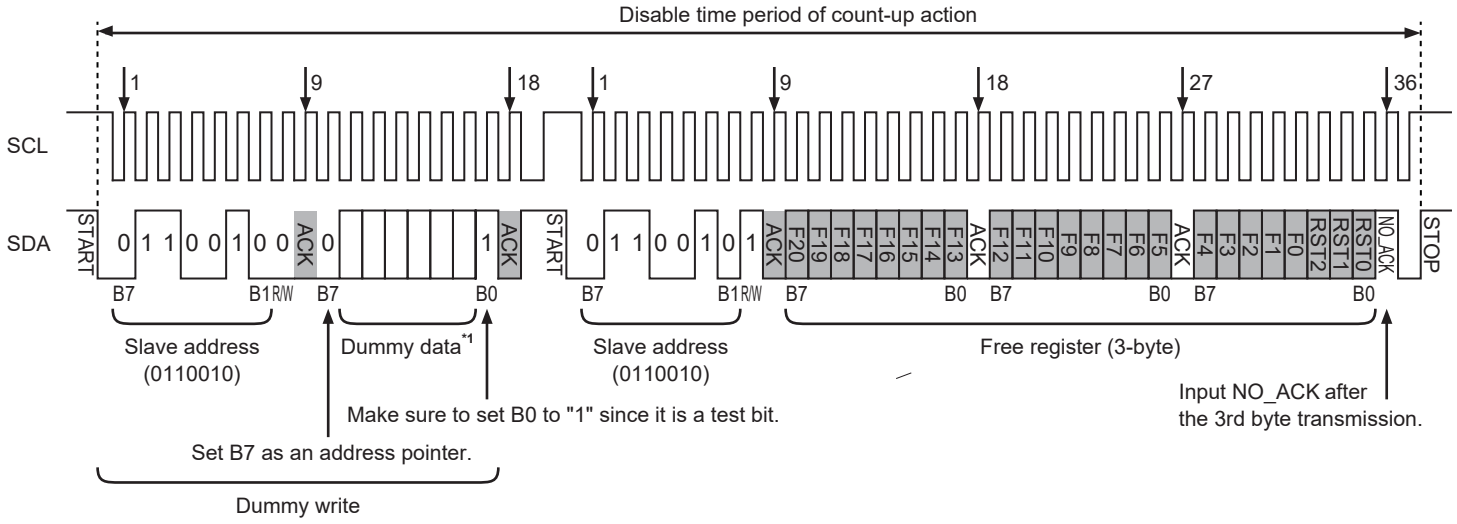
Figure 23 Write Timing of Free Register

7. Read operation of free register

Perform the read operation of the free register with the restart format. Regarding the restart format, refer to "**4. Data transmission format**".

Transmit the start condition and the slave address from the master device. The slave address of the S-35770 Series is specified to "0110010". Next, transmit "0" to the read / write bit.
B7 in the 2nd byte is an address pointer. Set B7 to "0" when reading the free register. Next, transmit the dummy data to B6 to B1. Make sure to set B0 to "1" since it is a test bit. This processing is called "dummy write".
Then transmit the start condition, the slave address and the read / write bit. If the read / write bit is set to "1", the S-35770 Series becomes the mode to read the free register.
Consequently, the data of the free register is output from the S-35770 Series. Each byte from B7 is transmitted.
When the read operation of the free register is finished, transmit "1" (NO_ACK) to the acknowledge after B0 output from the master device, and then transmit the stop condition.
The free register is a 3-byte register. "1" is read if the read operation is performed continuously after reading 3 bytes of the free register.
Regarding the free register, refer to "■ **Configuration of Registers**".

Moreover, the internal address pointer is reset if recognizing the stop condition. Therefore, do not transmit the stop condition after dummy write operation. The counter data is read when reading the free register after transmission of the stop condition.



***1.** Set B6 to B1 to "0" or "1" since they are dummy data.

Figure 24 Read Timing of Free Register

■ Release of SDA

The $\overline{RST}$ pin of the S-35770 Series does not perform the reset operation of the communication interface. Therefore, the stop condition is input to reset the internal interface circuit usually.
However, the S-35770 Series does not accept the stop condition from the master device when in the status that SDA outputs "L" (at the time of acknowledge outputting or reading). Consequently, it is necessary to finish the acknowledge output or the read operation. **Figure 25** shows the SDA release method.

First, input the start condition from the master device (since SDA of the S-35770 Series outputs "L", the S-35770 Series can not detect the start condition). Next, input the clocks for 1-byte data access (9 clocks) from SCL. During the time, release SDA of the master device. By this, the SDA input / output before communication interrupt is completed, and SDA of the S-35770 Series becomes release status. Continuously, if the stop condition is input, the internal circuit resets and the communication returns to normal status.

It is strongly recommended that the SDA release method is performed at the time of system initialization after the power supply voltage of the master device rises.

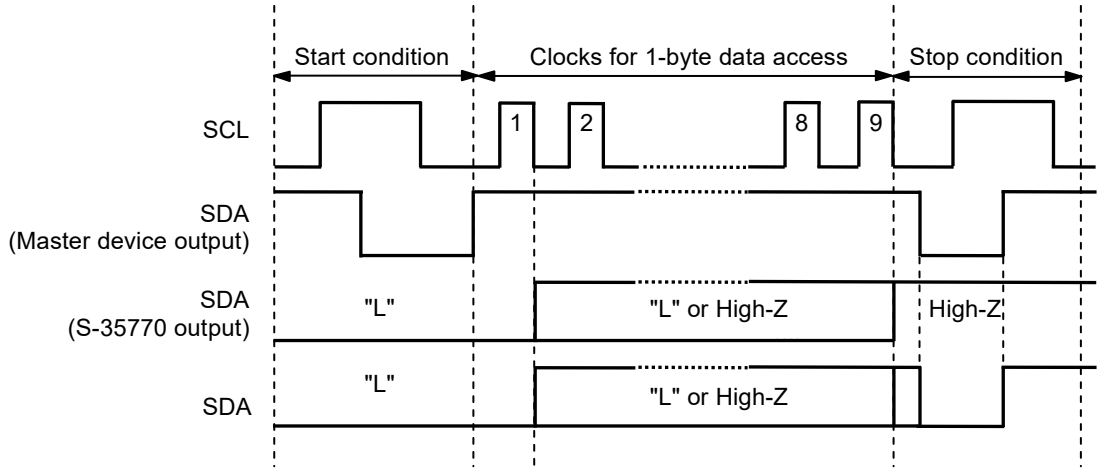
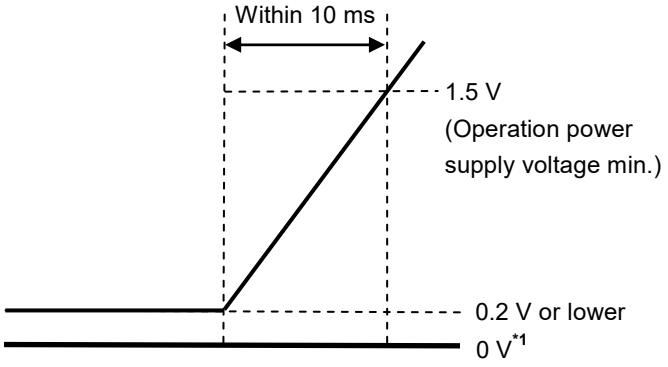


Figure 25 SDA Release Method

■ Power-on Detection Circuit

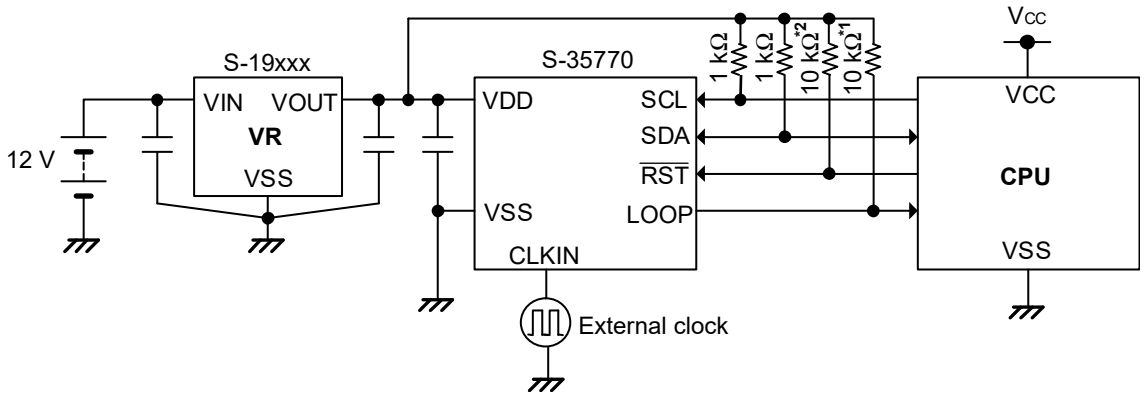
In order for the power-on detection circuit to operate normally, raise the power supply voltage of the IC from 0.2 V or lower so that it reaches 1.5 V of the operation power supply voltage minimum value within 10 ms, as shown in **Figure 26**.



***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35770 Series.

Figure 26 How to Raise the Power Supply Voltage

■ Example of Application Circuit



***1.** This resistor is unnecessary when a CMOS output product is selected.
***2.** This resistor is unnecessary when a product with a pull-up resistor is selected.

Figure 27

Caution 1. Start communication under stable condition after turning on the system power supply.
2. The above connection diagrams do not guarantee operation. Set the constants after performing sufficient evaluation using the actual application.

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
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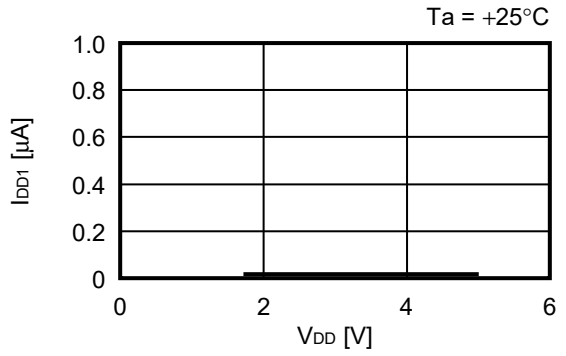
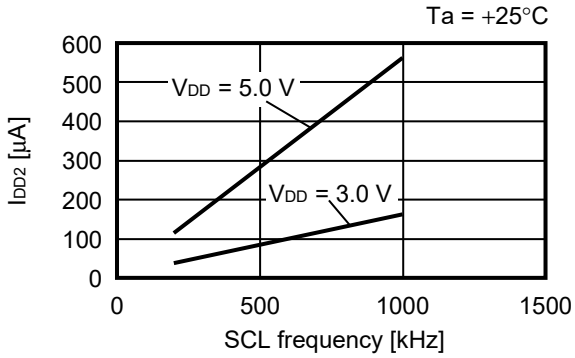
■ Characteristics (Typical Data)

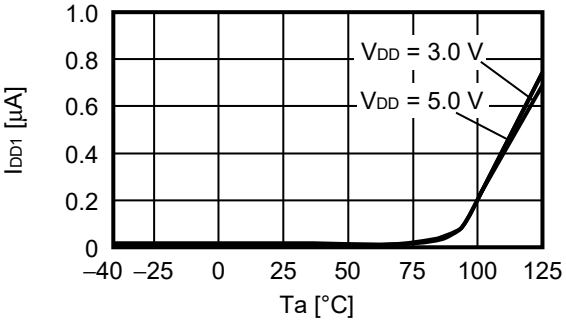
1. Current consumption 1 vs. Power supply voltage characteristics



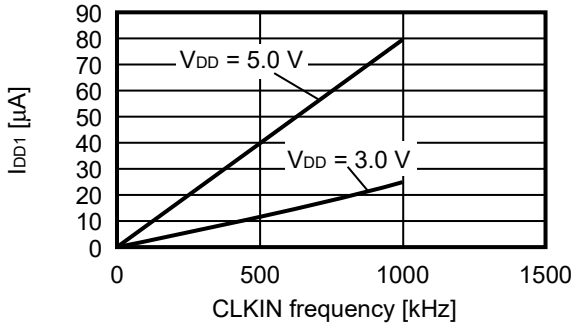
2. Current consumption 2 vs. SCL frequency characteristics



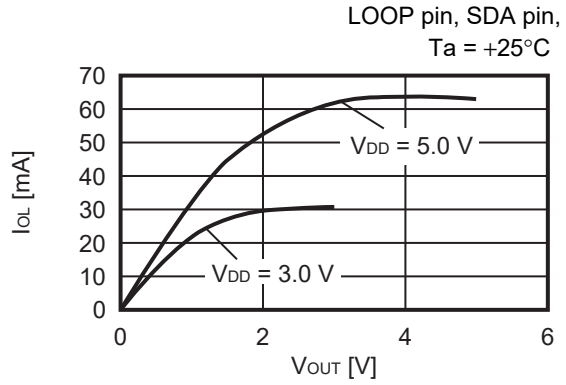
3. Current consumption 1 vs. Temperature characteristics



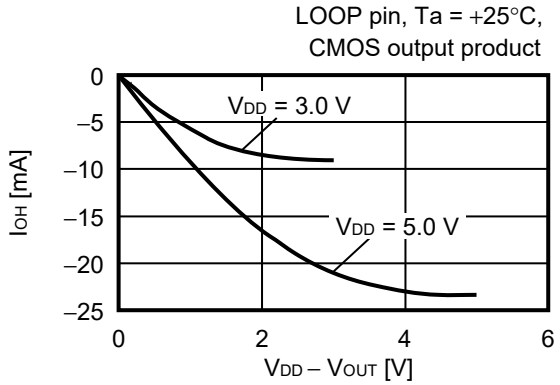
4. Current consumption 1 vs. CLKIN frequency characteristics



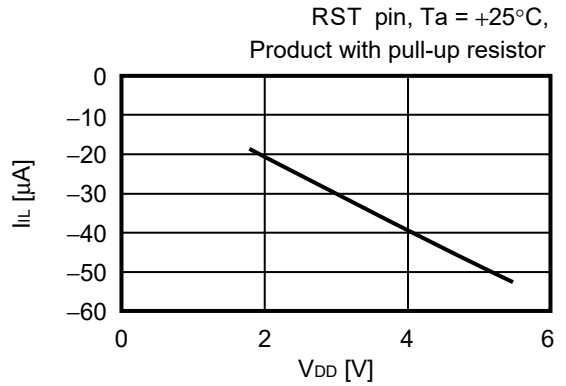
5. Low level output current vs. Output voltage characteristics

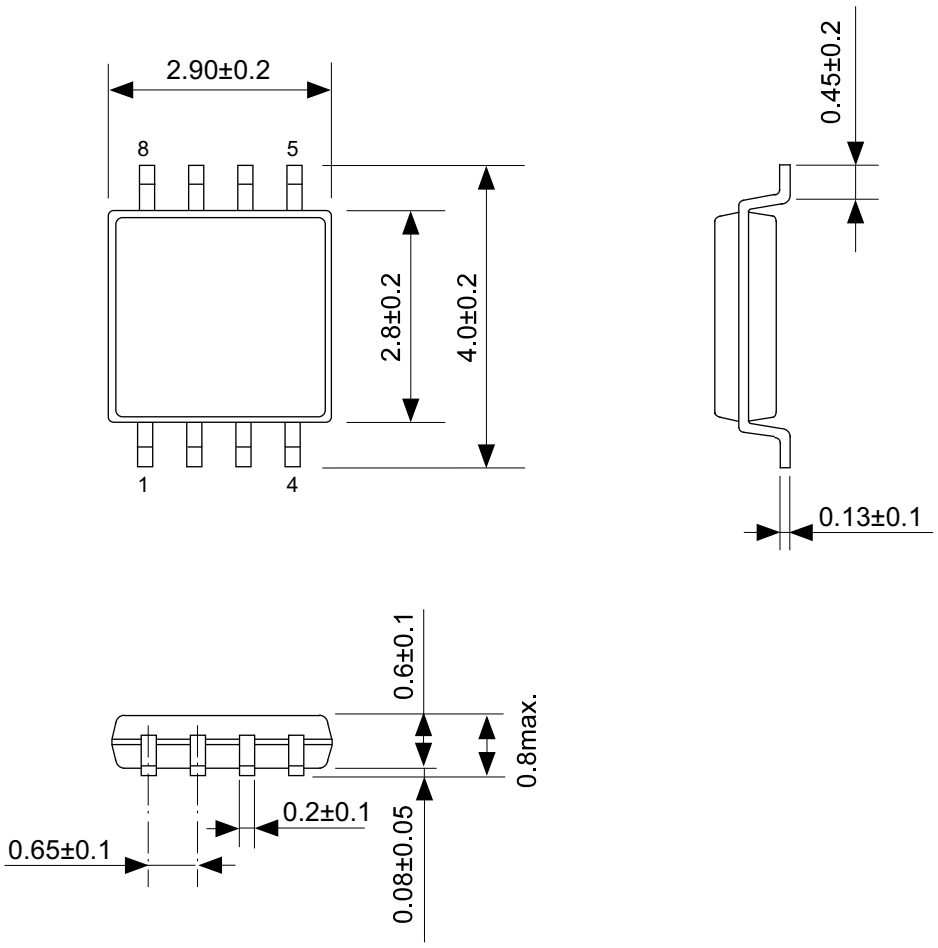


6. High level output current vs. V_{DD} – V_{OUT} characteristics



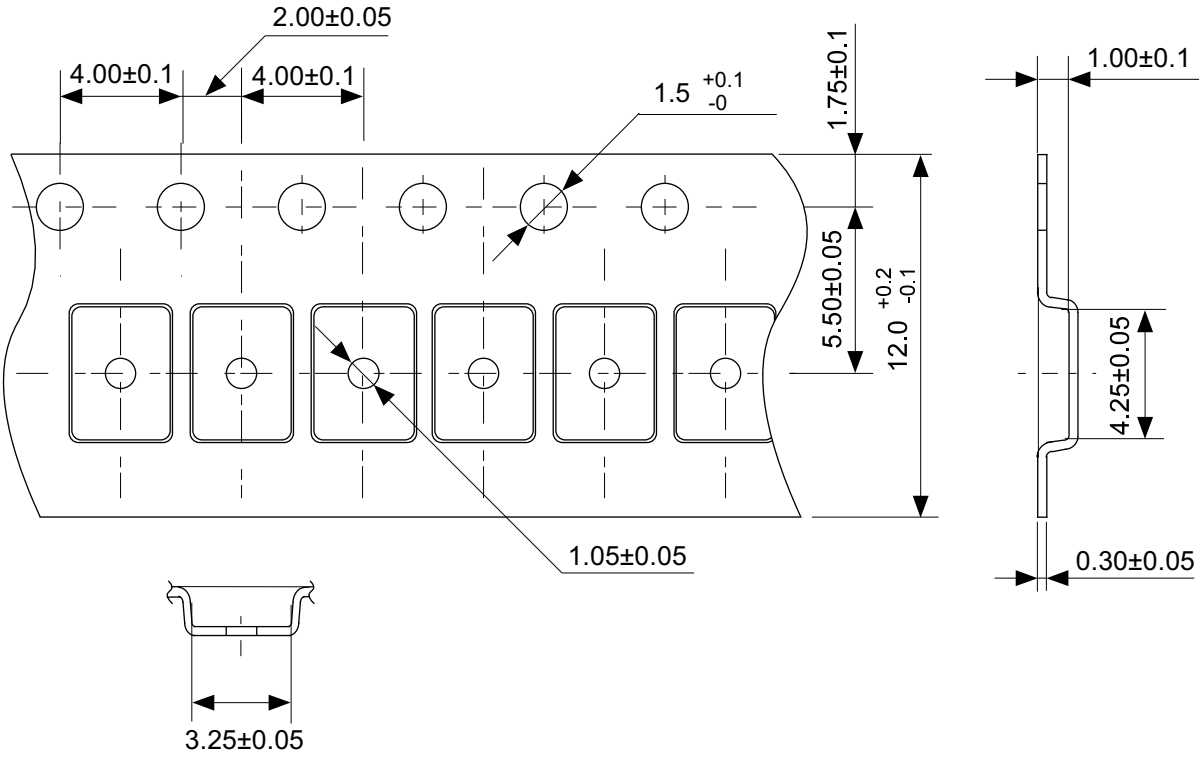
7. Low level input current vs. Power supply voltage characteristics

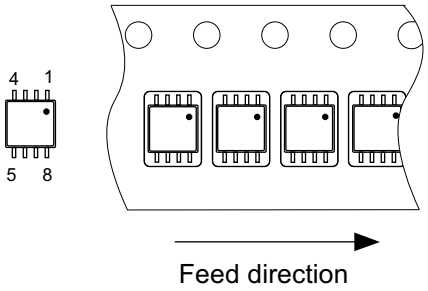




No. FM008-A-P-SD-1.2

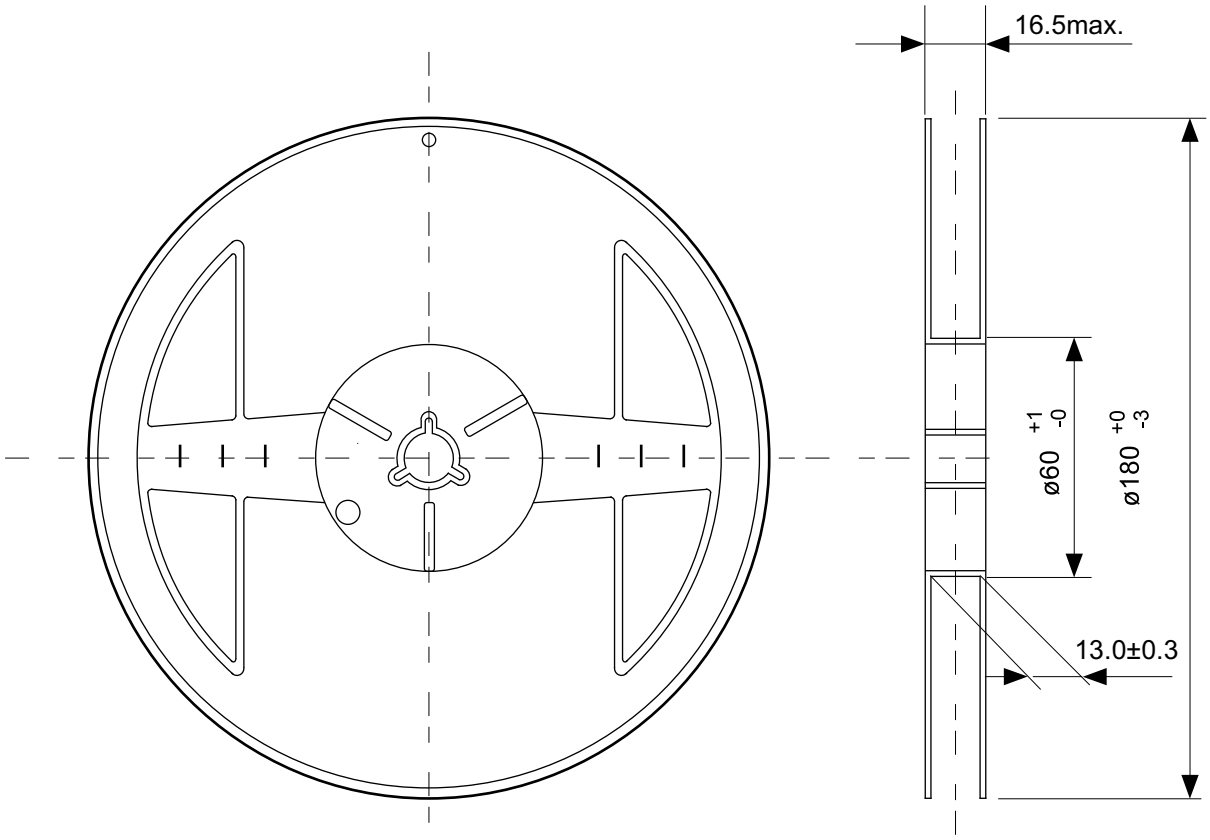
TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	



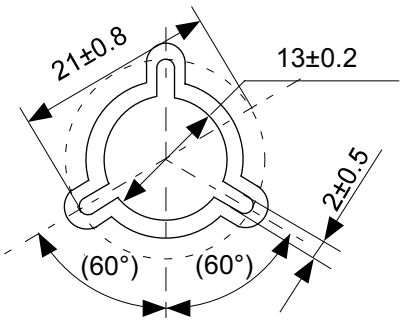


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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